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APPLICATION NOTE

MODEL NAME: UPS051

The content of this technical information is subject to change without notice.

Record of Revision

Version	Change Date	Content
3.5	24/Sep/2004	Modify document form

Contents:

A. Object

This application note contains additional information for using AUO COG series TFT-LCD module with UPS051 controller. There are two major topics contained in this note, they are “Typical reference circuit” and “Conversion process from an image data array to UPS051’s format”.

B. Applicable TFT-LCD models

AUO’s COG series panels, including A015AN03, A018AN02, A025CNXX, A035CNXX, A040CNXX, A056DNXX, A068ENXX, A070FWXX.

C. Block diagram

Please refer to Fig.1 for the application concept of UPS051.

D. Conversion process from an image data array to UPS051’s format

1. Input format for UPS051

UPS051 implements an 8-bit data to drive each TFT-LCD’s primary color. To reduce the I/O number, UPS051 accepts the color data in a sequence format, those are R0～R7, G0～G7 & B0～B7 which come from display memory and are extracted into the D0～D7 corresponding to the color filter arrangement of LCD. Please refer to Fig.2-b for the required format which UPS051 is operated under the normal scan mode (LR:H, UD:L) as an example.

To allow customer to drive the traditional CRT-TV & UPS051 simultaneously, UPS051 can accept the non-symmetric clock. That means customer can use the same clock (V-CLK) to drive DAC for CRT-TV and to generate the “wedding” clock (D-CLK) which will synchronize the UPS051’s operation. Please also refer to Fig.2-b for the “wedding” clock, D-CLK.

2. Implementation example of conversion

To give customer more clear idea about the conversion, we present an example here, and its source data array is VGA (640×3×480) and the target format is UPS051’s 280×220 mode. The procedure of implementing a conversion circuit is as below.

2-1. Calculation of the wedding cycle

There are 640 pixel’s data for each horizontal line stored in the display memory, and each pixel contains 3 primary color dots’ data. On the other hand, when UPS051 is operated at 280×220 mode, only 280 dots at each LCD horizontal line can be displayed. So the abundant pixel data in VGA display memory should be extracted to a limited number, which is 280 dot for each horizontal line. To get the wedding cycle, we calculate

$640 \div (280/3) = 6.86 \fallingdotseq 7$

This means only 3 dots (one pixel) can be extracted from every 7 pixels at VGA memory. Since UPS051 latchs each input data at the rising edge of every D-CLK, so the D-CLK’s frequance is 3/7 V-CLK. For example, at VGA mode, the V-CLK is 12.27MHz, and the D-CLK can be got by “MASKING 4 V-CLK IN EVERY 7 V-CLK”. Please refer to Fig.2 for the wedding’s operation.

2-2. Extration of display data

From the above calculation, only 3 dots data can be extracted from every 7 pixels. To accommodate the special arrangement of LCD’s color filter, the R.G.B data are extracted from different pixels’ positions. Please refer to Fig.3 for these data extraction. Due to the “Delta” type arrangement of LCD’s color filter, this means the color sequence and position of each primary color will be different at odd lines and even lines. So the extraction should also follow this difference. Please follow the corresponding sequence under different conditions which are shown in Tab.1

E. Typical reference circuit

Please refer to Fig.4 for the reference circuit, which contains all the pheripheral circuitry of UPS051

when it is used to drive the AUO's COG series TFT-LCD.

F. Detail timing

Please refer to the data sheet of UPS051.

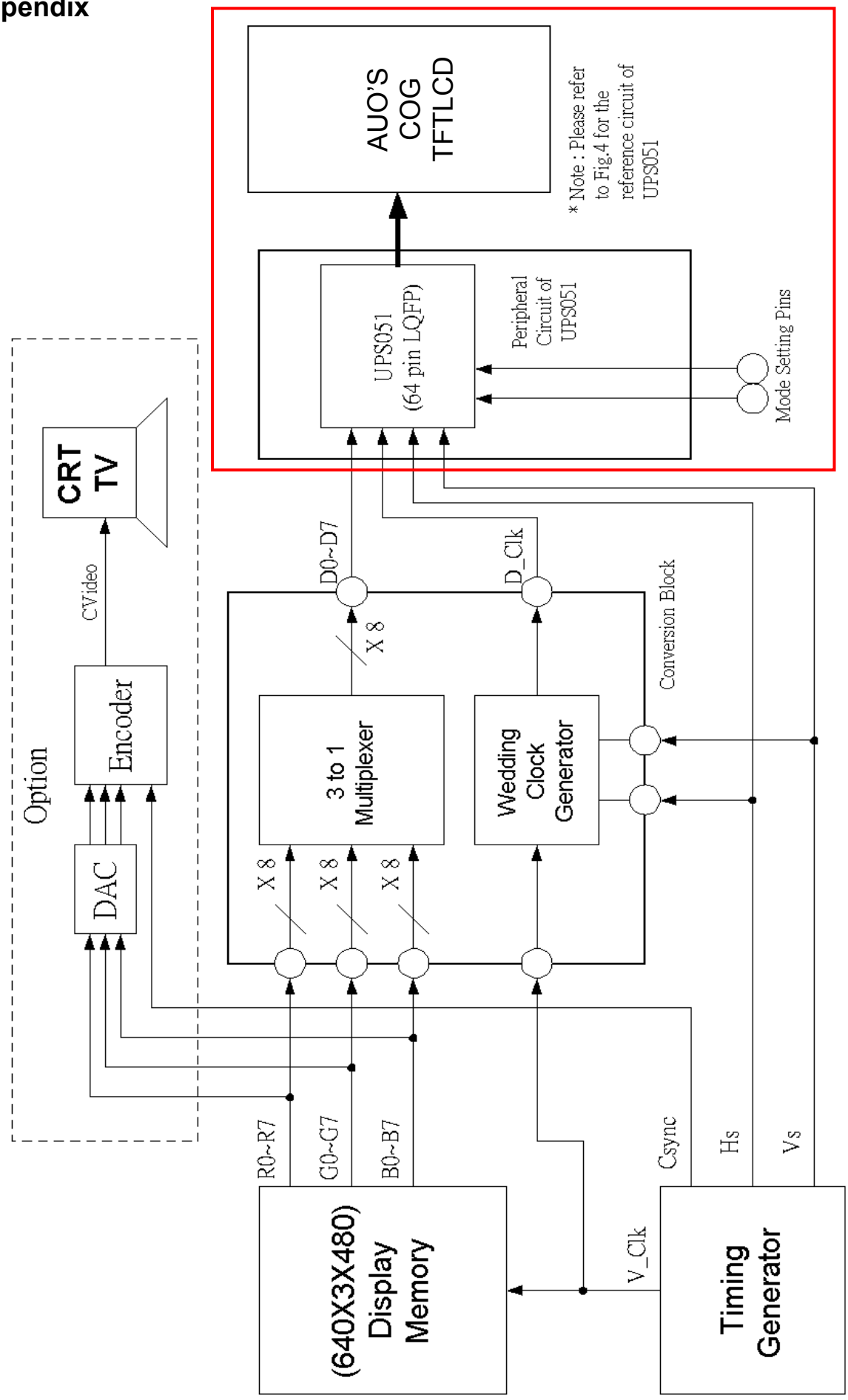
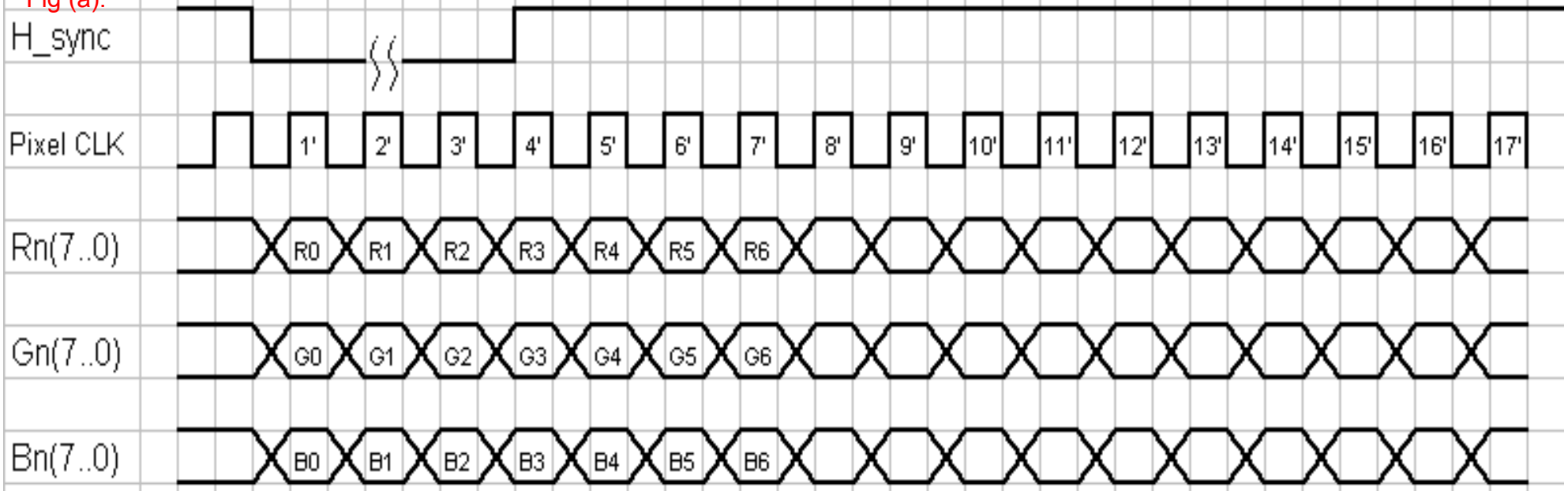


Fig.1 Block diagram of conversion circuit

Fig (a).



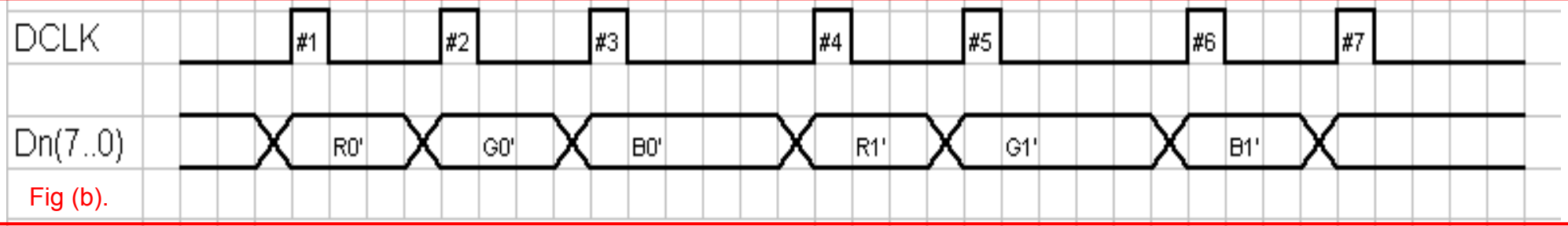
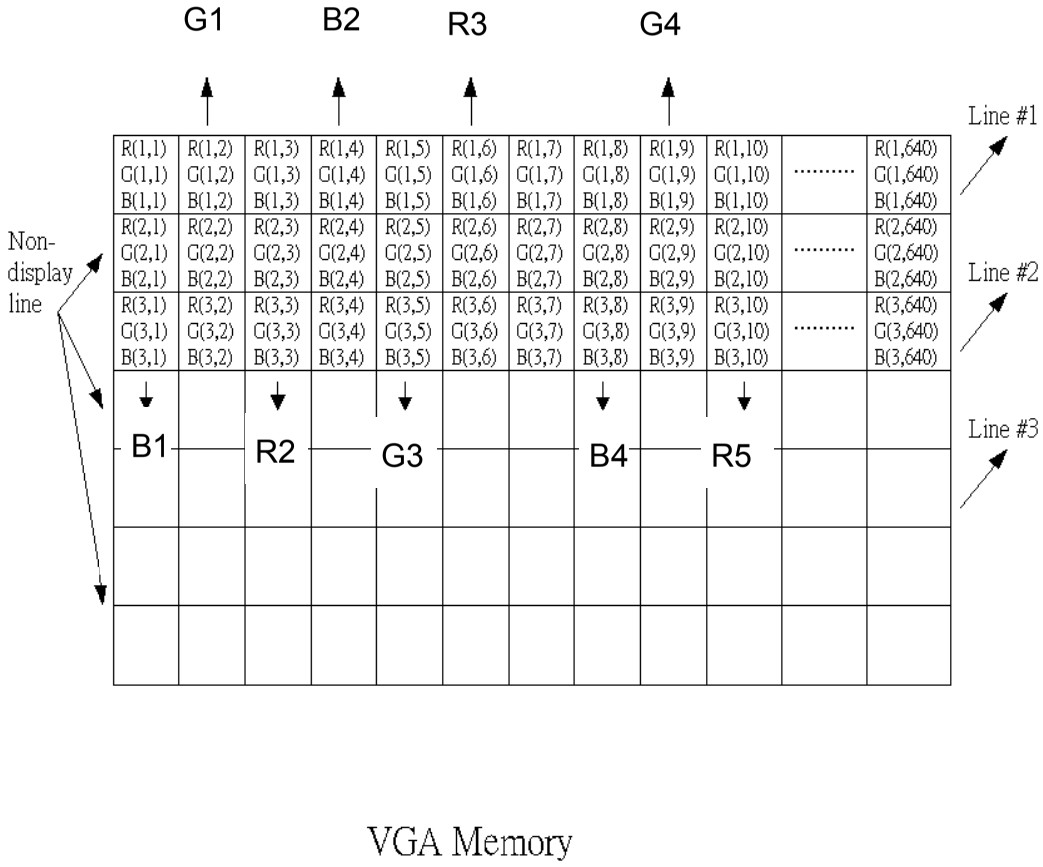
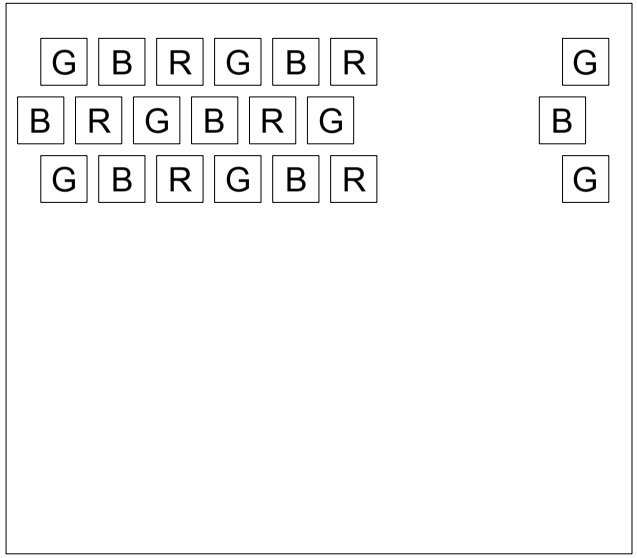


Fig (b).

Fig.2-(a) (Top) Input waveform to the conversion block

Fig.2-(b) (Bottom) Output waveform from the conversion block





LCD's color filter arrangement

Fig 3. Extraction example of display data from memory to UPS051

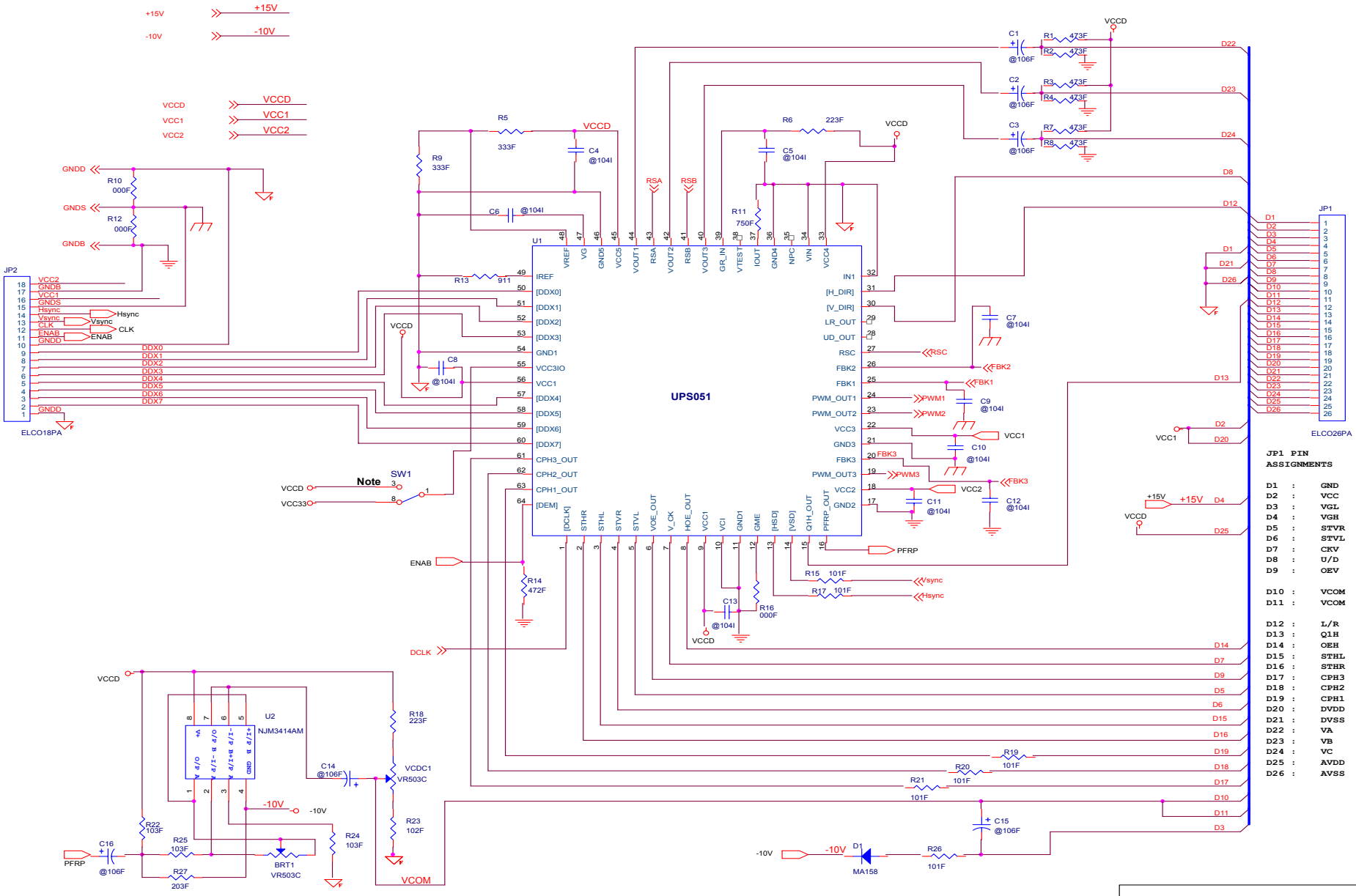


Fig. 4-1 Typical reference circuit of UPS051 (gernal 26pin product)

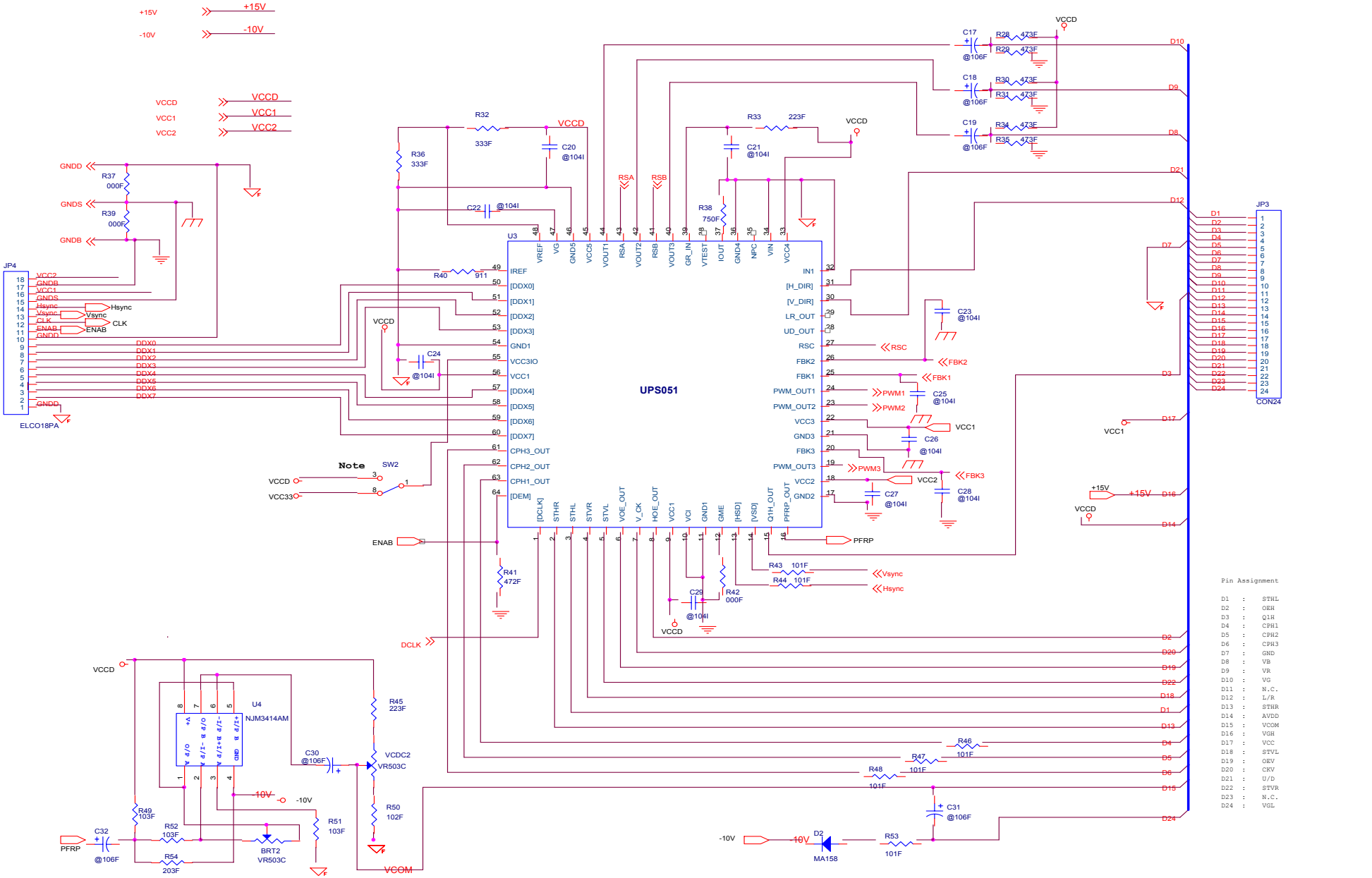


Fig. 4-2 Typical reference circuit of UPS051 (For A025CN00/01, A035CN00/01)

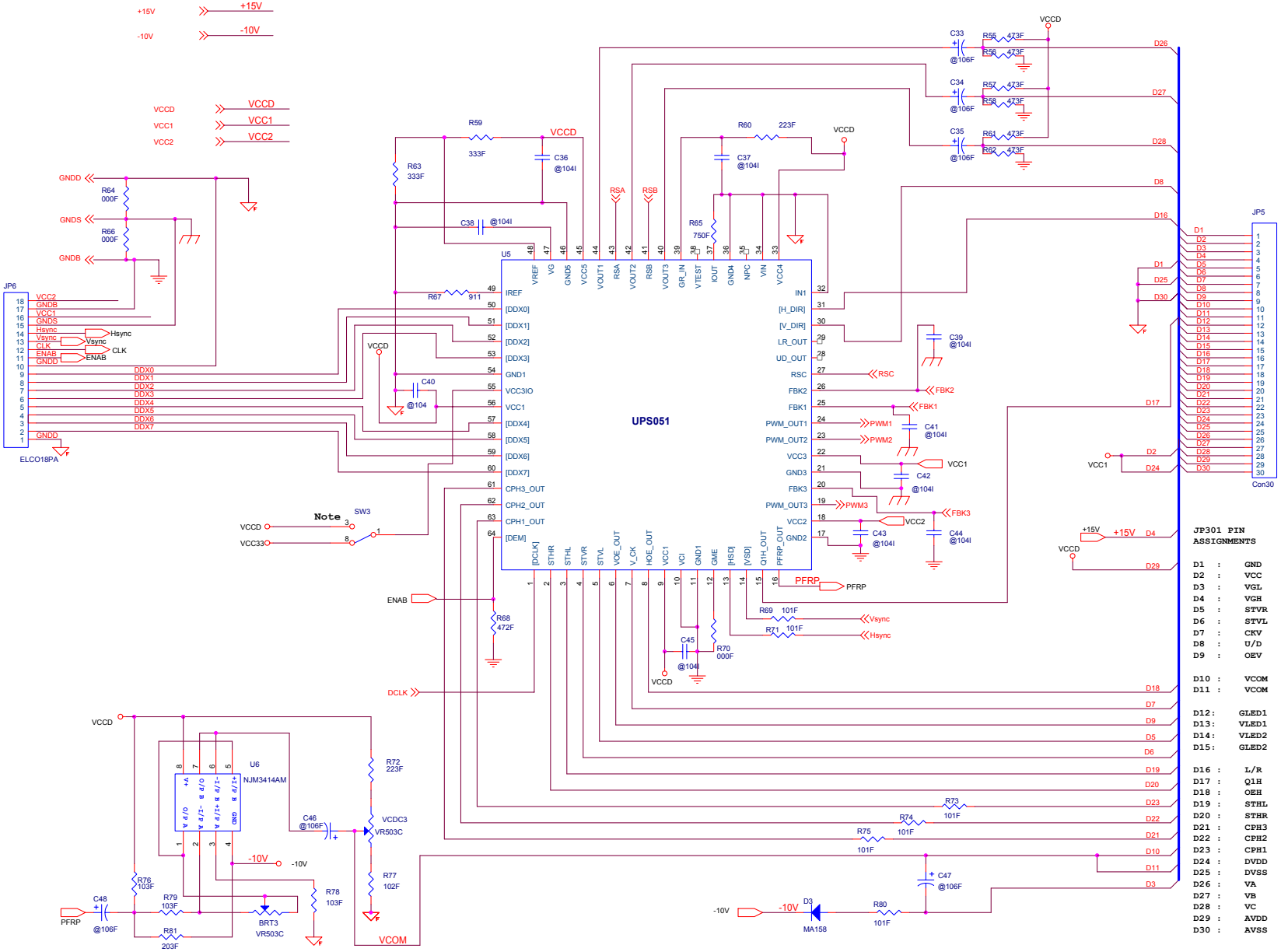


Fig. 4-3 Typical reference circuit of UPS051 (For A025CN03, A035CN02)

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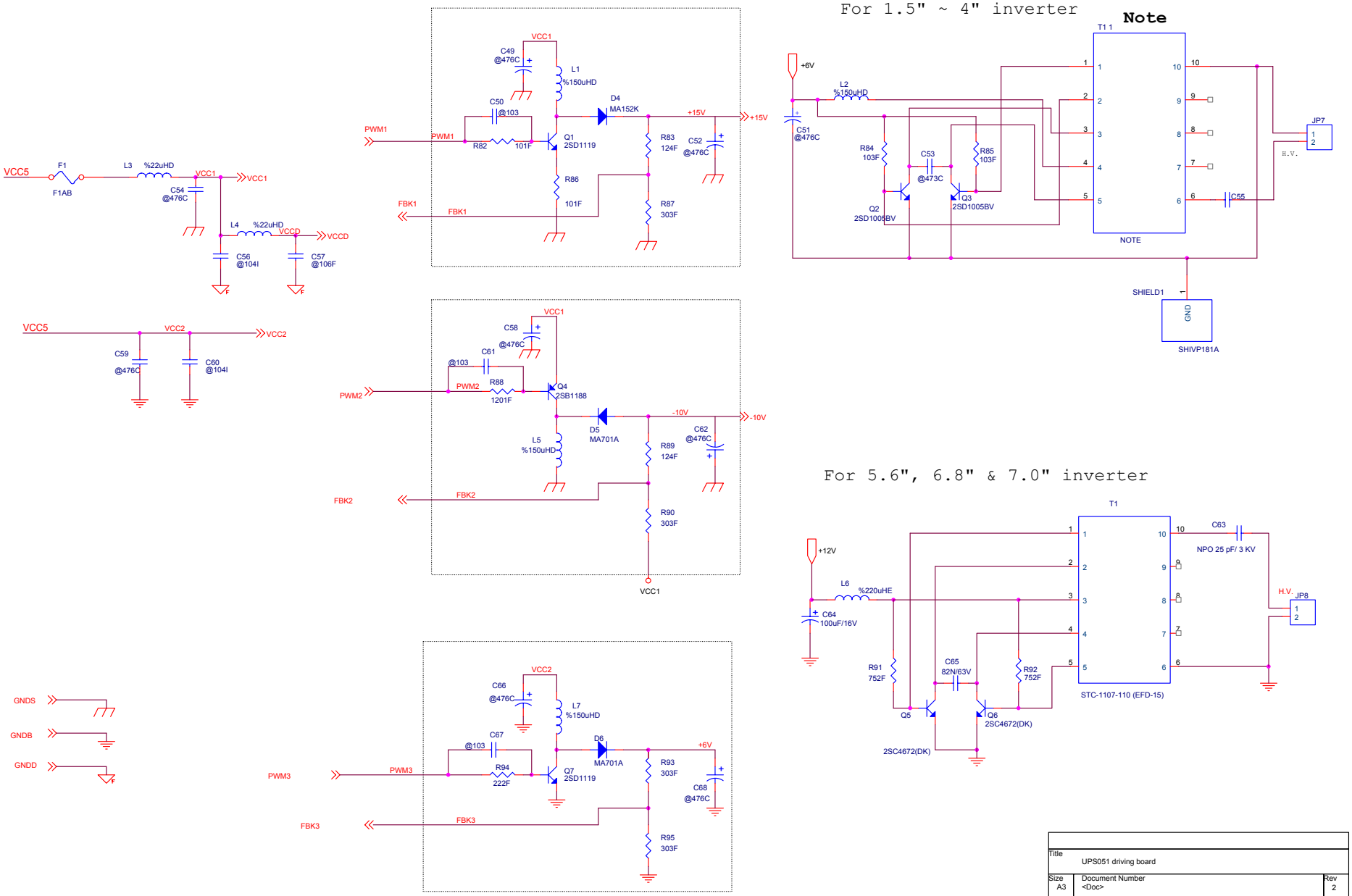

Fig 4-4 Typical reference circuit of UPS051 (Power)

Note:

1. Resolution setting

LCD size	Resolution	RSA	RSB	RSC	T11
1.5" & 1.8"	280	Low	Low	Low	BLC13/1025
2.5" & 3.5"	480	High	High	High	BLC13/1193
4"	480	High	High	High	BLC13/1193
5.6"	960	High	Low	High	
6.8"	1152	Low	High	Low	
7.0"	1440	Low	High	High	

2. PWM function un-used

Pin	Assignment	Set	Pin	Assignment	Set
24	PWM_OUT1	Open	25	FBK1	High
23	PWM_OUT2	Open	26	FBK2	Low
19	PWM_OUT3	Open	20	FBK3	High

3.Bits data input setting:
(D5 ~ D0)

Pin	Assignment	Setting
50	DDX0	Lo
51	DDX1	Lo
52	DDX2	D0
53	DDX3	D1
57	DDX4	D2
58	DDX5	D3
59	DDX6	D4
60	DDX7	D5

4. VCC3IO setting

VCC3IO Input	Input signals* level
VCCD(5V)	5V
VCC33(3.3V)	3.3V

* Input signals contain: DCLK, HSD, VSD, V_DIR, H_DIR, DDX0 ~ DDX7.

5. ENAB pin setting:
Please always pull low for Pin64 [DEM] in UPS051.

6. STVR (UPS051) should connect to STVL (panel).
STVL (UPS051) should connect to STVR (panel).
STHL (UPS051) should connect to STHL (panel).
STHR (UPS051) should connect to STHR (panel).

Table.1 Color sequence for different modes.

Display REesolution	UD (Note 1)	Low	Low	High	High
	LR (Note 2)	High	Low	High	Low
280×220 (1.5” / 1.8”)	Odd Line	G B R	G R B	B R G	B G R
	Even Line	B R G	B G R	G B R	G R B
480x234 (2.45” / 3.5”)	Odd Line	G B R	R B G	R G B	B G R
	Even Line	R G B	B G R	G B R	R B G

Note 1: UD is an Up/Down scanning direction control pin of UPS051.
Note 2: LR is a Left/Right scanning direction control pin of UPS051.
When LR is high, the scanning direction is from “Left to Right”.
When LR is low, the scanning direction is from “Right to Left”.
Note 3: The sequence specified in each column represents the order of data which should be sent to UPS051 for cycle #1, 2, 3, 4, 5.

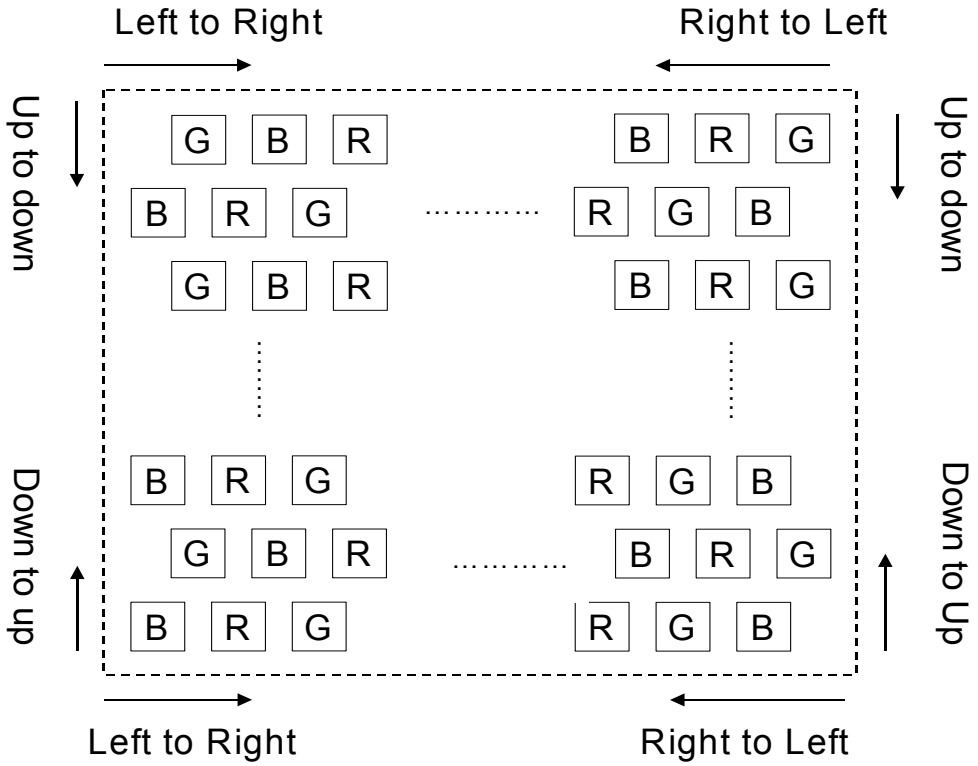

Fig. 5 1.5”/ 1.8” Color filter arrangement

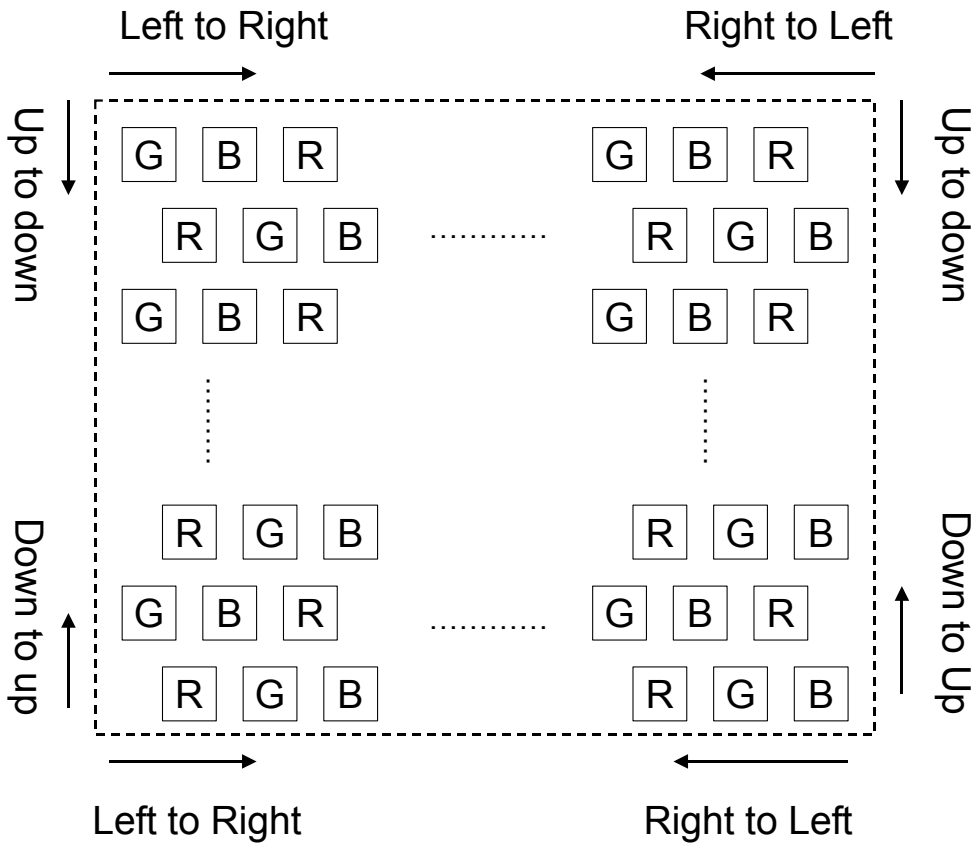

Fig.6 2.5”/ 3.5” Color filter arrangement