

# Specification

**Hilo 1-bit H36XX**

**Doc. No.: A63857-H36XX-D000-0A-7680**

**Version December 2005**

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**Title: Product Specification for Pictiva™ 96X16 OLED Module, SSD0303, Hilo 1-bit H36XX- OS096016PP08MXXB10**

<b>OSRAM</b>	<b>Opto Semiconductors Inc.</b>	<b>12/1/2005</b>	<b>A63857-H36XX-D000-0A-7680</b>
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**1. TITLE:**

1.1 Product Specification for Pictiva™ 96X16 OLED Module, SSD0303, Hilo 1-bit H36XX-OS096016PP08MXXB10

**2. REFERENCE DOCUMENTS:**

2.1 C63062-H36XX-A001-  
2.2 SSD0303

Hilo Module Product Drawing (with TAB IC)  
Solomon Systech SSD0303 96X64, Dot Matrix OLED/PLED  
Segment/Common Driver with Controller  
Remarks :  
The difference between SSD1303 and 0303 is that SSD0303 has the I<sup>2</sup>C interface feature whereas the SSD1303 only carries serial and parallel interface

**3. FEATURES, FUNCTIONS, and REQUIREMENTS****3.1 Product Summary:**

Table 3.1.1: General OLED Module Description

Display Format	96 columns x 16 rows
Pixel Pitch	0.22 (W) x 0.22 (H) mm
Pixel Size	0.19 (W) x 0.19 (H) mm
Display Diagonal	0.8"
Color	Monochrome
Grayscale	1 bit
Active Area	21.09 (W) X 3.49 (H) mm
Viewing Area	23.09 (W) X 5.49 (H) mm
Module Size	26.83 (W) X 25.3 (H) X 1.76 mm (T), TAB is foldable
Glass Size	26.83 (W) X 10.3 (H) X 1.76 (T) mm (including polarizer)
Driver IC	SSD0303
Packaging and Interconnect	TAB (TCP)
Bezel	None
OLED Power Supply	User Configurable Single or Dual voltage supplies

**3.2 Part Number:**

Table 3.2.1: Part Number Description

Part Number	Color	Factory Code
OS096016PP08MW1B10	Galaxy White	H3600
OS096016PP08MB2B10	Ocean Blue	H3610
OS096016PP08MY0B10	Elegance Yellow	H3650
OS096016PP08MG1B10	Lime Green	H3665
OS096016PP08MO1B10	Tiger Orange	H3675
OS096016PP08MO2B10	Golden Orange	H3672*

Remarks: H3672-OS096016PP08MO2B10 (Golden Orange) is an optional color, check with OSRAM for availability.

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## Electrical Characteristics

### 3.3.1.Functional Block Diagram:

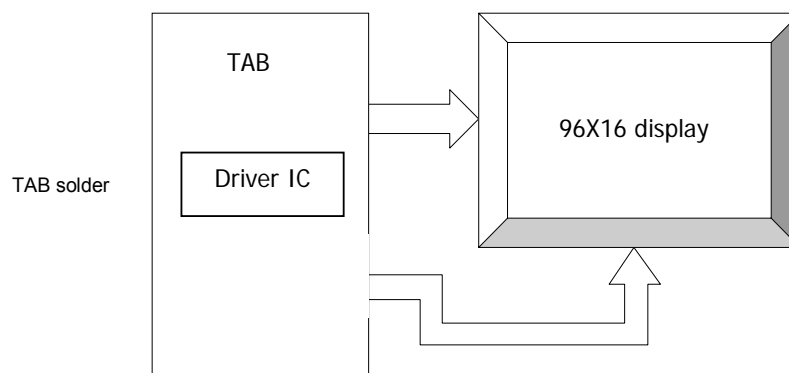


Figure 3-1: Overall block diagram of display module assembly and interface

### 3.3.2.Graphic Area Pixel Mapping:

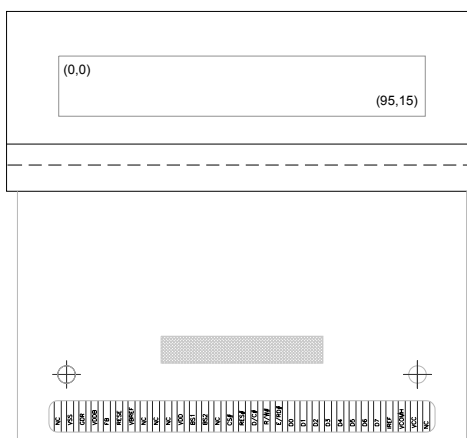


Figure 3-2: Pixel mapping

### 3.3.3. Graphic Display Data RAM (GDDRAM) access

To access display data RAM, the D/C pin should be pulled high. In SSD1303/SSD0303, the RAM is divided into eight pages, from page 0 to page 7, as shown in Figure 3-3.

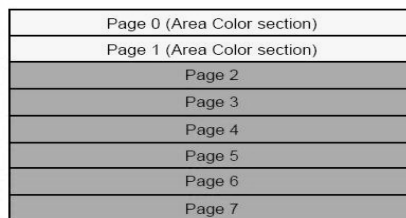


Figure 3-3: GDDRAM pages structure in SSD1303/SSD0303

In GDDRAM, page 0 and 1 are belonged to area color section with resolution 132x16. Page 2 to 7 is used for monochrome 132x48 dot matrix display.

In normal display data RAM read or write mode, the following steps are required to define the starting RAM access pointer location:

- Set the page address of the target display location by command B0h to B7h.
- Set the lower column address of pointer by command 00h~0Fh.
- Set the upper column address of pointer by command 10h~1Fh.

Let's take an example. Now page address is set to B2h, lower column address is 03h and upper column address is 00h. The RAM access pointer is located as shown in Figure 3-4. The input data byte will be written into RAM position of column 3.

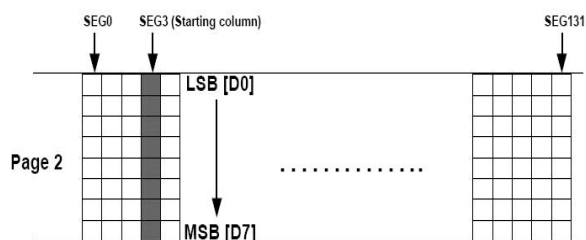


Figure 3-4. Example of GDDRAM access location setting

All the rows image data of current column are filled when one data byte is written into GDDRAM. Data bit 0 is written into the most upper row, while data bit is written into lowest row. GDDRAM column address pointer will increased by one column automatically after each data access. Users have to set a new page address, new lower and upper column address in order to access the next page RAM context.

### 3.3.4. Duty Cycle:

The pixel rows are multiplexed and will operate at a nominal duty cycle of 1/16. The default duty cycle is 1/64. During initialization a software command must be used to set the required duty cycle.

## 3.3.5.Interface Pin Out:

Table 3.3.5.1: TAB Connection Pin Out

PIN	Name	DESCRIPTION				
1	NC	No connect.				
2	VSS	Ground.				
3	GDR	Gate Drive for Multiplier. This output pin drives the gate of the external NMOS of the booster circuit.				
4	VDDb	Power supply pin for the GDR pin buffer.				
5	FB	Feedback Resistor input for Multiplier				
6	RESE	This pin connects to the source current pin of the external NMOS of the booster circuit.				
7	VBREF	Voltage Reference for Multiplier				
8	NC	No connect.				
9	NC	No connect.				
10	NC	No connect.				
11	VDD	Positive logic supply voltage.				
12	BS1	Interface Selection Pin 1: See BS2 below				
13	BS2	Interface Selection Pin 2:				
			6800 Parallel	8080 Parallel	Serial	I <sup>2</sup> C
		BS1	0	1	0	1
		BS2	1	1	0	0
14	NC (CL)	Clock Input. Not used (must be NC)				
15	CS#	Chip Select				
16	RES#	Reset				
17	D/C	HIGH = Bus contains data for DDRAM, LOW = Bus contains command.				
18	R/W (WR#)	Read/Write selector for 68 series; Write strobe for 80 series				
19	E (RD#)	E clock for 68 series; RD strobe for 80 series				
		Parallel		Serial	I <sup>2</sup> C	
20	D0	Parallel Data 0		Serial Clock	NC	
21	D1	Parallel Data 1		Data	Serial Data Input	
22	D2	Parallel Data 2		Floating	Serial Data Output	
23	D3	Parallel Data 3		NC	NC	
24	D4	Parallel Data 4		NC	NC	
25	D5	Parallel Data 5		NC	NC	
26	D6	Parallel Data 6		NC	NC	
27	D7	Parallel Data 7		NC	NC	
28	IREF	Segment (Column) Current Reference. A resistor should be connected between this pin and VSS.				
29	VCOMH	Common (Row) High Voltage, a capacitor should be connected between this pin and VSS				
30	VCC(VLL)	OLED power supply voltage VCC (VLL)				
31	NC	No connect.				

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## 3.3.6. Absolute Maximum Ratings:

Table 3.3.6.1: Absolute Maximum Ratings

Symbol	Description	Range	Unit
VDD	Supply Voltage for logic	-0.3 to +4.0	V
VCC	Supply Voltage for driver	0 to +16	V
Vin	Input Voltage	VSS-0.3 to VDD+0.4	V
Top	Operating Temperature	-30 to +70	°C
Tstg	Storage Temperature	-40 to +70	°C

3.3.7. DC Characteristics of Complete Module:  
(-20°C to +70°C Temperature Range, except as noted)

Table 3.3.7.1: Recommended DC Operating Conditions

Description		Symbol	Min.	Typ.	Max.	Unit
Logic operating voltage		VDD	2.4	3.0	3.5	V
OLED driver input voltage		VCC	8.0	9.0	10.0	V
VDD Operating Current		IDD	-	-	650	µA
VCC Operating Current		ICC	See Table below			
Driver Sleep Mode Current (at 25°C)		ISL	-	-	5.0	µA
Logic input voltage	High	VIH	.8 *VDD	-	VDD	V
	Low	VIL	0	-	.2*VDD	V
Logic output voltage	High (IOH=-.5mA)	VOH	.9 *VDD	-	VDD	V
	Low (IOL=.5mA)	VOL	0	-	.1*VDD	V

ICC Operating Current (VCC, All pixels ON, Luminance at typical value)

Color	Symbol	Min.	Typ.	Max.	Unit
Galaxy White/ Ocean Blue	ICC	4.0	4.5	5.0	mA
Elegance Yellow	ICC	2.0	2.5	3.0	mA
Elegance Yellow (High Luminance) / Lime Green / Tiger Orange/ Golden Orange	ICC	3.5	4.0	4.5	mA



3.3.8.Power Consumption: (VDD= 3.0V, VCC = 9V, Frame Frequency = 150 Hz, unless otherwise stated)

Table 3.3.8.1: Power Consumption (External Vcc mode)

Color	Typical Luminance cd/m <sup>2</sup>	Typical Power Consumption* (mW), Dual supply (VDD, VCC)				
		Power Save mode (Sleep mode)	All pixels ON @ typical brightness	10% ON @ typical brightness	10% ON @ 15% of typical	5% ON @ 15% of typical
Galaxy White	80	0.012	40	7	3	2
Ocean Blue	30	0.012	40	7	3	2
Elegance Yellow	100	0.012	22	5	2	2
Elegance Yellow (High Luminance)	200	0.012	38	7	2.5	2.5
Lime Green	120	0.012	38	7	2.5	2.5
Tiger Orange	50	0.012	38	7	2.5	2.5
Golden Orange	60	0.012	38	7	2.5	2.5

Note: For Single Supply configuration (VDD only), allow 20% higher power consumption for efficiency loss of the optional DC-DC converter.

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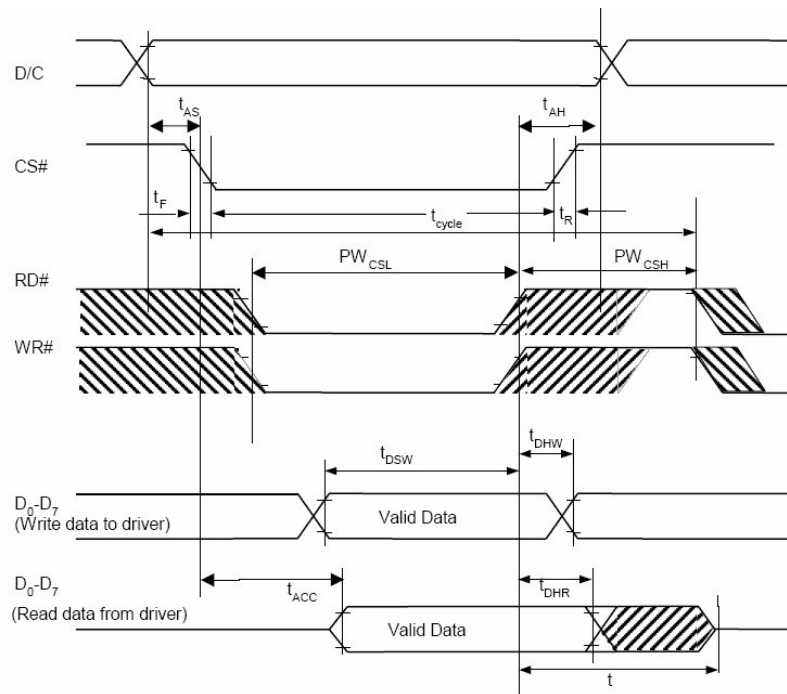


Figure 3-6: Parallel Interface Timing Diagram for 80 Series MPU

### 3.3.10. Serial Interface Timing Characteristics:

Table 3.4.10.1: Serial Interface Timing Characteristics

Description	Symbol	Min.	Typ.	Max.	Unit
Clock Cycle Time	$t_{cycle}$	250	-	-	ns
Address Setup Time	$t_{AS}$	150	-	-	ns
Address Hold Time	$t_{AH}$	150	-	-	ns
Chip Select Setup Time	$t_{CSS}$	120	-	-	ns
Chip Select Hold Time	$t_{CSH}$	60	-	-	ns
Write Data Setup Time	$t_{DSW}$	100	-	-	ns
Write Data Hold Time	$t_{DHW}$	100	-	-	ns
Clock Low Time	$t_{CLKL}$	100	-	-	ns
Clock High Time	$t_{CLKH}$	100	-	-	ns
Rise Time	$t_R$	-	-	15	ns
Fall Time	$t_F$	-	-	15	ns
Frame Frequency	$t_{FRM}$	70	75	85	Hz

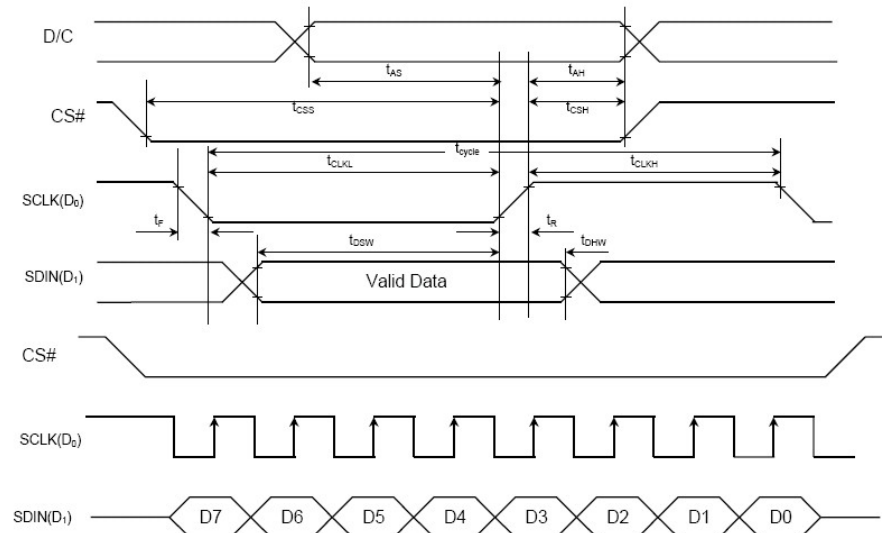
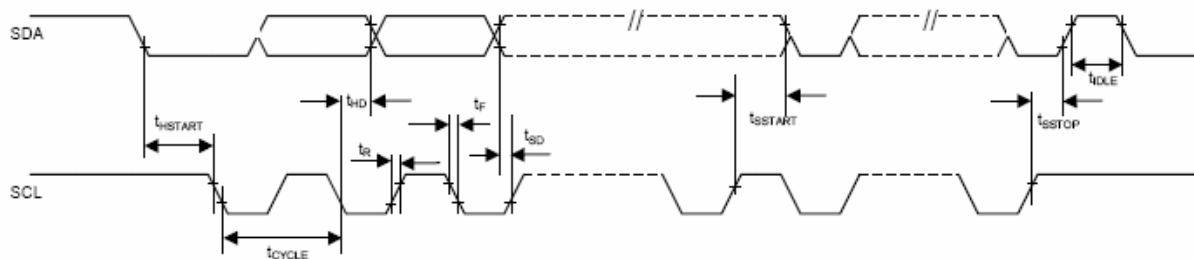


Figure 3-7: Serial Interface Timing Diagram

3.3.11. I<sup>2</sup>C Interface Timing Characteristics:Table 3.4.11.1: I<sup>2</sup>C Interface Timing Characteristics(V<sub>DD</sub>-V<sub>SS</sub>=2.4 to 3.5V, T<sub>A</sub>= -40 to 85° C)

Symbol	Parameter	Min	Typ	Max	Unit
t <sub>cycle</sub>	Clock Cycle Time	2.5	-	-	us
t <sub>HSTART</sub>	Start condition Hold Time	0.6	-	-	us
t <sub>HD</sub>	Data Hold Time	300	-	-	ns
t <sub>SD</sub>	Data Setup Time	100	-	-	ns
t <sub>SSTART</sub>	Start condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	-	us
t <sub>SSTOP</sub>	Stop condition Setup Time	0.6	-	-	us
t <sub>R</sub>	Rise Time for data and clock pin	-	-	300	ns
t <sub>F</sub>	Fall Time for data and clock pin	-	-	300	ns
t <sub>IDLE</sub>	Idle Time before a new transmission can start	1.3	-	-	us

Figure 3-8: I<sup>2</sup>C Interface Timing Diagram

### 3.4 Display Programming

#### 3.4.1. Power Up and Down Sequence

To protect the OLED panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources turn on/off.

##### 3.4.1.1 Power-Up Sequence:

1. Power-Up Vdd and wait until stable
2. Hardware reset
3. Send display off command
4. Power-Up Vcc
5. Delay 100ms (when Vcc is stable)
6. Send Display on command

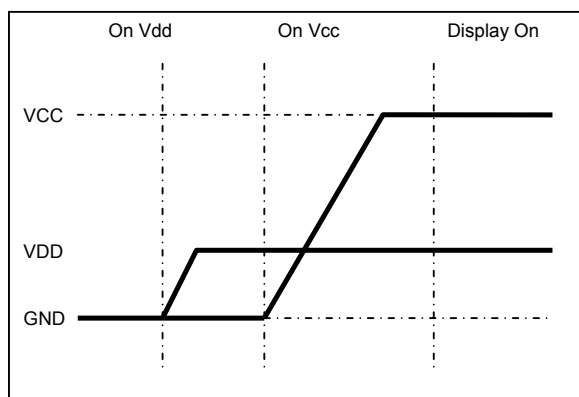


Figure 3-9. Power Up Diagram

##### 3.4.1.2 Power-Down Sequence:

1. Send Display off command
2. Power down Vcc
3. Delay 100ms (when Vcc is reach 0 and panel is completely discharges)
4. Power down Vdd

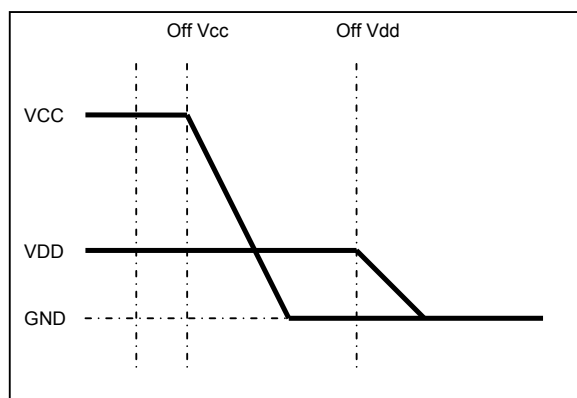


Figure 3-10. Power Down Diagram

## 3.4.2. Recommended Initialization Command

- 3.4.2.1. Refer to IC specification: Solomon SSD0303 OLED/PLED Segment/Common Driver with Controller CMOS. After power up, the commands specified in Table 1 must be executed during initialization.

Table 3.4.2.1.1: Initialization Sequence

Command	Code	Default	Initialization For Module		
Set Lower Column Address		00	04		
Set Higher Column Address		10	12		
Set Horizontal Scroll Setup	26		<sup>(1)</sup>		
Set Activate Horizontal Scroll			2F <sup>(2)</sup>		
Set Deactivate Horizontal Scroll			2E <sup>(3)</sup>		
Set Contrast Control	81	80	15 <sup>(7) (*)</sup>	2B <sup>(8) (*)</sup>	30 <sup>(9) (*)</sup>
Set Brightness For Color Banks	82	80	Default		
Set Look Up Table (LUT) For Area Color	91		<sup>(4)</sup>		
Set Bank Color Of For Bank 1-16 (Page 0)	92		<sup>(5)</sup>		
Set Bank Color Of For Bank 17-32 (Page 1)	93		<sup>(6)</sup>		
Set Segment Re-map		A0	A1		
Set Display Start Line		40	Default		
Set Display Offset	D3	00	Default		
Set Multiplex Ratio	A8	3F	0F		
Set Entire Display ON / OFF		A4	default		
Set Normal / Inverse Display		A6	default		
Set Display On/Off		AE	AF		
Set Page Address		B0-B7	B0-B1		
Set COM Output Scan Direction		C0	C8		
Set Clock Divide	D5	70	72		
Set Area Color Mode ON / OFF	D8	00	default		
Set Pre-Charge Period	D9	22	default		
Set COM Pins Hardware Configuration	DA	12	default		
Set VCOM Level	DB	35	04 <sup>(7) (*)</sup>	0F <sup>(8) (*)</sup>	34 <sup>(9) (*)</sup>
			<b>Single Supply (VDD) - Internal VCC</b>		
Set DC-DC ON / OFF	AD	8B	Default		
			<b>Dual Supply (VDD, VCC) - External VCC</b>		
Set DC-DC ON / OFF	AD	8B	8A		

(\*)- This setting represents maximum luminance for proper operation of the display. Lower setting can be used for dimming. Higher setting will adversely affect the operating lifetime as defined in this specification.

<sup>(1)</sup>. This command is used to setup the horizontal scrolling.

<sup>(2)</sup>. This command is used to activate the horizontal scrolling.

<sup>(3)</sup>. This command is used to deactivate the horizontal scrolling.

<sup>(4, 5, 6)</sup>. This command is not used (A different kind of Area color mode)

<sup>(7)</sup>. Elegance Yellow Product

<sup>(8)</sup>. Elegance Yellow (High Luminance), Lime Green, Tiger Orange, and Golden Orange Products

<sup>(9)</sup>. Galaxy White and Ocean Blue Products

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### 3.4.3 Sample Initialization Code

```

/*****
// SSD1303 Initialization Command
*****/
// Lower Column Address
WriteCommand(0x04); /* Set Lower Column Address */
// High Column Address
WriteCommand(0x12); /* Set Higher Column Address
*/
// Display Start Line
WriteCommand(0x40); /* Set Display Start Line */
// Contrast Control Register
WriteCommand(0x81); /* Set Contrast Control */
WriteCommand(0x2B); /* 0 ~ 127 (1) */
// Re-map
WriteCommand(0xA1); /* [A0]:column address 0 is
map to SEG0 , [A1]: column
address 131 is map to SEG0*/
// Entire Display ON/OFF
WriteCommand(0xA4); /* A4=ON */
// Normal or Inverse Display
WriteCommand(0xA6); /* Normal Display*/
// Multiplex Ratio
WriteCommand(0xA8); /* Set Multiplex Ratio */
WriteCommand(0x0F); /* Set to 16 Mux*/
// Set DC-DC
WriteCommand(0x8A); /* Set DC-DC */
/* 8B=ON, 8A=OFF */
// Display ON/OFF
WriteCommand(0xAF); /* AF=ON , AE=OFF*/
// Display Offset
WriteCommand(0xD3); /* Set Display Offset */
WriteCommand(0x00); /* No offset */
// Display Clock Divide
WriteCommand(0x72); /* Set Clock Divide */
/* Set to 150Hz */
// Area Color Mode
WriteCommand(0xD8); /* Set Area Color On or Off */
WriteCommand(0x00); /* Mono Mode */
// COM Pins Hardware Configuration
WriteCommand(0x12); /* Set Pins Hardware
Configuration */
// VCOMH
WriteCommand(0xDB); /* Set VCOMH (2) */
WriteCommand(0x0F);

```

- (1). The code for Contrast Control for Galaxy White and Ocean Blue Products = 30;  
 Elegance Yellow Product = 15;  
 Elegance Yellow (High Luminance), Lime Green, Tiger Orange, and Golden Orange Products = 2B.

- (2). The code for setting VCOM Level for Galaxy White and Ocean Blue Products = 34;  
 Elegance Yellow Product = 04;  
 Elegance Yellow (High Luminance), Lime Green, Tiger Orange, and Golden Orange Products = 0F.



### 3.4.4.MPU Serial Interface

The serial interface consists of serial clock SCLK, serial data SDIN, D/C#, CS#. In ISPI mode, D0 acts as SCLK, D1 acts as SDIN. For the unused data pins, D2 pin should be left open. D3 to D7, E and R/W pin can be connected to external ground.

SDIN is shifted into an 8-bit shift register on every rising edge of SCLK in the order of D7, D6 ... D0. D/C# sampled on every eighth clock and the data byte in the shift register is written to the Display Data RAM command register in the same clock.

During data writing, an additional NOP command should be inserted before the CS# goes high (Refer to Figure 3-11)

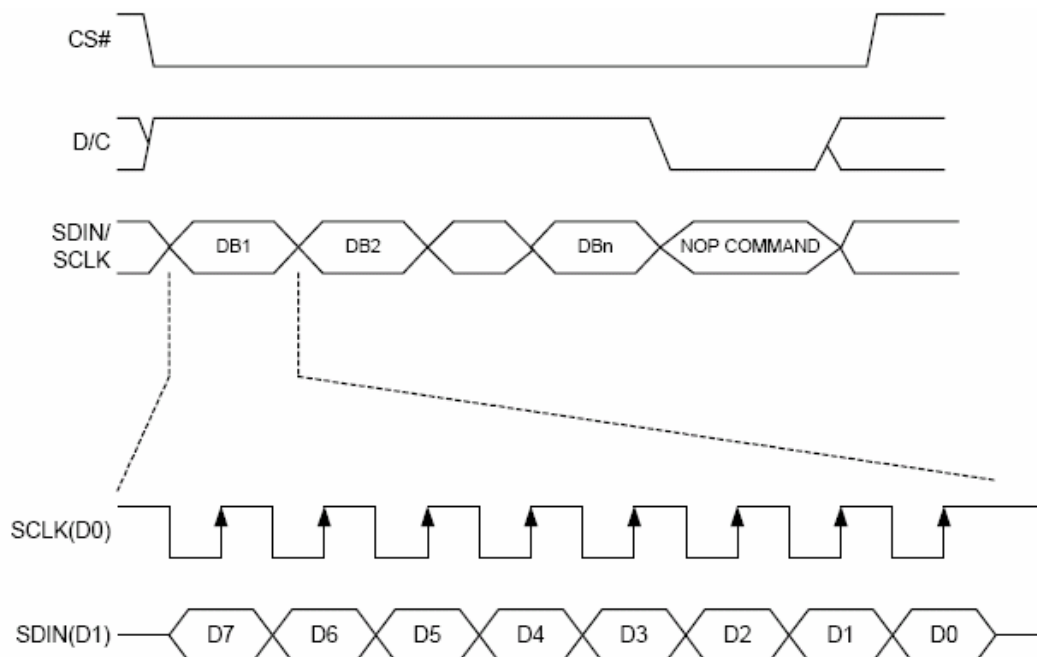


Figure 3-11: Display data write procedure in SPI mode

Note: Below is the sample command to be inserted before the CS# goes high.

```
for (i=0;i<96;i++) /* 96 COLUMN */
{
WriteData(0xFF); /* ALL PIXEL ON */
}
WriteCommand(0xE3); /* NOP COMMAND */
```

### 3.5 OPTICAL CHARACTERISTICS: (Ta = 25°C, unless otherwise stated)

Table 3.5.1: Optical & Operating Lifetime Characteristics

	Condition	Min.	Typ.	Max.	Unit
Contrast Ratio	$\theta = \phi = 0^\circ$ , Dark	-	2000	-	-
	Direct Sun Light	1.05	-	-	
Brightness Uniformity	$\theta = \phi = 0^\circ$	-	-	+20	%
Visible Flicker	$\theta = \phi = 0^\circ$	-	None	-	-
Cross Talk (Brightness variation of non-selected pixels)	$\theta = \phi = 0^\circ$	-	-	10	%

Product	Color	X color coordinate, 1931CIE $\pm 0.02$	Y color coordinate, 1931CIE $\pm 0.02$	Initial Luminance, $\text{cd/m}^2$			Operating Life*, hour, @ 25°C
				Min.	Typ.	Max.	
H3600-OS096016PP08MW1B10	Galaxy White	0.245 $\pm$ 0.030	0.250	70	80	90	-
H3610-OS096016PP08MB2B10	Ocean Blue	0.140	0.170	20	30	40	-
H3650-OS096016PP08MY0B10	Elegance Yellow	0.460	0.540	90	100	140	40K
H3650-OS096016PP08MY0B10 Programmed to higher luminance	Elegance Yellow	0.460	0.540	180	200	280	10K
H3665-OS096016PP08MG1B10	Lime Green	0.370	0.620	100	120	140	10K
H3675-OS096016PP08MO1B10	Tiger Orange	0.630	0.370	40	50	60	10K
H3672-OS096016PP08MO2B10	Golden Orange	0.600	0.400	50	60	70	10K

\*Operating Lifetime is Time to Half Luminance; based on the display operated at 25°C at typical brightness level with specified software settings, until 50% of initial luminance is reached.

#### 3.5.1 Polarizing Angle:

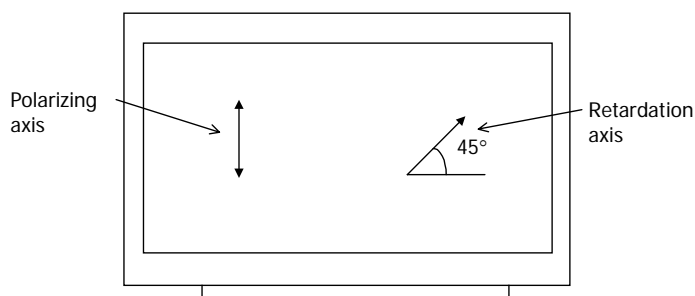


Figure 3-12: Orientation of OLED polarizer angle

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### 3.5.2 MECHANICAL CHARACTERISTICS:

3.5.2.1 Interconnections: The display module should be electrically connected to the user's board by soldering or hotbar reflow.

3.5.2.2 Product Marking: Parts are marked with a label on the module

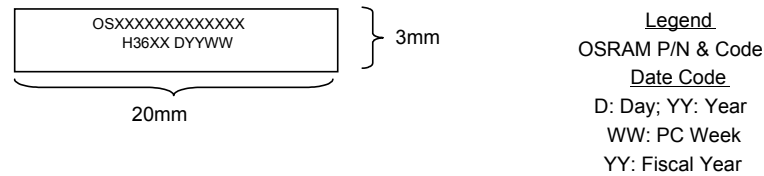
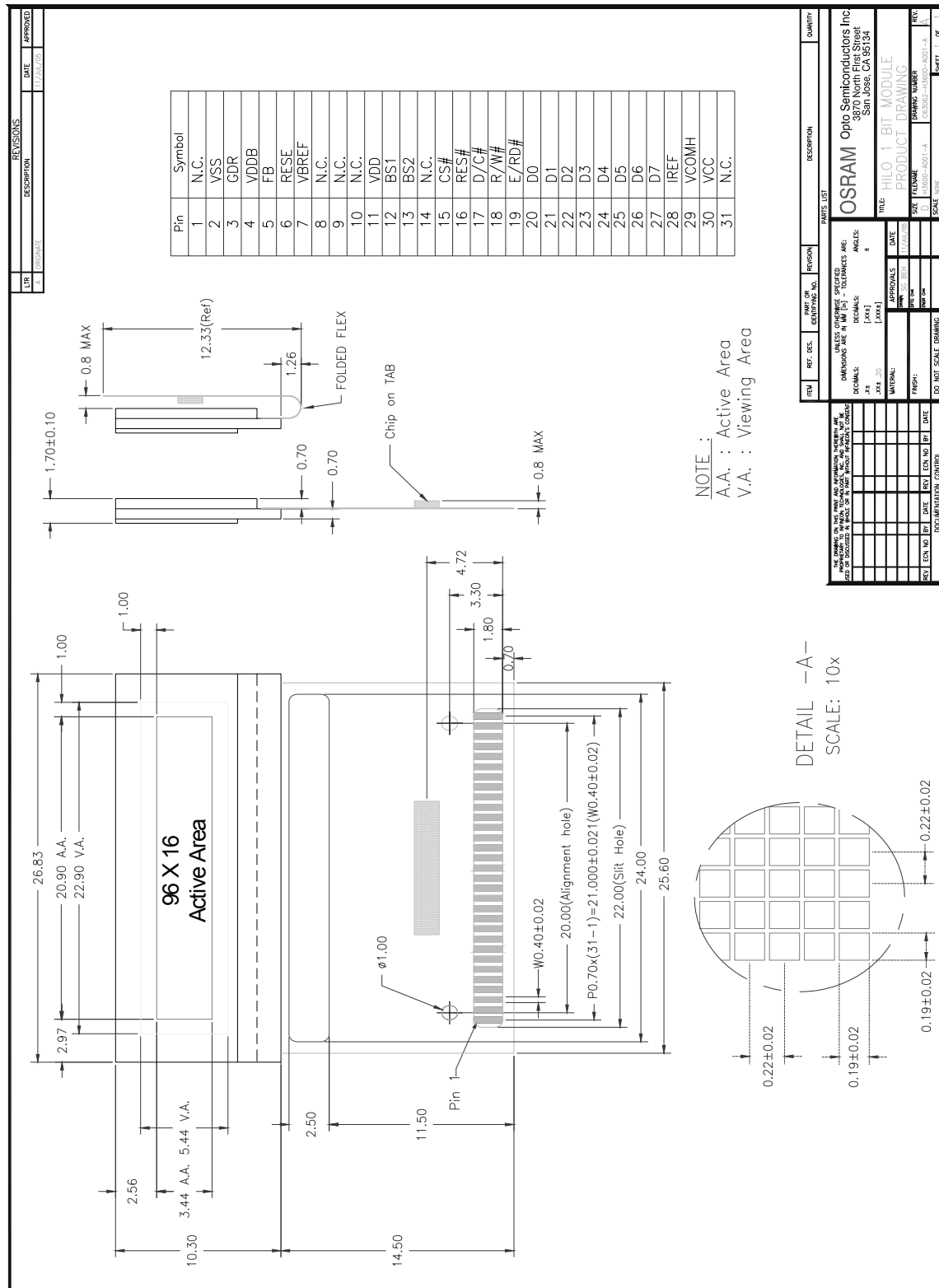


Figure 3-13: Description of part label marking requirements

### 3.6 MODULE MECHANICAL DRAWINGS:

The mechanical drawing shown in Figure 3-14 is for reference.

Figure 3-14: Hilo Module drawing

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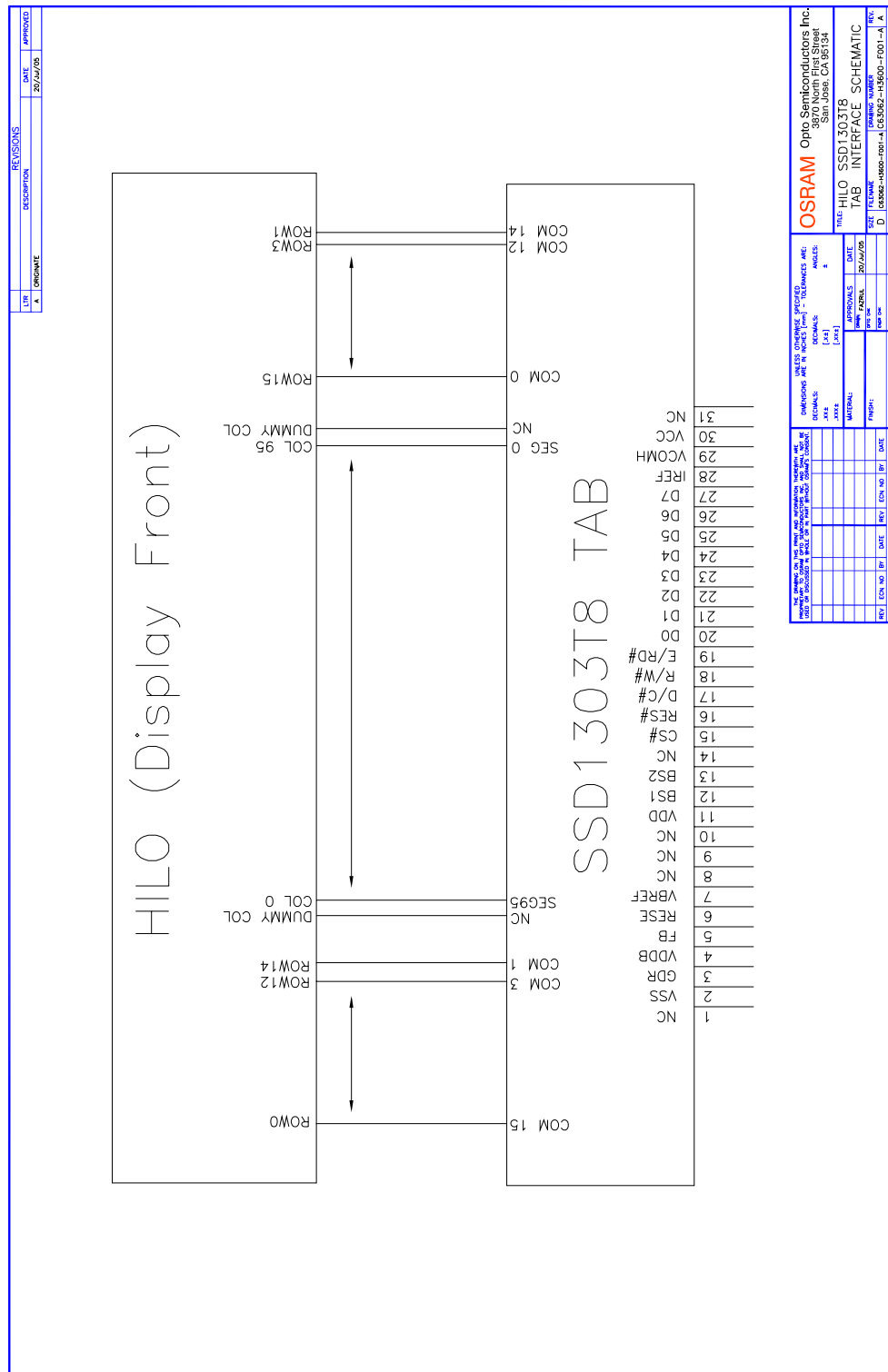
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## 4 SCHEMATIC DRAWING

Figure 4-1: Hilo SSD0303 TAB Interface Schematic



Remarks : SSD0303 is labeled with SSD1303T8 on TAB

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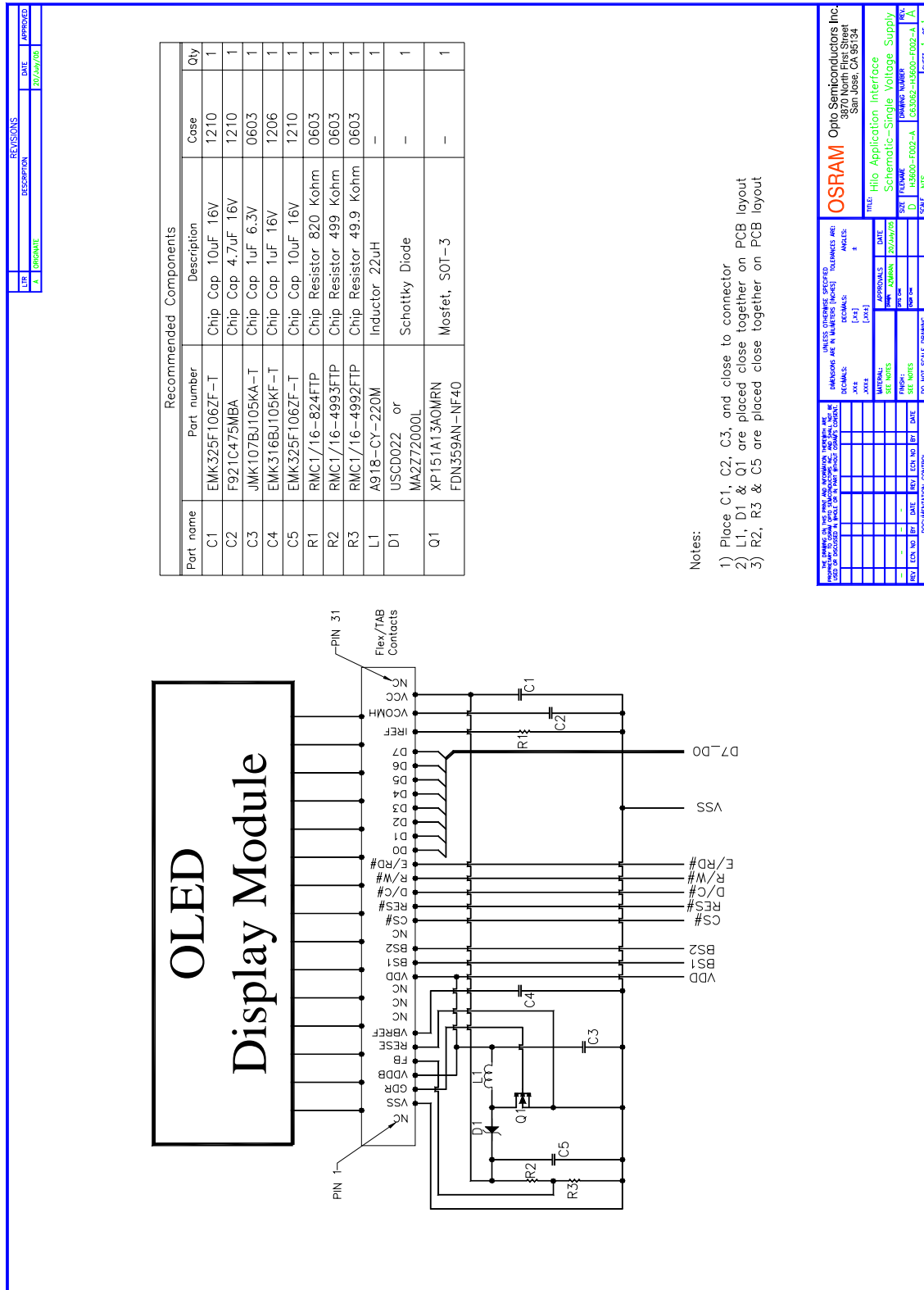
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Figure 4-2 Hilo Application Interface Schematic – Single Voltage Supply



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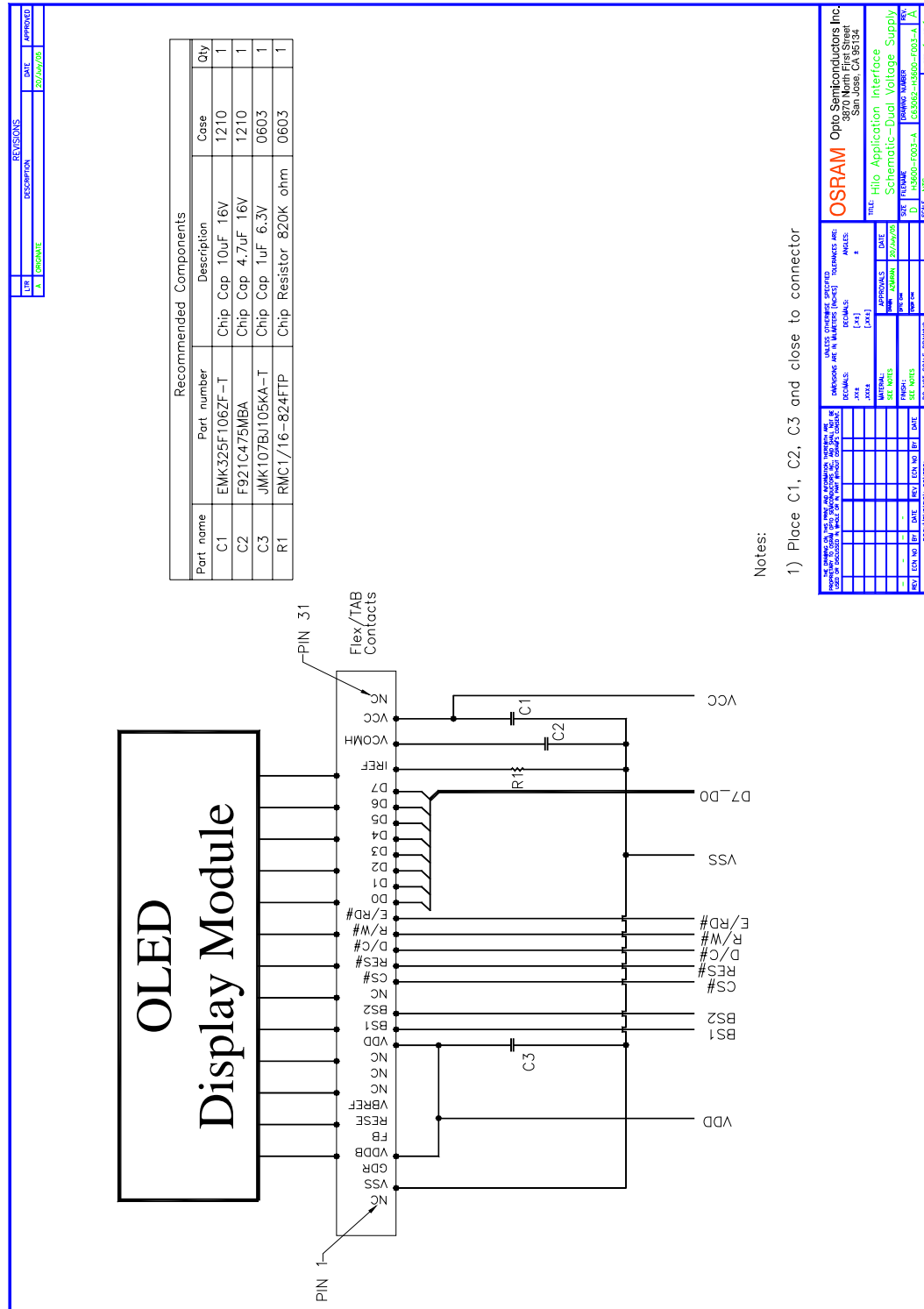
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Figure 4-3 Hilo Application Interface Schematic – Dual Voltage Supply



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## 5 QUALIFICATION TESTS:

- 5.1 For reference, the main qualification tests and test criteria done on the OLED module are indicated below in Table 5.1.1 and 5.1.2 respectively.

Table 5.1.1 OLED Module Internal Qualification Tests

Test	Condition	Duration	
		Elegance Yellow, Light Green, Tiger Orange, Golden Orange, Lime Green	Galaxy White/ Ocean Blue
High Temperature and Humidity Bias (THB)*	60°C / 90% RH	250 hrs	-
High Temperature Operating (ELT)*	70°C	336 hrs	-
High Temperature and Humidity unbiased (THS)*	60°C / 90% RH	-	250 hrs unbiased
Powered Temperature Cycle (PTC)*	-30°C / 70°C; 30 min. dwell time; 15 min. transition time	60 cycles	
Thermal Shock (TSK)	-40°C / 85°C; 45 min. dwell time; 15 sec. Transition time	100 cycles	
Low Temperature Storage (LTS)	-40°C	336 hrs	
High Temperature Storage (HTS)	70°C	336 hrs	
Low Air Pressure LAT **	15kPa 25°C (0.15bar)	16hrs	
Mechanical Vibration **	10-58hz 0.75mm 58-150Hz 10g, 1oct/min	10 sweeps per X, Y, Z direction	
Mechanical Shock **	11ms half sine 100g peak	6 shocks per X, Y, Z direction	
Mechanical Bump **	6ms half sine 40g Peak	1000 bumps per X, Y, Z direction	

\* **Note 1:** The modules are powered for these tests, with a standard OSRAM pattern (50% emission ratio)

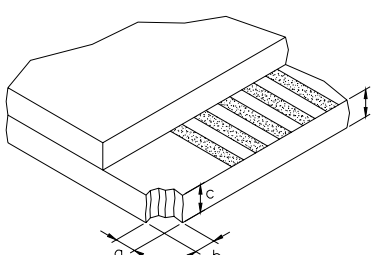
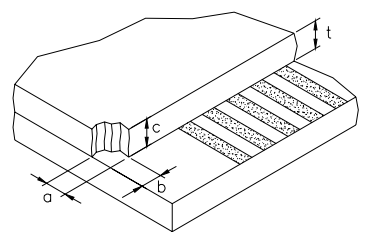
\*\* **Note 2:** These mechanical tests may not be performed on the specific part numbers in this specification.

Table 5.1.2: OLED Module Qualification Test Criteria

Acceptance Criteria (without polarizer):	Test Patterns for Powered Tests:
< 50% luminance loss after test	Checkerboard pattern
5 point luminance uniformity <20%	Inverse Checkerboard pattern
No mechanical failure	All pixels On
No electrical failure	All pixels Off
Pixel gap (initial + growth) $\leq$ 30%	



## 6 COSMETIC CRITERIA:

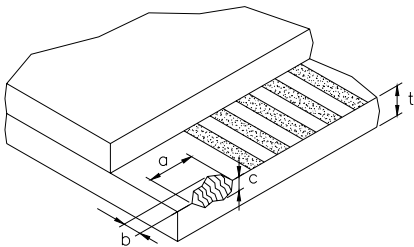
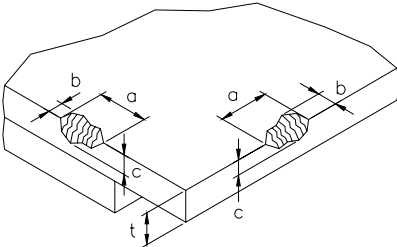
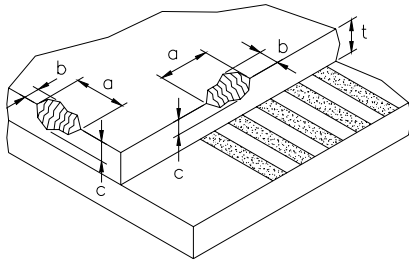
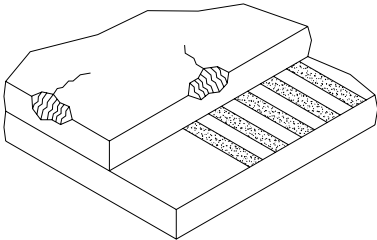
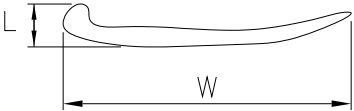
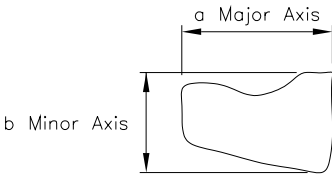
Items	Criterion for Defects	Defect Type								
Black / bright spot, particle, pin-hole (on the glass / polarizer), dent on polarizer	<p>Within Viewing Area</p> <table><tr><th>Size <math>\Phi</math> (mm)</th><th>Acceptable number</th></tr><tr><td><math>\Phi \leq 0.1</math></td><td>Not counted</td></tr><tr><td><math>0.1 \leq \Phi \leq 0.2</math></td><td>3</td></tr><tr><td><math>\Phi &gt; 0.2</math></td><td>0</td></tr></table> <p>* <math>\Phi = (\text{Long diameter} + \text{Short diameter})/2</math></p>	Size $\Phi$ (mm)	Acceptable number	$\Phi \leq 0.1$	Not counted	$0.1 \leq \Phi \leq 0.2$	3	$\Phi > 0.2$	0	Minor
Size $\Phi$ (mm)	Acceptable number									
$\Phi \leq 0.1$	Not counted									
$0.1 \leq \Phi \leq 0.2$	3									
$\Phi > 0.2$	0									
Scratches / lines on the polarizer	<p>Within Viewing Area</p> <table><tr><th>Size <math>\Phi</math> (mm)</th><th>Acceptable number</th></tr><tr><td><math>W \leq 0.1</math></td><td>Not counted</td></tr><tr><td><math>L \leq 2, 0.1 &lt; W \leq 0.2</math></td><td>3</td></tr><tr><td><math>W &gt; 0.2</math></td><td>0</td></tr></table>	Size $\Phi$ (mm)	Acceptable number	$W \leq 0.1$	Not counted	$L \leq 2, 0.1 < W \leq 0.2$	3	$W > 0.2$	0	Minor
Size $\Phi$ (mm)	Acceptable number									
$W \leq 0.1$	Not counted									
$L \leq 2, 0.1 < W \leq 0.2$	3									
$W > 0.2$	0									
Polarizer Bubble	<p>Reject if bubble is observed with naked eyes at 30cm distance. with the following criteria</p> <p>Within Viewing Area</p> <table><tr><th>Size <math>\Phi</math> (mm)</th><th>Acceptable number</th></tr><tr><td><math>\Phi \leq 0.2</math></td><td>Not counted</td></tr><tr><td><math>0.2 \leq \Phi \leq 0.3</math></td><td>3</td></tr><tr><td><math>0.3 &lt; \Phi</math></td><td>0</td></tr></table> <p>Outside Viewing Area – <b>IGNORE</b></p>	Size $\Phi$ (mm)	Acceptable number	$\Phi \leq 0.2$	Not counted	$0.2 \leq \Phi \leq 0.3$	3	$0.3 < \Phi$	0	Minor
Size $\Phi$ (mm)	Acceptable number									
$\Phi \leq 0.2$	Not counted									
$0.2 \leq \Phi \leq 0.3$	3									
$0.3 < \Phi$	0									
Polarizer coverage	Reject if the polarizer does not cover the Viewing Area.	Minor								
Corner Chip	<p><b>Criteria for Corner Chip</b></p> <p>t = Glass thickness</p> <p><b>Accept If</b></p> <p>a ≤ 1.5 mm or</p> <p>b ≤ 1.5 mm</p> <p>c ≤ t</p> 	Minor								
Corner Chip	<p><b>Accept If</b></p> <p>a ≤ 3.0 mm</p> <p>or</p> <p>b ≤ 3.0 mm</p> 	Minor								

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Chip on contact pad	<b>Criteria for Chips on contact pad</b> $t$ = Glass thickness Accept if $b \leq 1/3$ width of contact ledge		Minor
Chip on Face of Display	<b>Criteria for Chips on Face of Display</b> Accept if $b \leq 1.5\text{mm}$		Minor
Chip on Back of Display	<b>Criteria for Chips on Back of Display</b> Accept if $b \leq 3.0\text{ mm}$		Minor
Chip with crack	<b>No crack allowed</b>		Major
<b>Definition of W &amp; L &amp; <math>\phi</math> (Unit: mm)</b> <div style="display: flex; align-items: center; justify-content: space-around;"> <div style="text-align: center;">  </div> <div style="text-align: center;">  </div> <div> <math>\phi = \frac{(a+b)}{2}</math> </div> </div> <p><b>Note: Distance between any two defects should be over 5 mm</b></p>			

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