MF1511-03

S1D15714 Series

Rev. 1.0

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Contents

1. DESCRIPTION

The S1D15714 Series is a single chip MLS driver for dot matrix liquid crystal displays which can be directly connected to the microcomputer bus. It accepts the 8-bit parallel or serial display data from the microcomputer to store the data in the on-chip display data RAM, and issues liquid crystal drive signals independently of the microcomputer.

The S1D15714 Series incorporates a display data RAM (65 × 168 bits), 1 bit of the on-chip RAM respond to one-dot pixels.

The S1D15714 Series features 65 common output circuits and 168 segment output circuits. A single chip provides a display of 10 characters by 4 lines with 65 × 168 dots (16 × 16 dots) and display of 14 characters by 5 lines by the 12 × 12 dot-character font.

The S1D15714 Series incorporates the analog temperature sensor circuit that changes output voltage depending on ambient temperature and can be used to constitute a system to provide optimum LCD contrast throughout a wide temperature range without need for use of supplementary parts such as the thermistor, under controls of a micro computer.

Display data RAM read/write operations do not require operation clock from outside, thereby ensuring operation with the minimum current consumption. Furthermore, it incorporates a LCD-drive power supply characterized by low power consumption and a CR oscillator circuit for display clock; therefore, the display system of a handy and high-performance instrument can be realized by use of the minimum current consumption and minimum chip configuration.

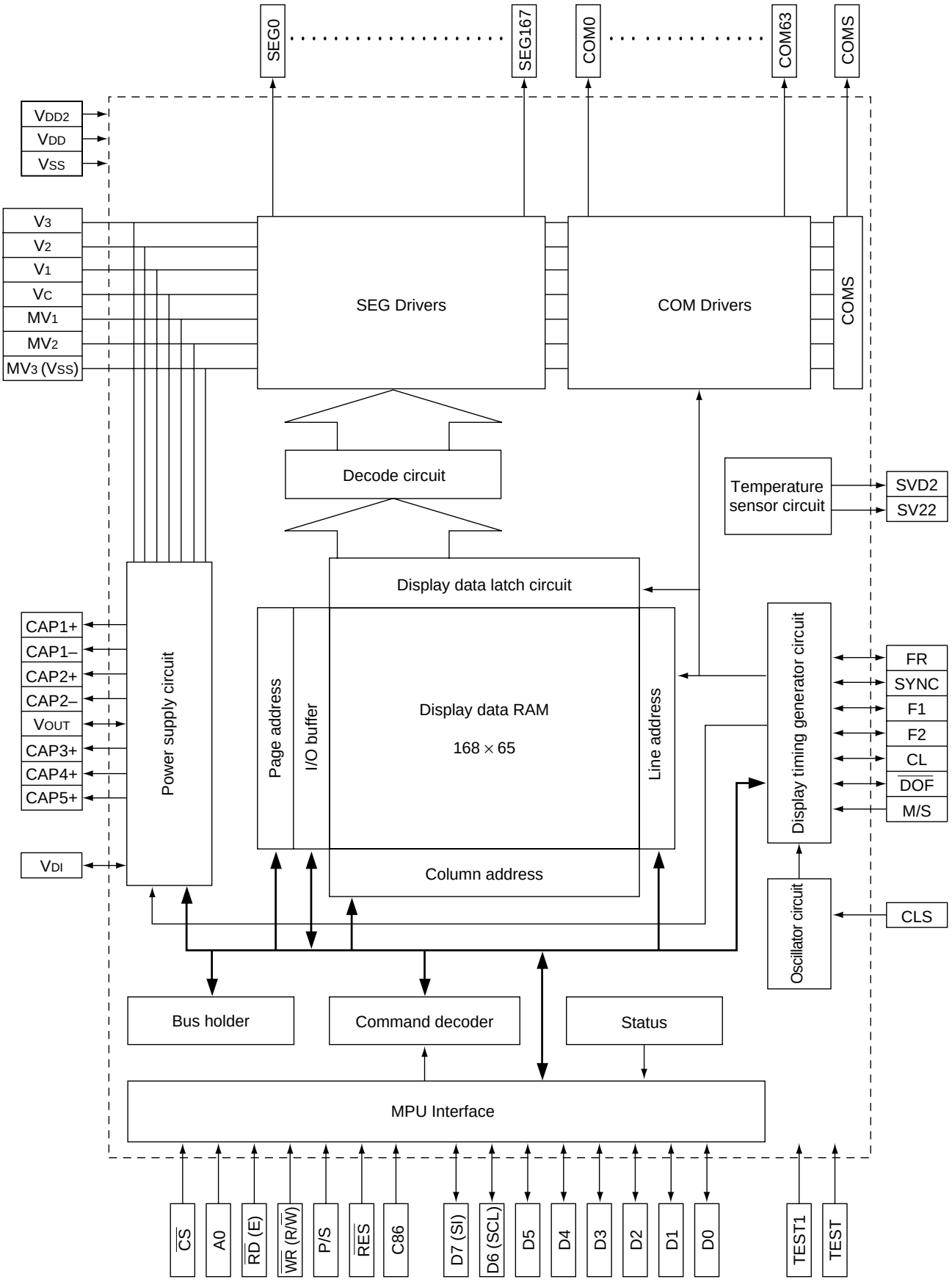
2. FEATURES

- Direct RAM data display by display data RAM
  Normally white display is in normal mode
  RAM bit data
  "1" : On and black
  "0" : Off and white
- RAM capacity
  65 × 168 = 10,920 bits
- Liquid crystal drive circuit
  65 common outputs and 168 segment outputs
- High-speed 8-bit MPU interface (directly connectable to the MPUs of both 80/68 series) /serial interface possible
- A variety of command functions
  n-line reversal, display data RAM address control, display ON/OFF, display normal/reverse rotation, display all lighting ON/OFF, liquid crystal drive power supply circuit control, display clock built-in oscillator circuit control
- MLS drive technology
  Built-in high precision voltage regulation function
- High precision CR oscillator circuit incorporated
- Low power consumption
- Built-in temperature sensor circuit
- Power supply
  Logic power supply 1: $V_{DI} - V_{SS}$ = 2.7 V to 3.3 V
  Logic power supply 2: $V_{DD} - V_{SS}$ = 2.7 V to 5.5 V
  Liquid crystal drive power supply: $V_3 - V_{SS}$ = 5.6 to 16.2 V
  Boosting power supply: $V_{DD2} - V_{SS} = V_{DD}$ to 5.5 V
- Wide operation temperature range: –40 to 85°C
- CMOS process
- Shipping form : Bare chips
- Light and radiation proof measures are not taken in designing.

Series specifications

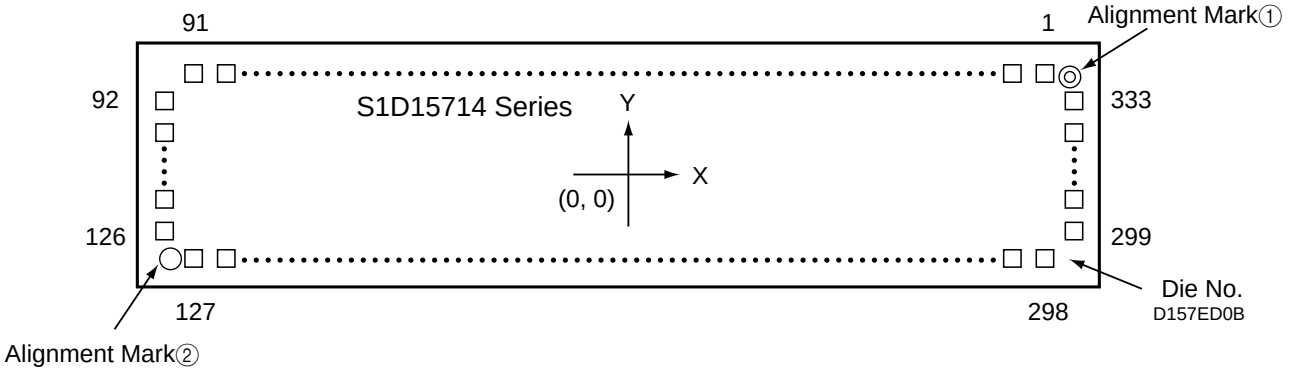
Product name	Form of shipping	Chip thickness
S1D15714D00B000	Bare chip	0.625mm

3. BLOCK DIAGRAM



4. PIN ASSIGNMENT

4.1 Chip Assignment

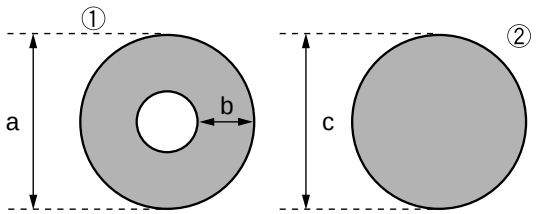


Item		Size X	×	Size Y	Unit
Chip size		11.20	×	2.27	mm
Chip thickness		0.625			mm
Bump pitch		51 (Min.)			µm
Bump size	PAD No.1, 2, 13, 16, 29, 91	36	×	84	µm
	PAD No.3 to 12, 14, 15, 17 to 28, 30 to 90	81	×	84	µm
	PAD No.92 to 126, 299 to 333	85	×	34	µm
	PAD No.127 to 298	42	×	85	µm
Bump height		17 (Typ.)			µm

4.2 Alignment mark

Alignment coordinate
- ① (5364, 975) µm
- ② (–5415, –942) µm

Mark size
- a = 70.5 µm
- b = 20.3 µm
- c = 79.5 µm



4.3 Pad Center Coordinates

Unit: µm

PAD No.	Pin Name	X	Y
1	NC	4986	982
2	V_{DD}	4935	
3	TEST1	4856	
4	SYNC	4750	
5	FR	4643	
6	$\overline{CL}$	4537	
7	$\overline{DOF}$	4430	
8	F1	4324	
9	$\overline{F2}$	4217	
10	$\overline{CS}$	4111	
11	$\overline{RES}$	4004	
12	A0	3898	
13	V_{SS}	3819	
14	$\overline{WR}$,R/$\overline{W}$	3740	
15	$\overline{RD}$,E	3634	
16	V_{DD}	3555	
17	D0	3476	
18	D1	3370	
19	D2	3263	
20	D3	3157	
21	D4	3050	
22	D5	2944	
23	D6, SCL	2837	
24	D6, SCL	2731	
25	D7, SI	2624	
26	D7, SI	2518	
27	V_{DI}	2411	
28	V_{DI}	2305	
29	V_{DD}	2226	
30	M/S	2147	
31	CLS	2041	
32	V_{SS}	1934	
33	V_{SS}	1828	
34	V_{SS}	1721	
35	V_{SS}	1615	
36	TEST	1508	
37	C86	1402	
38	P/S	1295	
39	V_{DD}	1189	
40	V_{DD}	1082	
41	V_{DD}	976	
42	V_{DD}	869	
43	V_{DD2}	763	
44	V_{DD2}	656	
45	V_{DD2}	550	
46	V_{DD2}	443	
47	V_{OUT}	–302	
48	V_{OUT}	–409	
49	V_{OUT}	–515	
50	CAP1+	–622	

PAD No.	Pin Name	X	Y
51	CAP1+	–728	982
52	CAP1+	–835	
53	CAP1–	–941	
54	CAP1–	–1048	
55	CAP1–	–1154	
56	CAP3+	–1261	
57	CAP3+	–1367	
58	CAP3+	–1474	
59	CAP5+	–1580	
60	CAP5+	–1687	
61	CAP5+	–1793	
62	V_{OUT}	–1900	
63	CAP4+	–2006	
64	CAP4+	–2113	
65	CAP4+	–2219	
66	CAP2–	–2326	
67	CAP2–	–2432	
68	CAP2–	–2539	
69	CAP2+	–2645	
70	CAP2+	–2752	
71	CAP2+	–2858	
72	V_3	–2965	
73	V_3	–3071	
74	V_2	–3178	
75	V_2	–3284	
76	V_1	–3391	
77	V_1	–3497	
78	V_C	–3604	
79	V_C	–3710	
80	MV_1	–3817	
81	MV_1	–3923	
82	MV_2	–4030	
83	MV_2	–4136	
84	V_{SS}	–4243	
85	V_{SS}	–4349	
86	V_{SS}	–4456	
87	V_{DD}	–4562	
88	NC	–4669	
89	SVD2	–4775	
90	SV22	–4882	
91	NC	–4961	
92	NC	–5449	922
93	COM31		871
94	COM30		820
95	COM29		769
96	COM28		718
97	COM27		667
98	COM26		616
99	COM25		565
100	COM24		514

PAD No.	Pin Name	X	Y
101	COM23	–5449	463
102	COM22		412
103	COM21		361
104	COM20		310
105	COM19		259
106	COM18		208
107	COM17		157
108	COM16		106
109	COM15		55
110	COM14		4
111	COM13		–47
112	COM12		–98
113	COM11		–149
114	COM10		–200
115	COM9		–251
116	COM8		–302
117	COM7		–353
118	COM6		–404
119	COM5		–455
120	COM4		–506
121	COM3		–557
122	COM2		–608
123	COM1		–659
124	COM0		–710
125	COMS		–761
126	NC		–812
127	NC	–5130	–982
128	NC	–5070	
129	SEG0	–5010	
130	SEG1	–4950	
131	SEG2	–4890	
132	SEG3	–4830	
133	SEG4	–4770	
134	SEG5	–4710	
135	SEG6	–4650	
136	SEG7	–4590	
137	SEG8	–4530	
138	SEG9	–4470	
139	SEG10	–4410	
140	SEG11	–4350	
141	SEG12	–4290	
142	SEG13	–4230	
143	SEG14	–4170	
144	SEG15	–4110	
145	SEG16	–4050	
146	SEG17	–3990	
147	SEG18	–3930	
148	SEG19	–3870	
149	SEG20	–3810	
150	SEG21	–3750	

Unit: µm

PAD No.	Pin Name	X	Y
151	SEG22	–3690	–982
152	SEG23	–3630	
153	SEG24	–3570	
154	SEG25	–3510	
155	SEG26	–3450	
156	SEG27	–3390	
157	SEG28	–3330	
158	SEG29	–3270	
159	SEG30	–3210	
160	SEG31	–3150	
161	SEG32	–3090	
162	SEG33	–3030	
163	SEG34	–2970	
164	SEG35	–2910	
165	SEG36	–2850	
166	SEG37	–2790	
167	SEG38	–2730	
168	SEG39	–2670	
169	SEG40	–2610	
170	SEG41	–2550	
171	SEG42	–2490	
172	SEG43	–2430	
173	SEG44	–2370	
174	SEG45	–2310	
175	SEG46	–2250	
176	SEG47	–2190	
177	SEG48	–2130	
178	SEG49	–2070	
179	SEG50	–2010	
180	SEG51	–1950	
181	SEG52	–1890	
182	SEG53	–1830	
183	SEG54	–1770	
184	SEG55	–1710	
185	SEG56	–1650	
186	SEG57	–1590	
187	SEG58	–1530	
188	SEG59	–1470	
189	SEG60	–1410	
190	SEG61	–1350	
191	SEG62	–1290	
192	SEG63	–1230	
193	SEG64	–1170	
194	SEG65	–1110	
195	SEG66	–1050	
196	SEG67	–990	
197	SEG68	–930	
198	SEG69	–870	
199	SEG70	–810	
200	SEG71	–750	

PAD No.	Pin Name	X	Y
201	SEG72	–690	–982
202	SEG73	–630	
203	SEG74	–570	
204	SEG75	–510	
205	SEG76	–450	
206	SEG77	–390	
207	SEG78	–330	
208	SEG79	–270	
209	SEG80	–210	
210	SEG81	–150	
211	SEG82	–90	
212	SEG83	–30	
213	SEG84	30	
214	SEG85	90	
215	SEG86	150	
216	SEG87	210	
217	SEG88	270	
218	SEG89	330	
219	SEG90	390	
220	SEG91	450	
221	SEG92	510	
222	SEG93	570	
223	SEG94	630	
224	SEG95	690	
225	SEG96	750	
226	SEG97	810	
227	SEG98	870	
228	SEG99	930	
229	SEG100	990	
230	SEG101	1050	
231	SEG102	1110	
232	SEG103	1170	
233	SEG104	1230	
234	SEG105	1290	
235	SEG106	1350	
236	SEG107	1410	
237	SEG108	1470	
238	SEG109	1530	
239	SEG110	1590	
240	SEG111	1650	
241	SEG112	1710	
242	SEG113	1770	
243	SEG114	1830	
244	SEG115	1890	
245	SEG116	1950	
246	SEG117	2010	
247	SEG118	2070	
248	SEG119	2130	
249	SEG120	2190	
250	SEG121	2250	

PAD No.	Pin Name	X	Y
251	SEG122	2310	–982
252	SEG123	2370	
253	SEG124	2430	
254	SEG125	2490	
255	SEG126	2550	
256	SEG127	2610	
257	SEG128	2670	
258	SEG129	2730	
259	SEG130	2790	
260	SEG131	2850	
261	SEG132	2910	
262	SEG133	2970	
263	SEG134	3030	
264	SEG135	3090	
265	SEG136	3150	
266	SEG137	3210	
267	SEG138	3270	
268	SEG139	3330	
269	SEG140	3390	
270	SEG141	3450	
271	SEG142	3510	
272	SEG143	3570	
273	SEG144	3630	
274	SEG145	3690	
275	SEG146	3750	
276	SEG147	3810	
277	SEG148	3870	
278	SEG149	3930	
279	SEG150	3990	
280	SEG151	4050	
281	SEG152	4110	
282	SEG153	4170	
283	SEG154	4230	
284	SEG155	4290	
285	SEG156	4350	
286	SEG157	4410	
287	SEG158	4470	
288	SEG159	4530	
289	SEG160	4590	
290	SEG161	4650	
291	SEG162	4710	
292	SEG163	4770	
293	SEG164	4830	
294	SEG165	4890	
295	SEG166	4950	
296	SEG167	5010	
297	NC	5070	
298	NC	5130	
299	NC	5449	–812
300	COM32	↓	–761

Unit: µm

PAD No.	Pin Name	X	Y
301	COM33	5449	–710
302	COM34		–659
303	COM35		–608
304	COM36		–557
305	COM37		–506
306	COM38		–455
307	COM39		–404
308	COM40		–353
309	COM41		–302
310	COM42		–251
311	COM43		–200
312	COM44		–149
313	COM45		–98
314	COM46		–47
315	COM47		4
316	COM48		55
317	COM49		106
318	COM50		157
319	COM51		208
320	COM52		259
321	COM53		310
322	COM54		361
323	COM55		412
324	COM56		463
325	COM57		514
326	COM58		565
327	COM59		616
328	COM60		667
329	COM61		718
330	COM62		769
331	COM63		820
332	COMS		871
333	NC		922

5. PIN DESCRIPTION

5.1 Power Pin

Pin name	I/O	Description	Number of pins
V_{DD}	Power supply	Connect to system MPU power supply pin V_{CC}.	8
V_{SS}	Power supply	Connect to the system GND. MV_3 is short circuited with M_{V3} inside the IC chip.	8
V_{DD2}	Power supply	Boosting power supply circuit. It is necessary to maintain the co-relation between the V_{DD2} and V_{DD} as: $V_{DD2} \geq V_{DD}$.	4
V_{DI}	Power supply	This is the power supply pin for operating internal circuits that are generated from V_{DD}. Connect a capacitor for stabilizing voltage between V_{DI} and V_{SS}. V_{DI} can be used for external inputs as well. In case of external input, make TEST1 = LOW and use this pin in the ranges of $3.3V \geq V_{DI} \geq 2.7V$ and $V_{DD} \geq V_{DI}$. When using it in the range of V_{DD} = 2.7 to 3.3V, make TEST1 = LOW and short-circuit this pin to V_{DD}.	2
V_3, V_2, V_1, V_C, MV_1, MV_2	Power supply	A liquid crystal drive multi-level power supply. The voltages determined by the liquid crystal cell are impedance-converted by resistive divider and operational amplifier for application. The following order must be maintained: $V_3 \geq V_2 \geq V_1 \geq V_C \geq MV_1 \geq MV_2 \geq MV_3$ (=V_{SS}) MV_3 is short circuited with MV_3 inside the IC chip. Master operation: When power supply is turned on, the following voltage is applied to each pin by the built-in power supply circuit. The voltage is selected by Bias Change Command. V_2 6/8·V_3 16/20·V_3 14/16·V_3 V_1 5/8·V_3 13/20·V_3 11/16·V_3 V_C 4/8·V_3 10/20·V_3 8/16·V_3 MV_1 3/8·V_3 7/20·V_3 5/16·V_3 MV_2 2/8·V_3 4/20·V_3 2/16·V_3	12 (2 each)

5.2 LCD Power Supply Circuit Pin

Pin name	I/O	Description	Number of pins
CAP1+	O	Pin connected to the positive side of the step-up capacitor. Connect the capacitor between this pin and CAP1– pin.	3
CAP1–	O	Pin connected to the negative side of the step-up capacitor. Connect the capacitor between this pin and CAP1+ pin.	3
CAP2+	O	Pin connected to the positive side of the step-up capacitor. Connect the capacitor between this pin and CAP2– pin.	3
CAP2–	O	Pin connected to the negative side of the step-up capacitor. Connect the capacitor between this pin and CAP2+ pin.	3
V_{OUT}	I/O	Output pin for step-up. Connect the capacitor between this pin and V_{DD} or V_{DD2}. When V_{OUT} is used with external voltage, this pin can be a input terminal.	4
CAP3+	O	Pin connected to the positive side of the step-up capacitor. Connect the capacitor between this pin and CAP2– pin.	3
CAP4+	O	Pin connected to the positive side of the step-up capacitor. Connect the capacitor between this pin and CAP1– pin.	3
CAP5+	O	Pin short circuited with V_{OUT} terminal. When V_{OUT} is used with external voltage, this pin can be left OPEN.	3

5.3 System Bus Connection Pin

<table>
<tr><th>Pin name</th><th>I/O</th><th>Description</th><th>Number of pins</th></tr>
<tr><td>D7 to D0

(SI)

(SCL)</td><td>I/O</td><td>Connects to the 8-bit or 16-bit MPU data bus via the 8-bit bi-directional data bus.
When the serial interface is selected (P/S = LOW and C86 = LOW), D7 serves as the
serial data input (SI) and D6 serves as the serial clock input (SCL), In this case, D0 through D5 go to a high impedance state. When the Chip select is inactive, D0 through D7 go to a high impedance state.</td><td>10</td></tr>
<tr><td>A0</td><td>I</td><td>Normally, the least significant bit MPU address bus is connected to distinguish between data and command.
A0 = HIGH : indicates that D0 to D7 are display data or command parameters.
A0 = LOW : indicates that D0 to D7 are control commands.</td><td>1</td></tr>
<tr><td>$\overline{RES}$</td><td>I</td><td>When the $\overline{RES}$ is LOW, initialization is achieved.
Resetting operation is done on the level of the RES signal.</td><td>1</td></tr>
<tr><td>$\overline{CS}$</td><td>I</td><td>A chip select signal. When $\overline{CS}$ = LOW, signals are active, and data/command input/output are enabled.</td><td>1</td></tr>
<tr><td>$\overline{RD}$
(E)</td><td>I</td><td>• When the 80 series MPU is connected. “Active” “LOW”
A pin for connection of the $\overline{RD}$ signal of the 80 series MPU.
When this signal is LOW, the data bus of the
S1D15714 Series is in the output state.
• When the 68 series MPU is connected. “Active” “HIGH”
Serves as a 68 series MPU enable clock input pin.</td><td>1</td></tr>
<tr><td>$\overline{WR}$
(R/$\overline{W}$)</td><td>I</td><td>• When the 80 series MPU is connected. “Active” “LOW”
A pin for connection of the $\overline{WR}$ signal of the 80 series MPU.
Signals on the data bus are latched at the leading edge of the $\overline{WR}$ signal.
• Serves as a read/write control signal input pin when the 68 series MPU is connected.
R/$\overline{W}$ = HIGH : Read
R/$\overline{W}$ = LOW : Write</td><td>1</td></tr>
<tr><td>C86</td><td>I</td><td>A MPU interface switching pin.
C86 = HIGH : 68 series MPU interface
C86 = LOW : 80 series MPU interface (Serial Interface)</td><td>1</td></tr>
<tr><td>P/S</td><td>I</td><td>Parallel data input/serial data input select pin
P/S = HIGH : Parallel data input
P/S = LOW : Serial data input
P/S = LOW and C86 = LOW : Serial interface spec
P/S = LOW and C86 = HIGH : Please do not set up
The following Table shows the summary:
<table>
<tr><th>P/S</th><th>C86</th><th>Data/Command</th><th>Data</th><th>Read/Write clock</th><th>Serial</th></tr>
<tr><td>HIGH</td><td>LOW</td><td>A0</td><td>D0 to D7</td><td>$\overline{RD}$, $\overline{WR}$</td><td></td></tr>
<tr><td>LOW</td><td>LOW</td><td>A0</td><td>SI (D7)</td><td>Write only</td><td>SCL (D6)</td></tr>
</table>
When P/S = LOW, D0 to D5 are high impedance.
D0 to D5 can be HIGH, LOW or open.
RD(E) and WR(R/W) are locked to HIGH or LOW.
The serial data input does not allow the RAM display data to be read.</td><td>1</td></tr>
</table>

<table>
<tr><th>Pin name</th><th>I/O</th><th>Description</th><th>Number of pins</th></tr>
<tr><td>CLS</td><td>I</td><td>A pin used to select Enable/Disable state of the built-in oscillator circuit for display clock.
CLS = HIGH : Built-in oscillator circuit Enabled
CLS = LOW : Built-in oscillator circuit Disabled (External input)
When CLS is LOW, display clock is input from the CL pin. When the S1D15714 Series is used in the master/slave mode, each CLS pins must be set to the same level.
<table><tr><th>Display clock</th><th>Master</th><th>Slave</th></tr><tr><td>Built-in oscillator circuit used</td><td>HIGH</td><td>HIGH</td></tr><tr><td>External input</td><td>LOW</td><td>LOW</td></tr></table></td><td>1</td></tr>
<tr><td>M/S</td><td>I</td><td>A pin used to select the master/slave operation for S1D15714 Series.
Liquid crystal display system is synchronized when the master operation outputs the timing signal required for liquid crystal display, while the slave operation inputs the timing signal required for liquid crystal display.
M/S = HIGH : Master operation
M/S = LOW : Slave operation
The following Table shows the relation in conformance to the M/S and CLS:
<table><tr><th>M/S</th><th>CLS</th><th>Oscillation circuit</th><th>Power circuit</th><th>CL</th><th>FR, $\overline{\text{DOF}}$, F1, F2, SYNC</th></tr><tr><td>HIGH</td><td>HIGH
LOW</td><td>Enabled
Disabled</td><td>Enabled
Enabled</td><td>Output
Input</td><td>Output
Output</td></tr><tr><td>LOW</td><td>HIGH
LOW</td><td>Disabled
Disabled</td><td>Disabled
Disabled</td><td>Input
Input</td><td>Input
Input</td></tr></table></td><td>1</td></tr>
<tr><td>CL</td><td>I/O</td><td>Display clock input/output pin.
The following Table shows the relation in conformance to the M/S and CLS state:
<table><tr><th>M/S</th><th>CLS</th><th>CL</th></tr><tr><td>HIGH</td><td>HIGH
LOW</td><td>Output
Input</td></tr><tr><td>LOW</td><td>HIGH
LOW</td><td>Input
Input</td></tr></table>When you want to use the S1D15714 Series in the master/slave mode, connect each CL pin.</td><td>1</td></tr>
<tr><td>FR</td><td>I/O</td><td>A liquid crystal alternating current input/output pin.
M/S = HIGH : Output
M/S = LOW : Input
When you want to use the S1D15714 Series in the master/slave mode, connect each FR pin.</td><td>1</td></tr>
<tr><td>F1, F2, SYNC</td><td>I/O</td><td>A liquid crystal sync signal input/output pin.
M/S = HIGH : Output
M/S = LOW : Input
When you want to use the S1D15714 Series in the master/slave mode, connect each F1, F2 and SYNC pins.</td><td>3
(1 each)</td></tr>
<tr><td>$\overline{\text{DOF}}$</td><td>I/O</td><td>A liquid crystal blanking control pin.
M/S = HIGH : Output
M/S = LOW : Input
When you want to use the S1D15714 Series in the master/slave mode, connect each $\overline{\text{DOF}}$ pin.</td><td>1</td></tr>
</table>

5.4 Liquid crystal drive pin

Pin name	I/O	Description	Number of pins
SEG0 to SEG167	O	Liquid crystal segment drive output pins. One of the V_2, V_1, V_C, MV_1, and MV_2 levels is selected by a combination of the display RAM content and FR/F1/F2 signals.	168
COM0 to COM63	O	Liquid crystal common drive output pins. One of the V_3, V_C, MV_3 (V_{SS}) levels is selected by a combination of the scan data and FR/F1/F2 signals.	64
COMS	O	COM output pins for indicator. These pins outputted the same signal. Set to OPEN not used. When COMS is used for the master/ slave configuration, the same signal is output to both the master and slave.	2

5.5 Temperature Sensor Pins

Pin name	I/O	Description	Number of pins
SVD2	O	This is analog voltage output pin for the temperature sensor.	1
SV22	O	This is test pin for the temperature sensor. Fix the pin OPEN.	1

5.6 Test pins

Pin name	I/O	Description	Number of pins
TEST	I	IC chip test pin. Fix the pin LOW.	1
TEST1	I	V_{DI} generation circuit control pin. When using this pin in the range of V_{DD} = 3.3 to 5.5V, fix this pin to HIGH. When using this pin in the range of V_{DD} = 2.7 to 3.3V, fix this to LOW and short-circuit V_{DD} to V_{DI}. When this pin is used after TEST1 is switched from LOW to HIGH, the initialization to make Reset $\overline{RES}$ = LOW is required after TEST1 is switched to HIGH. The V_{DI} generation circuit operates independently from power saving. To reduce the current consumption close to the static current with the power saving function while this pin is used in the range of V_{DD} = 3.3 to 5.5V, make it possible to switch TEST1 to LOW during power saving.	1

6. FUNCTIONAL DESCRIPTION

6.1 MPU Interface

6.1.1 Selection of Interface Type

S1D15714 Series allows data to be sent via the 8-bit bi-directional data buses (D7 to D0) or serial data input (SI). By setting the polarity of the P/S pin and C86 pin to HIGH or LOW, you can select either 8-bit parallel data input or serial data input, as shown in Table 6.1.

Table 6.1

P/S	C86		$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5 to D0
HIGH	—	Parallel input	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5 to D0
LOW	LOW	Serial input	$\overline{CS}$	A0	—	—	SI	SCL	(HZ)

—: Fixed to HIGH or LOW HZ: High impedance state

6.1.2 Parallel interface

When the parallel interface is selected (P/S = HIGH), direction connection to the MPU bus of either 80 series MPU or 68 series MPU is performed by setting the 86 pin to either HIGH or LOW, as shown in Table 6.2.

Table 6.2

P/S	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	D7 to D0
HIGH : 68 series MPU bus	$\overline{CS}$	A0	E	R/$\overline{W}$	D7 to D0
LOW : 80 series MPU bus	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	D7 to D0

The data bus signals are identified by a combination of A0, $\overline{RD}$ (E), and $\overline{WR}$ (R/$\overline{W}$) signals as shown in Table 6.3.

Table 6.3

Common	68 series	80 series		Function
A0	R/$\overline{W}$	$\overline{RD}$	$\overline{WR}$	
1	1	0	1	Display data read, status read
1	0	1	0	Display data write, Command parameter write
0	0	1	0	Command write

6.1.3 Serial interface

When the serial interface is selected (P/S = LOW and C86 = LOW), the chip is active ($\overline{CS}$ = LOW and C86 = LOW), and reception of serial data input (SI) and serial clock input (SCL) is enabled. Serial interface comprises a 8-bit shift register and 3-bit counter. The serial data are latched by the rising edge of serial clock signals in the order of D7, D6, ... and D0 starting from the serial data input pin. On the rising edge of 8th serial clock signal, they are converted into 8-bit parallel data to be processed.
Whether serial data input is a display data or command is identified by A0 input. A0 = HIGH indicates display data, while A0 = LOW shows command data. The A0 input is read and identified at every 8 × n-th rising edge of the serial clock after the chip has turned active.
Fig. 6.1 shows the serial interface signal chart.

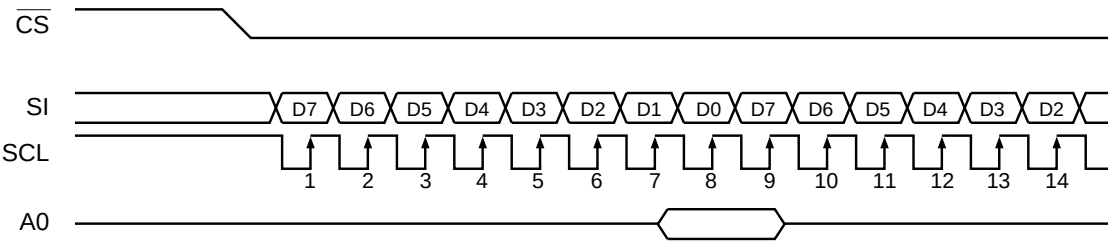


Fig. 6.1

* When the chip is inactive, the counter is reset to the initials state.
* Reading is not performed in the case of serial interface.
* For the SCL signal, a sufficient care must be taken against terminal reflection of the wiring and external noise. Recommend to use an actual equipment to verify the operation.

6.1.4 Chip Selection

The S1D15714 Series has chip select pin. MPU interface or serial interface is enabled only when $\overline{CS}$ = LOW. When the chip select pin is inactive, D0 to D5 are in the state of high impedance, while A0, $\overline{RD}$ and $\overline{WR}$ inputs are disabled. When serial interface is selected, the shift register and counter are reset.

6.1.5 Access to display data RAM and internal register

Access to S1D15714 Series series viewed from the MPU side is enabled only if the cycle time requirements are kept. This does not required waiting time; hence, high-speed data transfer is allowed.
Furthermore, at the time of data transfer with the MPU, S1D15714 Series provides a kind of inter-LSI pipe line processing via the bus holder accompanying the internal data bus.
For example, when data is written to the display data RAM by the MPU, the data is once held by the bus holder. It is written to the display data RAM before the next data write cycle comes.
On the other hand, when the MPU reads the content of the display data RAM, it is read in the first data read cycle (dummy), and the data is held in the bus holder. Then it is read onto on the system bus from the bus holder in the next data read cycle. Restrictions are imposed on the display data RAM read sequence. When the address has been set, specified address data is not output to the Read command immediately after that. The specified address data is output in the second data reading. This must be carefully noted. Therefore, one dummy read operation is mandatory subsequent to address setting or write cycle. Fig. 6.2 illustrates this relationship.

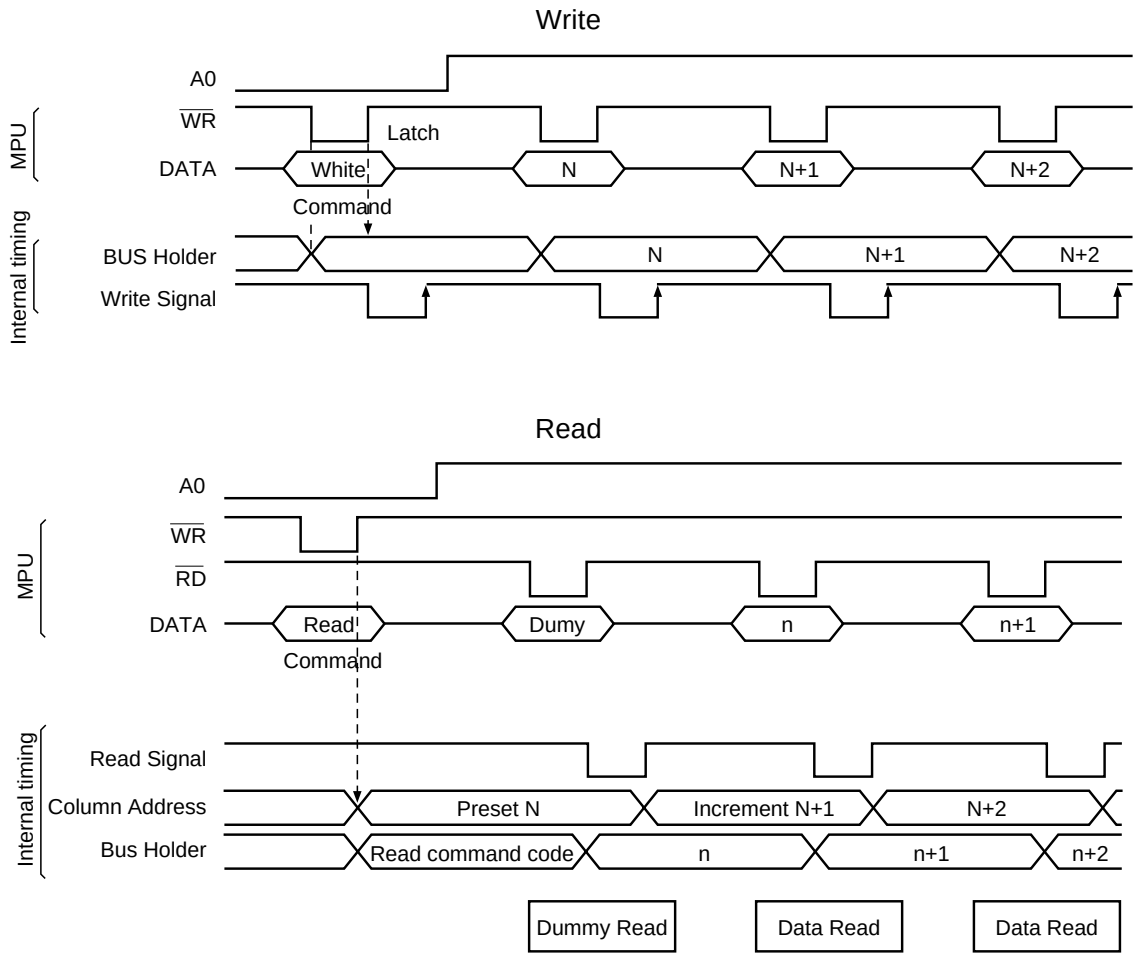


Fig. 6.2

6.2 Display data RAM

6.2.1 Display Data RAM

This is a RAM to store the display dot data, and comprises 65 × 168 bits. Access to the desired bit is enabled by specifying the page address and column address.

The RAM 1 bit built in the one-dot pixel responds to it. When the RAM bit data is “1”, the display is black. If it is “0”, the display is given in white.

RAM bit data

“1” : Light On	Black (when display is in normal mode)
“0” : Light Off	White (when display is in normal mode)

Display data D7 to D0 from the MPU correspond to LCD common direction, as shown in Fig. 6.3 and 6.4. Therefore, less restrictions when multi-chip usage.
Furthermore, read/write operations from the MPU to the RAM are carried out via the input/output buffer. The read operation from Display data RAM is designed as an independent operation. Accordingly, even if the MPU accesses the RAM asynchronously during LCD display, no adverse effect is given to display.

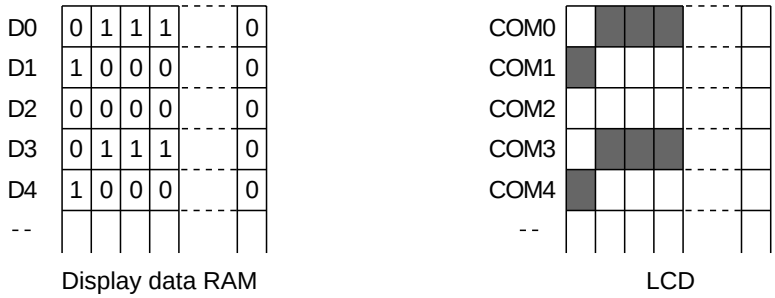


Fig. 6.3 Binary

6.2.2 Page address circuit/column address circuit

The address of the display data RAM to be accessed is specified by the Page Address Set command and Column Address Set command, as shown in Fig. 6.4.
For Address incremental direction, either the column direction or page direction can be selected by the Address Direction command. Whichever direction is chosen, increment is carried out by positive one (+1) after write or read operation.
When the column direction is selected for address increment, the column address is increased by +1 for every write or read operation. After the column address has accessed up to A7H, the page address is incremented by +1 and the column address shifts to 0H.
When the page direction is selected for address increment, the page address is increased with the column address locked in position. When the page address has accessed up to Page 8, the column address is incremented by +1, and the page address goes to Page 0.
Whichever direction is selected for address increment, the page address goes back to Page 0 and the column address to 0H after access up to the column address A7H of page address Page 8.
As shown in Fig. 6.4, relationship between the display data RAM column address and segment output can be reversed by the Column Address Set Direction command. This will reduce restrictions on IC layout during LCD module assembling.
Page 8 is a RAM domain only for indicators, only D0 of its display data is effective.

Table 6.4

SEG output		SEG0		SEG167
ADC	"0"	0(H)→	Column Address	→A7(H)
(D0)	"1"	A7(H)←	Column Address	←0(H)

6.2.3 Line address circuit

The line address circuit specifies the line address corresponding to COM output when the contents of the display data RAM is displayed, as shown in Fig. 6.4. Normally, the top line of the display (COM0 output in the case of normal rotation of the common output status and COM63 output in the case of reverse rotation) is specified by the Display Start Line Address Set command. The display area starts from the specified display start line address to cover the area corresponding to the lines specified by the DUTY Set command in the direction where the line address increments.
If the display start line address set command is used for dynamic modification of the line address, screen scroll and page change are enabled.

6.2.4 Display data latch circuit

The display data latch circuit is a latch to temporarily latch the display data output from then display data RAM to the liquid crystal drive circuit. Display normal/reverse, display ON/OFF, and display all lighting ON/OFF commands control the data in this latch, without the data in the display data RAM being controlled.

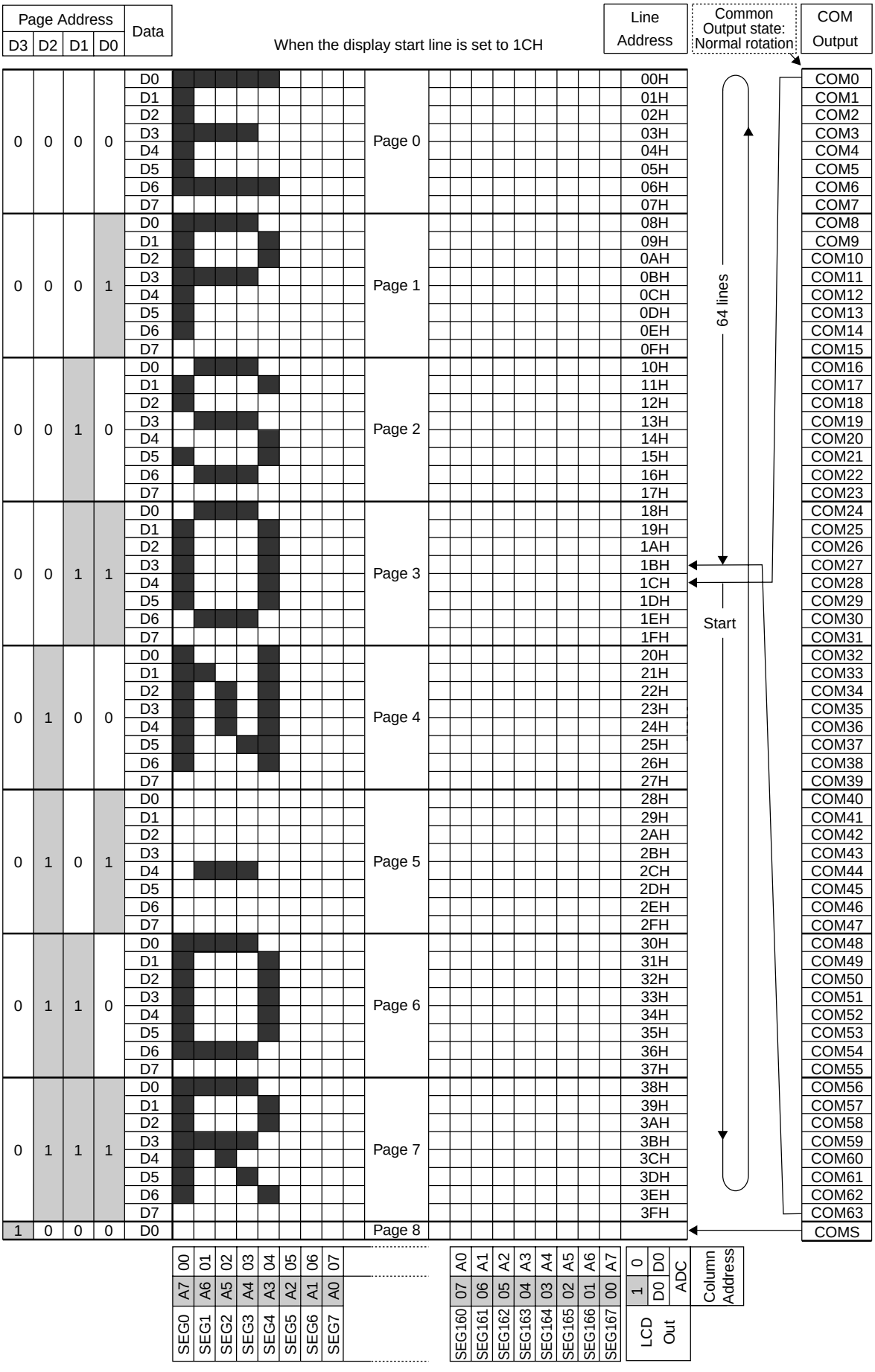


Fig. 6.4 Binary display

6.3 Oscillator circuit

A display clock is generated by the CR oscillator. The oscillator circuit is enabled only when M/S = HIGH and CLS = HIGH. Oscillation starts after input of the built-in oscillator circuit ON command input.
When CLS = LOW, oscillation stops, and display clock is input from the CL pin.

6.4 Display timing generation circuit

Timing signals are generated from the display clock to the line address circuit and display data latch circuit. Synchronized with display clock, display data is latched in display data latch circuit, and is output to the segment drive output pin. Reading of the display data into the LCD drive circuit is completely independent of access from the MPU to the display data RAM. Accordingly, asynchronous access to the display data RAM during LCD display does not give any adverse effect; like as flicker.
Furthermore, the display clock generates internal common timing, liquid crystal alternating signal(FR), field start signal (SYNC) and drive pattern signal (Fl and F2).
The FR normally generates 2-frame alternating drive system drive waveform to the liquid crystal drive circuit. The n-line reverse alternating drive waveform is generated for each $4 \times (a+1)$ line by setting data on the n–line reverse drive register. When there is a display quality problem including crosstalk,the problem may be solved using the n-line reverse alternating drive.
Execute liquid crystal display to determine the number of lines “n” for alternation.
When you want to use the S1D15714 Series in multi-chip configuration, supply display timing signal (FR, SYNC, F1, F2, CL, $\overline{DOF}$) to the slave side from the master side. Table 6.5 shows the statuses of FR, SYNC, F1, F2, CL, $\overline{DOF}$.

Table 6.5

Operating mode		CL	FR,SYNC, F1, F2, $\overline{DOF}$
Master (M/S = HIGH)	Built-in oscillator circuit enabled (CLS = HIGH)	Output	Output
	Built-in oscillator circuit disabled (CLS = LOW)	Input	Output
Slave (M/S = LOW)	Built-in oscillator circuit enabled (CLS = HIGH)	Input	Input
	Built-in oscillator circuit disabled (CLS = LOW)	Input	Input

6.5 Liquid crystal drive circuit

6.5.1 SEG Drivers

This is a SEG output circuit. It selects the five values of V_2, V_1, V_C, MV_1 and MV_2 using the driver control signal determined by the decoder, and output them.

6.5.2 COM Drivers

This is a COM output circuit. It selects three values of V_3, V_C and MV_3(V_{SS}) using the driver control signal determined by the decoder, and output them.
S1D15714 Series allows the COM output scanning direction to be set by the common output status select command. (See Table 6.6). This will reduce restrictions on IC layout during LCD module assembling.

Table 6.6

Status	Direction of COM scanning		
Normal	COM 0	→	COM63
Reverse	COM63	→	COM 0

6.6 Power supply circuit

This is a power supply circuit to generate voltage required for liquid crystal drive, and is characterized by a low power consumption. It consists of a step-up circuit, voltage regulating circuit and liquid crystal drive voltage generating circuit, and is enabled only during master operation. The power supply circuit uses the power control set command to provide an on/off control of step-up circuit, voltage regulating circuit and liquid crystal drive potential generating circuit. This allows a combined use of the external power supply and part of built-in power supply functions. Table 6.7 shows functions controlled by the 3-bit data of the control set command, and Table 6.8 shows reference combinations. Also, by use of the magnification of amplification changing over command, it is possible to select the amplifying magnification from five different steps. The power supply circuit is enabled only during master operation.

Table 6.7 Respective Bit Control Contents by Power Control Set Command

Item	State	
	"1"	**"0"**
D2 Boosting circuit control bit	ON	OFF
D1 Voltage regulator circuit (V_3 regulator circuit) control bit	ON	OFF
D0 LCD driving potential generating circuit (LCDV circuit) control bit	ON	OFF

Table 6.8 Reference combination

Circuits used	D2	D1	D0	Boosting circuit	V_C regulator circuit	LCDV circuit	Eternal input power supply
① Use of all built-in power supplies	1	1	1	○ "1"	○ "1"	○ "1"	—
② V_3 regulating circuit and LCDV circuit only	0	1	1	× "0"	○ "1"	○ "1"	V_{OUT}
③ LCDV circuit only	0	0	1	× "0"	× "0"	○ "1"	V_3
④ External power supply only	0	0	0	× "0"	× "0"	× "0"	V_3, V_2, V_1, V_C, MV_1, MV_2

* Any combinations other than the above are not available.

The V_3 voltage is generated from V_{OUT}. To use the circuit as shown in ② in the above table, input the voltage, which makes $V_{OUT} \geq V_3+0.2V$, from the V_{OUT} pin.

6.6.1 Amplification circuit

By use of the amplification circuit being built into the S1D15714 Series, it is possible to make amplification of the electric potential between V_{DD2}–V_{SS} onto quintuple amplification, quadruple amplification, triple amplification or double amplification. Also, by use of the relevant command, it is possible to select either one from the quintuple amplification, quadruple amplification, triple amplification, double amplification and equal amplification.

① When using the quintuple-boosting, connect the capacitor C1 between CAP1+ <–> CAP1–, between CAP2+ <–> CAP2–, between CAP3+ <–> CAP1–, between CAP4+ <–> CAP2–, between V_{DD2} <–> V_{OUT} and short-circuit the CAP5+, CAP4+ and V_{OUT} pin before use.
② When using the quadruple-boosting, connect the capacitor C1 between CAP1+ <–> CAP1–, between CAP2+ <–> CAP2–, between CAP3+ <–> CAP1– and between V_{DD2} <–> V_{OUT} and short-circuit the CAP5+, CAP4+ pin and the V_{OUT} pin before use.
③ When using the triple-boosting, connect the capacitor C1 between CAP1+ <–> CAP1–, between CAP2+ <–> CAP2– and between V_{DD2} <–> V_{OUT} and short-circuit the CAP5+, CAP4+ pin, CAP3+ pin and the V_{OUT} pin before use.
④ When using the double-boosting, connect the capacitor C1 between CAP1+ <–> CAP1– and between V_{DD2} <–> V_{OUT}, open the CAP2– pin and short-circuit the CAP5+, CAP4+ pin, CAP3+ pin, CAP2+ pin and the V_{OUT} pin before use.

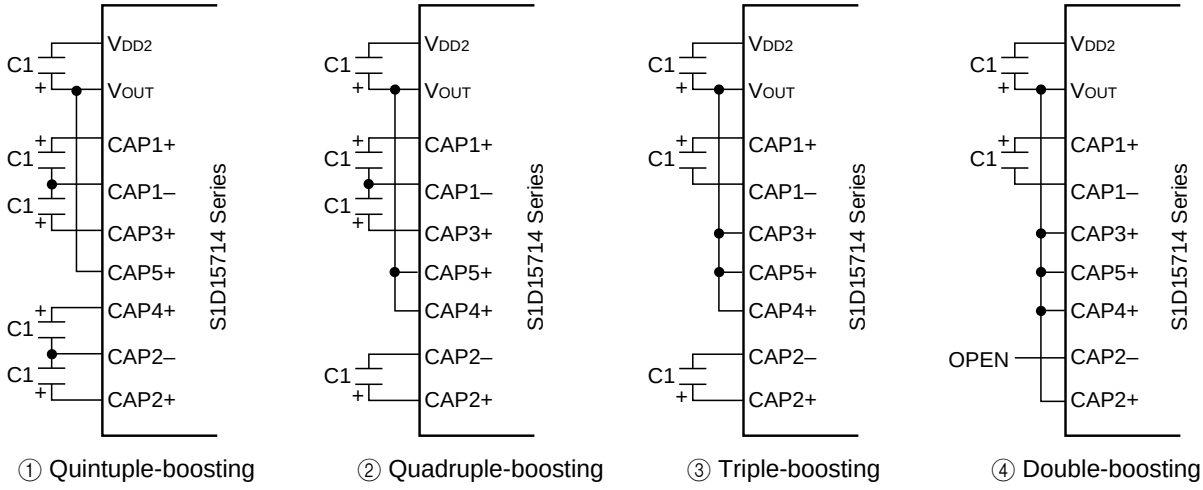


Fig. 6.5 below shows the electric potential relations when making respective amplifications.

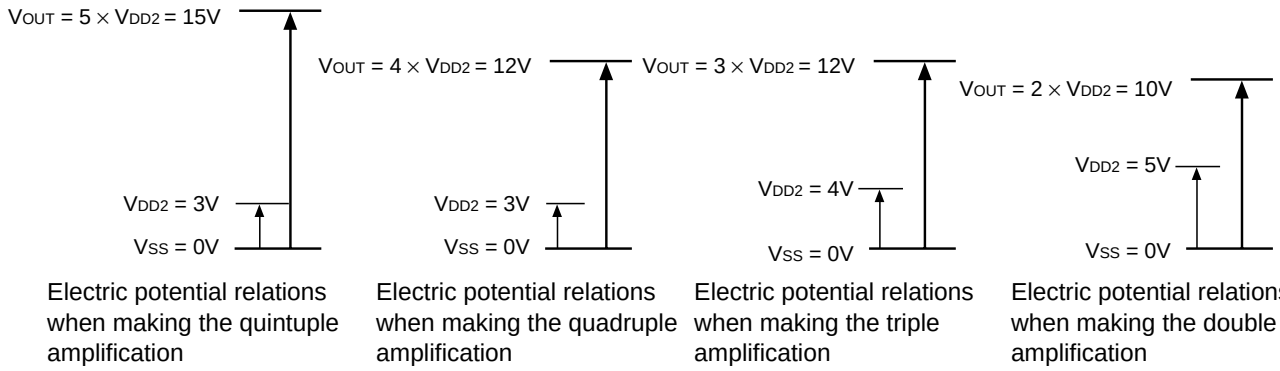


Fig. 6.5

* Set the voltage range of the V_{DD2} so that the voltage of the V_{OUT} pin may not exceed the absolute maximum rating.

6.6.2 Voltage Regulating Circuit

V_{OUT} generated from the step-up circuit or V_{OUT} input from the outside produces liquid crystal drive voltage V_C via the voltage regulating circuit. The voltage regulating circuit is controlled by liquid crystal drive voltage change command and electronic volume.
The S1D15714 Series has a high precision constant voltage source, and incorporates 8-step liquid crystal drive voltage change command and 128-step electronic volume functions. This makes it possible to provide a high precision liquid crystal drive voltage regulation only by the command without adding any external parts.

• Electronic volume

α of Table 6.10 indicates an electronic volume command value. It takes one of 128 states when the data is set in the 7-bit electronic volume register.
Table 6.9 shows the value of α by setting the data in the electronic volume register.

Table 6.9

D6	D5	D4	D3	D2	D1	D0	α	V_3 Voltage
0	0	0	0	0	0	0	0	Small
0	0	0	0	0	0	1	1	↑
0	0	0	0	0	1	0	2	↕
1	1	1	1	1	0	1	125	↕
1	1	1	1	1	1	0	126	↓
1	1	1	1	1	1	1	127	Large

• Liquid crystal drive voltage selection

The liquid drive voltage range can be selected from 8 states by the liquid crystal drive voltage select command using the 3-bit crystal drive voltage select command register. Table 6.10 shows V_3 voltage output ranges at 25°C.

Table 6.10

D2	D1	D0	V_3 voltage output range
0	0	0	5.6 to 7.0V
0	0	1	6.3 to 7.8V
0	1	0	7.1 to 8.9V
0	1	1	8.0 to 10.0V
1	0	0	9.2 to 11.4V
1	0	1	10.3 to 12.8V
1	1	0	11.7 to 14.5V
1	1	1	12.8 to 16.0V

•V_3 Output Voltage Value

Table 6.11 and Fig. 6.6 show logical values of V3 at 25°C. Regard the dispersion to logical values as ±3%.

Table 6.11

Unit [V]

LCD voltage selection			V_3[V]
D2	D1	D0	(α = 0 to 127)
0	0	0	5.576+0.0109 × α
0	0	1	6.256+0.0122 × α
0	1	0	7.125+0.0139 × α
0	1	1	8.016+0.0156 × α
1	0	0	9.161+0.0178 × α
1	0	1	10.26+0.0200 × α
1	1	0	11.659+0.0227 × α
1	1	1	12.825+0.0250 × α

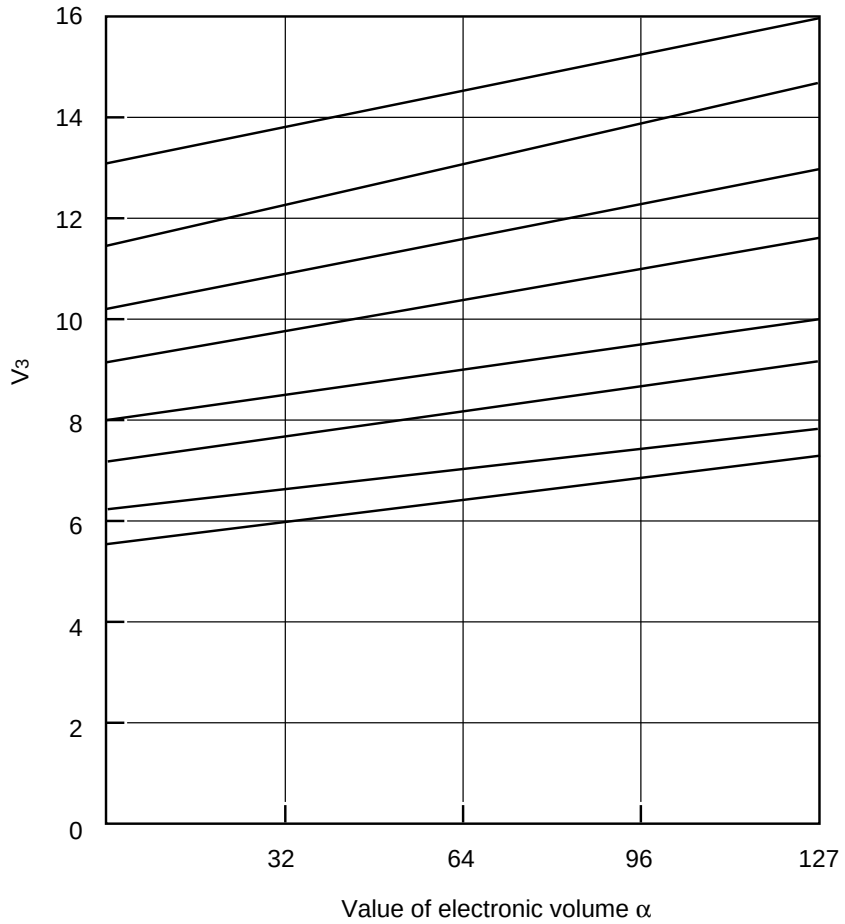


Fig. 6.6

6.6.3 Liquid crystal drive voltage generation circuit

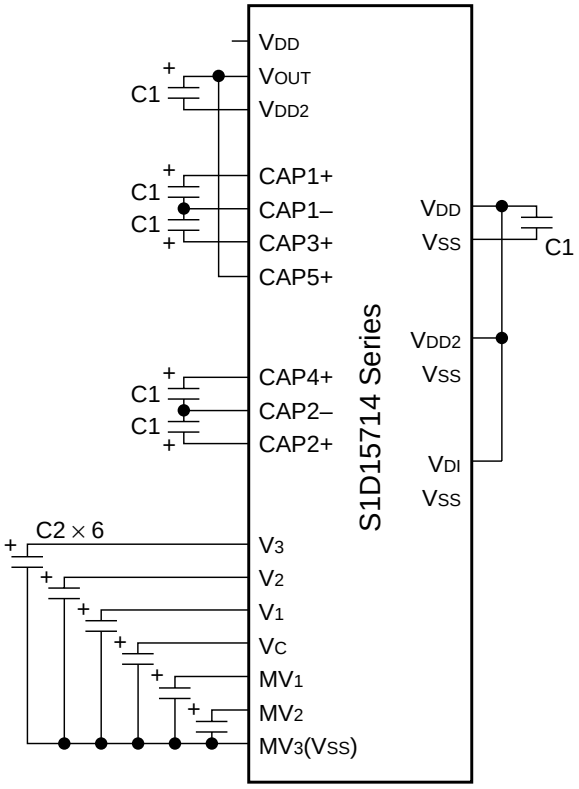
Voltages V_3 is converted by resistive divider to produce V_2, V_1, V_C, MV_1 and MV_2 voltages. V_2, V_1, V_C, MV_1 and MV_2 voltages are impedance-converted by the voltage follower, and is supplied to the liquid crystal drive circuit. A bias ratio is chosen by the bias set command.

Table 6.12 LCD bias set command register contents

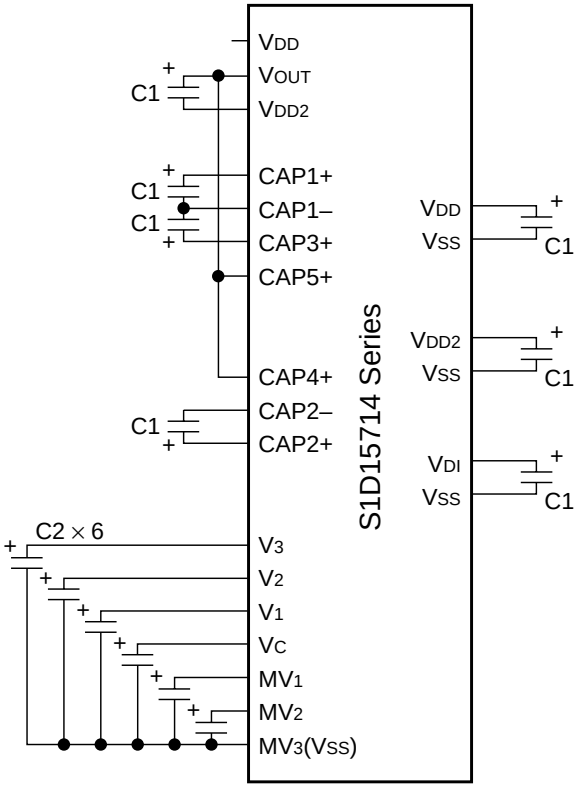
	Bias change command register value (D1, D0)		
	1/8 bias (0, 0)	**1/6, 7 bias (0, 1)**	**1/5, 3 bias (1, 0)**
V_2	$6/8 \cdot V_3$	$16/20 \cdot V_3$	$14/16 \cdot V_3$
V_1	$5/8 \cdot V_3$	$13/20 \cdot V_3$	$11/16 \cdot V_3$
V_C	$4/8 \cdot V_3$	$10/20 \cdot V_3$	$8/16 \cdot V_3$
MV_1	$3/8 \cdot V_3$	$7/20 \cdot V_3$	$5/16 \cdot V_3$
MV_2	$2/8 \cdot V_3$	$4/20 \cdot V_3$	$2/16 \cdot V_3$

6.6.4 Examples of the peripheral circuits of the power circuit

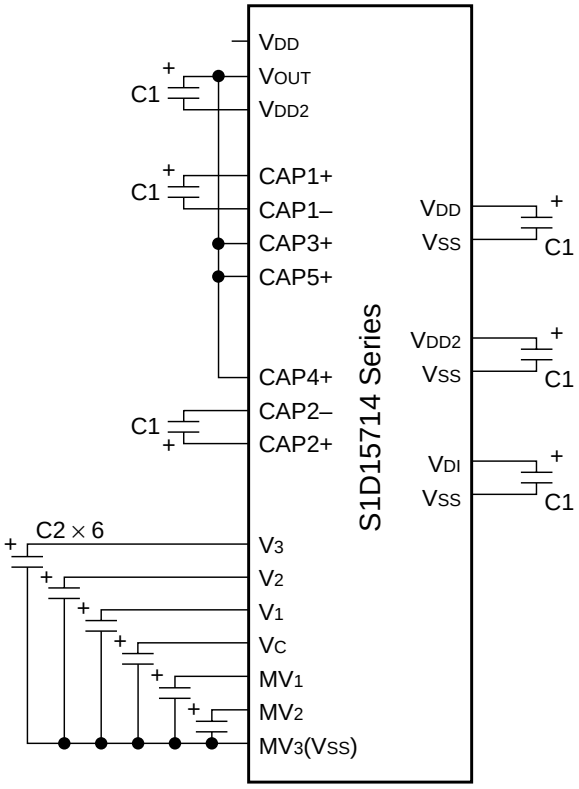
①When using all the built-in power supply
When using the quintuple-boosting
(C: 12 units V_{DD} = V_{DI} = 3.0 V)



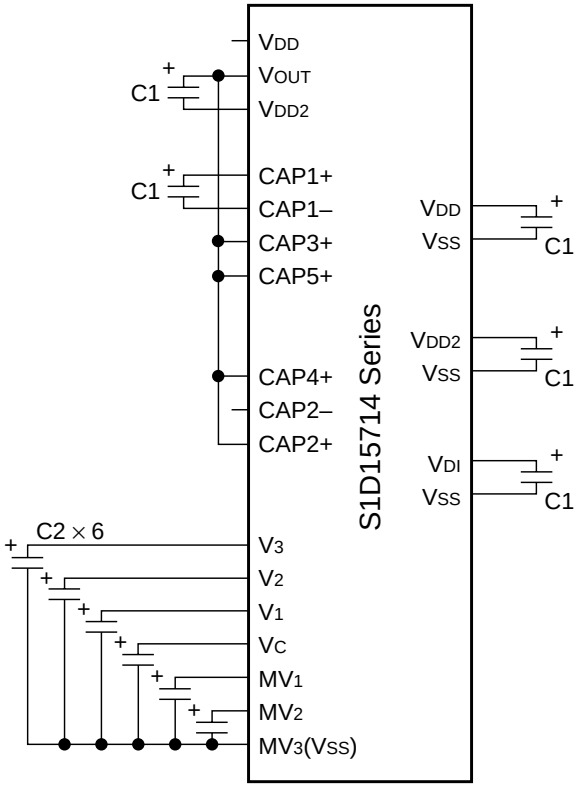
When using the quadruple-boosting (C: 13 units)



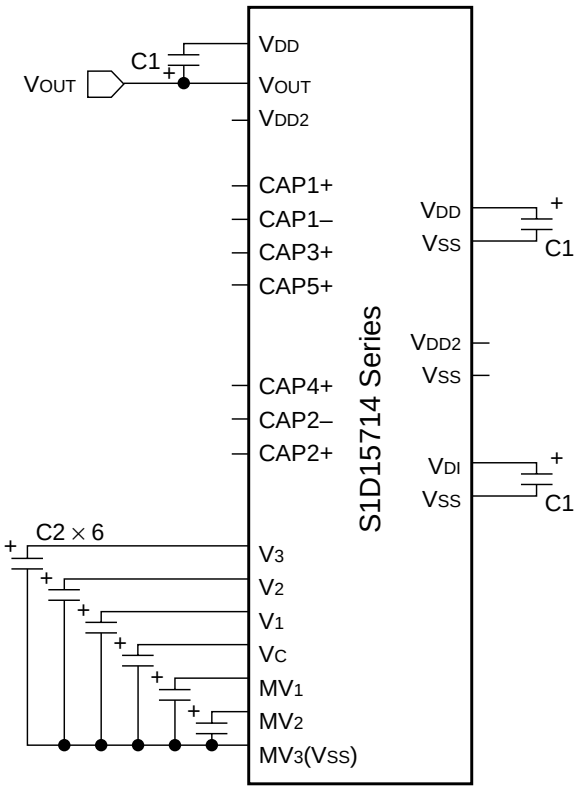
When using the triple-boosting (C: 12 units)



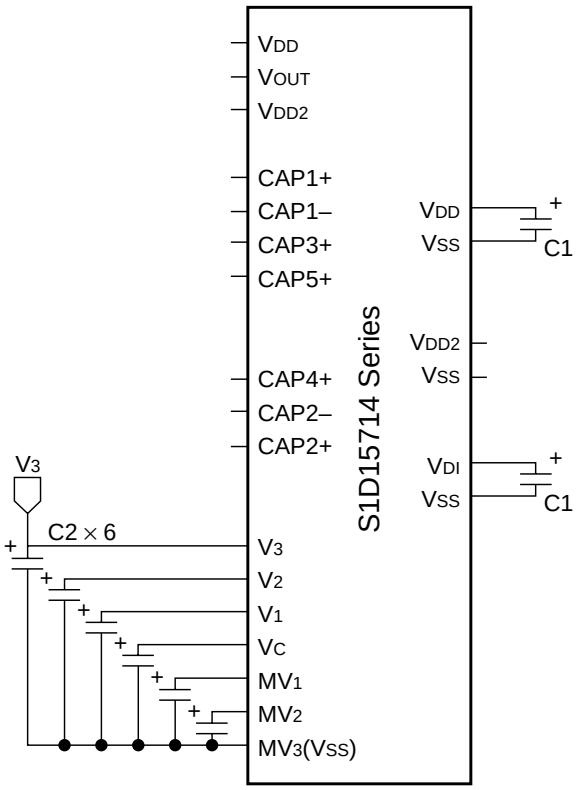
When using the double-boosting (C: 11 units)



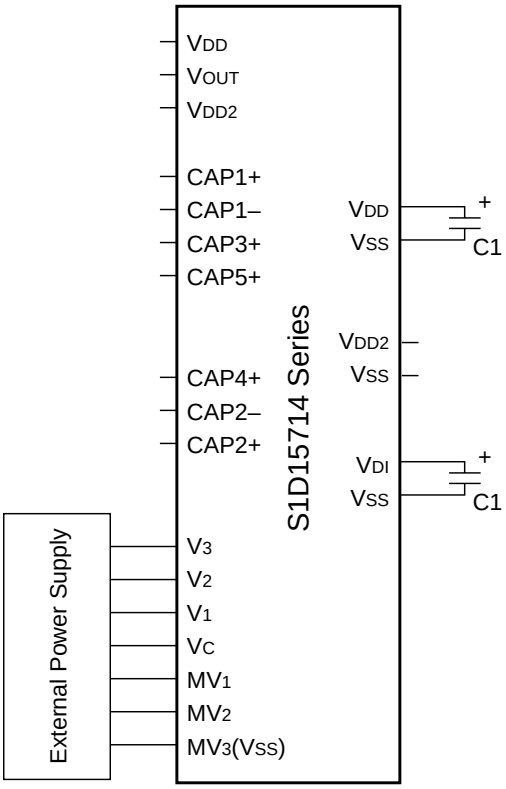
② V_3 adjusting circuit and LCDV circuit
V_{OUT} external input (C: 9 units)



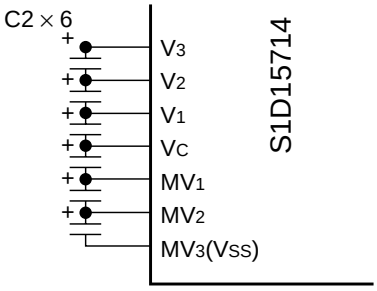
③ LCDV circuit only
V_3 external input (C: 8 units)



④ External power supply only
External input (C: 2 unit)



⑤ Connection Example of Smoothing Capacitor for Liquid Crystal Drive Voltage
In addition to the connections shown in the above ① to ③, the following connection is also possible.



Examples of common reference settings		
Item	**Settings**	**Unit**
C1	1.0 to 4.7	µF
C2	0.1 to 1.0	

*1 Optimum values of C1 and C2 above vary depending on the LCD panel to be driver. Above values should be referenced as information only. It is recommended to check how patterns with hish-load are displayed before finalizins the values.

*2 When the display panel is large and sufficient display dignity is not available by driving the built-in power supply circuit only, do not use the built-in power supply circuit and supply the voltage for driving the LC from outside.

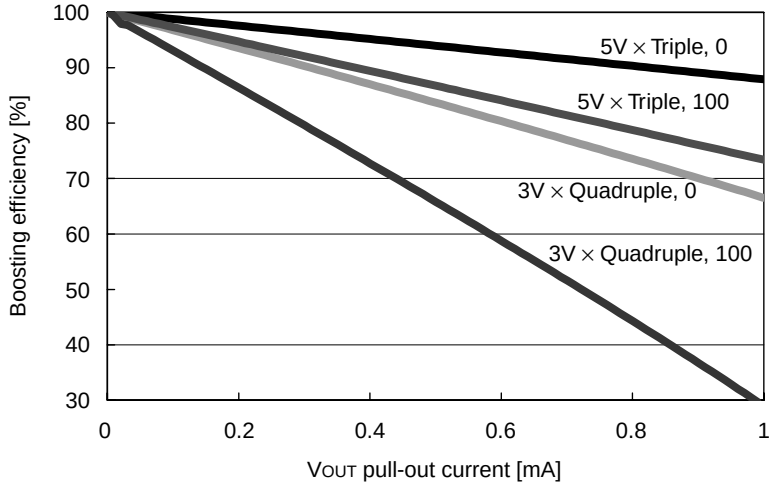
6.6.5 Precautions at Mounting COG

When mounting the COG, there are resistance components caused by ITO wiring between the IC or external connecting parts (capacitor, resistor) and the power supply. These resistance components may degrade liquid crystal display dignity or may malfunction the IC. When designing modules, take the following three points into account and evaluate them under the practical prerequisites:

(1) Minimize the resistance between the IC pin and the external connecting parts.
This IC's boosting circuit is switched with a transistor with very low ON resistance. In mounting the COG, ITO's wiring resistance gets into the switching transistor in series and controls the boosting capacity. Try to make the ITO wiring as thick as possible considering proper wiring to each boosting capacitor.

(2) Minimize the resistance to the IC power supply pin.
When current flow changes momentarily as in case of display clock switching, the supply voltage may drop momentarily sometimes. When the ITO's wiring resistance to the power supply pin is high, the supply voltage fluctuates greatly inside the IC and may malfunction the IC. Consider proper wiring of the power line so that stable supply voltage can be supplied to the IC.
In addition, the power supply V_{DD2} is provided to this IC separately from the power supply V_{DD} for the logical circuit. When the logical circuit is influenced by noises generated to the power supply circuit if V_{DD} and V_{DD2} are short-circuited, provide this IC with a power supply independent from V_{DD} and V_{DD2} or supply a liquid crystal drive voltage from outside without using the built-in power supply.

[Current Load Characteristics of Built-in Boosting Circuit (Reference Value)]



[Conditions]
V_{DD} = V_{DD2} = 5V, 3V
Triple boosting, Quadruple boosting
Boosting capacitor 1µF
Add 50Ω to both V_{DD} and V_{SS} in series to the power supply.

Fig. 6.9

Current load characteristics of built-in boosting circuit without resistance between each CAP pin and capacitor but with /100Ω.
This figure shows changes of the boosting efficiency when the current is pulled out from the V_{OUT} pin and when the V_{OUT} voltage is made 100% at the time of OUT=0mA.

(3) Prepare a COG module sample by changing the sheet resistance.
Evaluate the sample after changing the resistance value of the ITO wiring and select the one with sheet resistance as well as some operation margin.

6.6.6 Temperature gradient select circuit

This is a circuit to select the temperature gradient characteristics of the liquid crystal drive power supply voltage. Temperature gradient characteristics can be selected from eight states by the Temperature Gradient command. Selection of temperature gradient characteristics conforming to the temperature characteristics of the liquid crystal to be used makes it possible to configure a system without providing an external element for temperature characteristics compensation.

6.7 Temperature sensor circuit

The S1D15714 Series incorporate a temperature sensor circuit with an analog voltage output pin of the temperature gradient –4.70 mV/°C (Typ.). Input a proper electronic volume resistor value corresponding to the temperature sensor output value from the MPU to control the liquid crystal drive voltage V3, and liquid crystal displays of proper tint will become possible in a wide temperature range.
In order to control liquid crystal drive voltage more precisely, construct a system that feeds back values sampled output voltages at a certain temperature to the MPU and saves them as reference voltages to absorb dispersions of output voltages.
When a large current load is caused to the IC due to high-speed writing in the display RAM, the internal power supply of the IC will be vibrated and correct values may not be output at certain temperature sometimes. So, read temperature sensor outputs only when a large current load is not caused to the IC.
For pins related to the temperature sensor, see 5. Pin Description and 5.5 Temperature Sensor Pin, and for electric characteristics, see 9. DC Characteristics and 9.2 Characteristics of Temperature Sensor.

6.8 Reset circuit

When the $\overline{RES}$ input becomes LOW, this LSI is set to the initialized state.
The following shows the initially set state:

1. Display : OFF
2. Display : normal mode
3. Display all lighting : OFF
4. Common output status : normal
5. Display start line : Set to 1st line
6. Page address : Set to 0 page
7. Column address : Set to 0 address
8. Display data input direction : Column direction
9. Column address direction : forward
10. n-line a.c. reverse drive : OFF (reverse drive for each frame)
11. n-line reverse drive register : (D3, D2, D1, D0) = (1, 1, 0, 0)
12. DUTY register : (D3, D2, D1, D0) = (0, 0, 1, 1) (1/64 duty)
    Start spot (block) register : (D3, D2, D1, D0) = (0, 0, 0) (COM0)
13. Read modify write : OFF
14. Built-in oscillation circuit : stop
15. Oscillation frequency register : (D3, D2, D1,D0) = (0, 0, 0, 0) (60kHz (TBD))
16. Power control register : (D2, D1, D0) = (0, 0, 0)
17. LCD drive voltage selection resister : (D2, D1, D0) = (0,0,0)
18. LCD bias change register : (D1, D0) = (0, 0)
19. Electronic volume register : (D6, D5, D4, D3, D2, D1, D0) = (0, 0, 0, 0, 0, 0, 0)
20. Discharge : ON (only for when $\overline{RES}$ = LOW)
21. Power save : OFF
22. Temperature gradient resistor : (D2, D1, D0) = (0, 0, 0) (–0.06/°C)
23. Register data in the serial interface : Clear
24. MLS drive select register: (D4, D3, D2, D1, D0) = (0, 1, 0, 1, 1) (Non-dispersion drive)
25. Temperature sensor

When the Reset command is used, only the above-mentioned inilialized items 7, 8 and 13 are executed.

When power is turned on, initialization by the $\overline{RES}$ pin is necessary. After initialization by the $\overline{RES}$ pin, each input pin must be controlled correctly.
Furthermore, when control signals from the MPU have a high impedance, the excessive current may flow to the IC.
After V_{DD} is applied, measures should be taken to ensure that the input pin does not have a high impedance.
The S1D15714 Series discharges the electric charge of V_{OUT} and liquid crystal drive voltage (V_3,V_2, V_1, V_C, MV_1, MV_2) at the level of $\overline{RES}$ pin = LOW. When liquid crystal drive external power supply is used, external power supply should not be supplied during the period of $\overline{RES}$ = LOW to prevent external power supply and V_{DD} and V_{SS} from being short circuited.

7. COMMAND

The S1D15714 Series identifies data bus signals by a combination of A0, $\overline{RD}$(E) and $\overline{WR}$(R/$\overline{W}$). Interpretation and execution of the command are executed by the internal timing alone which is independent of the external clock. This allows high-speed processing.
The 80 series MPU interface allows the command to be started by entering the low pulse in the $\overline{RD}$ pin during reading and by entering the low pulse in the $\overline{WR}$ pin during writing.
The 68 series MPU interface allows a read state to occur by entering HIGH in the R/$\overline{W}$ pin, and permits a write state to occur by entering LOW. It also allows the command to be started by entering the high pulse in the pin E. (For timing, see the description of "10. Timing characteristics").

Accordingly, the 68 series MPU interface is different from 80 series MPU interface in that $\overline{RD}$(E) is "1(H)" in the case of display data/read shown in the Command Description and Command Table. The following describes the commands, based on the example of the 80 series MPU interface:
When the serial interface is selected, enter data sequentially starting from D7.

Command Description

(1) Display ON/OFF

This command sets the display ON/OFF.
When Display OFF is specified, the driver common to segments outputs the V_C level.

A0	E ($\overline{RD}$)	R/$\overline{W}$ ($\overline{WR}$)	D7	D6	D5	D4	D3	D2	D1	D0	Output level
0	1	0	1	0	1	0	1	1	1	0	Display OFF
										1	Display ON

(2) Display Normal/Reverse

This command allows the display ON/OFF state to be reversed, without having to rewrite the contents of the display data RAM. In this case, contents of the display data RAM are maintained.

A0	E ($\overline{RD}$)	R/$\overline{W}$ ($\overline{WR}$)	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	1	1	0	RAM data = HIGH LCD ON Voltage (normal)
										1	RAM data = LOW LCD ON Voltage (reverse)

(3) Display All Lighting ON/OFF

This command forces all the displays to be turned on independently of the contents of the display data RAM. In this case, the contents of the display data RAM are maintained. Fully white display can also be made by a combination of the Display Reverse command.

A0	E ($\overline{RD}$)	R/$\overline{W}$ ($\overline{WR}$)	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	1	0	0	Normal display status
										1	Display all lighting

(4) Common Output Status Select

This command allows the scanning direction of the COM output pin to be selected. For details, see the description of "6.5.2 COM Drivers" in the Function Description.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Selected state	
0	1	0	1	1	0	0	0	1	0	0	Normal	COM0 → COM63 → COMS
										1	Reverse	COM63 → COM0 → COMS

(5) Display Start Line set (2-byte command)

The parameter following this command specifies the display start line address of the display data RAM shown in Fig. 6.4.
The display area is indicated in the direction where line address numbers are incremented, starting from the specified line address. If a dynamic change of the line address is made by this command, smooth scrolling in the longitudinal direction and page breaking are enabled. For details, see the description of "6.2.3 Line address circuit" in the Function Description.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	0	0	0	1	0	1	0	Mode setting
1	1	0	L7	L6	L5	L4	L3	L2	L1	L0	Register setting

• Display Start Line Set command parameter

L7	L6	L5	L4	L3	L2	L1	L0	Line address
*	*	0	0	0	0	0	0	00H
*	*	0	0	0	0	0	1	01H
*	*	0	0	0	0	1	0	02H
				↓				↓
*	*	1	1	1	1	1	0	3EH
*	*	1	1	1	1	1	1	3FH

Set to line address 000H at the time of resetting.
* : denote invalid bits.

• Line address setting sequence

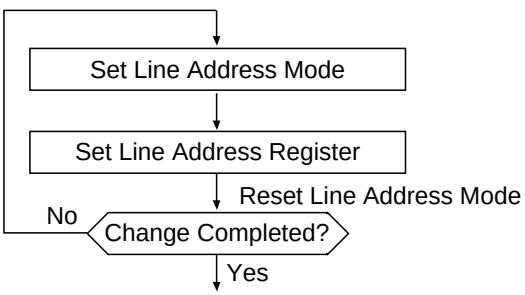


Fig. 7.1

(6) Page Address Set

This command specifies the page address corresponding to row address when MPU access to the display data RAM shown in Fig. 6.4. The column address is split into two sections (higher 4 bits and lower 4 bits) when it is set. Each time the display data RAM is accessed, the column address automatically increments (+1), making it possible for the MPU to continuously read and write the display data. For details, see the description of "6.2.2 Page address circuit" in the Function Description.

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0	Page address
0	1	0	1	0	1	1	P3	P2	P1	P0	Page address set

*: denote invalid bits.

P3	P2	P1	P0	Page address
0	0	0	0	Page 0
0	0	0	1	Page 1
		↓		↓
0	1	1	1	Page 7
1	0	0	0	Page 8

(7) Column Address Set

This command specifies the column address of the display data RAM shown in Fig. 6.4. A column address should be set separately, higher 4 bits and lower 4 bits. Since the increment (+1) of the column address is carried out automatically everytime a display data RAM is accessed MPU can Read/Write display data continuously. Please refer to 6.2.2 column address circuits of functional explanation for more details.

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	0	0	0	1	C7	C6	C5	C4	Column address higher set
0	1	0	0	0	0	0	C3	C2	C1	C0	Column address lower set

C7	C6	C5	C4	C3	C2	C1	C0	Column address
0	0	0	0	0	0	0	0	00H
0	0	0	0	0	0	0	1	01H
0	0	0	0	0	0	1	0	02H
				↓				↓
1	0	1	0	0	1	1	0	A6H
1	0	1	0	0	1	1	1	A7H

(8) Display Data Write

This command allows the 8-bit data to be written to the address specified by the display data RAM. After writing, column address or page address is automatically incremented +1 by the Display Data Input Direction Select command. This enables the MPU to write the display data continuously.

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	Write Data							

(9) Display Data Read

This command allows the 8-bit data to be read from the address specified by the display data RAM. After reading, column address or page address is automatically incremented +1 by the Display Data Input Direction select command. This enables the MPU to read multiple word data continuously.
It should be noted that one dummy reading is essential immediately after the column address or page address has been set. For details, see the description of "6.1.5 Access to display data RAM and internal register" in the Function Description. When the serial interface is used, display data cannot be read.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	Read Data							

(10) Display Data Input Direction Select

This command sets the direction where the display RAM address number is automatically incremented. For details, see the description of "6.2.3 Column address circuit" in the Function Description.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Direction
0	1	0	1	0	0	0	0	1	0	0	Column
										1	Page

(11) Column Address Set Direction

This command can reverse the relationship between the display RAM data column address and segment driver output shown in Fig. 6.4. So you can reverse the sequence of segment driver output pins using this command. When the display data is written or read, the column address is incremented by (+1) according to the column address given in Fig. 6.4. For details, see the description of "6.2.2 Column address circuit" in the Function Description.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	0	0	0	Normal
										1	Reverse

(12) n-line Inversion Drive Register Set

This command sets the liquid crystal alternating drive reverse line count in the register to start line reverse driving operation. The line count to be set is 4 to 60 (15 states for each 4 lines. For details, see the description of "6.4 Display timing generation circuit" in the Function Description.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Reverse line count
0	1	0	0	0	1	1	N3	N2	N1	N0	Reverse line count

N3	N2	N1	N0	Reverse line count
0	0	0	0	4 (1 × 4)
0	0	0	1	8 (2 × 4)
		↓		↓
1	1	0	1	56 (14 × 4)
1	1	1	0	60 (15 × 4)

(13) n-line Inversion Drive ON/OFF

This command provides ON/OFF control of n-line inverting drive.

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0	n-line
0	1	0	1	1	1	0	0	1	0	0	OFF
										1	ON

(14) Duty Set Command

Liquid crystal drive at a lower power consumption is ensured by using this command to change the duty. Use of this command also allows display at a desired position on the panel (continuous CON pins + COM on a 4-line basis). This command is used with a pair of the duty set parameter and start point (block) parameter, so be sure to set both parameters so that one of them will immediately follow the other.

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0	Selected state
0	1	0	0	1	1	0	1	1	0	1	Duty set command
0	1	0	U3	U2	U1	U0	S3	S2	S1	S0	Duty set, Start point set

*: denote invalid bits.

• Duty set

Duty can be set in the range from 1/5 duty to 1/65 duty by 4 steps. It should be set in higher 4 bits (D7, D6, D5, D4). Set to 1/65 duty after resetting.

U3	U2	U1	U0	Display duty
0	0	0	0	1/5
0	0	0	1	1/9
0	0	1	0	1/13
0	0	1	1	1/17
0	1	0	0	1/21
0	1	0	1	1/25
0	1	1	0	1/29
0	1	1	1	1/33
1	0	0	0	1/37
1	0	0	1	1/41
1	0	1	0	1/45
1	0	1	1	1/49
1	1	0	0	1/53
1	1	0	1	1/57
1	1	1	0	1/61
1	1	1	1	1/65

• Start point (block) register set parameter

Use this parameter to set 4-bit data in the start point (block) register. Then one of 16 start point blocks will be determined. It should be set in lower 4 bits (D3, D2, D1, D0).

S3	S2	S1	S0	Start piont setting
0	0	0	0	0 (COM0 to 3)
0	0	0	1	1 (COM4 to 7)
0	0	1	0	2 (COM8 to 11)
		↓		↓
1	1	1	0	14 (COM56 to 59)
1	1	1	1	15 (COM60 to 63)

Set to 0 block at the time of resetting

*1 Voltage optimum to liquid crystal drive is changed when the duty is changed. Use the electronic volume and set the voltage to get the optimum display.
*2 For display scroll, use (5) Display Start Line Set Command, and do not scroll displays by using this command.

• Duty command setup example

1. Duty 1/49 When 1 (COM4 to COM7) is specified as the start point (block)
   Display area COM4 to COM51, COMS
2. Duty 1/33 When 10 (COM44 to COM47) is specified as the start point (block)
   Display area COM44 to COM63 and COM0 to COM11, COMS

* When the COM pin is not commonly used for the master and the slave in a master/slave two-chip operation (SEG 168 pieces are made common and two screens of 168×120dots are driven up and down with COM 60 pieces + COM 60 pieces), the display thick will become different between the master-side display area and the slave-slave display area unless the master and the salve a re of the same duty. Set a same duty to both the master and the slave. When either the master side or the slave side is not displayed, input the Display OFF Command to the side, which you do not want to display, so that the VC level is output.

(15) Read Modify Write

This command is paired with end command for use. If this command is entered, the column address is not changed by the Display Data Read command. It can be incremented +1 by the Display Data Read command alone. This state s retained until the End command is input. If the End command is input, the column address goes back to the address when the Read Modify Write command is input. This function reduces the MPU loads when changing the data repeated in the specific display area such as blinking cursor.

A0	$\overline{E}$ $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	0

* A command other than display data Read/Write command can be used in the Read Modify Write mode. However, you cannot use the column address set command.

• Sequence for cursor display

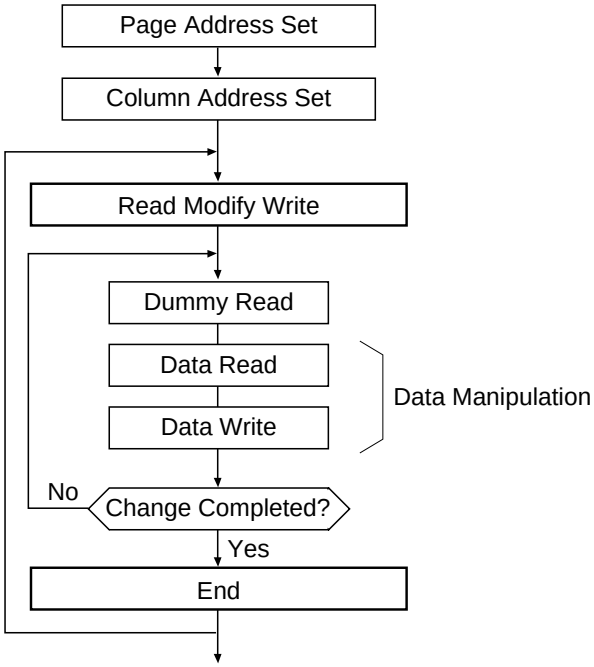


Fig. 7.2

(16) End

This command releases the read modify write mode and gets column address back to the initial address of the mode.

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	1	0

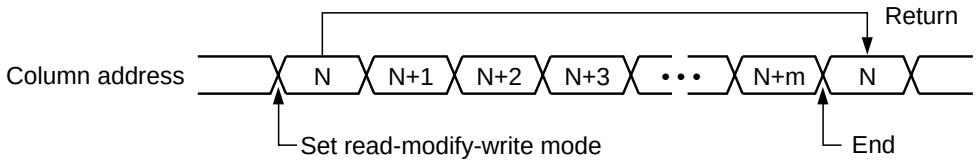


Fig. 7.3

(17) Built-in Oscillator Circuit ON/OFF

This command starts the built-in oscillator circuit operation. It is enabled only in the master operation mode (M/S = HIGH) when built-in oscillator circuit is valid (CLS = HIGH).
When the built-in power supply is used, the Oscillator Circuit ON command must be executed before the Power Control Set command. (See the description of "(21) power control command"). If the built-in oscillator circuit is turned off when the built-in power supply is used, display failure may occur.

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0	Built-in oscillator circuit
0	1	0	1	0	1	0	1	0	1	0	OFF
										1	ON

(18) Built-in Oscillator Circuit Frequency Select

This command sets the built-in oscillator circuit frequency. The frequency can be selected whether the built-in oscillator circuit is turned on or off.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	fCL kHz
0	1	0	0	1	1	1	F3	F2	F1	F0	Frequency Set

F3	F2	F1	F0	CL Frequency fCL [kHz]	Frame frequency, fFR [Hz] 1/65Duty	1/49Duty	1/33Duty
0	0	0	0	100	92	120	174
0	0	0	1	86.8	80	104	151
0	0	1	0	78.0	72	94	135
0	0	1	1	69.8	64	84	121
0	1	0	0	65.1	60	78	113
0	1	0	1	59.4	55	71	103
0	1	1	0	55.3	51	66	96
0	1	1	1	51.3	47	62	89
1	0	0	0	49.0	45	59	85
1	0	0	1	45.8	42	55	80
1	0	1	0	43.5	40	52	75
1	0	1	1	41.0	38	49	71
1	1	0	0	39.4	36	47	68
1	1	0	1	37.4	34	45	65
1	1	1	0	35.8	33	43	62
1	1	1	1	34.1	31	41	59

(F3, F2, F1, F0) = (0, 0, 0, 0) is set after resetting.

* The values in the above table are representative values at 25°C. Consider that there are dispersions of ±8% at 25°C. fFR means the cycle to rewrite a screen (frame frequency) and is calculated from the following equation:

$$f_{FR} = \frac{f_{CL}}{(n+3)\times 16} \quad (n = 1/Duty)$$

This does not indicate the frequency of the fFR signal.

(19) Power Control Set

This command sets the built-in power supply circuit function. For details, see the description of "6.6 Power supply circuit" in the Function Description.

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0	Selected state
0	1	0	0	0	1	0	0	1	0	1	Command
1	1	0	0	0	0	0	0	P2	P1	P0	Register set

P2	P1	P0	Selected state
0			Step-up: OFF
1			Step-up: ON
	0		V_3: OFF
	1		V_3: ON
		0	LCD voltage: OFF
		1	LCD voltage: ON

V_3 : Voltage adjustment circuit (V_3 adjustment circuit)
LCDV : Liquid crystal rive potential (V_2, V_1, V_C, NV1, NV2) generation circuit

An internal clock is required to operate the built-in power supply circuit. During the operation of the built-in power supply circuit, be sure that the internal clock is present inside.
If the built-in oscillator circuit is used, execute the built-in oscillator circuit ON command before the power control set command. If an external oscillator circuit is used, operate the external oscillator circuit before the power control set command.
If the internal clock is cut off during the operation of the built-in power supply circuit, display failure may occur. To avoid this, do not cut it off.

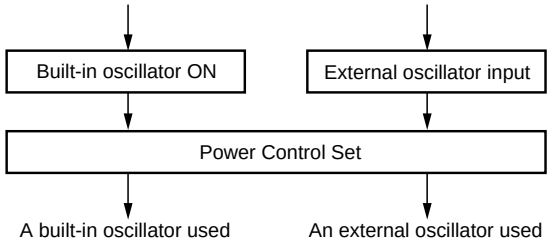


Fig. 7.4

(20) Liquid Crystal Drive Voltage Select

The liquid crystal drive voltage range issued from the liquid crystal drive voltage regulating circuit is selected from 3 states by this command.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	V_3 voltage output range
0	1	0	0	0	1	0	0	V2	V1	V_0	V_3 voltage range set

V2	V1	V0	V_3 voltage output range
0	0	0	5.6 to 7.0V
0	0	1	6.3 to 7.8V
0	1	0	7.1 to 8.9V
0	1	1	8.0 to 10.0V
1	0	0	9.2 to 11.4V
1	0	1	10.3 to 12.8V
1	1	0	11.7 to 14.5V
1	1	1	12.8 to 16.0V

(V2, V1, V0) = (0, 0, 0) is set after resetting.

(21) LCD Bias Change

With this command, the bias ratio of liquid crystal drive voltage should be chosen from 4 states.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Bias ratio
0	1	0	0	1	0	1	0	0	B1	B0	Bias ratio set

B1	B0	Bias ratio
0	0	1/8
0	1	1/6.7
1	0	1/5.3

(22) Electronic Volume

This command controls liquid crystal drive voltage V3 issued from the built-in liquid crystal power supply voltage regulating circuit, and adjusts the liquid crystal display density. For details, see the description of "6.6.2 Voltage Regulating Circuit" in the Function Description.

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	0	0	0	0	0	0	1	Mode set
0	1	0	R7	R6	R5	R4	R3	R2	R1	R0	Register

• Electronic Volume Mode Set

Inputting this command makes the Electronic Volume Register Set Command valid. Once the Electronic Volume Mode Set Command is input, any command other than the Electronic Volume Register Set Command cannot be used. After data are saved in the register by the Electronic Volume Register Set Command, this command is released.

• Electronic Volume Register Set

When a 7-bit data to the electronic volume register is set by this command, liquid crystal drive voltage V3 assumes one state out of voltage values in 128 states.
After this command is input, and the electronic volume register is set, the electronic volume mode is reset.

R7	R6	R5	R4	R3	R2	R1	R0	Vc
*	0	0	0	0	0	0	0	Smaller
*	0	0	0	0	0	0	1	
*	0	0	0	0	0	1	0	
				↓				↓
*	1	1	1	1	1	1	0	
*	1	1	1	1	1	1	1	Larger

*: denote invalid bits.

• Electronic volume register set sequence

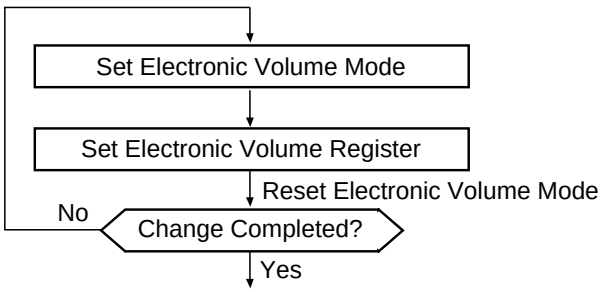


Fig. 7.5

(23) Discharge ON/OFF

This command discharges the capacitors connected to the power supply circuit. This command is used when the system power of this IC (S1D15714 Series) is turned off, and the duty is changed. See the description of (3) Power Supply OFF and (4) Changing the Duty in the Instruction Setup: Reference.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	1	1	0	1	0	1	0	Discharge OFF
										1	Discharge ON

* If this command is executed when the external power supply is used, a large current may flow to damage the IC. If external power supply is used to drive liquid crystal, be sure to turn off the external power supply before executing this command.

(24) Power Saving

This command establishes the power save mode, thereby ensuring a substantial reduction of current consumption.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Power save mode
0	1	0	1	0	1	0	1	0	0	0	OFF
										1	ON

In the power save mode, display data and operation before power saving are maintained. Access to the display data RAM from the MPU is also possible. The current consumption is reduced to the value close to static current if all operations of the LCD display system are stopped and there is no access from the MPU.

In the power save mode, the following occurs:

Stop of oscillator circuit
Stop of LCD power supply circuit
Stop of all liquid crystal drive circuit (V_{SS} level output is issued as the segment and common driver output).

When the temperature sensor is set to ON, the sensor circuit operates even under the power saving status. To reduce current consumption, use the Temperature Sensor ON/OFF Command to control current as the need arises.

When the Power Save OFF Command is input, the power saving status will be released, and the system will return to the status before the power save mode started.

• Power Save Sequence

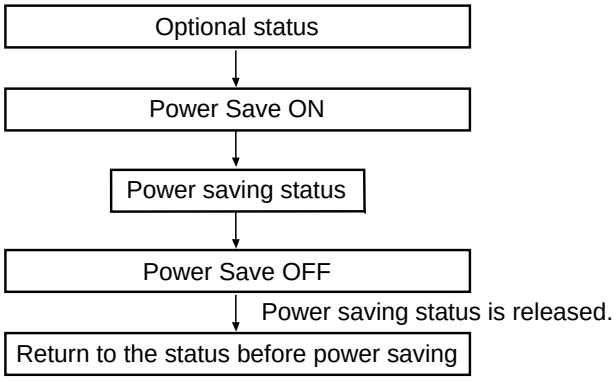


Fig. 7.6

* When the external power supply is used, it is recommended to stop the external power supply circuit function when the power save mode is started. For example, when each level of the liquid crystal drive voltage is given from the external resistive divider circuit, it is recommended to add a circuit to cut off the current flowing to the resistive divider circuit when power save function is started. The S1D15714 Series has a liquid crystal display blanking control control pin DOF, and the level goes LOW when power save function is started. You can use the DOF output to stop the external power supply circuit function.

(25) Temperature Gradient Set

The 3-bit data of this command is used to set the temperature gradient characteristics of the liquid crystal drive voltage output from the built-in power supply circuit from eight states to one state. The temperature gradient of the liquid crystal drive voltage can be set according to the liquid crystal temperature gradient to be used. This eliminates the need of a temperature characteristics regulating circuit to be installed outside this IC (S1D15714 Series).

A0	$\overline{E}$ / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Temperature gradient [%/°C]
0	1	0	0	1	0	0	1	T2	T1	T0	Temperature gradient set

T2	T1	T0	Temperature gradient [%/°C]
0	0	0	–0.06
0	0	1	–0.08
0	1	0	–0.10
0	1	1	–0.11
1	0	0	–0.13
1	0	1	–0.15
1	1	0	–0.17
1	1	1	–0.18

(T2, T1, T0) = (0, 0, 0) is set after resetting. *: denote invalid bits.

(26) Status Read

This command reads out the temperature gradient select bit set on the register.
After inputting the Status Read Mode Set Command, continue reading. After the status reading ends, the Status Read Mode will be released.

A0	$\overline{E}$ / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Temperature gradient [%/°C]
0	1	0	1	0	0	0	1	1	1	0	Mode Set
0	0	1	*	*	*	*	*	T2	T1	T0	Register

*: denote invalid bits.

T2	T1	T0	Temperature gradient [%/°C]
0	0	0	–0.06
0	0	1	–0.08
0	1	0	–0.10
0	1	1	–0.11
1	0	0	–0.13
1	0	1	–0.15
1	1	0	–0.17
1	1	1	–0.18

(27) Reset

This command resets the column address and the page address to 0 and releases the read modify write mode and test mode without giving adverse effect to the display data RAM. For details, see the description of "6.7 Reset" in Function Description. Resetting is carried out after the reset command has been input.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	0

Initialization upon application of power supply is carried out by the reset signal to the $\overline{RES}$ pin. The reset command cannot be used for this purpose.

(28) Temperature Sensor ON/OFF

ON/OFF of a temperature sensor is specified with this command.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Set up
0	1	0	0	1	1	0	1	0	0	0	Temperature sensor OFF
										1	Temperature sensor ON

The temperature sensor off is set up after reset.

When using a built-in temperature sensor, the temperature sensor should be ON by using this command. Although there is no problem setting a temperature sensor ON even if it is not used, 10 μA grade current is consumed. The temperature sensor circuit is independently controlled from the Power Save Command.

(29) MLS Drive Select (2-byte Command)

This command is for selecting MLS drives and switches the dispersion drive and the non-dispersion drive. This command is a 2-byte command and is used together with the MLS Drive Select Mode Set Command and the MLS Drive Select Pattern Set Command. Be sure to input the both command in succession.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	1	1	0	0	1	1	1	Mode Set
0	1	0	*	*	*	0	M3	0	1	1	Pattern Set

* denotes invalid bit.

M3	M2	M1	M0	Pattern Set
0	0	1	1	Dispersion Drive
1	0	1	1	Non-dispersion Drive

The non-dispersion drive is set after resetting.

* The dispersion drive and the non-dispersion drive are liquid crystal driving methods unique to the MLS drive.
  The SID15714 Series adopt 4-line MLS drive. Selected voltages are output for the period (the period of 4/(65+3) of one frame for 65-line display) of about quadruple the selection period for the normal drive mode in which one line is selected and scanned each time (the period o 1/65 of one frame for 65-line display).
  In the non-dispersion drive, selection signals of 4-line data are output 4 times in succession. We recommend this drive when displays are frequently changed.
  In case of the dispersion drive, selection signals are divided into and output 4 times in one frame period. This driving method allows reducing the frame frequency. To reduce consumption current, we recommend this drive. In this case, however, displays may blink, and this drive is not suitable for movie display.

(30) NOP

This is a Non-Operation command.

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	1

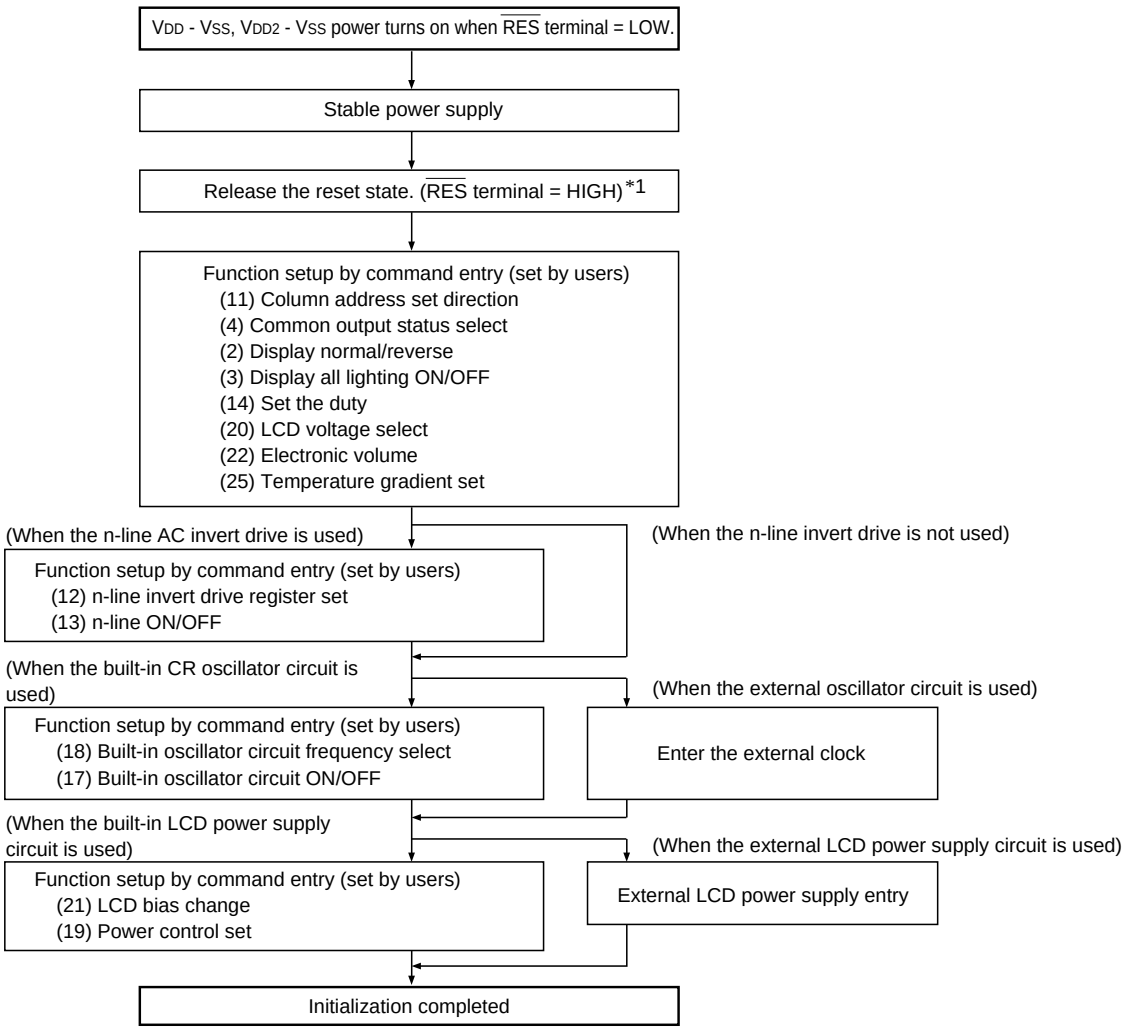
Note: S1D15714 Series maintains the operation status due to the command. However, when exposed to excessive external noise, internal status may be changed. This makes it necessary to take some measures which reduces noise generation in terms of installation or system configuration, or which protects the system against adverse effect of noise. To cope with sudden noise, it is recommended to refresh the operation status on a periodic basis.

Table 7.1 Table of commands in S1D15714 Series series

Command	Command code											Function
	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
(1) Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0 1	LCD display ON/OFF control. 0: OFF, 1: ON
(2) Display Normal /Reverse	0	1	0	1	0	1	0	0	1	1	0 1	LCD display normal/reverse 0: Normal, 1: Reverse
(3) Display All Lighting ON/OFF	0	1	0	1	0	1	0	0	1	0	0 1	Display All Lighting 0: Normal display, 1: All ON
(4) Common Output Status Select	0	1	0	1	1	0	0	0	1	0	0 1	Selects COM output scan direction. 0: Normal, 1: Reverse
(5) Display Start Line Set	0 0	1 1	0 0	1 *	0 *	0 Display start line address	0	1	0	1	0	Sets display start line.
(6) Page Address Set	0	1	0	1 *	0 *	1	1 Page address	0	0	0	1	Sets the display RAM page address.
(7) Column Address Set Higher bits	0	1	0	0	0	0	1	Higher column address				Higher 4 bits of column address in Display RAM are set.
Column Address Set Lower bits	0	1	0	0	0	0	0	Lower column address				Lower 4 bits of column address in Display RAM are set.
(8) Display Data Write	1	1	0	Writes data								Writes data to the display RAM.
(9) Display Data Read	1	0	1	Reads data								Reads data to the display RAM.
(10) Display Data Input Direction Select	0	1	0	1	0	0	0	0	1	0	0 1	Display RAM data input direction 0: Column direction 1: Page direction
(11) Column Address Set Direction	0	1	0	1	0	1	0	0	0	0	0 1	Compatible with display RAM address SEG output 0: Normal 1: Reverse
(12) n-line inversion Drive Register Set	0	1	0	0	0	1	1	Invert line count				Line invert drive. Sets the line count.
(13) n-line ON/OFF	0	1	0	1	1	1	0	0	1	0	0	Resets the line invert drive. 0: n-line OFF 1: n-line ON
(14) Duty Set Command Duty Set Static spot set	0 0	1 1	0 0	0 *	1 *	1 Static spot (block)	0	1	1	0	1	2 byte command
(15) Read Modify Write	0	1	0	1	1	1	0	0	0	0	0	Increments the column address. Increments +1 in the write mode. Does not increment in the read mode.
(16) End	0	1	0	1	1	1	0	1	1	1	0	Resets read modify write functions.
(17) Built-in Oscillator Circuit ON/OFF	0	1	0	1	0	1	0	1	0	1	0 1	Built-in oscillator circuit operation 0: OFF, 1: ON
(18) Built-in Oscillator Circuit Frequency Select	0	1	0	0	1	1	1	Frequency				
(19) Power Control Set	0	1	0	0	0	1	0	1 Operation state				Selects built-in power supply operation state.
(20) Liquid Crystal Drive Voltage Select	0	1	0	0	0	1	0	0	V_3 range			
(21) LCD bias change	0	1	0	1	0	1	0	0	0	bias		Bias ratio select
(22) Electronic Volume Mode Set	0	1	0	1	0	0	0	0	0	0	1	
Electronic Volume Register Set	0	1	0	*	Electronic volume							V_3 output voltage is set to the electronic volume register. 128 states
(23) Discharge ON/OFF	0	1	0	1	1	1	0	1	0	1	0 1	Discharges Power supply circuit connection capacitor. 0: OFF (normal), 1: ON
(24) Power Save ON/OFF	0	1	0	1	0	1	0	1	0	0	0 1	Power Save 0: OFF, 1: ON
(25) Temperature Gradient Select	0	1	0	0	1	0	0	1 Temperature gradient				Sets to 8 steps.
(26) Stator Read	0 0	1 0	0 1	1 *	0 *	0 *	0 *	1 *Temperature gradient	1	1	0	Issues the temperature gradient select bit. * : denote invalid bits.
(27) Reset	0	1	0	1	1	1	0	0	0	1	0	Resets the column, page and address registers.Resets the read modify write function.
(28) Temperature Sensor ON/OFF	0	1	0	0	1	1	0	1	0	0	0	Temperature sensor 0 : OFF (normal), 1 : ON
(29) MLS Drive Select (2-byte command)	0 0	1 1	0 0	1 *	1 *	1 *	0 0	0 MLS	1 0	1 1	1 1	Mode Set MLS 0 : Dispersion, 1: Non-dispersion
(30) NOP	0	1	0	1	1	1	0	0	0	1	1	Non-operation command

Instruction Setup Example (Reference)

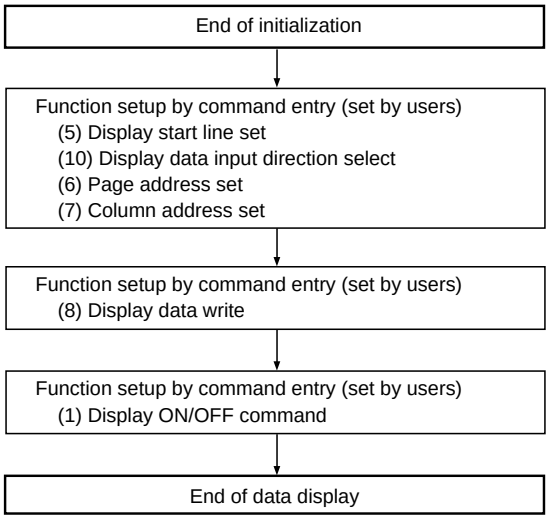
(1) Initial setup



Note: *1 DDRAM contents are not determined even in the initialized state after resetting. See “6.7 Reset Circuit” in the “6. Function Description”.

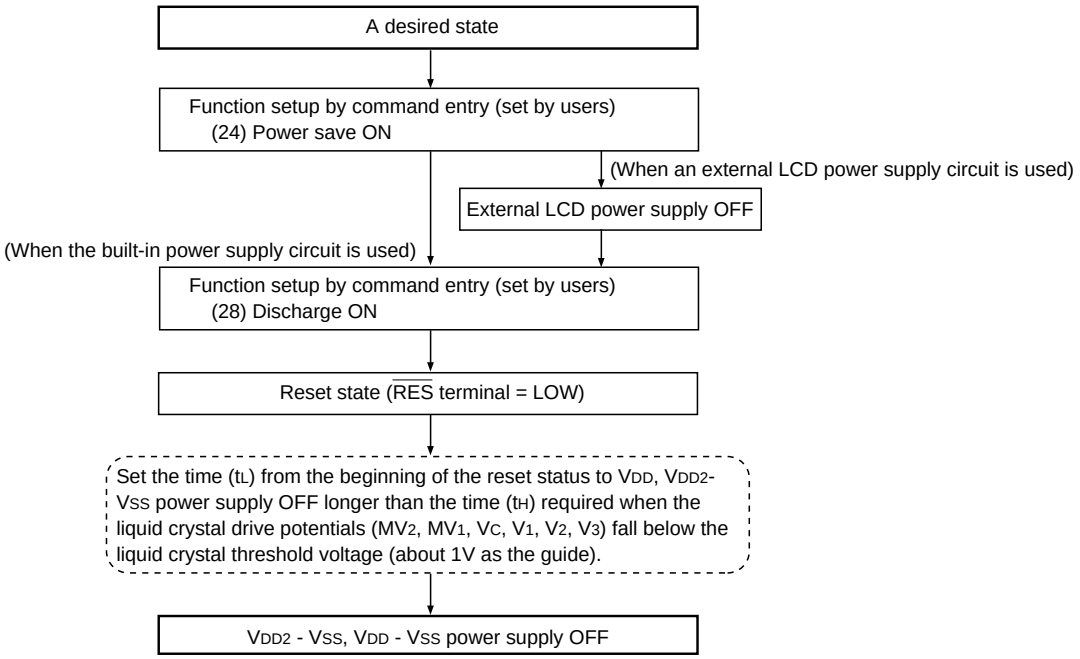
* Numerals in the command parenthesis correspond to the numerals of the items in Command Description.

(2) Data display



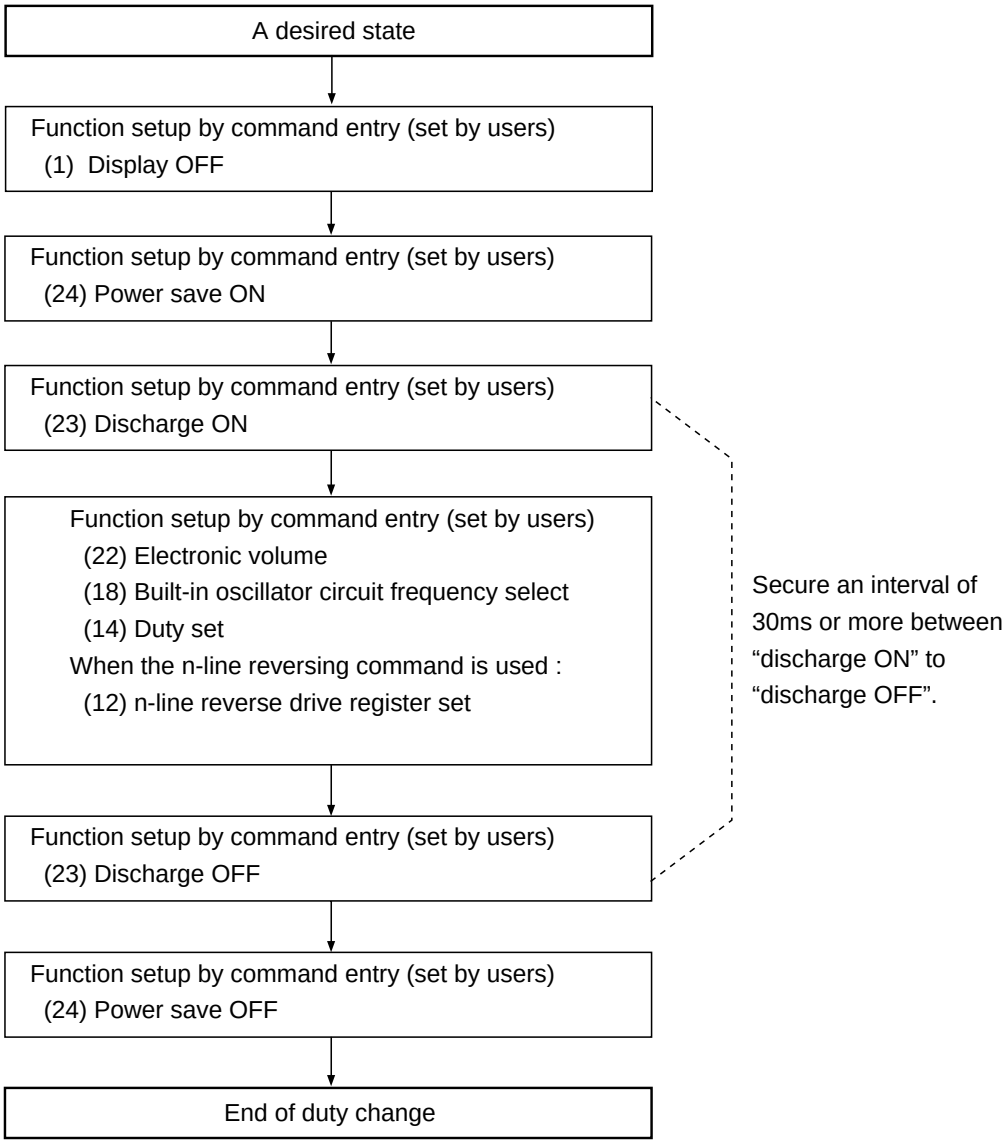
Note: * DDRAM contents are not determined after end of initialization. Write data to all the DDRAM used for display. See “9. Display data write” in the “7. Command Description”.

(3) Power OFF



Note: * This IC controls the circuit of the liquid crystal drive power supply system using the V_{DD}, V_{DD2}–V_{SS} power supply circuit. If the V_{DD}, V_{DD2}–V_{SS} power supply is cut off with voltage remaining in the liquid crystal drive power supply system, voltage not controlled will be issued from the SEG and COM pins, and this may result in display failure. To avoid this, follow the above-mentioned power off sequence.

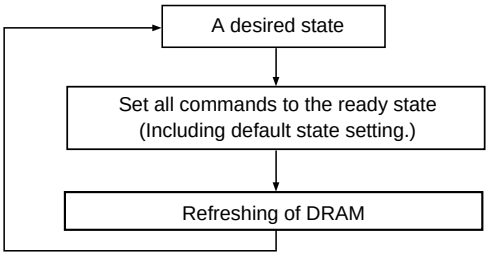
(4) How to change the duty



Note: * In the above sequence, the display disappears for the time from Power Save ON to Power Save OFF + about 350ms (in case of frame frequency 80Hz). When the Duty Set Command is executed while the liquid crystal display is on, there may occur the trouble that the display blinks momentarily. Observe the above sequence strictly.

(5) Refresh

It is recommended that the operating modes and display contents be refreshed periodically to prevent the effect of unexpected noise.



8. ABSOLUTE MAXIMUM RATINGS

Table 8.1 V_{SS} = 0V unless otherwise specified.

Item		Symbol	Specified value	Unit
Power voltage (1)		V_{DD}	–0.3 to +6.0	V
Power voltage (2)		V_{DD2}	–0.3 to +6.0	
Power voltage (3) when external input		V_{DI}	–0.3 to 3.6	
Power voltage (4)		V_3, V_{OUT}	–0.3 to 18.0	
Power voltage (5)		V_2, V_1, V_C, MV_1, MV_2	–0.3 to V_3	
Input voltage		V_{IN}	–0.3 to V_{DD}+0.3	
Output voltage		V_O	–0.3 to V_{DD}+0.3	
Operating temperature		T_{OPR}	–40 to +85	°C
Storage temperature	bare chip	T_{STR}	–55 to +125	

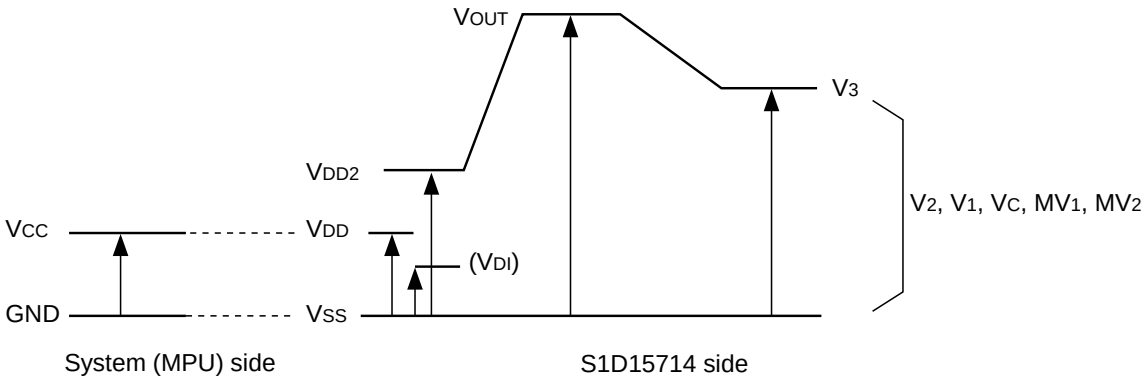


Fig. 8.1

Notes: 1. Voltages V_3, V_2, V_1, V_C, MV_1, MV_2 and MV_3 (V_{SS}) must always meet the conditions of $V_3 \geq V_2 \geq V_1 \geq V_C \geq MV_1 \geq MV_2 \geq MV_3$ (V_{SS}).
2. Voltage V_{OUT} must always meet the conditions of $V_{OUT} \geq V_{DD2} \geq V_{DD}$.
When inputting V_{OUT} from outside, maintain the condition of $V_{OUT} \geq V_3$+0.2V.
3. If the LSI has been used in excess of the absolute maximum rating, it may be subjected to permanent breakdown. So in the normal operation, the LSI is preferred to be used under the condition of electrical characteristics. If this condition is not met, LSI operation error may occur and LSI reliability may be deteriorated.

9. DC CHARACTERISTICS

V_{SS} = 0V, V_{DD} = (5V±10%) and Ta = –40 to +85°C unless otherwise specified.

Table 9.1

Item		Symbol	Conditions		Specified value Min.	Typ.	Max.	Unit	Applicable pin
Working voltage (1)	Operation enabled	V_{DD}	—		2.7	—	5.5	V	V_{DD} *1
Working voltage (2)	Operation enabled	V_{DD2}	—		V_{DD}	—	5.5		V_{DD2}
Working voltage (3)	Operation enabled	V_{DI}	External input		2.7	—	3.3		V_{DI}
Working voltage (4)	Operation recommended	V_{OUT}	—		V_{DD2}	—	16.2		V_{OUT}
Working voltage (5)	Operation enabled	V_3	—		5.6	—	16.2		V_3 *2
High-level input voltage Low-level input voltage		V_{IHC} V_{ILC}	V_{DD}=2.7V to 5.5V		0.8×V_{DD} V_{SS}	— —	V_{DD} 0.2×V_{DD}		*3 *3
High-level output voltage (1) Low-level output voltage (1)		V_{OHC1} V_{OLC1}	V_{DD}=2.7V to 5.5V	I_{OH}=–25µA I_{OL}=25µA	0.8×V_{DD} V_{SS}	— —	V_{DD} 0.2×V_{DD}		*4 *4
High-level output voltage (2) Low-level output voltage (2)		V_{OHC2} V_{OLC2}	V_{DD}=2.7V to 5.5V	I_{OH}=–100µA I_{OL}=100µA	0.8×V_{DD} V_{SS}	— —	V_{DD} 0.2×V_{DD}		*5 *5
High-level output voltage (3) Low-level output voltage (3)		V_{OHC3} V_{OLC3}	V_{DD}=2.7V to 3.3V	I_{OH}=–100µA I_{OL}=100µA	0.8×V_{DI} V_{SS}	— —	V_{DI} 0.2×V_{DI}		*6 *6
Input leak current Output leak current		I_{LI} I_{LO}	V_{IN}=V_{DD} or V_{SS}		–1 –3	— —	1 3	µA	*7 *8
LCD driver ON resistance		R_{ON}	Ta=25°C	V_3=7.2V V_3=14.0V	— —	10 5	20 10	kΩ	SEGn COMn *9
Static current consumption		I_{DDQ} I_{3Q}	Ta=25°C	V_{DD}=3.0V V_3=16V	— —	0.3 5	5 20	µA	V_{DD} *10 V_3
Input pin capacity		C_{IN}	Ta=25°C, f=1MHz		—	8	16	pF	—
Oscillation frequency	Internal oscillation External input	f_{CL} f_{CL}	Ta=25°C at the maximum frequency Ta=25°C at the maximum frequency		92 92	100 100	108 108	kHz kHz	*11 *11

[Asterisked references]

*1. Does not guarantee if there is an abrupt voltage variation during MPU access.

*2. For V_{DD2} and V_3 system operating voltage range, see Fig. 9.4.
Applicable when the external power supply is used.

*3. A0, D0 to D5, D6(SCL), D7(SI), $\overline{RD}$(E), $\overline{WR}$(R/$\overline{W}$), $\overline{CS}$, CS2, CLS, CL, FR, F1, F2, SYNC, M/S, C86, P/S, $\overline{DOF}$, $\overline{RES}$, TEST and TEST 1 pins.

*4. Do to D7 pin.

*5. CL pin.

*6. FR, $\overline{DOF}$, F1, F2, SYNC pins.

*7. A0, $\overline{RD}$(E), $\overline{WR}$(R/$\overline{W}$), $\overline{CS}$, CLS, M/S, C86, P/S, $\overline{RES}$, TEST and TEST 1 pins.

*8. Applicable when D0 to D5, D6(SCL), D7(S1), CL, FR, $\overline{DOF}$, F1, F2 and SYNC pins have a high impedance.

*9. Indicates the resistance when 0.1V voltage is applied between the output pin SEGn or COMn and each power supply (V_2, V_1, V_C, MV_1, MV_2).
R_{ON} =0.1V/ΔI (where ΔI denotes current when 0.1V is applied when power is on).

*10. Current value when TEST1 = LOW

*11. For the relations between oscillation frequency and frame frequency, see Table 9.7. Specified values of external input items are recommended.

Table 9.2

Item		Symbol	Conditions	Specified value			Unit	Applicable pin
				Min.	Typ.	Max.		
Built-in power circuit	Input voltage	V_{DD2}	Equal boosting	2.7	—	5.5	V	V_{DD2}
		V_{DD2}	Double boosting	2.7	—	5.5		
		V_{DD2}	Triple boosting	2.7	—	5.3		
		V_{DD2}	Quadruple boosting	2.7	—	4.0		
		V_{DD2}	Quintraple boosting	2.7	—	3.2		
	Amplified output voltage	V_{OUT}	—	—	—	16.2		V_{OUT}
	Voltage adjusting circuit operating voltage	V_3	—	5.6	—	16.2		V_3 *12

*12. The V_3 voltage adjusting circuit is adjusted within the electronic volume operating range.

Dynamic current consumption value (1)

The built-in power supply is ON while the display is on.

Table 9.3 All displays in white

Symbol : $I_{SS}(1)$

V_{DD}	Boosting	V_3 voltage	1/65 Duty		1/33 Duty		Unit	Remarks
			Typ.	Min.	Typ.	Min.		
5V	Triple	14V	64	107	48	80	µA	*13
		10V	61	102	45	75		
	Double	8V	60	100	42	70		
3V	Quintuple	14V	74	123	—	—		
	Quadruple	10V	61	102	47	78		
	Triple	8V	57	95	42	70		

[* marked section: Refer to page 51.]

Table 9.4 Display heavy load display *14

Symbol : $I_{SS}(1)$

V_{DD}	Boosting	V_3 voltage	1/65 Duty		1/33 Duty		Unit	Remark
			Typ.	Min.	Typ.	Min.		
5V	Triple	14V	103	172	66	110	µA	*13
		10V	82	137	55	92		
	Double	8V	72	120	47	78		
3V	Quintuple	14V	128	213	—	—		
	Quintuple	14V	86	143	58	97		
	Triple	8V	72	120	49	82		

[* marked section: Refer to page 51.]

• Current consumption under power saving mode: V_{SS} = 0V, V_{DD} = 5V, TEST1 = HIGH, Ta = 25°C

Table 9.5

Item	Symbol	Condition	Specified value			Unit	Remarks
			Min.	Typ.	Max.		
Sleep state	I_{DDS1}	—	—	6	20	µA	—

• Current Consumption at power saving(2) V_{SS} = 0V, V_{DD} = V_{DI} = 3V, TEST1 = LOW, Ta = 25°C

Table 9.6 Temperature sensor characteristics

Item	Symbol	Condition	Specified value			Unit	Applicable pin
			Min.	Typ.	Max.		
Sleep state	I_{DDS1}	—	—	0.3	5	µA	—

[Reference Data 1]
• Dynamic current consumption during LCD display when the internal power supply is used. V_3 = 14V *13

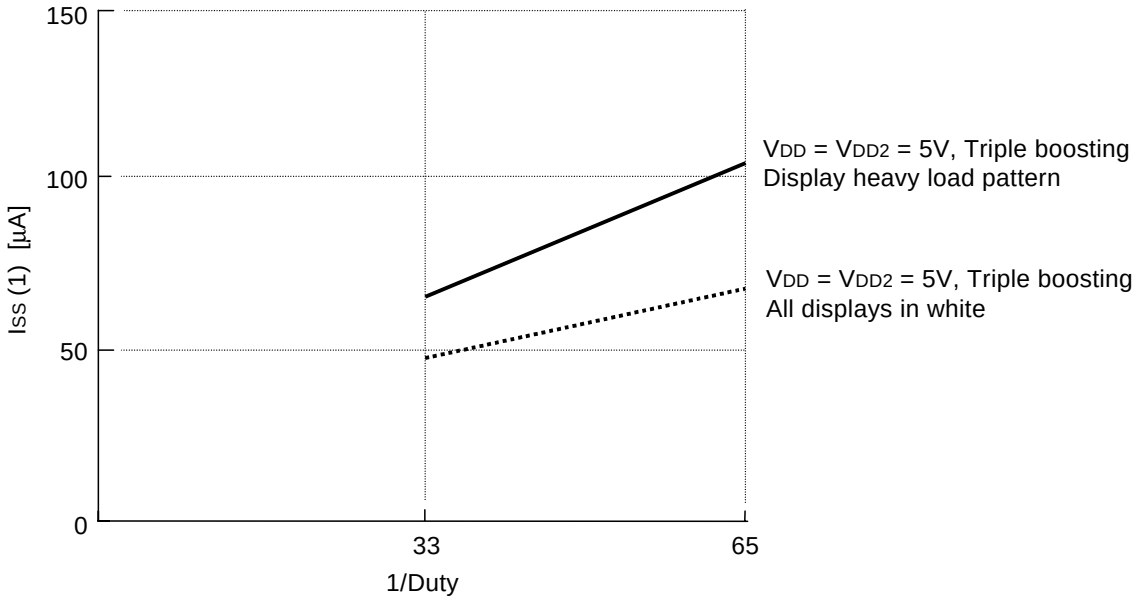


Fig. 9.1

[Reference Data 2]
• Dynamic current consumption during LCD display when the internal power supply is used. V_3 = 10V *13

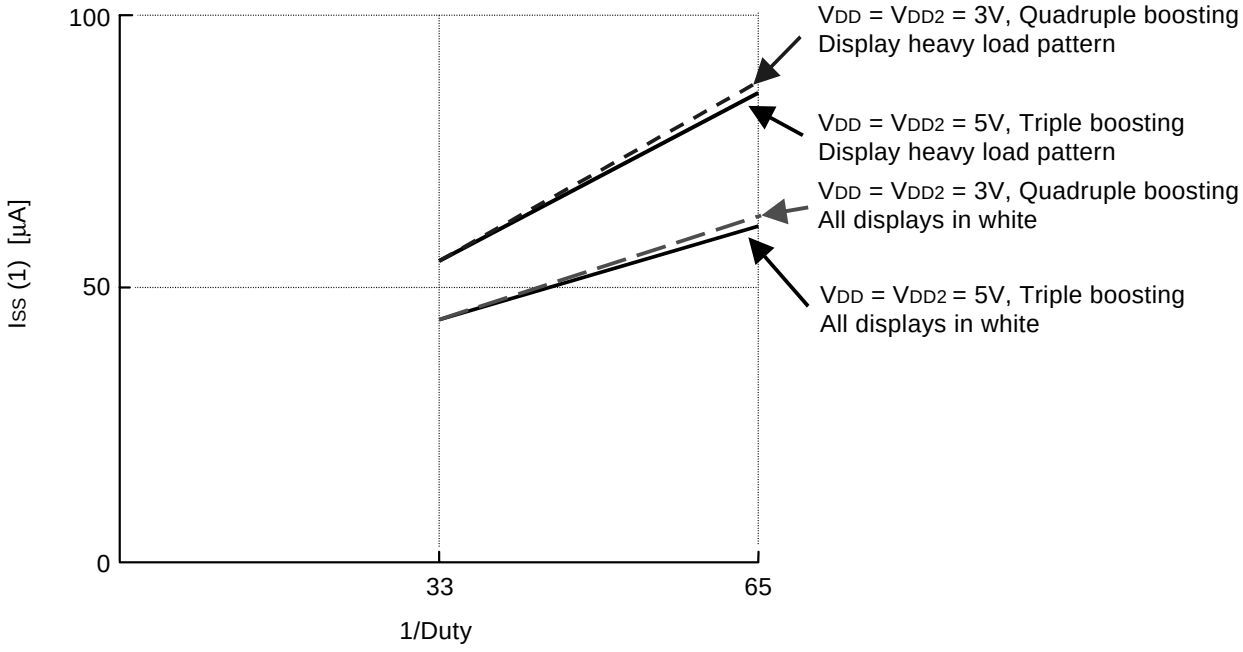
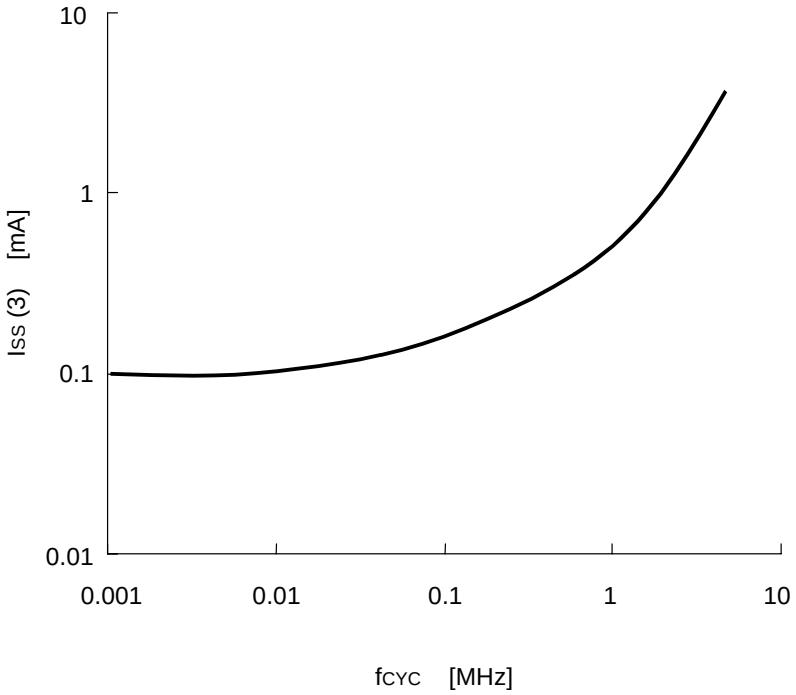


Fig. 9.2

[For the items marked with *, see Page 51.]

[Reference Data 3]

• Dynamic current consumption during access



This indicates the current consumption when the heavy load pattern is always written by fcyc.
When not accessed, only ISS(1) remains.

Conditions : V_{DD} = V_{DD2} = 5.0V,
V_3 = 14V
*13

Fig. 9.3

[Reference Data 4]

• Operating voltage range of V_{DD} and V_3 Systems
(Applicable when an external power supply is used.)

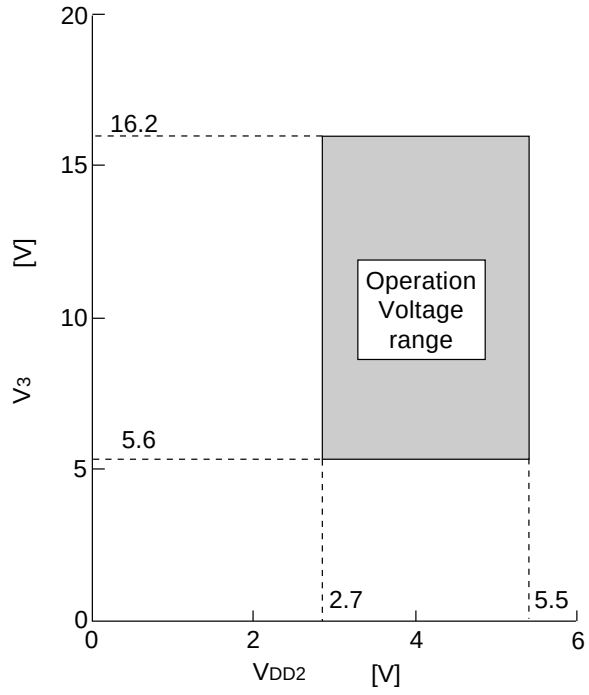


Fig. 9.4

[For the item marked with *, see Page 51.]

• Relationship between oscillation frequency f_{OSC}, display clock frequency f_{CL} and liquid crystal frame f_{FR}

Table 9.7

Item	f_{CL}	f_{FR}
Built-in oscillator circuit used	See p.33	$\frac{f_{CL}}{(n+3)\times 16}$
Built-in oscillator circuit not used	External input (f_{CL})	$\frac{f_{CL}}{(n+3)\times 16}(n = \frac{1}{Duty})$

(f_{FR} indicates the cycle of rewriting one screen; it does not indicate FR signal cycle.)

[Reference Matters for Items marked with *]

*13 Indicate the current consumed by the IC only as well as by the internal power supply when the display is ON. f_{FR} = 80Hz, $V_{DD} = V_{DD2}$, without n-line inversion, 1/8 bias, all internal power supply circuits are used. The internal oscillator circuit is not used. Current consumed by LCD panel capacity, wiring capacity, etc. is not included. This applies when no access is made from the MPU.

*14 Heavy load means the display pattern status when the maximum current is consumed.

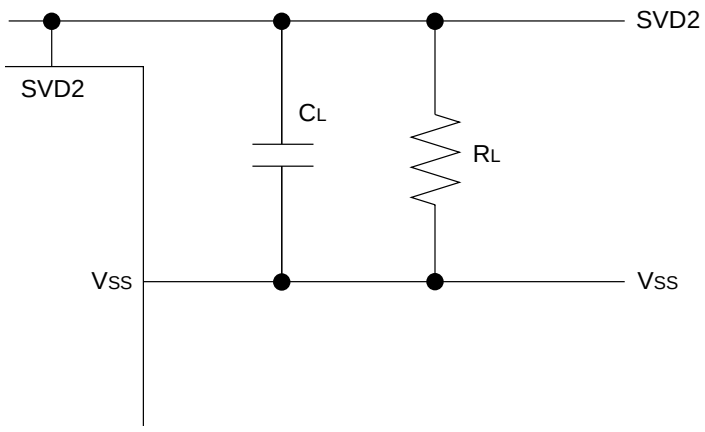
9.2 Characteristics of Temperature Sensor

Table 9.8

Item	Symbol	Condition	Specified value			Unit	Applicable pin
			Min.	Typ.	Max.		
Output voltage	V_{SVD2}	–35°C 25°C 80°C	1.430 1.164 0.907	1.475 1.200 0.935	1.519 1.236 0.963	V	SVD2 *1
Output voltage temperature gradient	V_{GRA}	*2	—	–4.70	—	mV/°C	SVD2
Output voltage linearity	ΔV_L	*3	–1.5	—	1.5	%	SVD2
Output voltage setup time	t_{SEN}	*4	100	—	—	mS	SVD2
Operating current	I_{SEN}	25°C	—	10	30	µA	V_{DD}

[Reference Matters for Items marked with *]

*1 Set the load capacity C_L of the sensor voltage output pin SVD2 to 100pF or below and the load resistance RL to 1MΩ or more. In order to get accurate output voltage values, do not provide with any current path between SVD2 and V_{SS}.



*2 Inclination of approximate straight line of Typ. output voltage between -35°C and 80°C . See Fig. 9.6.

*3 Maximum deviation between output voltage curve and approximate straight line. See Fig. 9.6.
When the output voltage difference between –35°C and 85°C is ΔVSVD2, the difference between the approximate straight line and the output voltage linearity is ΔDIFF, and the maximum value is ΔDIFF (Max.), the output voltage linearity ΔV_L is expressed by the following formula

$$\Delta V_L = \frac{\Delta DIFF(MAX)}{\Delta V_{SEN}} \times 100$$

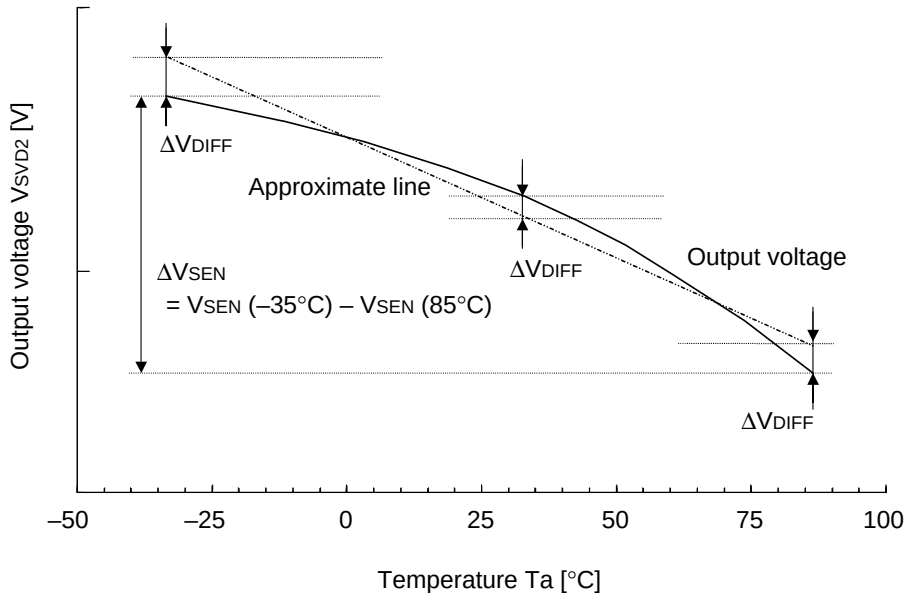


Fig. 9.6

*4 The waiting time until the output voltage is stabilized and can be monitored after the temperature sensor ON command is input. Be sure to sample output voltages after a waiting time more than the specified one elapsed.

10. TIMING CHARACTERISTICS

(1) System path read/write characteristics 1 (80 system MPU)

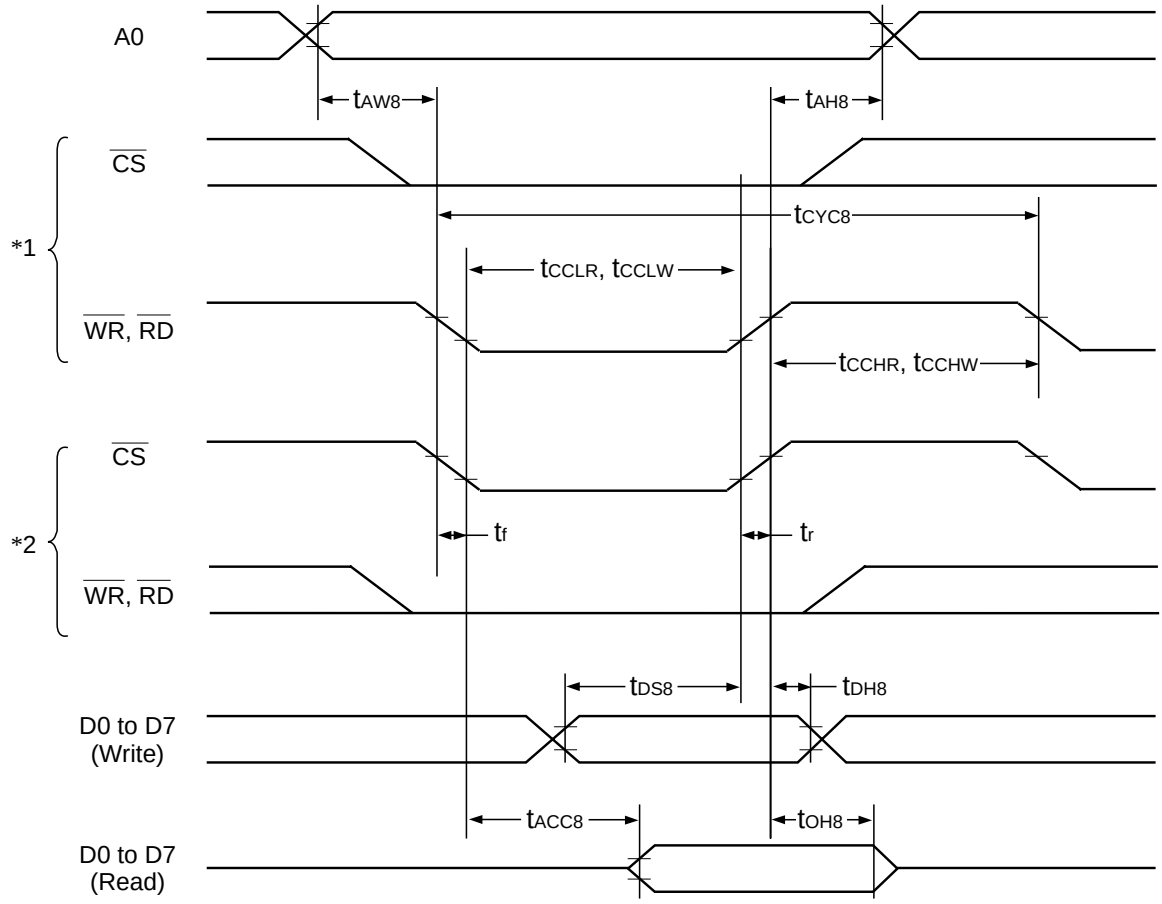


Fig. 10.1

Table 10.1

[V_{DD} = 2.7V to 5.5V, Ta = –40 to +85°C]

Parameter	Signal	Symbol	Condition	Specified value		Unit
				Min.	Max.	
Address hold time	A0	t_{AH8}	—	0	—	ns
Address setup time		t_{AW8}		0	—	
System write cycle time	$\overline{WR}$	t_{WCYC8}	—	500	—	
System read cycle time	$\overline{RD}$	t_{RCYC8}		7000	—	
Control LOW-pulse width (Write)	$\overline{WR}$	t_{CCLW}	—	200	—	
Control LOW-pulse width (Read)	$\overline{RD}$	t_{CCLR}		3000	—	
Control HIGH-pulse width (Write)	$\overline{WR}$	t_{CCHW}		200	—	
Control HIGH-pulse width (Read)	$\overline{RD}$	t_{CCHR}		200	—	
Data setup time	D0 to D7	t_{DS8}	—	200	—	
Data hold time		t_{DH8}		30	—	
$\overline{RD}$ access time		t_{ACC8}	C_L=100pF	—	3500	
Output disable time		t_{OH8}		5	200	

*1. This is in case of making the access by $\overline{WR}$ and $\overline{RD}$, setting the $\overline{CS}$ = LOW.
*2. This is in case of making the access by $\overline{CS}$, setting the $\overline{WR}$, $\overline{RD}$ = LOW.
*3. Input signal rise and fall time (tr, tf) must not exceed 15 ns. When the system cycle time is used at a high speed, it is specified by $(t_r + t_f) \leq (t_{CYC8} - t_{CCLW} - t_{CCHW})$ or $(t_r + t_f) \leq (t_{CYC8} - t_{CCLR} - t_{CCHR})$.
*4. Timing is entirely specified with reference to 20% or 80% of V_{DD}.
*5. t_{CCLW} and t_{CCLR} are specified in terms of the overlapped period when $\overline{CS}$ is at LOW level and $\overline{WR}$ and $\overline{RD}$ are at LOW level.

(2) System path read/write characteristics 2 (68 system MPU)

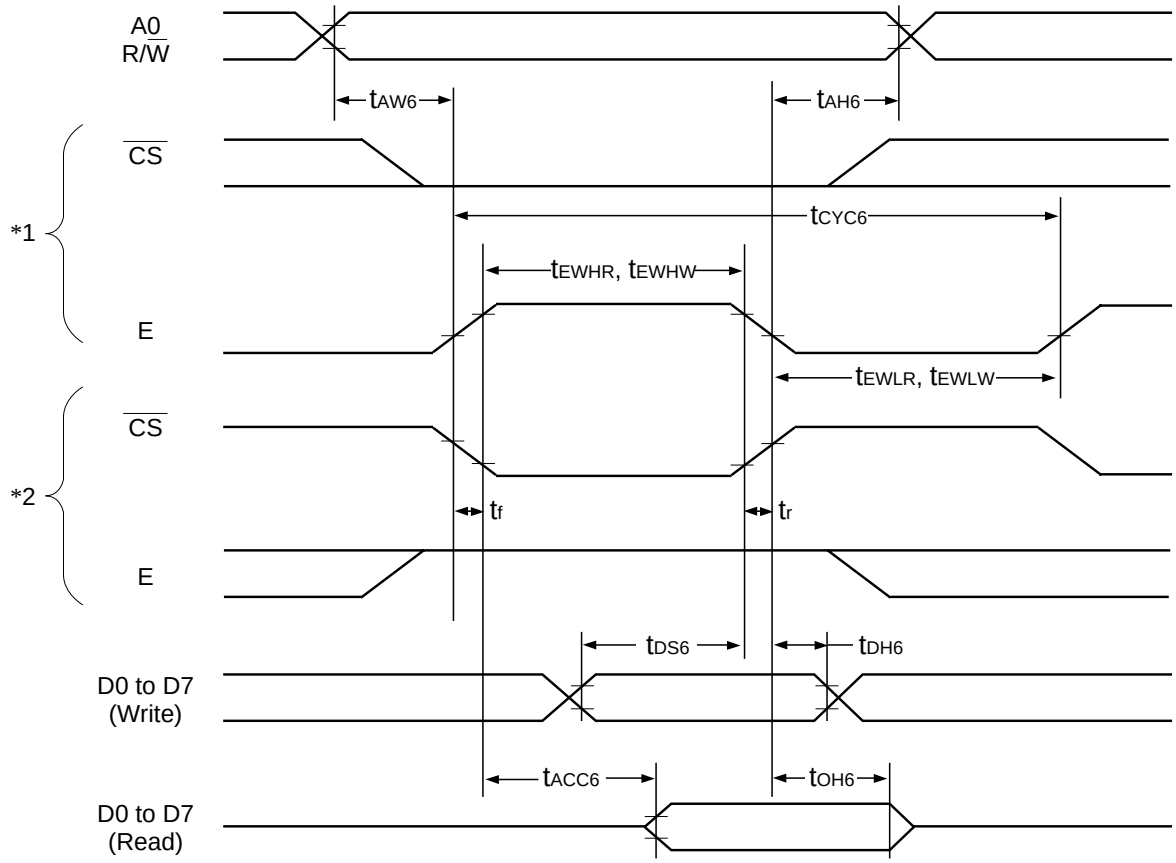


Fig. 10.2

Table 10.2

[V_{DD} = 2.7V to 5.5V, Ta = –40 to +85°C]

Parameter		Signal	Symbol	Condition	Specified value		Unit
					Min.	Max.	
Address hold time Address setup time		A0	t_{AH6} t_{AW6}	—	20 0	— —	ns
System write cycle time System read cycle time		E	t_{WCYC6} t_{RCYC6}	—	500 7000	— —	
Data setup time Data hold time		D0 to D7	t_{DS6} t_{DH6}	—	200 60	— —	
Access time Output disable time			t_{ACC6} t_{OH6}	C_L=100pF	— 5	3500 200	
Enable HIGH-pulse width	Read Write	E	t_{EWHR} t_{EWHW}	—	3000 200	— —	
Enable LOW-pulse width	Read Write	E	t_{EWLR} t_{EWLW}	—	200 200	— —	

*1 This is in case of making the access by E, setting the $\overline{CS}$ = LOW.
*2 This is in case of making the access by $\overline{CS}$, setting the E = HIGH.
*3 The rise time and the fall time (tr & tf) of the input signals should be set to 15ns or less. When it is necessary to use the system cycle time at high speed, the rise time and the fall time should be so set to conform to $(t_r+t_f) \le (t_{CYC6}-t_{EWLW}-t_{EWHW})$ or $(t_r+t_f) \le (t_{CYC6}-t_{EWLR}-t_{EWHR})$.
*4 All the timing should basically be set to 20% and 80% of the "V_{DD}".
*5 t_{EWLW}, t_{EWLR} should be set to the overlapping zone where the $\overline{CS}$ is on the LOW level and where the E is on the HIGH level.

(3) Serial interface

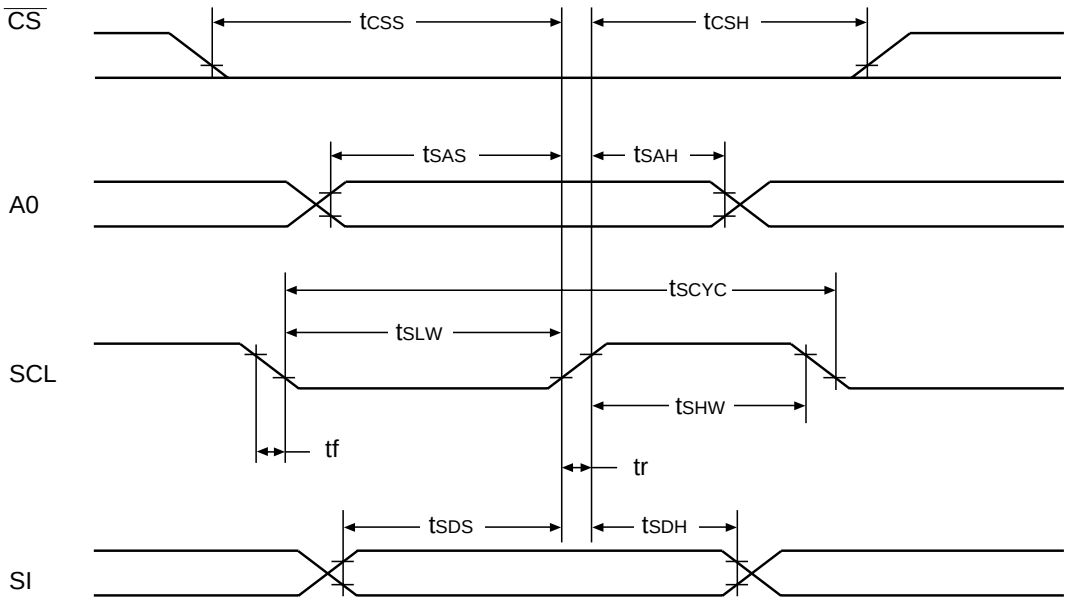


Figure 10.3

Table 10.3

[V_{DD} = 2.7V to 5.5V, Ta = –40 to +85°C]

Parameter	Signal	Symbol	Condition	Specified value		Unit
				Min.	Max.	
Serial clock period	SCL	t_{SCYC}	—	250	—	ns
SCL HIGH pulse width		t_{SHW}		100	—	
SCL LOW pulse width		t_{SLW}		100	—	
Address setup time	A0	t_{SAS}	—	150	—	
Address hold time		t_{SAH}		150	—	
Data setup time	SI	t_{SDS}	—	200	—	
Data hold time		t_{SDH}		100	—	
CS-SCL time	CS	t_{CSS}	—	150	—	
		t_{CSH}		150	—	

*1. Input signal rise and fall time (tr, tf) must not exceed 15 ns.
*2. Timing is entirely specified with reference to 20% or 80% of V_{DD}.

(4) Display control input/output timing

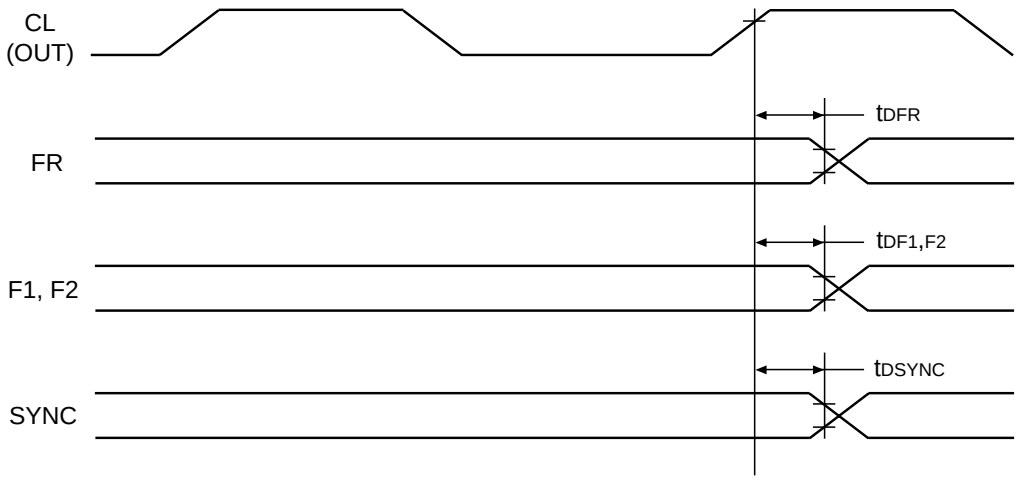


Fig. 10.4

Table 10.4 Output Timing

[V_{DD} = 2.7V to 5.5V, Ta = –40 to +85°C]

Parameter	Signal	Symbol	Condition	Specified value			Unit
				Min.	Typ.	Max.	
FR delay time	FR	t_{DFR}	C_L = 50pF	—	60	200	ns
F1, F2 delay time	F1, F2	t_{DF1}, t_{F2}		—	60	200	ns
SYNC delay time	SYNC	t_{DSYNC}		—	60	200	ns

Table 10.5 Input Timing

[V_{DD} = 2.7V to 5.5V, Ta = –40 to +85°C]

Parameter	Signal	Symbol	Condition	Specified value			Unit
				Min.	Typ.	Max.	
FR delay time	FR	t_{DFR}		–1.0	—	1.0	µs
F1, F2 delay time	F1, F2	t_{DF1}, t_{F2}		–1.0	—	1.0	µs
SYNC delay time	SYNC	t_{DSYNC}		–1.0	—	1.0	µs
Low-level pulse width	C_L	t_{WLCL}		1.0	—	—	µs
High-level pulse width		t_{WHCL}		1.0	—	—	µs

*1. Timing is entirely specified with reference to 20% or 80% of V_{DD}.

(5) Reset input timing

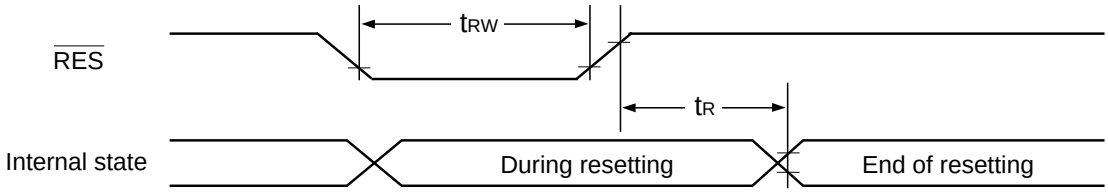


Fig. 10.5

Table 10.5

[V_{DD} = 2.7V to 5.5V, Ta = –40 to +85°C]

Parameter	Signal	Symbol	Condition	Specified value			Unit
				Min.	Typ.	Max.	
Reset time	—	t_R	—	—	—	1000	µs
Reset LOW pulse width	$\overline{RES}$	t_{RW}		1000	—	—	

*1. Timing is entirely specified with reference to 20% or 80% of V_{DD}.

11. MPU INTERFACE

The S1D15714 Series can be connected to the 80 series MPU and 68 series MPU. Use of a serial interface allows operation with a smaller number of signal lines.
You can expand the display area using the S1D15714 Series as a multi-chip. In this case, the IC to be accesses can be selected individually by the chip select signal. After initialization by the $\overline{RES}$ pin, each input terminal of the S1D15714 Series must be placed under normal control.

(1) 80 series MPU

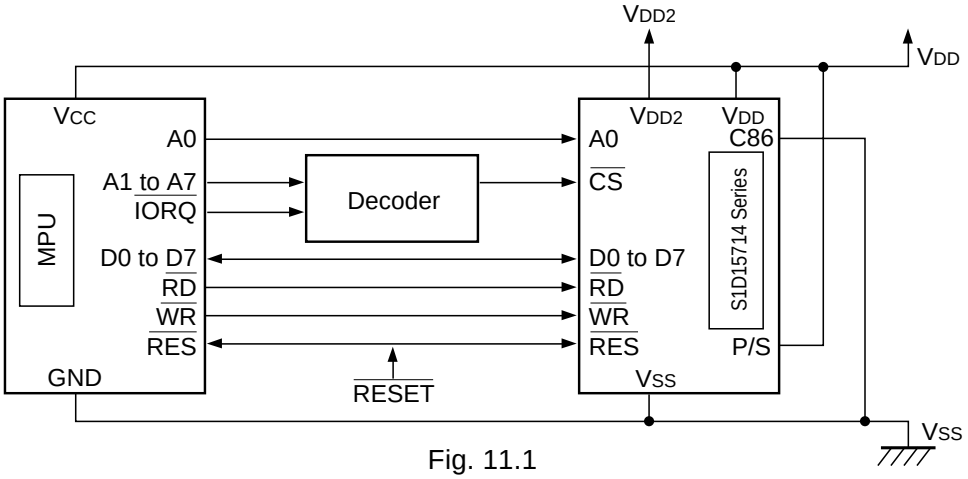


Fig. 11.1

(2) 68 series MPU

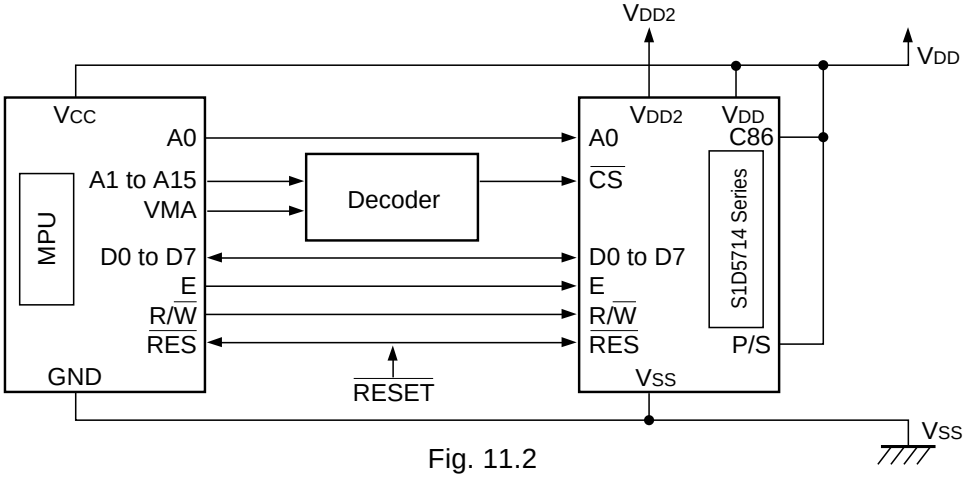


Fig. 11.2

(3) Serial interface

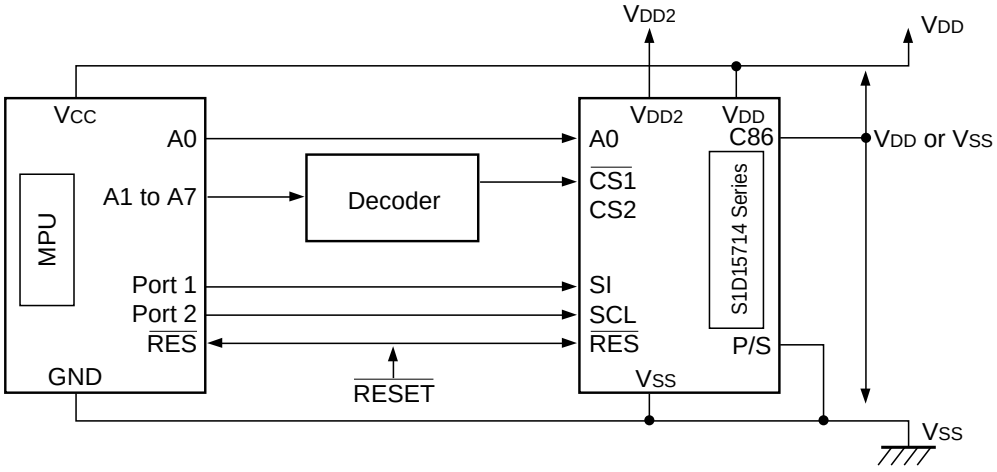


Fig. 11.3

12. CONNECTION BETWEEN LCD DRIVERS

You can easily expand the liquid crystal display area using the S1D15714 Series as a multi-chip. In this case, use the same model (S1D15714/S1D15714) as the master and slave systems.

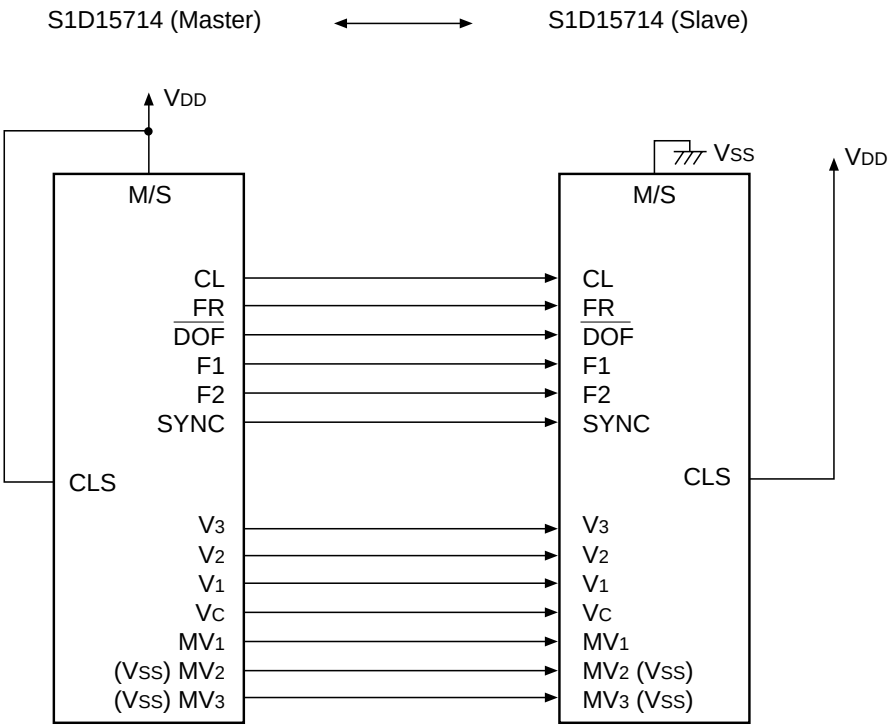


Fig. 12 Master/slave connection example

13. LCD PANEL WIRING

You can easily expand the liquid crystal display area using the S1D15714 Series as a multi-chip. In the case of multi-chip configuration, use the same models.

(1) Single chip configuration example

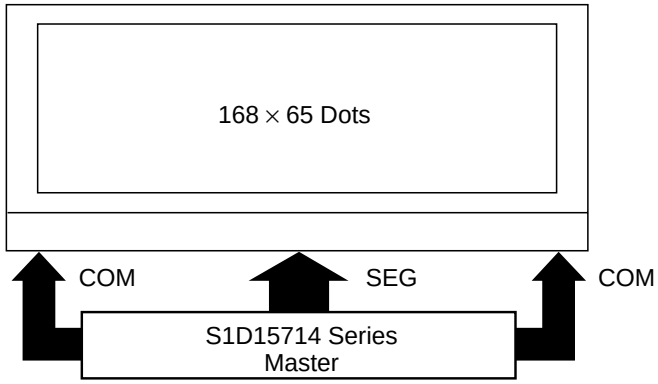


Fig. 13.1 Single chip configuration example

(2) Double chip configuration example

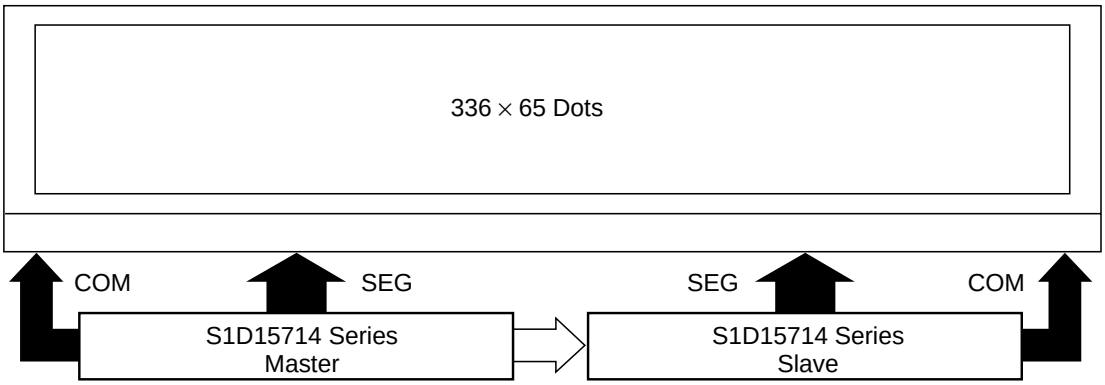


Fig. 13.2 Double chip configuration example

14. CAUTIONS

Cautions must be exercised on the following points when using this Development Specification:

1. This Development Specification is subject to change for engineering improvement.
2. This Development Specification does not guarantee execution of the industrial proprietary rights or other rights, or grant a license. Examples of applications described in This Development Specification are intended for your understanding of the Product. We are not responsible for any circuit problem or the like arising from the use of them.
3. Reproduction or copy of any part or whole of this Development Specification without permission of our company, or use thereof for other business purposes is strictly prohibited.

For the use of the semi-conductor,cautions must be exercised on the following points:

[Cautions against Light]

The semiconductor will be subject to changes in characteristics when light is applied. If this IC is exposed to light, operation error may occur. To protect the IC against light, the following points should be noted regarding the substrate or product where this IC is mounted:

(1) Designing and mounting must be provided to get a structure which ensures a sufficient resistance of the IC to light in practical use.
(2) In the inspection process, environmental configuration must be provided to ensure a sufficient resistance of the IC to light.
(3) Means must be taken to ensure resistance to light on all the surfaces, backs and sides of the IC

S1D15714 Series

SEIKO EPSON CORPORATION
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