7.15 INT1_THS (32h)

Table 42. INT1_THS register

0	THS6	THS5	THS4	THS3	THS2	THS1	THS0

Table 43. INT1_THS description

THS6 - THS0	Interrupt 1 threshold. Default value: 000 0000

7.16 INT1_DURATION (33h)

Table 44. INT1_DURATION register

0	D6	D5	D4	D3	D2	D1	D0

Table 45. INT2_DURATION description

D6 - D0	Duration value. Default value: 000 0000

The **D6 - D0** bits set the minimum duration of the interrupt 2 event to be recognized. Duration steps and maximum values depend on the ODR chosen.

7.17 INT2_CFG (34h)

Table 46. INT2_CFG register

AOI	0	ZHIE	ZLIE	YHIE	YLIE	XHIE	XLIE

Table 47. INT2_CFG description

AOI	AND/OR combination of interrupt events. Default value: 0. (See *Table 48*)
ZHIE	Enable interrupt generation on Z high event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)
ZLIE	Enable interrupt generation on Z low event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value lower than preset threshold)
YHIE	Enable interrupt generation on Y high event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)
YLIE	Enable interrupt generation on Y low event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value lower than preset threshold)