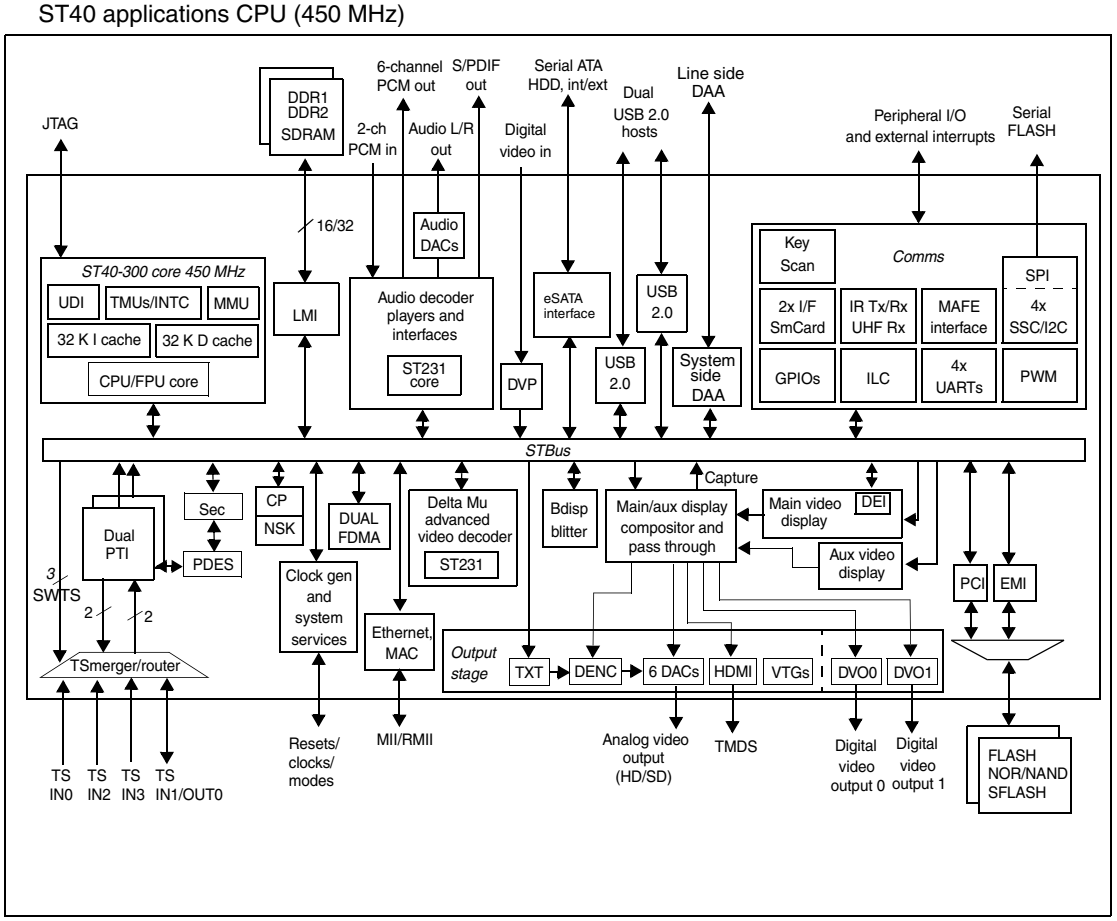
STi7105

Advanced HD decoding IC for STB

Preliminary Data

Features

- Advanced high definition video decoding (H264/VC-1/MPEG2)
- Advanced standard definition video decoding (H264/VC-1/MPEG2/AVS)
- Advanced multi-channel audio decoding (MPEG 1, 2, MP 3, DD/DD+, AAC/AAC+, and WMA9/WMA9pro)
- Linux, Windows CE, and OS21 compatible ST40 applications CPU (450 MHz)
- 32-bit DDR1/DDR2 compatible local memory interface
- Multi-stream, DVR capable transport stream processing
- Extensive connectivity (dual USB 2.0 hosts, e-SATA, Ethernet MAC/MII/RMII, and PCI)
- Advanced security and DRM support including SVP, MS-DRM, and DTCP-IP
- DVD data decryption



Contents

1 Related documents

This datasheet is part of the STi7105 documentation suite which forms a complete system description and programming guide. This datasheet is intended for hardware engineers, and describes the pins, package, electrical characteristics, and timing information for the STi7105 device.

The documents related to this datasheet are described in the sections below.

1.1 STi7105 programming manual

The *STi7105 programing manual* describes how to program and configure the STi7105 device. It is intended for software and system engineers.

1.2 CPU documentation

The ST40 core and its instruction set are documented in the *ST40 32-bit CPU Core Architecture manual.*

The ST231 core and its instruction set are documented in the *ST231 CPU Core and Instruction Set Architecture Manual.*

2 Description

The STi7105 includes in a single IC, multi-stream transport de-multiplexing and descrambling, an ST40 applications CPU, advanced audio/video decoding, video processing, graphics and display composition, advanced security, STB peripherals, audio/video DACs, HDMI, Digital A/V outputs, two Host USB ports, e-SATA port HDD interface, and Ethernet MAC/MII/RMII.

2.1 Transport

The STi7105 receives transport streams from broadcast networks through three parallel/serial transport stream inputs and one serial transport stream input. The fourth transport interface can be configured as a fourth input or as an output. ST provides a range of front end channel decoder ICs for cable, satellite and terrestrial networks that can be interfaced directly with the STi7105. Transport stream routing for DVB-CI+ (HD/SD profiles) modules can also be supported.

Transport streams are processed by two integrated programmable transport stream engines (PTIs). These perform demultiplexing, descrambling, and section filtering on multiple transport streams received from Broadcast, IP, and HDD sources.

2.2 Connectivity

The STi7105 has a wide range of options for connecting to external peripherals or IP network devices, such as wired ethernet, xDSL, and Wi-fi. These interfaces enable the delivery of IP streams received over broadband networks and support streaming over home networks. These interfaces include 2 USB host ports, a 32-bit PCI interface, and a high speed Ethernet MAC/MII/RMII interface.

PCI uses the same physical interface as the EMI with dynamic interleaving of access types possible. Transport streams received through IP can be routed internally to the PTIs for demultiplexing and descrambling similar to the broadcast TS streams. The PTIs can concurrently process multiple TS streams from both sources.

2.3 Audio/Video decoding

The STi7105 can decode H264, VC -1/WMV9, and MPEG2 HD and SD streams with concurrent decoding of one HD stream and one SD stream possible for PIP applications. AVS SD decoding is also supported. Multiple decoding of lower resolution streams can also be supported for Mosaic applications. The decoder is well proven in the industry and is powerful and flexible enough to decode other video formats, such as MPEG4 part2 and DivX (3.x, 4.x, and 5.x). It can also support concurrent H263 encode and decode for video conference applications.

A programmable ST231 CPU core provides the flexibility and performance for decoding multi-channel advanced audio streams. Concurrent decoding of an audio description channel is also supported.

2.4 Graphics and display

The STi7105 integrates a graphics and display sub-system that can deliver a high quality visual experience for applications. Graphics generation can use both the CPU and an independent multi-operator graphics accelerator that supports 2D graphics and 3D user interface effects. Graphics can be displayed on any one of three graphics planes. The graphics planes are combined, with video, using alpha blending and color keying. The graphics and video are combined by two independent display compositors, one for the Main TV and a second for output to a VCR or DVD-R. Two video planes are available for PIP on the main composition or downscaled video on the second composition. Video post-processing can be applied to resize, reformat and de-interlace video between the encoded and intended display formats prior to composition. Advanced de-blocking processing can be applied to decoded MPEG2 SD video. With such capabilities, feature-rich displays can be generated including PIP, POP, Mosaics, animations, highlighting, blended overlays, scrolling subtitles etc.

2.5 Audio/Video outputs

The STi7105 has both HDMI and analog interfaces for outputting video to the TV/panel. In addition to the standard 720p and 1080i HD formats, the STi7105 supports 1080p60 display output on the HDMI interface. The Analog interface comprises 6 Video DACs with CGMS-A, Macrovision and Dwight-Cavendish copy protection, whilst the HDMI interface supports HDCP copy protection. HDMI interface is in full compliance with all features of v1.3a except deep color, enhanced colorimetry (xvYCC, gamut metadata), and DST/DSD audio features.

Audio is output over HDMI, SPDIF, stereo analog DACs, and a digital PCM output interface. It is possible to output both compressed and decoded audio streams at the same time over different interfaces (for example, Dolby Digital 5.1 over SPDIF with decoded and downmixed AAC-plus audio via the analog output). A 2-channel PCM input is also available for inputting audio from external sources such as a microphone (for example, for VOIP telephony).

2.6 Processors and memory

The STi7105 embeds the latest ST40 class applications processor, the ST40-300 with 2–way, set associative caches, a 32 K instruction cache, and a 32 K data cache. At an operating frequency of 450 MHz it can deliver > 800 DMIPs performance.

The STi7105 supports the latest DDR2 memory technology on its 32-bit local memory interface (LMI) providing a high bandwidth unified memory for code, data, audio and video buffers, graphics etc. With two 2-Gbit devices in a x16 configuration, up to 512 Mbytes capacity can be supported. The STi7105 also retains the ability to support DDR1 memory types.

A 16-bit External memory interface is used for connecting to FLASH and SRAM/peripherals supporting a standard 8/16-bit asynchronous read/write protocol. Synchronous or burst mode FLASH can also be supported. Both NOR and NAND Flash types can be used, with the ability to boot from, and perform code authentication checking from both types. Interfacing and booting from Serial FLASH attached through SPI is also supported.

2.7 DVR

The STi7105 supports attachment of an HDD through e-SATA, USB, or EIDE (PIO mode) allowing DVR STBs to be developed. The e-SATA interface can independently support either internal or external SATA drive attachment. The STi7105 can support recording of up to four HD streams with local playback of an HD stream with trick modes, as well as playback of additional streams for export to client STBs over a home network. Streams can be encrypted to/from the HDD and to/from a home network for copy protection using AES, T-DES, or DES ciphers.

2.8 STB peripherals

The STi7105 integrates a range of peripherals and interfaces to minimize or eliminate the external cost of implementing basic STB functions. These include UARTs and SSCs used for serial interfaces, I2C control busses, two smart card controllers, a PWM module, IR receiver and transmitter, general purpose programmable I/O, external interrupt inputs, and a controller for scanning/debouncing a 4 x 4 key matrix. There are also two options available for implementing a software modem on the STi7105; a MAFE interface to connect to an external modem codec and integration of a system-side DAA circuit to connect to an external line-side DAA device. For HDMI interfacing, a dedicated I2C port is available, together with a hardware CEC line controller.

Figure 1. Typical DVR cable STB with DOCSIS

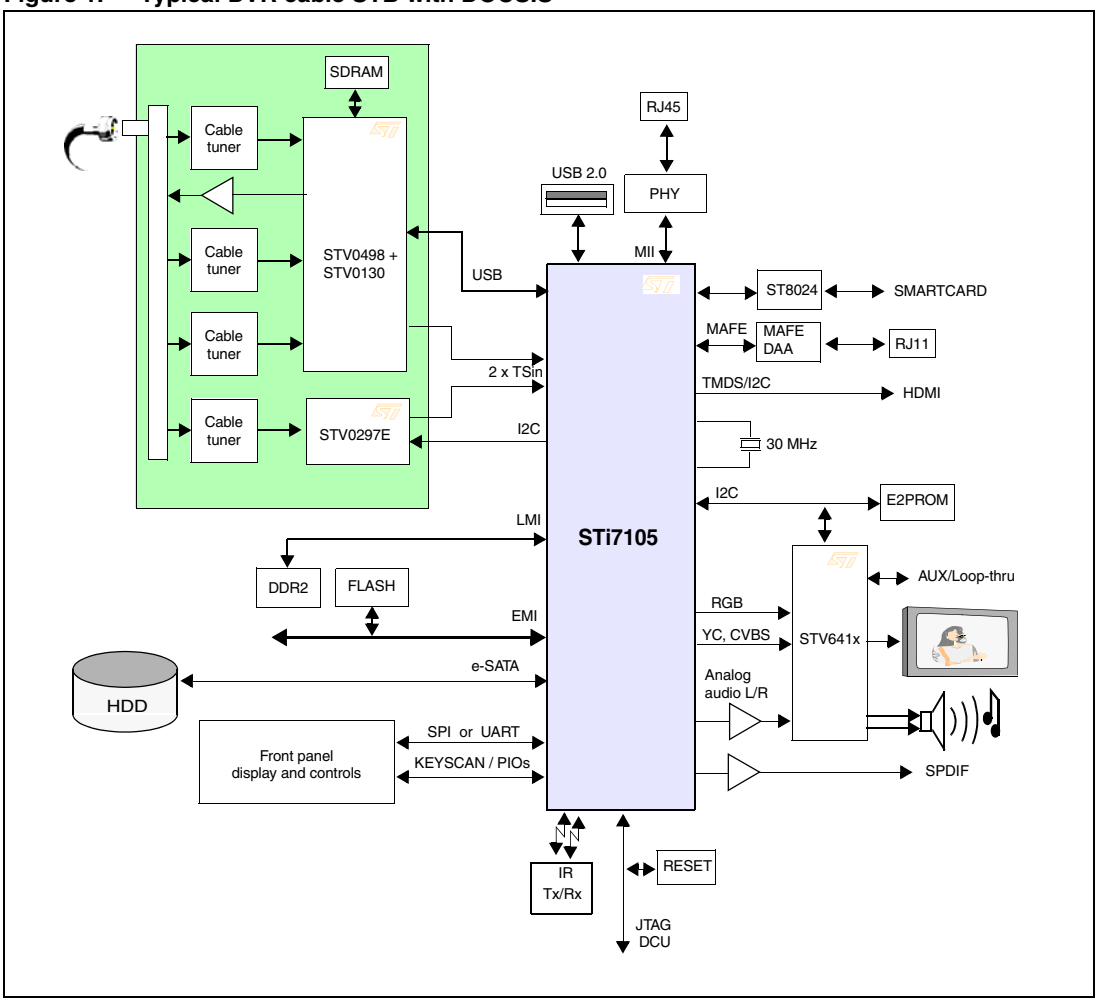


Figure 2. IP client

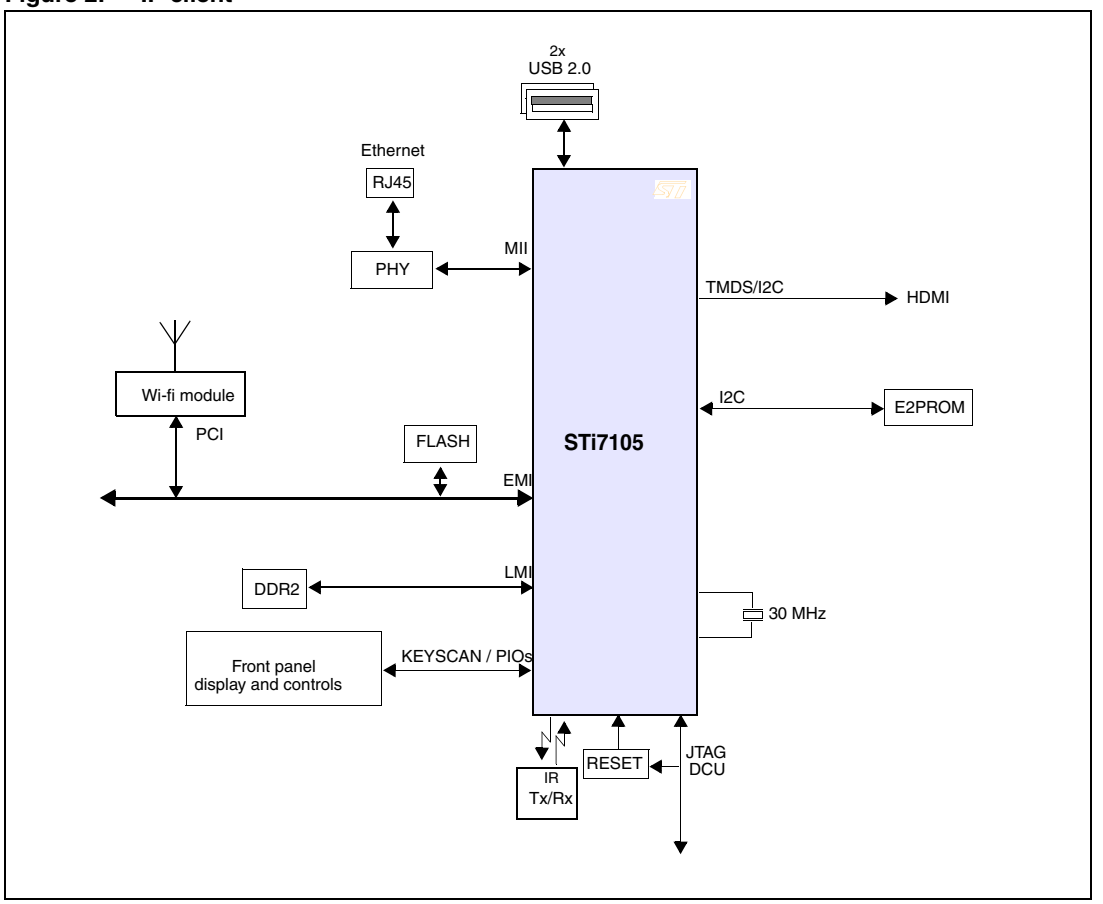


Figure 3. High definition DVR satellite STB

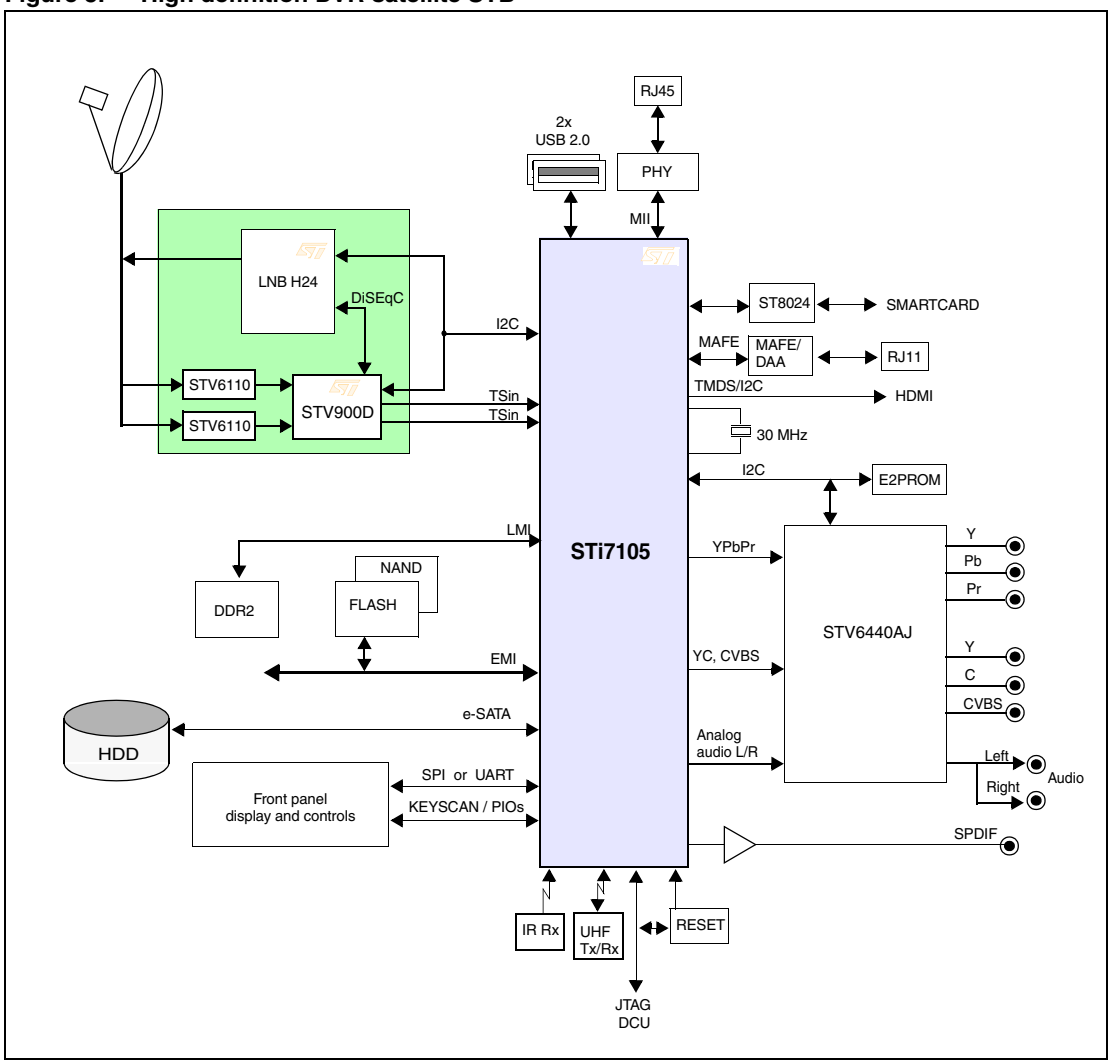
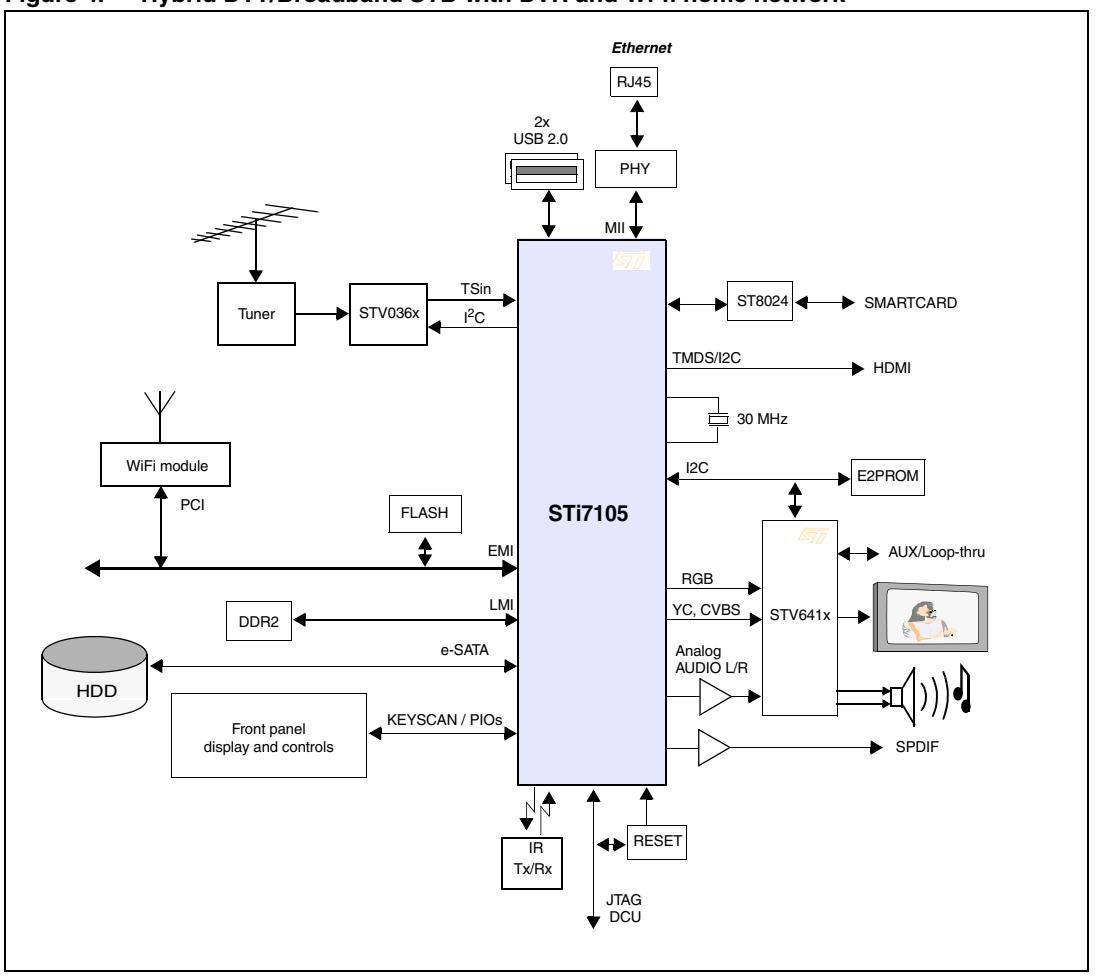


Figure 4. Hybrid DTT/Broadband STB with DVR and Wi-fi home network



3 System on chip subsystem overview

This section gives a top-level overview of the device components.

3.1 STBus interconnect

The STBus multipath unified interconnect provides high on-chip bandwidth and low latency accesses between modules. The interconnect operates hierarchically, with latency-critical modules placed at the top level. The multipath router allows simultaneous access paths between modules, and simultaneous read and write phases from different transactions to and from the modules. Split transactions maximize the use of the available bandwidth.

3.2 Processor core

The STi7105 integrates a 450 MHz ST40-300 processor core that features a 32-bit superscalar RISC CPU and IEEE-754 compliant floating point unit (FPU). The ST40-300 includes 2-way, set-associative caches and an interrupt controller with 15 user interrupt sources and an interrupt expansion port.

3.3 External memory interface (EMI)

The EMI is a general-purpose interface for attaching Flash memory and peripherals. The EMI features are:

- 5 banks
- Addressing up to at least 64 Mbytes of NOR Flash
- External bus master support through BUSREQ/BUSGNT signals
- Slave Mode EMI support
- Single level cell (SLC) NAND Flash and boot from SLC NAND Flash
- Serial Flash support
- PCI interface, host and device selected on boot
- ATAPI PIO mode 4
- DVB-CI+

3.4 Local memory interface (LMI)

The STi7105 integrates one 32-bit DDR2-DDR1 interface. The interface can run up to 400 MHz when configured in DDR2 mode or up to 250 MHz when in DDR1 mode.

The LMI supports 16-bit and 32-bit configurations. The following 32-bit configurations are supported:

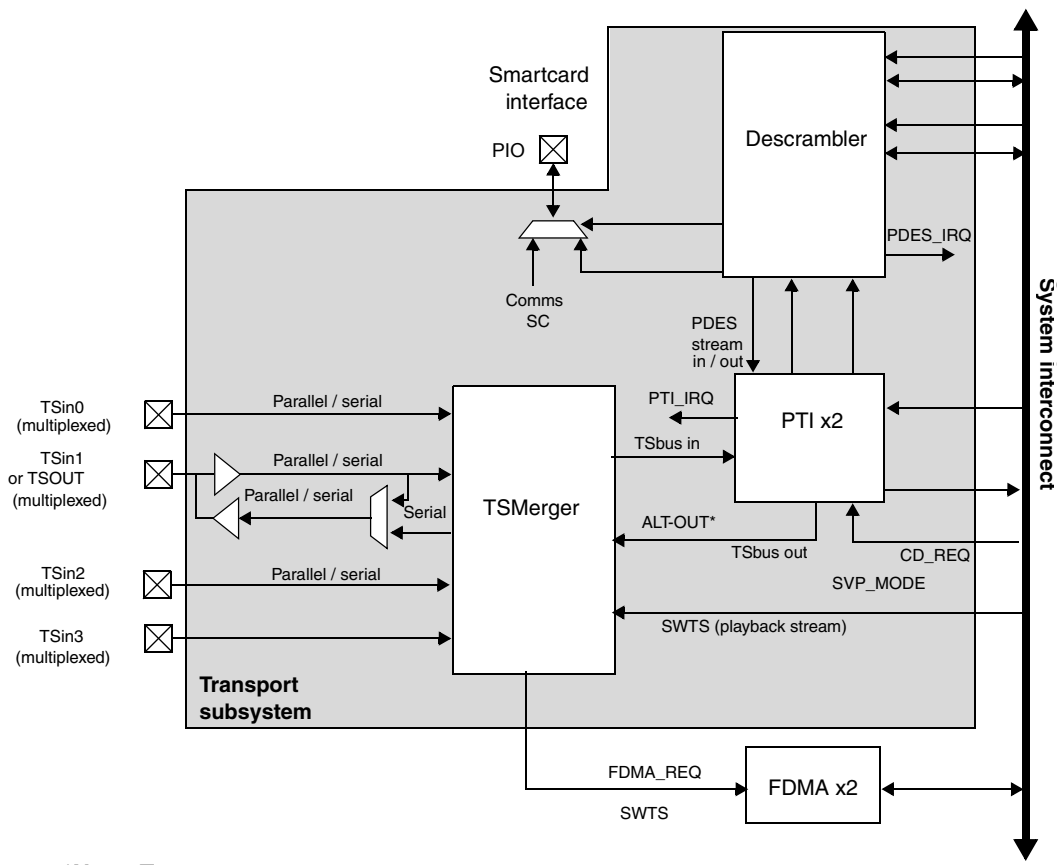
- 2 x 512 Mbits (x16) devices resulting in 128 Mbytes memory space
- 4 x 512 Mbits (x8) devices resulting in 256 Mbytes memory space
- 2 x 1 Gbits (x16) devices resulting in 256 Mbytes memory space
- 2 x 2 Gbits (x16) devices resulting in 512 Mbytes memory space

3.5 STB transport subsystem

3.5.1 Overview

The transport subsystem (TS) is able to receive ATSC, DVB, DIRECTV, DCII, OpenCable, ARIB BS4 transport streams containing high definition (HD) and standard definition (SD) programs. It demultiplexes and descrambles the transport streams to deliver PES packets to the video and audio decoders.

Figure 5. Transport subsystem block diagram



***Note**: The ALT_OUT function is not usually supported in firmware. Contact STMicroelectronics for information if the ALT_OUT function is required by your application.

Transport streams are input to the STi7105 through the four TS interfaces. Two of these interfaces (TSin0 and TSin2) are parallel inputs that can also be configured as serial inputs. The third interface is a bidirectional interface that can be configured as a third parallel input (TSin1) or a third serial input (TSin1), or can be configured as a parallel output(TSOUT). Also, a serial input interface (TSin3) is available if four TS inputs are required.

The serial formats of each, TSin1 and TSin2, are available multiplexed with PIOs in two different locations to maximize the availability of chip functions for a given application.

Transport streams can also be input to the STi7105 from network or HDD. These streams can be input through the MII, PCI, or USB interfaces (and e-SATA for HDD) buffered in memory and merged with the transport streams from the TS inputs. These merged TS streams are then forwarded to the PTIs for processing. Streams can also be output to a network or HDD.

3.5.2 Dual Programmable transport interface (PTI)

Each PTI is a dedicated transport engine and integrates its own CPU to handle the transport stream PID filtering, demultiplexing, descrambling, and data filtering. It interfaces with the programmable descrambler (PDES) for descrambling. Each PTI receives a transport stream from a dedicated input port, processes it, and outputs it either to the memory through its DMA channels or to a dedicated transport output port.

The PTIs perform PID filtering, demultiplexing, descrambling, and data filtering on up to four transport streams. The PTIs extract PCRs with time stamps and make them available to the CPU for clock recovery and audio/video synchronization.

PES data is transferred by DMA to memory buffers. Section data is transferred by DMA to separate buffers for further processing by the CPU. The PTIs extract indexing information and transfer packets, using DMA, to an intermediate buffer for writing to HDD.

The following transport streams are supported:

- AVS video
- MPEG2 transport stream demultiplexing, and service information extraction, conforming to:
  - MPEG2 systems
  - MPEG4 systems
  - DVB
  - DirecTV DSS format
  - DirecTV AMC stream format
- MPEG2 TS audio/visual formats:
  - MPEG2 A/V over MPEG2 TS
  - H264 video over MPEG2 TS
  - VC-1 over MPEG2 TS
  - WMA9, WMA9 pro over MPEG2 TS
  - AAC and AAC+ audio over MPEG2 TS
- A/V streams encapsulated in RTP packets according to these protocols (parsing):
  - MPEG2 A/V in RTP
  - MPEG 4 pt2 video in RTP
  - MPEG 4 audio including AAC and AAC+ in RTP
  - H264 video in RTP
  - VC-1 video in RTP
  - AVS video in RTP
- processing of:
  - WMV9/WMA9 streaming content in ASF files using client server interaction
  - parsing of MP3 or MPEG 4 AAC audio from Audio File format versions 2, 3 and 4
  - A/V streams, such as DivX, delivered in AVI files
  - WAV and AIFF files

Each PTI performs PID filtering to select audio, video, and data packets to be processed. It supports up to 151 PID slots, and routes streams to and from the descrambler. Streams can be descrambled using:

- DES
- TDES
- AES
- Multi-2
- DVB-CSA
- NDS ICAM

The PTI has a 64 x 16 byte section filter core. Four filtering modes are available:

- wide match mode: 64 x 16 byte filters
- long match mode: 128 x 8 byte filters
- positive/negative mode: 64 x 8 byte filters with positive/negative filtering at the bit level
- APG filtering mode

Matching sections are transferred to memory buffers for processing by software.

3.6 DVD decryption

CSS (DVD-video), CPRM (DVD-RW), and CPPM (DVD-audio) decryption is provided for the DVD stream.

3.7 Video decoder

The STi7105 video decoding subsystem includes the Delta-Rasta core capable of decoding H264/VC-1/MPEG2 HD/SD streams and AVS SD streams.

The following are Delta-Rasta features:

- Supports H264 in-loop deblocking filter, VC-1 deblocking filter and overlapped transform, AVS deblocking filter, and deblocking post processing algorithm for MPEG2
- Supports non-real-time MPEG2 to H264 transcoding

The decoder is partially implemented in software which is executed on a dedicated ST231 CPU core. The decoder gets its data from memory and stores decoded data back into memory.

The decoder uses a mixed hardware and firmware architecture with a hardwired data path and an ST231 core engine. It provides flexibility for firmware upgrades, error concealment, or trick modes. The ST231 core can be used for other coders or decoders at lower resolution, when the VC-1, H264, AVS SD, or MPEG2 decoders are not running.

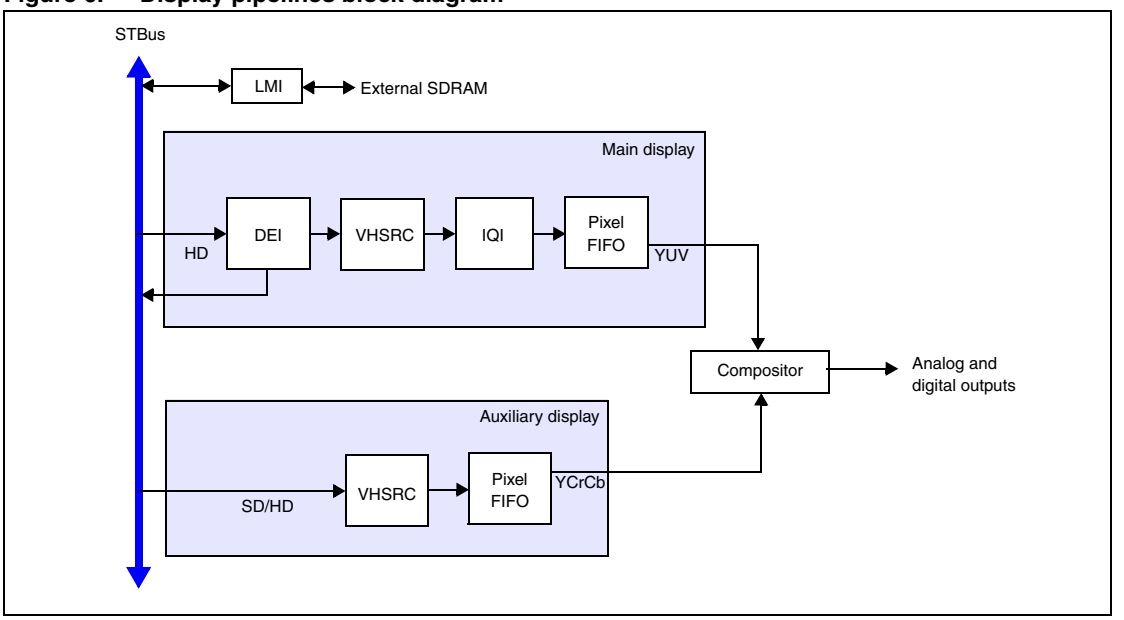
Streams are decoded picture-by-picture from an elementary stream buffer. Decoding, reconstruction, and prediction buffers are set up by the CPU. CPU control of bit-buffer pointers provides flexibility for trick modes and out-of-sequence decoding.

Semantic or syntax errors are detected by the decoder and failing slices are replaced up to the next slice or picture.

3.8 Main and auxiliary display

The main and auxiliary display pipelines form a high-quality scaling engine for video display processing. The two display pipelines are shown in *Figure 6*.

Figure 6. Display pipelines block diagram



The same video is displayed through both displays, but each display processor can be set up to format the video differently and display video with different timing. Separate video timing generators (VTGs) are provided to support this feature. The display processors adapt the decoded video to a format suitable for display, taking into account differences in scanning method, resolution, aspect ratio, and scanning frequency.

The main-display processor receives decoded or acquired video from memory, and performs block-to-line conversion, pan and scan, and vertical and horizontal format conversion. There is also a de-interlacer (DEI) to perform interlace-to-progressive conversion using motion estimation. This is used to display 480i, 576i, or 1080i interlaced sources on a progressive display (480p, 720p, or 1080p). The main display processor has IQI that improves the subjective image quality by methods, such as high frequency peaking and edge sharpening.

The auxiliary-display processor receives decoded or acquired (and possibly decimated) video, and performs pan and scan, vertical format conversion, horizontal format conversion and color tint and saturation control. The output line size is limited to SD on the auxiliary-display processor and is intended to output video for VCR recording.

3.9 Compositor

3.9.1 Overview

The compositor comprises two real-time, multiplane digital mixers.

The main mixer (mixer A), which is intended for main HDTV video output, is composed of:

- one background color
- two video planes
- three graphics planes
- one cursor plane

The auxiliary mixer (mixer B), which is intended for auxiliary SDTV video output, is composed of:

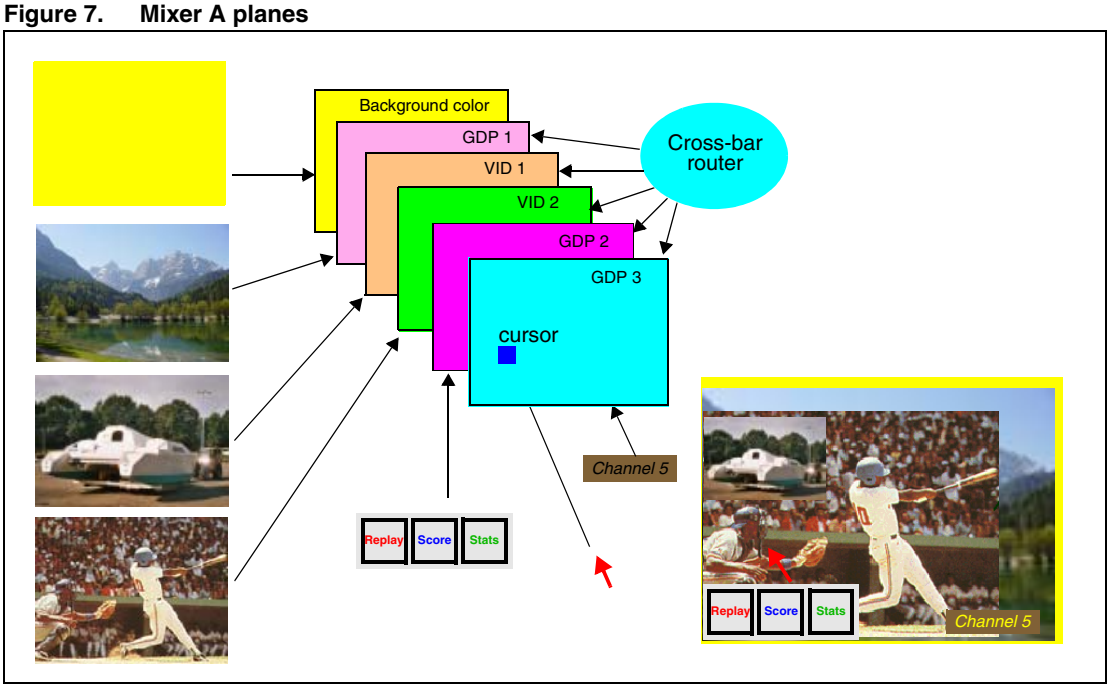
- one background color
- the video 2 plane
- the graphics 3 plane

The compositor receives the video planes from the video display processor, and the 2D graphics planes from the memory through GDP. Each mixer alpha blends graphics and video layers on a pixel basis based on alpha component values provided by each layer.

After real-time processing by the display plane pipelines, pixel data is mixed in mixer A or mixer B. The output of mixer A supports up to full HD resolutions and is intended as the main TV display (*Figure 7*). The output of mixer B (*Figure 8*) supports up to full SD resolutions and is intended as an auxiliary display for applications, including connection to a VCR. The mixer outputs are fed to the STi7105's output stage.

The mixers provide RGB and/or YCbCr digital outputs that are used by the video output subsystem to produce the HDTV video outputs (analog, digital, and composite) and the SDTV video outputs (analog and digital).

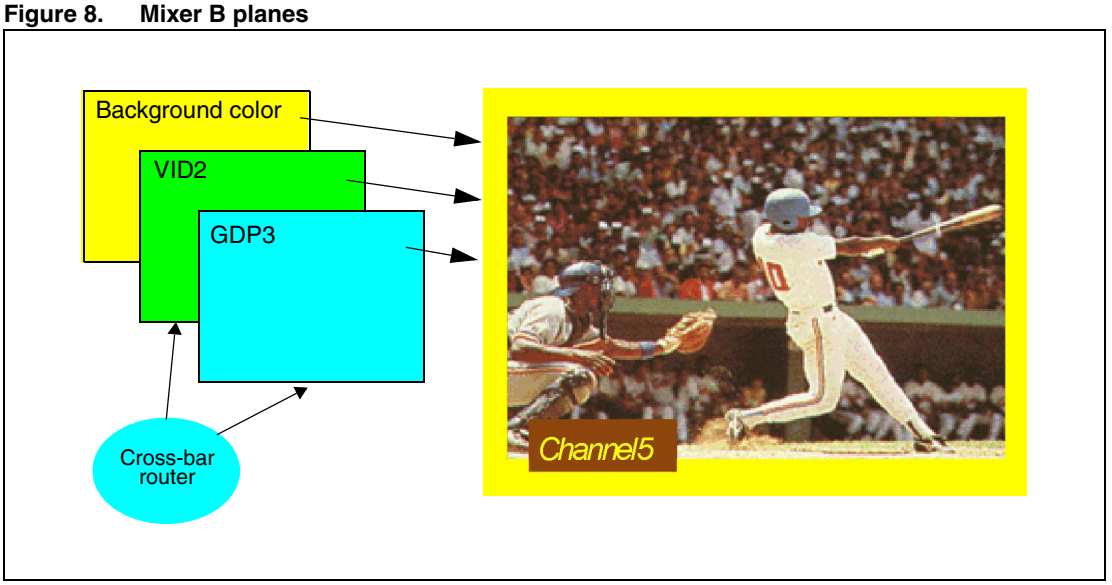
Figure 7. Mixer A planes



The compositor also comprises additional components that can be used to enhance the display presentation of video and graphics. These include an alpha plane attachment and a

cross-bar router. A capture pipeline is also provided for capturing main video streams or mixer A or B output streams and storing them in memory.

Figure 8. Mixer B planes



3.9.2 Compositor layout

Figure 9 shows a block diagram of the compositor. It presents the dataflow and memory access of all the compositor modules.

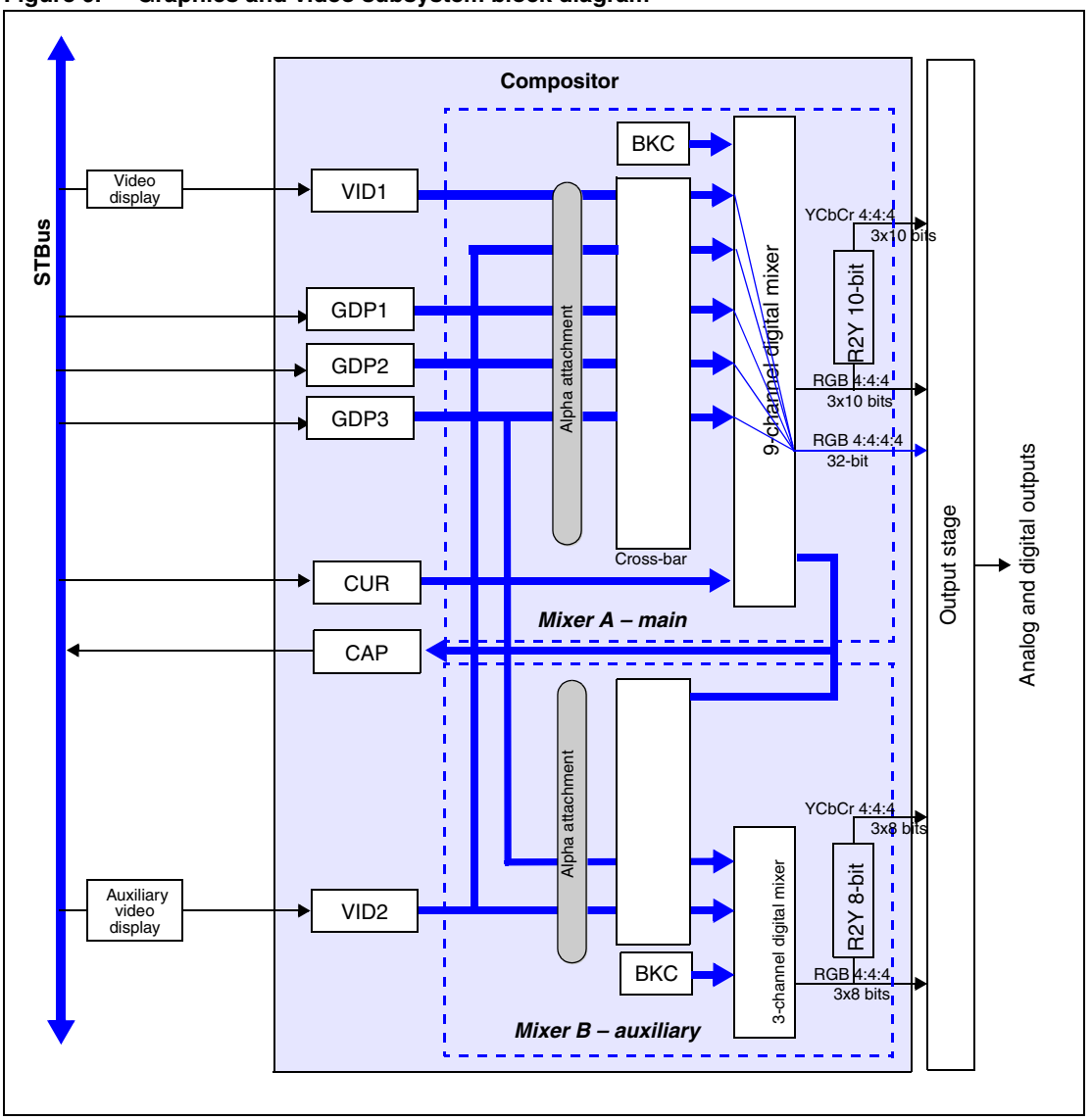
The graphics and cursor pipelines read pixel data and related control information directly from memory. The video input pipelines accept data from the main and auxiliary video display pipelines. Video and graphics data (captured for the compositor data flow by the capture pipeline) is written back to memory with a resolution up to 32 bits/pixel. The real-time processing performed by each pipeline is controlled by register programming.

Digital mixer A successively blends video layers VID1, VID2, graphics layers (GDP1, GDP2, and GDP3), the cursor layer (CUR), and a background color. A cross-bar router enables the hierarchy of the GDP1, GDP2, GDP3 and VID1, VID2 layers to be programmed. Each layer can be independently enabled or disabled. The blending operates in the RGB color domain, so each layer supplies an RGB signal (3x12 bits), with transparency information that provides the weighting coefficients for the mixing operation at a given depth.

Digital mixer B successively blends one video layer (VID2) with one graphics layer (GDP3) and a background color. A cross-bar router enables the hierarchy of the GDP3 and VID2 layers to be programmed. In Digital mixer B, each layer can be independently enabled or disabled, and blending operates in the RGB color domain.

All sub-blocks are controlled by hardware registers. All these registers can be read but not necessarily written. The graphics planes are link-list based and have their register set written through the memory (register download is controlled directly by the hardware after initialization). All other registers can be written. Each plane block supports a specific set of bitmap formats. Each plane starts reading data from memory when it is enabled in mixer A or mixer B.

Figure 9. Graphics and video subsystem block diagram

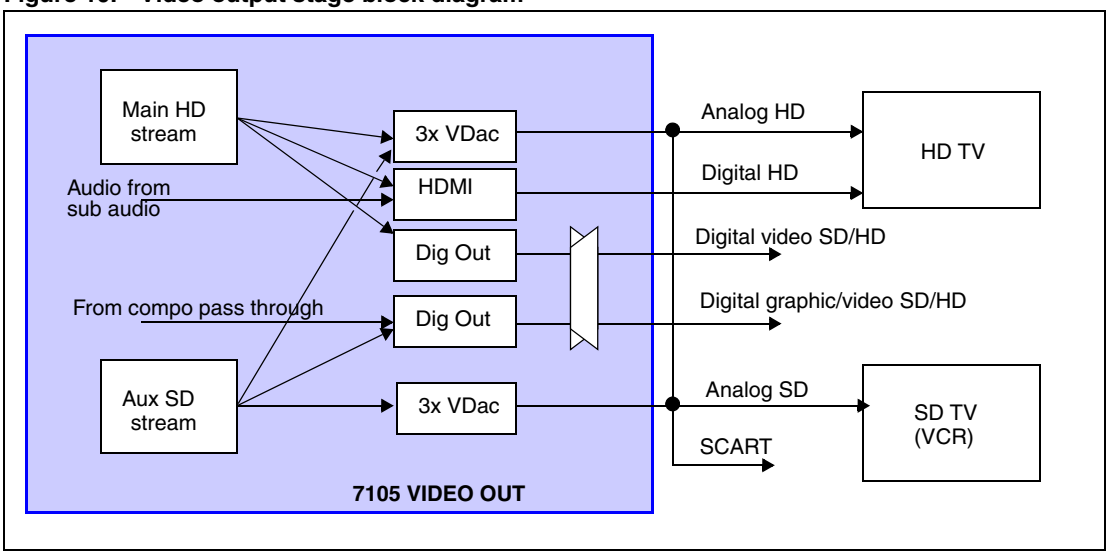


3.10 Video output

The Video Output subsystem is the unit responsible for reading decoded video frames and graphics data from external memory to reformat, rasterize, and mix them for display.

The STi7105 can output video program on main HD TV Out and on aux SD TV (VCR) Out with separate timebase if required (VTG0, VTG1). It is also able to deliver the same SD video on both main and auxiliary video outputs using the capture feature. The main data paths corresponding to these typical configurations are shown in *Figure 10* as well as the principal units which constitute the Video Output Stage.

Figure 10. Video output stage block diagram



3.10.1 Main HDTV video output

The following are the main functional blocks included in the main video flow:

- Main VDP, including High Definition Display Pipeline with IQI and DEI engines
- VTG0 (free running or master of the aux VTG1)
- Capture output port with vertical and horizontal resizing, shared with auxiliary video flow
- Compositor—Mixer five to four (in: video: RGB or YCbCr, 3x graphic: RGB; out: 2x video: RGB and YCbCr, pass through, capture), shared GDP3 and VDP aux with auxiliary compositor
- TV Out—receives its data from the compositor channel (video: RGB or YCbCr, graphic: RGB); the video data is then formatted and output in digital and analog and audio-video composite to be used by external devices
- DVI-HDCP or HDMI compliant copy-protected digital output
- Player multichannel (8-ch) and GP FIFO
- S/PDIF Player and GP FIFO
- Four S/PDIF Players with I2S to S/PDIF converters
- Triple HD/SD DAC (analog output)
- Two digital video outputs, i.e., DVO0 (video) is 8-bit or 16-bit and DVO1(GFX) is 24-bit
- AWG—arbitrary waveform generator (Dwight Cavendish and Macrovision copy protection support)

Note: The compositor includes a pipeline, which is able to mix one cursor, one or two video, up to three graphic layers, and one background layer. The data is then delivered to the TV Out. The capture port supports vertical and horizontal resizing output data with filtering for upsizing.

3.10.2 Auxiliary SDTV video flow

The following are the main functional blocks included in the auxiliary video flow:

- VTG1—free running or slave of the main HDTV VTG0
- Video Display Pipe High-definition (VDP aux)
- Capture output port with vertical and horizontal resizing, shared with main HDTV video flow
- Compositor—mixer two to three (YCbCr 8-bit and RGB 8-bit and capture), shared GDP3, and VDP aux with main HDTV compositor
- SD DENC—SDTV/VCR Video Encoder
- AWG—arbitrary waveform generator (Dwight Cavendish and Macrovision copy protection support)
- Triple HD/SD DAC (analog output)—The DAC outputs can be components (Y/C) or composite (PAL, SECAM, NTSC CVBS); all 6 DACs can output the auxiliary display in SD format for SCART output

Note: The Compositor includes a pipeline, which is able to mix one video, one graphic layer, and one background layer. The data is then delivered to the TV Out. The capture port supports vertical and horizontal resizing output data with filtering for upsizing.

3.11 2D blitter display engine

The 2D blitter display engine (BDisp 2 engine) is a software controlled output display generator, which can also be used as a CPU accelerator for graphics picture handling. The BDisp 2 engine, is an evolution of BDisp engine. It is a triple-source 2D DMA, with a set of powerful operators.

The 2D blitter display engine retrieves data from the local memory through three input sources, source 1, source 2, and source 3. Sources 1, 2, and 3 are used simultaneously for read/modify/write operations.

2D blitter display engine features are as follows:

- 2 composition queues
- 4 application queues
- Subbyte S1 and S2 access
- 5-tap vertical filters
- 8-tap horizontal filters
- Flicker filter adaptative
- Matrix conversion on input and output for: rgb2ycbcr, ycbcr2rgb,bt601, and bt709
- CLUT 1/2/4/8
- Color reduction
- Logical operation
- Clipmask
- Rotation
- Plane mask
- Color key capability
- BlueRay Disc run-length decoder (BD RLD)
- High definition-DVD 2/8-bit run-length decoder (HD-DVD RLD)

2D blitter display engine functions are as follows:

- Solid color fill of rectangular window
- Solid color shade (fill and alpha blending)
- 1 source copy, with one or several operators enabled (color format conversion, 2D scaling)
- 2 source copy with alpha blending
- 4:2:2 / 4:20 capabilities, as source format
- Fully programmable matrix used for color space conversion, PSI, special effects
- Color expansion (CLUT to true color)
- Color correction (gamma, contrast, gain)
- 2D resize engine with high quality filtering
- Adaptive flicker filter from memory-to-memory
- Rectangular clipping
- VC-1 range mapping/range reduction compensation algorithm
- Programmable source/target scanning direction, both horizontally and vertically, to cope correctly with overlapping source and destination area.

3.12 Audio subsystem

Overview

The main function of the STi7105 Audio subsystem is to decode and play different standards of multi-channel compressed audio streams. The audio stream (encoded or decoded) is received either from an external source through the PCM input interface or an internal source, such as the Transport subsystem through memory.

The audio decoder may have to decode simultaneously two different encoded audio streams when an audio description channel is provided (the main audio stream and a 2-channel audio description channel) or when recording and listening to two different audio streams.

PCM mixing

The decoded audio stream can be mixed with a PCM file stored in memory following an optional sample rate conversion to adapt the sampling rate of the two streams. PCM mixing is also used when a description channel is decoded and then mixed with the main audio stream. The PCM mixing is fully implemented in the software running on the ST231.

PCM output: downmixing

The multi-channel decoded PCM stream can be downmixed to generate a 2-channel PCM stream. This down mixed stream can be then output unmixed through a stereo 24-bit DAC while the PCM-mixed decoded audio stream can be delivered onto a 6-channel digital PCM output and a digital S/PDIF output.

Compressed data: S/PDIF output

Compressed audio data can also be delivered on the S/PDIF output to be decoded by an external decoder/amplifier.

HDMI output

The STi7105 HDMI output can deliver audio data to an HDMI sink device. The audio data is delivered by the audio subsystem to the HDMI subsystem through internal I^2S-S/PDIF players/converters (see *Figure 11*).

Audio decoder features

The audio decoder features are as follows:

- Decoding of the following audio formats: MPEG1 layer I/II, MP3, MPEG2- Layer II, Dolby Digital, Dolby Digital Plus (up to 7.1), MPEG4 AAC-LC, MPEG4 AACplus (HE-AAC, AAC+SBR) v1 and v2 (up to 5.1), WMA9, WMA9pro (up to 7.1)
- PCM mixing with internal or external source with sample rate conversion (32, 44.1, 48 kHz)
- Encoded (IEC 61937) or decoded (IEC 60958) digital audio on S/PDIF output
- Multi-channel down-mixing for output over HDMI (up to 8 channels), PCM output (up to 6 channels), and analog output (up to 2 channels)
- PCM audio input (I2S format)
- Audio description channel decoding
- Postprocessing (channel virtualization)—Dolby Prologic downmix, volume control, and bass redirection

Audio transcoding

The STi7105 supports the transcoding of advanced audio formats for output over S/PDIF as formats recognized by external audio decoders. The following two transcode operations are available:

- Dolby Digital Plus to Dolby Digital
- MPEG4 AACplus to DTS

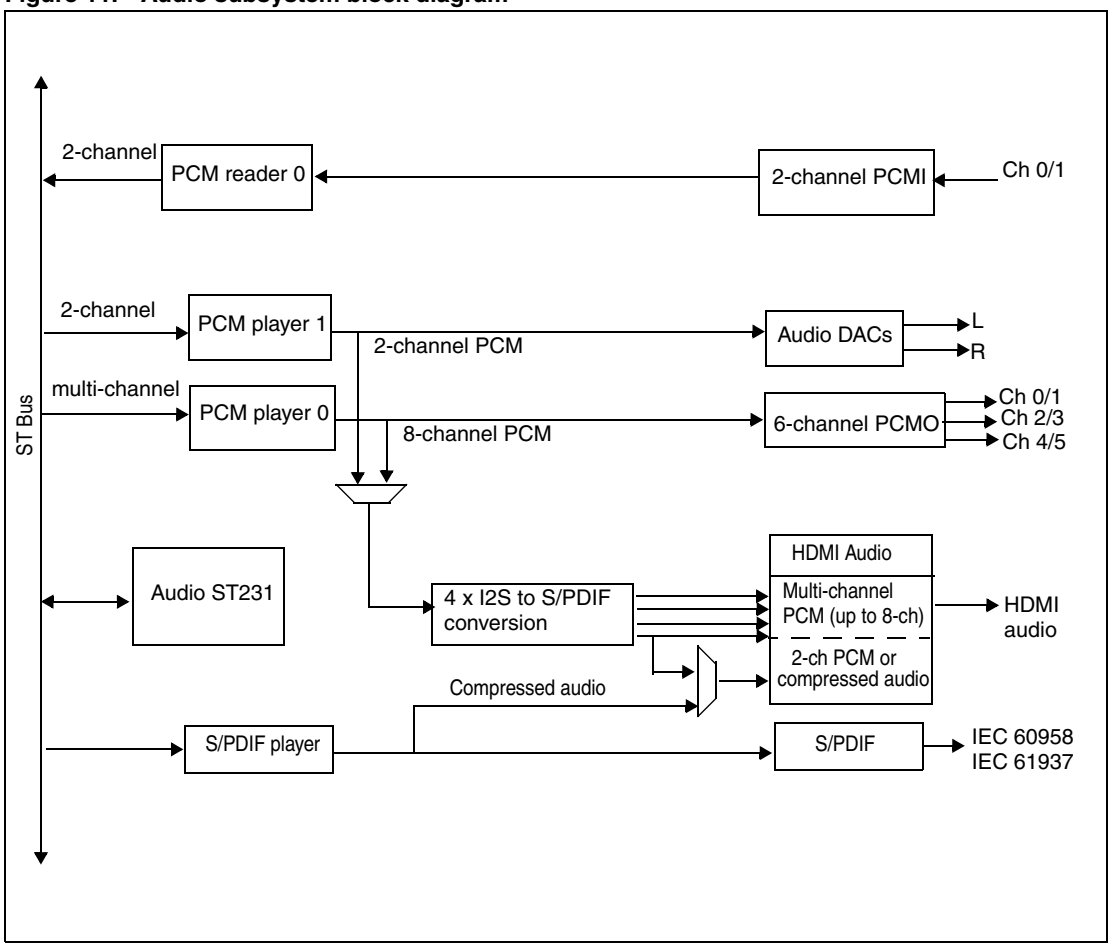
Audio subsystem blocks

The audio subsystem includes the following functional units.

- One audio processor ST231 core, running at 450 MHz, which executes the decoding algorithms, the sample-rate conversion, the post-processing and the volume control.
- One PCM reader, which captures the data at the PCM input and stores it in memory through an FDMA channel. (This is mutually exclusive with PCM player 0 since they share the same pads.)
- Two PCM players, which get decoded PCM data from memory through FDMA channels. One PCM player delivers the down-mixed PCM output to the audio DAC. The other PCM player produces the stereo or multi-channel decoded audio stream on a 7-wire PCM output (I2S protocol).
- Two quad-frequency synthesizers, which generate the PCM clock (oversampling clock 256 x Fs), used by the S/PDIF, PCM players, and audio DAC. One synthesizer clocks the S/PDIF, one clocks the PCM player associated to the audio DAC and one clocks the PCM player associated to the PCM output.
- One stereo 24-bit audio DAC with differential outputs.
- An S/PDIF player, which reads decoded PCM data or encoded data from memory through an FDMA channel, and outputs them on the S/PDIF output.

See *Figure 11* for a detailed block diagram of the audio subsystem.

Figure 11. Audio subsystem block diagram



The host CPU and the FDMA assist in the audio decoding process. Since the audio decoder is a frame decoder, the host CPU (ST40 core) controls the audio processor frame by frame. A mailbox is used for communication between the two processors.

The host CPU is also required to do the PES parsing and the frame syncword detection.

The FDMA builds the ES buffer to feed the PCM and S/PDIF players, and stores the data captured by the PCM reader in memory.

The PCM reader, PCM player, and S/PDIF player transfer data to/from memory through FDMA.

3.13 FDMA controllers

The STi7105 has two multichannel, burst-capable, direct memory access controllers:

- FDMA0—real-time paced channels: S/PDIF, PcmPlayer 0-1, and SWTS
- FDMA1—PES Parsing, PCI-Master, SWTS when streaming from Ethernet or USB, UART, SSC, and free-running general purpose DMAs

External pacing signals are available for DMA transfers with external peripherals.

3.14 Interfaces

3.14.1 Internal peripherals

The STi7105 has many dedicated internal peripherals, including:

- 4 ASCs (UARTs), two of which are generally used by the smartcard controllers, one to support hardware flow control signals
- 2 smartcard interfaces and clock generators
- 4 external SSCs for I^2C/SPI master/slave interfaces
- 1 four-channel PWM module with 2 PWM outputs and programmable frequency
- 1 teletext serializer
- 17 GPIO ports (3.3 V tolerant)
- 1 modem analog front end (MAFE) interface
- 1 single infrared transmitter/receiver supporting RC5, RC6 and RECS80, RC-MM 1.5, DIRECTV and Echostar codes
- 1 UHF remote control digital input
- 1 interrupt level controller with external interrupt inputs
- 2 independent USB 2.0 host controllers each with its own integrated PHY
- 1 front panel key scanning support
- 1 e-SATA interface

3.14.2 Ethernet controller

The STi7105 has an integrated Ethernet controller and MAC processor for delivery of IP based A/V streams in hybrid IP STBs and for home network connectivity. It also includes an MII/RMII port for connection to an external PHY. Ethernet features are as follows:

- Half/full duplex, full duplex flow control
- VLAN tagging support
- MII and RMII external interface
- Direct interface with STE101P and similar PHYs through MII or RMII
- Able to accept clock from external PHY/Home network Device in MII mode
- Dedicated scatter/gather link list DMA
- 100 Mbits/s sustained transfer rates to and from memory
- 32 H/W perfect match MAC address filters

The controller can also be used to interface through overclocked MII interface (up to 300 Mbits/s) to an external non-Ethernet Phy as a MoCA Phy for example.

3.14.3 Dual smartcard interfaces

Both smartcard interfaces are ISO7816, EMV2000 and NDS compliant, with the addition of a simple external power switch.

A programmable hardware power control feature allows the power control signal to be switched when card insertion or removal is detected.

3.15 Clock generation

The STi7105 features five clock generation blocks:

- ClockGen A: 2 x PLLs main for CPU and interconnect clocks
- ClockGen B: 2 x FreqSynth for video, display and peripheral clocks
- ClockGen C: 1 x FreqSynth for audio clocks
- ClockGen D: 1 x PLL for memory clocks

3.16 System services

The STi7105 supports a number of on-chip system service functions including:

- integrated VCXOs (DCOs) for clock recovery
- debug through a single JTAG port
- reset and watchdog controller
- two power saving modes: reduced power mode and low power/standby mode

4 Package mechanical data

4.1 27 x 27 package

Package type: PBGA 620 balls. Body: 27 x 27 mm.

Figure 12. Top view

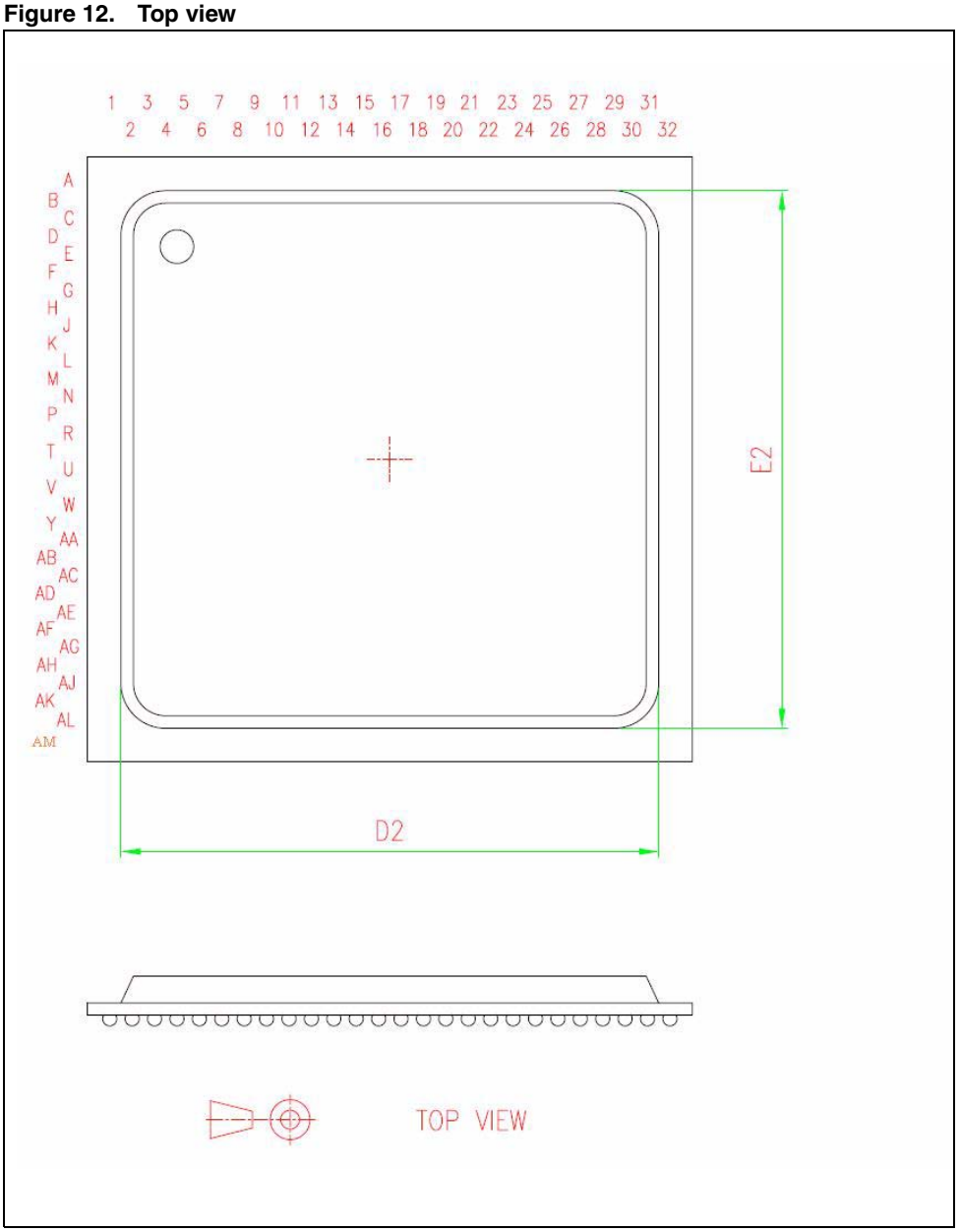


Figure 13. Bottom view

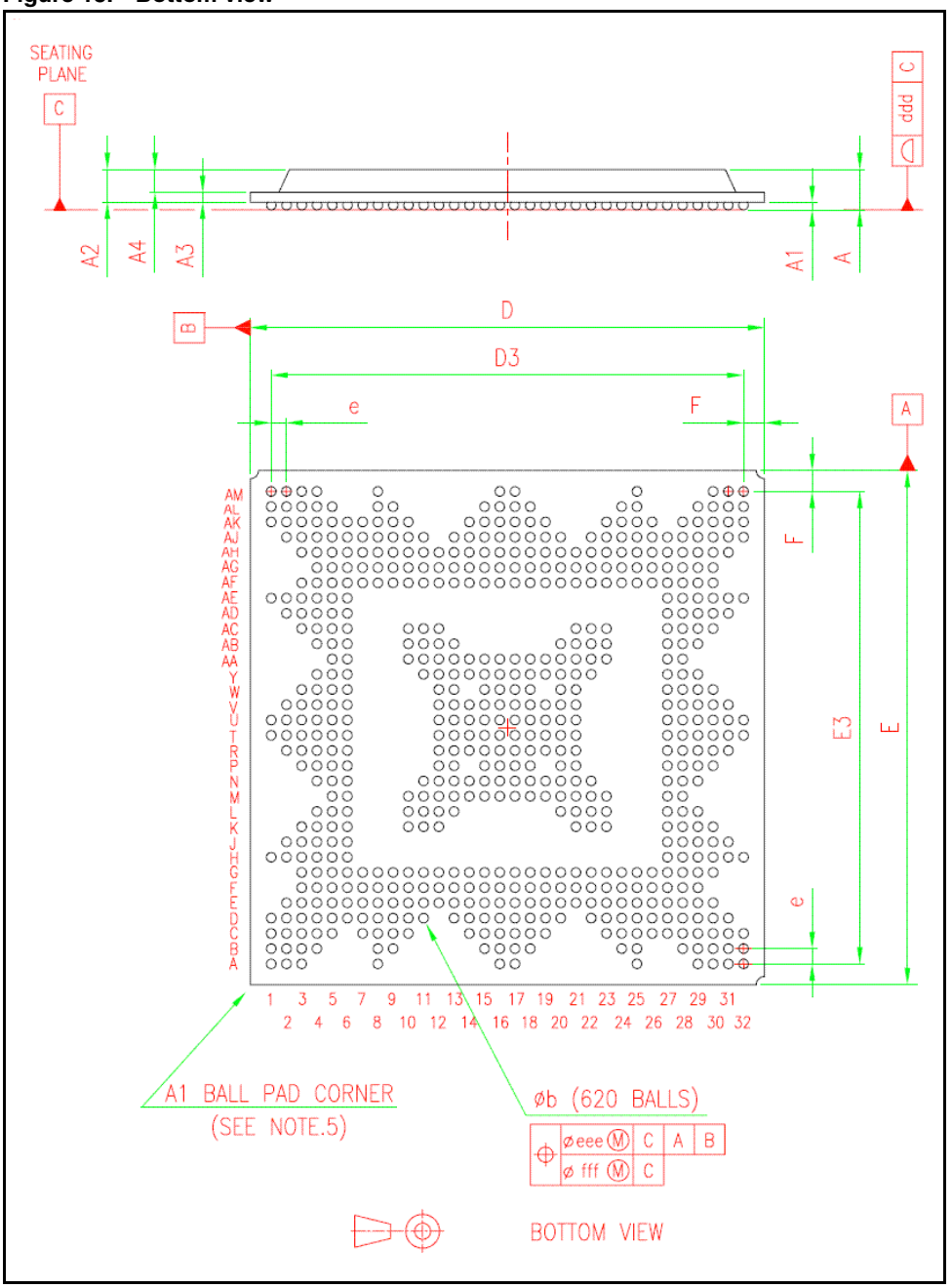


Table 1. JEDEC standard package dimensions

Dimension	Millimeters			Inches			Notes
	Min	Typ	Max	Min	Typ	Max	
A			2.19			0.8622	(1)
A1	0.27			0.0106			
A2		1.72			0.0677		
A3		0.52			0.0205		
A4		1.20			0.0472		
b	0.45	0.50	0.55	0.0177	0.0197	0.0217	(2)
D	26.80	27.00	27.20	1.055	1.063	1.070	
D1		24.80			0.9764		
D2		24.00			0.9449		
E	26.80	27.00	27.20	1.055	1.063	1.070	
E1		24.80			0.9764		
E2		24.00			0.9449		
e		0.80			0.0315		
F		1.10			0.0433		
ddd			0.20			0.0079	
eee			0.15			0.0059	(3)
fff			0.08			0.0315	(4)

1. FPBGA stands for Fine pitch Plastic Ball Grid Array.

   Fine pitch: e < 1.00 mm

   The total profile height (Dim A) is measured from the seating plane to the top of the component.

   The maximum total package height is calculated by the following methodology:

   A2 Typ+A1 Typ + V ($A1^2$+$A3^2$+$A4^2$ tolerance values)

2. The typical ball diameter before mounting is 0.50mm.

3. The tolerance of position that controls the location of the pattern of balls with respect to datums A and B. For each ball there is a cylindrical tolerance zone eee perpendicular to datum C and located on true position with respect to datums A and B as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone

4. The tolerance of position that controls the location of the balls within the matrix with respect to each other. For each ball there is a cylindrical tolerance zone fff perpendicular to datum C and located on true position as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone. Each tolerance zone fff in the array is contained entirely in the respective zone eee above. The axis of each ball must lie simultaneously in both tolerance zones.

   The terminal A1 corner must be identified on the top surface by using a corner chamfer, ink or metallized markings, or other feature of package body or integral heatslug.

   A distinguishing feature is allowable on the bottom surface of the package to identify the terminal A1 corner. Exact shape of each corner is optional.

4.2 Environmentally friendly packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

5 BGA footprint and pin lists

5.1 Ball grid array

The ball grid array (BGA) diagrams give the allocation of pins to the package, shown from the top looking down using the PCB footprint.

Signal names are prefixed by NOT if they are active low; otherwise they are active high.

Some signal names in BGA diagrams have been abbreviated. Cross refer with *Table 3: Pin list on page 42* for the full signal names.

Table 2. Key to BGA diagrams

Function	Type	Key
Transport	SIG	
PIO/peripheral	SIG	
Video	SIG	
Audio	SIG	
System (JTAG, interrupts)	SIG	
Memory (EMI, LMI)	SIG	
Power	VCC/VDD	
Ground	VSS/GND	
No connect	NC	
No ball		

Figure 14. Top-left quadrant

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
A	NOTTRST	NOTLMICLK[1]	LMIDATA[21]					LMIDATAMASK[2]								LMIADDR[11]	NOTLMICLK[0]
B	TDO	TDI	LMIDATA[18]	LMIDATA[16]				LMIDATAMASK[3]	NOTLMICS[0]						LMIBA[2]	LMIADDR[13]	LMICLK[0]
C	TCK	TMS	LMICLK[1]	LMIDATA[23]	LMIDQS[2]		LMIDATA[31]	LMIDQSN[3]	NOTLMICAS	LMIDATA[25]				LMIADDR[8]	LMIADDR[6]	LMIDUMMY[1]	LMIADDR[12]
D	PIO7[0]	PIO7[1]	PIO7[2]	NOTLMICS[1]	LMIDQSN[2]	LMIDATA[26]	LMIDQS[3]	LMI_GND1V8	NOTLMIRAS	LMIDATA[27]	LMIDATA[22]		LMIBA[0]	LMIADDR[2]	LMIDUMMY[0]	LMI_GND1V8	LMI_GND1V8
E		PIO6[1]	PIO6[2]	PIO6[0]	LMICLKEN[1]	LMIDATA[24]	ODT[0]	LMI_GND1V8	LMI_GND1V8	LMIDATA[30]	LMIDATA[17]	LMIDATA[20]	LMIADDR[4]	LMIBA[1]	LMI_GND1V8	LMI_GND1V8	LMI_GND1V8
F			PIO6[4]	PIO6[5]	PIO6[3]	LMIDATA[29]	VDD1V2	LMIPLL_AGND2V5	LMIPLL_AGND1V2	LMI_GND1V8	LMIDATA[28]	LMIDATA[19]	LMIVREF[1]	LMI_GND1V8	LMI_GND1V8	LMI_GND1V8	LMI_GND1V8
G			PIO6[7]	PIO6[6]	PIO7[3]	VDD1V2	VDD1V2	LMIPLL_AVDD2V5	LMIPLL_AVDD1V2	LMI_GND1V8	LMI_GND1V8	LMIADDR[10]	VDD1V8_2V5	LMI_GND1V8	LMI_GND1V8	LMI_GND1V8	LMI_GND1V8
H	PIO13[2]	PIO13[3]	PIO13[0]	VDD3V3	VDD3V3	VDD3V3											
J		PIO12[6]	PIO12[5]	PIO13[1]	VDD3V3	VDD3V3											
K			PIO12[2]	PIO12[4]	PIO12[0]	PIO12[7]				VDD1V8_2V5	VDD1V8_2V5	VDD1V8_2V5					
L				PIO12[1]	PIO14[7]	PIO12[3]				DGND	DGND	VDD1V8_2V5	VDD1V8_2V5				
M					PIO14[4]	PIO14[6]				DGND	DGND	DGND	VDD1V8_2V5	VDD1V2	VDD1V2	VDD1V8_2V5	VDD1V8_2V5
N				PIO14[2]	PIO14[1]	PIO14[5]					DGND	DGND	DGND	DGND	VDD1V2	VDD1V2	VDD1V2
P			PIO13[6]	PIO14[0]	PIO13[4]	PIO14[3]						VDD1V2	DGND		DGND	VDD1V2	VDD1V2
R		PIO13[5]	NOTEMICSA	PIO13[7]	CKGA1_DGND1V2	CKGA0_DGND1V2						VDD1V2	VDD1V2	DGND	DGND	DGND	DGND
T	NOTEMICSC	NOTEMICSB	NOTEMICSE	CKGA0_AGND2V5	CKGA1_DVDD1V2	CKGA0_DVDD1V2						VDD3V3	VDD1V2	VDD1V2	DGND	DGND	DGND
U	NOTEMICSD	EMIFLASHCLK	NOTEMIBAA	CKGA1_AGND2V5	CKGA1_AVDD2V5	CKGA0_AVDD2V5						VDD3V3	VDD1V2	VDD1V2	DGND	DGND	DGND
V		EMIADDR[3]	EMITREADYORWAIT	EMIADDR[2]	EMIADDR[4]	EMIADDR[5]						VDD1V2	VDD1V2	DGND	DGND	VDD1V2	DGND
W			EMIADDR[7]	EMIADDR[1]	EMIADDR[12]	EMIADDR[6]						VDD1V2	DGND		DGND	VDD1V2	DGND
Y				EMIADDR[10]	NOTEMIOE	EMIADDR[11]					VDD3V3	VDD3V3	DGND	DGND	VDD1V2	VDD1V2	DGND

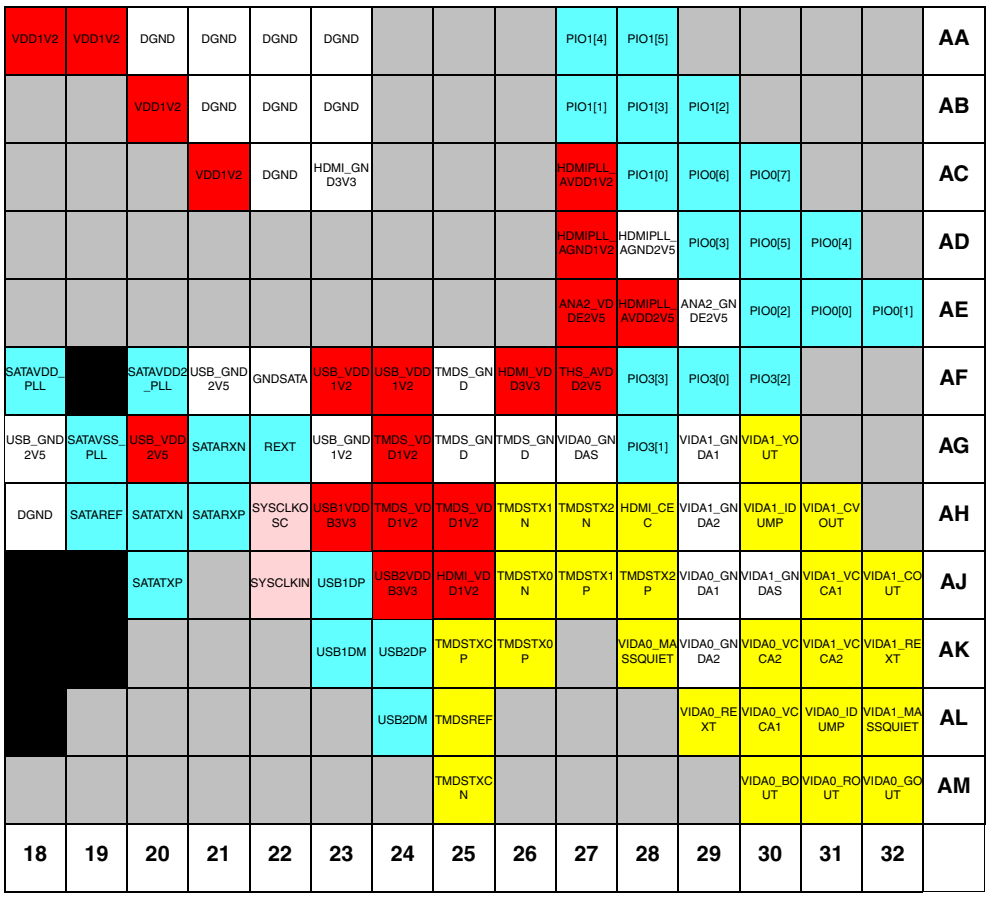
Figure 15. Top-right quadrant

18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	
							LMIDQS[0]				WDOGRSTOUT	SYSITRQ[3]	SYSITRQ[1]	SYSITRQ[0]	A
LMIDATA[2]						LMIDQSN[1]	LMIDQSN[0]			LMIDATA[3]	NOTASEBRK	SYSITRQ[2]	TRIGGERIN	NOTRESETIN	B
LMIDATA[0]	LMIADDR[9]				LMICLKEN[0]	LMIDQS[1]	LMIDATA[14]	LMIDATA[11]	LMIDATA[6]	LMIDATA[4]	TRIGGEROUT	SYSCLKINALT	NMI	SYSCLKOUT	C
LMIDATA[5]	LMIADDR[7]	LMIDATA[10]		LMIADDR[1]	NOTLMIWE	LMIDATAMASK[1]	VDD3V3	LMIDATA[9]	LMIDATA[1]		PIO16[2]	PIO16[4]	PIO16[3]		D
VDD1V8_2V5	LMIDATA[7]	LMIDATA[13]	LMIADDR[3]	ODT[1]	LMIDATAMASK[0]	VDD3V3	VDD3V3	LMIDATA[12]	LMIVREF[0]	PIO11[7]	PIO16[1]	PIO16[0]			E
VDD1V8_2V5	VDD1V8_2V5	LMIADDR[15]	LMIDATA[15]	LMIADDR[10]	VDD1V8_2V5	LMI_COMP_GND	VDD3V3	GND_SENSE	PIO11[4]	PIO11[6]	PIO11[5]				F
VDD1V8_2V5	VDD1V8_2V5	VDD1V8_2V5	LMIDATA[8]	VDD1V8_2V5	VDD1V8_2V5	LMI_COMP_REF	VDD3V3	VDD_SENSE	VDD1V2	PIO16[7]	PIO11[3]	PIO11[2]			G
									VDD2V5	VDD1V2	VDD1V2	PIO16[6]	PIO15[6]	PIO15[7]	H
									FDMAREQ[3]	PIO16[5]	PIO9[7]	DAA_C2A	DAA_C1A		J
			DGND	DGND	DGND				PIO5[3]	FDMAREQ[2]	FDMAREQ[0]	FDMAREQ[1]			K
		DGND	DGND	DGND	VDD3V3				PIO5[0]	PIO5[2]	PIO5[1]				L
VDD1V2	VDD1V2	DGND	DGND	DGND	VDD3V3				PIO4[6]	PIO4[7]					M
VDD1V2	DGND	DGND	DGND	VDD3V3					PIO4[3]	PIO4[5]	PIO4[4]				N
DGND		DGND	VDD1V2						DGND	PIO4[2]	PIO4[0]	PIO4[1]			P
DGND	DGND	VDD1V2	VDD1V2						VDD2V5	VDD1V2	PIO3[5]	PIO3[7]	PIO3[6]		R
DGND	DGND	VDD3V3	VDD3V3						CKGB1_DGND1V2	CKGB1_DVDD1V2	DGND	PIO3[4]	PIO5[6]	PIO5[7]	T
DGND	DGND	VDD3V3	VDD3V3						CKGB0_AVDD2V5	CKGB1_AVDD2V5	DGND	PIO5[4]	PIO2[7]	PIO5[5]	U
DGND	DGND	VDD1V2	VDD1V2						CKGB0_DGND1V2	CKGB_AGND2V5	PIO2[4]	PIO2[6]	PIO2[5]		V
DGND		DGND	DGND						CKGB0_DVDD1V2	PIO2[3]	PIO2[1]	PIO2[2]			W
VDD1V2	DGND	DGND	DGND	DGND					PIO1[6]	PIO2[0]	PIO1[7]				Y

Figure 16. Bottom-left quadrant

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
AA					EMIADDR[13]	EMIRDNOTWR				VDD3V3	VDD3V3	DGND	DGND	VDD1V2	VDD1V2	VDD1V2	DGND
AB				EMIADDR[8]	EMIADDR[16]	EMIADDR[14]				VDD3V3	DGND	DGND	DGND				
AC			EMIADDR[9]	EMIADDR[18]	NOTEMIBE[0]	EMIADDR[17]				DGND	DGND	DGND					
AD		EMIADDR[21]	EMIADDR[22]	EMIADDR[20]	VDD1V2	EMIBUSREQ											
AE	NOTEMIBE[1]	EMIADDR[15]	EMIBUSGNT	VDD1V2	VDD1V2	VDD1V2											
AF			EMIADDR[25]	EMIDATA[2]	EMIADDR[24]	VDD1V2	PIO9[4]	PIO9[6]	PIO8[3]	ANA1_VDD2V5	ANA1_VDD2V5	CKGC_AVDD2V5	CKGC_AGND2V5	PIO10[0]	VDD3V3	SATAVSS	
AG				NOTEMILBA	NANDWAIT	EMIADDR[19]	PIO9[3]	PIO8[4]	PIO10[7]	ANA1_GND2V5	CKGC_DGND1V2	AUDA_DVDD1V2	PIO10[4]	CKGC_DVDD1V2	VDD3V3	SATAVDDR	SATAVDDT
AH			EMIDATA[11]	EMIDATA[6]	EMIDATA[13]	PIO15[5]	PIO7[7]	DGND	ANA1_GND2V5	PIO8[5]	PIO9[5]	AUDA_DGND1V2	PIO11[1]	PIO10[1]	VDD3V3	VDD3V3	DGND
AJ		EMIDATA[15]	EMIDATA[14]	EMIADDR[23]	PIO15[2]	PIO7[6]	PIO9[2]	DGND	PIO8[6]	PIO10[5]	PIO10[6]		PIO11[0]	PIO10[2]	DGND	DGND	DGND
AK	EMIDATA[4]	EMIDATA[1]	EMIDATA[7]	EMIDATA[5]	PIO15[4]	PIO8[1]	PIO8[2]	PIO7[5]	PIO7[4]	PIO9[0]				PIO10[3]	AUDA_RIGHTOUTN	AUDA_GNDAS	DGND
AL	EMIDATA[8]	EMIDATA[3]	EMIDATA[10]	PIO15[1]	PIO15[3]			PIO8[0]	PIO8[7]						AUDA_RIGHTOUTP	AUDA_IREF	AUDA_LEFTOUTN
AM	EMIDATA[0]	EMIDATA[12]	EMIDATA[9]	PIO15[0]				PIO9[1]								AUDA_VBGOUT	AUDA_LEFTOUTP

Figure 17. Bottom-right quadrant



5.2 Pin lists

5.2.1 Full pin list sorted by pin number

Table 3. Pin list

Pin number	Net name
A1	NOTTRST
A2	NOTLMICLK[1]
A3	LMIDATA[21]
A8	LMIDATAMASK[2]
A16	LMIADDR[11]
A17	NOTLMICLK[0]
A25	LMIDQS[0]
A29	WDOGRSTOUT
A30	SYSITRQ[3]
A31	SYSITRQ[1]
A32	SYSITRQ[0]
B1	TDO
B2	TDI
B3	LMIDATA[18]
B4	LMIDATA[16]
B8	LMIDATAMASK[3]
B9	NOTLMICS[0]
B15	LMIBA[2]
B16	LMIADDR[13]
B17	LMICLK[0]
B18	LMIDATA[2]
B24	LMIDQSN[1]
B25	LMIDQSN[0]
B28	LMIDATA[3]
B29	NOTASEBRK
B30	SYSITRQ[2]
B31	TRIGGERIN
B32	NOTRESETIN
C1	TCK
C2	TMS
C3	LMICLK[1]

Table 3. Pin list (continued)

Pin number	Net name
C4	LMIDATA[23]
C5	LMIDQS[2]
C7	LMIDATA[31]
C8	LMIDQSN[3]
C9	NOTLMICAS
C10	LMIDATA[25]
C14	LMIADDR[8]
C15	LMIADDR[6]
C16	LMIDUMMY[1]
C17	LMIADDR[12]
C18	LMIDATA[0]
C19	LMIADDR[9]
C23	LMICLKEN[0]
C24	LMIDQS[1]
C25	LMIDATA[14]
C26	LMIDATA[11]
C27	LMIDATA[6]
C28	LMIDATA[4]
C29	TRIGGEROUT
C30	SYSCLKINALT
C31	NMI
C32	SYSCLKOUT
D1	PIO7[0]
D2	PIO7[1]
D3	PIO7[2]
D4	NOTLMICS[1]
D5	LMIDQSN[2]
D6	LMIDATA[26]
D7	LMIDQS[3]
D8	LMI_GND1V8
D9	NOTLMIRAS
D10	LMIDATA[27]
D11	LMIDATA[22]
D13	LMIBA[0]
D14	LMIADDR[2]

Table 3. Pin list (continued)

Pin number	Net name
D15	LMIDUMMY[0]
D16	LMI_GND1V8
D17	LMI_GND1V8
D18	LMIDATA[5]
D19	LMIADDR[7]
D20	LMIDATA[10]
D22	LMIADDR[1]
D23	NOTLMIWE
D24	LMIDATAMASK[1]
D25	VDD3V3
D26	LMIDATA[9]
D27	LMIDATA[1]
D28	NC
D29	PIO16[2]
D30	PIO16[4]
D31	PIO16[3]
E2	PIO6[1]
E3	PIO6[2]
E4	PIO6[0]
E5	LMICLKEN[1]
E6	LMIDATA[24]
E7	ODT[0]
E8	LMI_GND1V8
E9	LMI_GND1V8
E10	LMIDATA[30]
E11	LMIDATA[17]
E12	LMIDATA[20]
E13	LMIADDR[4]
E14	LMIBA[1]
E15	LMI_GND1V8
E16	LMI_GND1V8
E17	LMI_GND1V8
E18	VDD1V8_2V5
E19	LMIDATA[7]
E20	LMIDATA[13]

Table 3. Pin list (continued)

Pin number	Net name
E21	LMIADDR[3]
E22	ODT[1]
E23	LMIDATAMASK[0]
E24	VDD3V3
E25	VDD3V3
E26	LMIDATA[12]
E27	LMIVREF[0]
E28	PIO11[7]
E29	PIO16[1]
E30	PIO16[0]
F3	PIO6[4]
F4	PIO6[5]
F5	PIO6[3]
F6	LMIDATA[29]
F7	VDD1V2
F8	LMIPLL_AGND2V5
F9	LMIPLL_AGND1V2
F10	LMI_GND1V8
F11	LMIDATA[28]
F12	LMIDATA[19]
F13	LMIVREF[1]
F14	LMI_GND1V8
F15	LMI_GND1V8
F16	LMI_GND1V8
F17	LMI_GND1V8
F18	VDD1V8_2V5
F19	VDD1V8_2V5
F20	LMIADDR[5]
F21	LMIDATA[15]
F22	LMIADDR[10]
F23	VDD1V8_2V5
F24	LMI_COMP_GND
F25	VDD3V3
F26	GND_SENSE
F27	PIO11[4]

Table 3. Pin list (continued)

Pin number	Net name
F28	PIO11[6]
F29	PIO11[5]
G3	PIO6[7]
G4	PIO6[6]
G5	PIO7[3]
G6	VDD1V2
G7	VDD1V2
G8	LMIPLL_AVDD2V5
G9	LMIPLL_AVDD1V2
G10	LMI_GND1V8
G11	LMI_GND1V8
G12	LMIADDR[0]
G13	VDD1V8_2V5
G14	LMI_GND1V8
G15	LMI_GND1V8
G16	LMI_GND1V8
G17	LMI_GND1V8
G18	VDD1V8_2V5
G19	VDD1V8_2V5
G20	VDD1V8_2V5
G21	LMIDATA[8]
G22	VDD1V8_2V5
G23	VDD1V8_2V5
G24	LMI_COMP_REF
G25	VDD3V3
G26	VDD_SENSE
G27	VDD1V2
G28	PIO16[7]
G29	PIO11[3]
G30	PIO11[2]
H1	PIO13[2]
H2	PIO13[3]
H3	PIO13[0]
H4	VDD3V3
H5	VDD3V3

Table 3. Pin list (continued)

Pin number	Net name
H6	VDD3V3
H27	VDD2V5
H28	VDD1V2
H29	VDD1V2
H30	PIO16[6]
H31	PIO15[6]
H32	PIO15[7]
J2	PIO12[6]
J3	PIO12[5]
J4	PIO13[1]
J5	VDD3V3
J6	VDD3V3
J27	FDMAREQ[3]
J28	PIO16[5]
J29	PIO9[7]
J30	DAA_C2A
J31	DAA_C1A
K3	PIO12[2]
K4	PIO12[4]
K5	PIO12[0]
K6	PIO12[7]
K10	VDD1V8_2V5
K11	VDD1V8_2V5
K12	VDD1V8_2V5
K21	DGND
K22	DGND
K23	DGND
K27	PIO5[3]
K28	FDMAREQ[2]
K29	FDMAREQ[0]
K30	FDMAREQ[1]
L4	PIO12[1]
L5	PIO14[7]
L6	PIO12[3]
L10	DGND

Table 3. Pin list (continued)

Pin number	Net name
L11	DGND
L12	VDD1V8_2V5
L13	VDD1V8_2V5
L20	DGND
L21	DGND
L22	DGND
L23	VDD3V3
L27	PIO5[0]
L28	PIO5[2]
L29	PIO5[1]
M5	PIO14[4]
M6	PIO14[6]
M10	DGND
M11	DGND
M12	DGND
M13	VDD1V8_2V5
M14	VDD1V2
M15	VDD1V2
M16	VDD1V8_2V5
M17	VDD1V8_2V5
M18	VDD1V2
M19	VDD1V2
M20	DGND
M21	DGND
M22	DGND
M23	VDD3V3
M27	PIO4[6]
M28	PIO4[7]
N4	PIO14[2]
N5	PIO14[1]
N6	PIO14[5]
N11	DGND
N12	DGND
N13	DGND
N14	DGND

Table 3. Pin list (continued)

Pin number	Net name
N15	VDD1V2
N16	VDD1V2
N17	VDD1V2
N18	VDD1V2
N19	DGND
N20	DGND
N21	DGND
N22	VDD3V3
N27	PIO4[3]
N28	PIO4[5]
N29	PIO4[4]
P3	PIO13[6]
P4	PIO14[0]
P5	PIO13[4]
P6	PIO14[3]
P12	VDD1V2
P13	DGND
P15	DGND
P16	VDD1V2
P17	VDD1V2
P18	DGND
P20	DGND
P21	VDD1V2
P27	DGND
P28	PIO4[2]
P29	PIO4[0]
P30	PIO4[1]
R2	PIO13[5]
R3	NOTEMICSA
R4	PIO13[7]
R5	CKGA1_DGND1V2
R6	CKGA0_DGND1V2
R12	VDD1V2
R13	VDD1V2
R14	DGND

Table 3. Pin list (continued)

Pin number	Net name
R15	DGND
R16	DGND
R17	DGND
R18	DGND
R19	DGND
R20	VDD1V2
R21	VDD1V2
R27	VDD2V5
R28	VDD1V2
R29	PIO3[5]
R30	PIO3[7]
R31	PIO3[6]
T1	NOTEMICSC
T2	NOTEMICSB
T3	NOTEMICSE
T4	CKGA0_AGND2V5
T5	CKGA1_DVDD1V2
T6	CKGA0_DVDD1V2
T12	VDD3V3
T13	VDD1V2
T14	VDD1V2
T15	DGND
T16	DGND
T17	DGND
T18	DGND
T19	DGND
T20	VDD3V3
T21	VDD3V3
T27	CKGB1_DGND1V2
T28	CKGB1_DVDD1V2
T29	DGND
T30	PIO3[4]
T31	PIO5[6]
T32	PIO5[7]
U1	NOTEMICSD

Table 3. Pin list (continued)

Pin number	Net name
U2	EMIFLASHCLK
U3	NOTEMIBAA
U4	CKGA1_AGND2V5
U5	CKGA1_AVDD2V5
U6	CKGA0_AVDD2V5
U12	VDD3V3
U13	VDD1V2
U14	VDD1V2
U15	DGND
U16	DGND
U17	DGND
U18	DGND
U19	DGND
U20	VDD3V3
U21	VDD3V3
U27	CKGB0_AVDD2V5
U28	CKGB1_AVDD2V5
U29	DGND
U30	PIO5[4]
U31	PIO2[7]
U32	PIO5[5]
V2	EMIADDR[3]
V3	EMITREADYORWAIT
V4	EMIADDR[2]
V5	EMIADDR[4]
V6	EMIADDR[5]
V12	VDD1V2
V13	VDD1V2
V14	DGND
V15	DGND
V16	VDD1V2
V17	DGND
V18	DGND
V19	DGND
V20	VDD1V2

Table 3. Pin list (continued)

Pin number	Net name
V21	VDD1V2
V27	CKGB0_DGND1V2
V28	CKGB_AGND2V5
V29	PIO2[4]
V30	PIO2[6]
V31	PIO2[5]
W3	EMIADDR[7]
W4	EMIADDR[1]
W5	EMIADDR[12]
W6	EMIADDR[6]
W12	VDD1V2
W13	DGND
W15	DGND
W16	VDD1V2
W17	DGND
W18	DGND
W20	DGND
W21	DGND
W27	CKGB0_DVDD1V2
W28	PIO2[3]
W29	PIO2[1]
W30	PIO2[2]
Y4	EMIADDR[10]
Y5	NOTEMIOE
Y6	EMIADDR[11]
Y11	VDD3V3
Y12	VDD3V3
Y13	DGND
Y14	DGND
Y15	VDD1V2
Y16	VDD1V2
Y17	DGND
Y18	VDD1V2
Y19	DGND
Y20	DGND

Table 3. Pin list (continued)

Pin number	Net name
Y21	DGND
Y22	DGND
Y27	PIO1[6]
Y28	PIO2[0]
Y29	PIO1[7]
AA5	EMIADDR[13]
AA6	EMIRDNOTWR
AA10	VDD3V3
AA11	VDD3V3
AA12	DGND
AA13	DGND
AA14	VDD1V2
AA15	VDD1V2
AA16	VDD1V2
AA17	DGND
AA18	VDD1V2
AA19	VDD1V2
AA20	DGND
AA21	DGND
AA22	DGND
AA23	DGND
AA27	PIO1[4]
AA28	PIO1[5]
AB4	EMIADDR[8]
AB5	EMIADDR[16]
AB6	EMIADDR[14]
AB10	VDD3V3
AB11	DGND
AB12	DGND
AB13	DGND
AB20	VDD1V2
AB21	DGND
AB22	DGND
AB23	DGND
AB27	PIO1[1]

Table 3. Pin list (continued)

Pin number	Net name
AB28	PIO1[3]
AB29	PIO1[2]
AC3	EMIADDR[9]
AC4	EMIADDR[18]
AC5	NOTEMIBE[0]
AC6	EMIADDR[17]
AC10	DGND
AC11	DGND
AC12	DGND
AC21	VDD1V2
AC22	DGND
AC23	HDMI_GND3V3
AC27	HDMIPLL_AVDD1V2
AC28	PIO1[0]
AC29	PIO0[6]
AC30	PIO0[7]
AD2	EMIADDR[21]
AD3	EMIADDR[22]
AD4	EMIADDR[20]
AD5	VDD1V2
AD6	EMIBUSREQ
AD27	HDMIPLL_AGND1V2
AD28	HDMIPLL_AGND2V5
AD29	PIO0[3]
AD30	PIO0[5]
AD31	PIO0[4]
AE1	NOTEMIBE[1]
AE2	EMIADDR[15]
AE3	EMIBUSGNT
AE4	VDD1V2
AE5	VDD1V2
AE6	VDD1V2
AE27	ANA2_VDDE2V5
AE28	HDMIPLL_AVDD2V5
AE29	ANA2_GNDE2V5

Table 3. Pin list (continued)

Pin number	Net name
AE30	PIO0[2]
AE31	PIO0[0]
AE32	PIO0[1]
AF3	EMIADDR[25]
AF4	EMIDATA[2]
AF5	EMIADDR[24]
AF6	VDD1V2
AF7	PIO9[4]
AF8	PIO9[6]
AF9	PIO8[3]
AF10	ANA1_VDD2V5
AF11	ANA1_VDD2V5
AF12	CKGC_AVDD2V5
AF13	CKGC_AGND2V5
AF14	PIO10[0]
AF15	VDD3V3
AF16	SATAVSS
AF17	NC
AF18	SATAVDD_PLL
AF19	NC
AF20	SATAVDD2_PLL
AF21	USB_GND2V5
AF22	GNDSATA
AF23	USB_VDD1V2
AF24	USB_VDD1V2
AF25	TMDS_GND
AF26	HDMI_VDD3V3
AF27	THS_AVDD2V5
AF28	PIO3[3]
AF29	PIO3[0]
AF30	PIO3[2]
AG4	NOTEMILBA
AG5	NANDWAIT
AG6	EMIADDR[19]
AG7	PIO9[3]

Table 3. Pin list (continued)

Pin number	Net name
AG8	PIO8[4]
AG9	PIO10[7]
AG10	ANA1_GND2V5
AG11	CKGC_DGND1V2
AG12	AUDA_DVDD1V2
AG13	PIO10[4]
AG14	CKGC_DVDD1V2
AG15	VDD3V3
AG16	SATAVDDR
AG17	SATAVDDT
AG18	USB_GND2V5
AG19	SATAVSS_PLL
AG20	USB_VDD2V5
AG21	SATARXN
AG22	REXT
AG23	USB_GND1V2
AG24	TMDS_VDD1V2
AG25	TMDS_GND
AG26	TMDS_GND
AG27	VIDA0_GNDAS
AG28	PIO3[1]
AG29	VIDA1_GNDA1
AG30	VIDA1_YOUT
AH3	EMIDATA[11]
AH4	EMIDATA[6]
AH5	EMIDATA[13]
AH6	PIO15[5]
AH7	PIO7[7]
AH8	DGND
AH9	ANA1_GND2V5
AH10	PIO8[5]
AH11	PIO9[5]
AH12	AUDA_DGND1V2
AH13	PIO11[1]
AH14	PIO10[1]

Table 3. Pin list (continued)

Pin number	Net name
AH15	VDD3V3
AH16	VDD3V3
AH17	DGND
AH18	DGND
AH19	SATAREF
AH20	SATATXN
AH21	SATARXP
AH22	SYSCLKOSC
AH23	USB1VDDB3V3
AH24	TMDS_VDD1V2
AH25	TMDS_VDD1V2
AH26	TMDSTX1N
AH27	TMDSTX2N
AH28	HDMI_CEC
AH29	VIDA1_GNDA2
AH30	VIDA1_IDUMP
AH31	VIDA1_CVOUT
AJ2	EMIDATA[15]
AJ3	EMIDATA[14]
AJ4	EMIADDR[23]
AJ5	PIO15[2]
AJ6	PIO7[6]
AJ7	PIO9[2]
AJ8	DGND
AJ9	PIO8[6]
AJ10	PIO10[5]
AJ11	PIO10[6]
AJ13	PIO11[0]
AJ14	PIO10[2]
AJ15	DGND
AJ16	DGND
AJ17	DGND
AJ18	NC
AJ19	NC
AJ20	SATATXP

Table 3. Pin list (continued)

Pin number	Net name
AJ22	SYSCLKIN
AJ23	USB1DP
AJ24	USB2VDDB3V3
AJ25	HDMI_VDD1V2
AJ26	TMDSTX0N
AJ27	TMDSTX1P
AJ28	TMDSTX2P
AJ29	VIDA0_GNDA1
AJ30	VIDA1_GNDAS
AJ31	VIDA1_VCCA1
AJ32	VIDA1_COUT
AK1	EMIDATA[4]
AK2	EMIDATA[1]
AK3	EMIDATA[7]
AK4	EMIDATA[5]
AK5	PIO15[4]
AK6	PIO8[1]
AK7	PIO8[2]
AK8	PIO7[5]
AK9	PIO7[4]
AK10	PIO9[0]
AK14	PIO10[3]
AK15	AUDA_RIGHTOUTN
AK16	AUDA_GNDAS
AK17	DGND
AK18	NC
AK19	NC
AK23	USB1DM
AK24	USB2DP
AK25	TMDSTXCP
AK26	TMDSTX0P
AK28	VIDA0_MASSQUIET
AK29	VIDA0_GNDA2
AK30	VIDA0_VCCA2
AK31	VIDA1_VCCA2

Table 3. Pin list (continued)

Pin number	Net name
AK32	VIDA1_REXT
AL1	EMIDATA[8]
AL2	EMIDATA[3]
AL3	EMIDATA[10]
AL4	PIO15[1]
AL5	PIO15[3]
AL8	PIO8[0]
AL9	PIO8[7]
AL15	AUDA_RIGHTOUTP
AL16	AUDA_IREF
AL17	AUDA_LEFTOUTN
AL18	NC
AL24	USB2DM
AL25	TMDSREF
AL29	VIDA0_REXT
AL30	VIDA0_VCCA1
AL31	VIDA0_IDUMP
AL32	VIDA1_MASSQUIET
AM1	EMIDATA[0]
AM2	EMIDATA[12]
AM3	EMIDATA[9]
AM4	PIO15[0]
AM8	PIO9[1]
AM16	AUDA_VBGOUT
AM17	AUDA_LEFTOUTP
AM25	TMDSTXCN
AM30	VIDA0_BOUT
AM31	VIDA0_ROUT
AM32	VIDA0_GOUT

6 Connections

This chapter contains detail of pins, pad reset conditions, alternative functions and connection diagrams, listed in the following functional groups:

- power supplies (analog and digital) on *page 60*
- system on *page 71*
- JTAG on *page 71*
- transport interface on *page 72*
- Ethernet on *page 88*
- display analog output interface on *page 74*
- HDMI interface on *page 75*
- audio digital interface on *page 75*
- audio analog interface on *page 76*
- SATA interface on *page 76*
- FDMA interface on *page 77*
- programmable I/O (PIO) on *page 78*
- external memory interface (EMI) on *page 82*
- local memory interface on *page 85*
- USB 2.0 interface on *page 90*
- peripherals:
  - DAA interface on *page 91*
  - asynchronous serial controller (ASC) on *page 91*
  - infrared transmitter/receiver on *page 92*
  - modem analog front-end interface on *page 92*
  - PWM on *page 92*
  - smartcard on *page 93*
  - synchronous serial controller (SSC) on *page 93*
- pad reset conditions on *page 94*
- for external circuitry information, refer to *External circuitry recommendations on page 233*.

6.1 Power supplies

Table 4. Power/ground pins

Pin	Assignment	Voltage	Type	Description
USB 2.0				
AF23	USB_VDD1V2	1.2	Analog	USB 1.2 V power
AF24				
AG20	USB_VDD2V5	2.5	Analog	USB 2.5 V power
AG23	USB_GND1V2	0		USB ground

Table 4. Power/ground pins (continued)

Pin	Assignment	Voltage	Type	Description
AF21	USB_GND2V5	0		USB ground
AG18				
AH23	USB1VDDB3V3	3.3	Analog	USB1 3.3 V power
AJ24	USB2VDDB3V3	3.3	Analog	USB2 3.3 V power
SATA				
AF16	SATAVSS	0		SATA ground
AF17	NC	0		SATA ground
AG16	SATAVDDR	1.2	Analog	SATA power
AG17	SATAVDDT	1.2	Analog	SATA power
AF18	SATAVDD_PLL	1.2	Analog	SATA PLL power
AG19	SATAVSS_PLL	0		SATA PLL ground
AF20	SATAVDD2_PLL	2.5	Analog	SATA PLL power
AJ18	NC	-		No connect
AF19	NC	-		No connect
AF22	GNDSATA	0	-	SATA ground
HDMI				
AG24	TMDS_VDD1V2	1.2	Analog	TMDS 1.2 V power
AH24				
AH25				
AF25	TMDS_GND	0		TMDS ground
AG25				
AG26				
AE28	HDMIPLL_AVDD2V5	2.5	Analog	HDMI PLL 2.5 V power
AD28	HDMIPLL_AGND2V5	0		HDMI PLL ground
AC27	HDMIPLL_AVDD1V2	1.2	Analog	HDMI PLL power
AD27	HDMIPLL_AGND1V2	0		HDMI PLL ground
AC23	HDMI_GND3V3	0		HDMI ground
AF26	HDMI_VDD3V3	3.3	Digital	HDMI 3.3 V power
AJ25	HDMI_VDD1V2	1.2	Digital	HDMI 1.2 V power
LMIPLL				
G8	LMIPLL_AVDD2V5	2.5	Analog	LMI PLL 2.5 V power
F8	LMIPLL_AGND2V5	0		LMI PLL ground
G9	LMIPLL_AVDD1V2	1.2	Analog	LMI PLL 1.2 V power
F9	LMIPLL_AGND1V2	0		LMI PLL ground
Video DACs				
AG27	VIDA0_GNDAS	0		

Table 4. Power/ground pins (continued)

Pin	Assignment	Voltage	Type	Description
AK29	VIDA0_GNDA2	0		
AK30	VIDA0_VCCA2	2.5	Analog	
AL30	VIDA0_VCCA1	2.5	Analog	
AJ29	VIDA0_GNDA1	0		
AJ30	VIDA1_GNDAS	0		
AH29	VIDA1_GNDA2	0		
AK31	VIDA1_VCCA2	2.5	Analog	
AJ31	VIDA1_VCCA1	2.5	Analog	
AG29	VIDA1_GNDA1	0		
AE27	ANA2_VDDE2V5	2.5	Analog	
AE29	ANA2_GNDE2V5	0		
Audio DAC				
AG10	ANA1_GND2V5	0		
AH9				
AF10	ANA1_VDD2V5	2.5	Analog	
AF11				
AH12	AUDA_DGND1V2	0		ADCAC 1.2 V ground
AG12	AUDA_DVDD1V2	1.2	Digital	ADCAC 1.2 V power
AK16	AUDA_GNDAS	0		
ClockGenA				
R5	CKGA1_DGND1V2	0		CKGA PLL1 1.2 ground
T5	CKGA1_DVDD1V2	1.2	Digital	CKGA PLL1 1.2 power
U4	CKGA1_AGND2V5	0		CKGA PLL1 2.5 V ground
U5	CKGA1_AVDD2V5	2.5	Analog	CKGA PLL1 2.5 V power
R6	CKGA0_DGND1V2	0		CKGA PLL0 1.2 ground
T6	CKGA0_DVDD1V2	1.2	Digital	CKGA PLL0 1.2 power
T4	CKGA0_AGND2V5	0		CKGA PLL0 2.5 V ground
U6	CKGA0_AVDD2V5	2.5	Analog	CKGA PLL0 2.5 V power
ClockGenB				
U27	CKGB0_AVDD2V5	2.5	Analog	CKGB FS0 2.5 V power
V28	CKGB_AGND2V5	0		CKGB FS0,1 2.5 V ground
U28	CKGB1_AVDD2V5	2.5	Analog	CKGB FS1 2.5 V power
W27	CKGB0_DVDD1V2	1.2	Digital	CKGB FS 1.2 V power
V27	CKGB0_DGND1V2	0		CKGB FS 1.2 V ground
T27	CKGB1_DGND1V2	0		CKGB FS1 1.2 V ground
T28	CKGB1_DVDD1V2	1.2	Digital	CKGB FS1 1.2 V power

Table 4. Power/ground pins (continued)

Pin	Assignment	Voltage	Type	Description
ClockGenC				
AG11	CKGC_DGND1V2	0		CKGC FS 1.2 ground
AG14	CKGC_DVDD1V2	1.2	Digital	CKGC FS 1.2 power
AF13	CKGC_AGND2V5	0		CKGC FS 2.5 V ground
AF12	CKGC_AVDD2V5	2.5	Analog	CKGC FS 2.5 V power
LMI				
E18	VDD1V8_2V5	1.8	Digital	LMI DDR2 1.8/2.5 V power
F18				
F19				
F23				
G13				
G18				
G19				
G20				
G22				
G23				
K10				
K11				
K12				
L12				
L13				
M13				
M16				
M17				

Table 4. Power/ground pins (continued)

Pin	Assignment	Voltage	Type	Description
D8	LMI_GND1V8	0		LMI 1.8 V ground
D16				
D17				
E8				
E9				
E15				
E16				
E17				
F10				
F14				
F15				
F16				
F17				
G10				
G11				
G14				
G15				
G16				
G17				
Analog 2.5V				
H27	VDD2V5	2.5	Analog	Analog 2.5 V power
Digital 2.5V				
R27	VDD2V5	2.5	Digital	Digital 2.5 V power
Tsensor				
AF27	THS_AVDD2V5	2.5	Analog	Thermal sensor analog supply

Table 4. Power/ground pins (continued)

Pin	Assignment	Voltage	Type	Description
Digital 3.3 V				
D25	VDD3V3	3.3	Digital	Digital 3.3 V power
E24				
E25				
F25				
G25				
H4				
H5				
H6				
J5				
J6				
L23				
M23				
N22				
T12				
T20				
T21				
U12				
U20				
U21				
Y11				
Y12				
AA10				
AA11				
AB10				
AF15				
AG15				
AH15				
AH16				
DGND				

Table 4. Power/ground pins (continued)

Pin	Assignment	Voltage	Type	Description
K21	DGND	0		Digital 3.3/2.5/1.2 V ground
K22				
K23				
L10				
L11				
L20				
L21				
L22				
M10				
M11				
M12				
M20				
M21				
M22				
N11				
N12				
N13				
N14				
N19				
N20				
N21				
P13				
P15				
P18				
P20				
P27				
R14				
R15				
R16				
R17				
R18				
R19				
T15				
T16				
T17				
T18				

Table 4. Power/ground pins (continued)

Pin	Assignment	Voltage	Type	Description
T19				
T29				
U15				
U16				
U17				
U18				
U19				
U29				
V14				
V15				
V17				
V18				
V19				
W13				
W15				
W17				
W18				
W20	DGND	0		Digital 3.3/2.5/1.2 V ground
W21				
Y13				
Y14				
Y17				
Y19				
Y20				
Y21				
Y22				
AA12				
AA13				
AA17				
AA20				
AA21				
AA22				
AA23				
AB11				
AB12				

Table 4. Power/ground pins (continued)

Pin	Assignment	Voltage	Type	Description
AB13	DGND	0		Digital 3.3/2.5/1.2 V ground
AB21				
AB22				
AB23				
AC10				
AC11				
AC12				
AC22				
AH8				
AH17				
AH18				
AJ8				
AJ15				
AJ16				
AJ17				
AK17				

Table 4. Power/ground pins (continued)

Pin	Assignment	Voltage	Type	Description
Digital 1.2 V				
F7	VDD1V2	1.2	Digital	Digital power 1.2 V core power
G6				
G7				
G27				
H28				
H29				
M14				
M15				
M18				
M19				
N15				
N16				
N17				
N18				
P12				
P16				
P17				
P21				
R12				
R13				
R20				
R21				
R28				
T13				
T14				
U13				
U14				
V12				
V13				
V16				
V20				

Table 4. Power/ground pins (continued)

Pin	Assignment	Voltage	Type	Description
V21	VDD1V2	1.2	Digital	Digital 1.2 V core power
W12				
W16				
Y15				
Y16				
Y18				
AA14				
AA15				
AA16				
AA18				
AA19				
AB20				
AC21				
AD5				
AE4				
AE5				
AE6				
AF6				

6.2 System

Table 5. System pins

Pin	Assignment	I/O	Voltage	Description	Comments
B32	NOTRESETIN	I	3.3	System reset-in	System reset
A29	WDOGRSTOUT	O	3.3	System reset-out (from System reset-in or Internal watchdog timer reset)	
B29	NOTASEBRK	I/O	3.3	ST40 debugger breakpoint	CPUs debug
B31	TRIGGERIN	I	3.3	ST231 debugger controller in	
C29	TRIGGEROUT	O	3.3	ST231 debugger controller out	
A32	SYSITRQ[0]	I/O	3.3	Interrupt line	Interrupts
A31	SYSITRQ[1]				
B30	SYSITRQ[2]				
A30	SYSITRQ[3]				
C31	NMI	I	3.3	Nonmaskable interrupt	
C30	SYSCLKINALT	I	3.3	2nd system alternate clock (30 MHz) with external VCXO	
C32	SYSCLKOUT	O	3.3	Programmable output clock for debug	
AJ22	SYSCLKIN	I	2.5	30 MHz oscillator (USB/SATA) with internal VCXO	
AH22	SYSCLKOSC	O	2.5		
F26	GND_SENSE	A	-	Ground voltage sense	
G26	VDD_SENSE	A	-	Voltage sense	

6.3 JTAG

Table 6. JTAG pins

Pin	Assignment	I/O	Voltage	Description	Comments
B2	TDI	I	3.3	CPUs debug port and TAP data input	No internal pull-up or pull-down resistors
C2	TMS	I	3.3	CPUs debug port and TAP mode select	
C1	TCK	I	3.3	CPUs debug port and TAP clock	
A1	NOTTRST	I	3.3	CPUs debug port and TAP logic reset	
B1	TDO	O	3.3	CPUs debug port and TAP data output	

6.4 Transport interface

This transport interface is an alternative to the PIO bits. By default, the PIO is bypassed. To enable the transport interface, the PIO setting must be done at boot (refer to *Chapter 19: Alternate functions on PIO on page 263* for programming details).

Note: The parallel/serial mode selection is done by selecting the TSmerger channel.

Table 7. Parallel mode transport pins

Pad	I/O	Voltage	PIO	Description	Comments
TSIN0BYTECLK	I/O	3.3	PIO13[5]	TSIN0 control signals	
TSIN0BYTECLKVALID	I/O	3.3	PIO13[6]		
TSIN0ERROR	I/O	3.3	PIO13[7]		
TSIN0PACKETCLK	I/O	3.3	PIO14[0]		
TSIN0DATA[0]	I/O	3.3	PIO14[7]	TSIN0 parallel data	
TSIN0DATA[1]			PIO14[6]		
TSIN0DATA[2]			PIO14[5]		
TSIN0DATA[3]			PIO14[4]		
TSIN0DATA[4]			PIO14[3]		
TSIN0DATA[5]			PIO14[2]		
TSIN0DATA[6]			PIO14[1]		
TSIN0DATA[7]			PIO13[4]		
TSIN1BYTECLK	I	3.3	PIO12[1]/ PIO15[1]	TSIN1 control signals	
TSIN1BYTECLKVALID	I	3.3	PIO12[2]/ PIO15[2]		
TSIN1ERROR	I	3.3	PIO12[3]/ PIO15[3]		
TSIN1PACKETCLK	I	3.3	PIO12[4]/ PIO15[0]		
TSIN1DATA[0]	I	3.3	PIO13[3]	TSIN1 parallel data	
TSIN1DATA[1]			PIO13[2]		
TSIN1DATA[2]			PIO13[1]		
TSIN1DATA[3]			PIO13[0]		
TSIN1DATA[4]			PIO12[7]		
TSIN1DATA[5]			PIO12[6]		
TSIN1DATA[6]			PIO12[5]		
TSIN1DATA[7]			PIO12[0]/ PIO15[4]		

Table 7. Parallel mode transport pins (continued)

Pad	I/O	Voltage	PIO	Description	Comments
TSIN2BYTECLK	I	3.3	PIO6[1], PIO14[2]	TSIN2 control signals	
TSIN2BYTECLKVALID	I	3.3	PIO6[2], PIO14[3]		
TSIN2ERROR	I	3.3	PIO6[3], PIO14[4]		
TSIN2PACKETCLK	I	3.3	PIO6[4], PIO14[5]		
TSIN2DATA[0]	I	3.3	PIO7[3]	TSIN2 parallel data	
TSIN2DATA[1]			PIO7[2]		
TSIN2DATA[2]			PIO7[1]		
TSIN2DATA[3]			PIO7[0]		
TSIN2DATA[4]			PIO6[7]		
TSIN2DATA[5]			PIO6[6]		
TSIN2DATA[6]			PIO6[5]		
TSIN2DATA[7]			PIO6[0], PIO14[1]		
TSIN3BYTECLK	I	3.3	PIO12[6]	TSIN3 control signals	
TSIN3BYTECLKVALID	I	3.3	PIO12[7]		
TSIN3ERROR	I	3.3	PIO13[0]		
TSIN3PACKETCLK	I	3.3	PIO13[1]		

Table 8. Serial mode transport pins

Pad	I/O	Voltage	PIO	Description	Comments
TSIN0SER/DATA[7]	I	3.3	PIO13[4]	TSIN0 serial data	
TSIN1SER/DATA[7]	I	3.3	PIO12[0]/ PIO15[4]	TSIN1 serial data	
TSIN2SER/DATA[7]	I	3.3	PIO6[0]/ PIO14[1]	TSIN2 serial data	
TSIN3SER/DATA[7	I	3.3	PIO12[5]	TSIN3 serial data	
TSOUTSER/DATA[7]	O	3.3	PIO12[0]	TSOUT serial data	

Table 9. 1394OUT mode transport pins

Signal	I/O	Voltage	PIO	Description	Comments
TSOUTBYTECLK	O	3.3	PIO12[1]	TSOUT control signals	
TSOUTBYTECLKVALID	O	3.3	PIO12[2]		
TSOUTERROR	O	3.3	PIO12[3]		
TSOUTPACKETCLK	O	3.3	PIO12[4]		
TSOUTDATA[0]	O	3.3	PIO13[3]	TSOUT parallel data	
TSOUTDATA[1]			PIO13[2]		
TSOUTDATA[2]			PIO13[1]		
TSOUTDATA[3]			PIO13[0]		
TSOUTDATA[4]			PIO12[7]		
TSOUTDATA[5]			PIO12[6]		
TSOUTDATA[6]			PIO12[5]		

6.5 Display analog output interface

Table 10. Display analog output pins

Pin	Assignment	I/O	Voltage (a)	Description	Comments
AM31	VIDA0_ROUT	O	-	Analog main display - red output	Connect an external 140 Ω 1% resistor between these pins and analog ground.
AM32	VIDA0_GOUT	O	-	Analog main display -green output	
AM30	VIDA0_BOUT	O	-	Analog main display - blue output	
AL29	VIDA0_REXT	-	-	VDAC0 external resistor interface	Connect an external 7.81 kΩ 1% resistor between each of these pins
AJ32	VIDA1_COUT	O	-	Analog auxiliary display - chrominance output	Connect an external 140 Ω 1% resistor between these pins and analog ground.
AH31	VIDA1_CVOUT	O	-	Analog auxiliary display - CVBS output	
AG30	VIDA1_YOUT	O	-	Analog auxiliary display - luminance output	
AK32	VIDA1_REXT	-	-	VDAC1 external resistor interface	Connect an external 7.81 kΩ 1% resistor between each of these pins
AK28	VIDA0_MASSQUIET	-	-	Analog ground connection	It must be connected to noiseless board analog ground because it is sensitive pin for DAC output signal performance.
AL31	VIDA0_IDUMP	O	-	Current return path for the DAC output	It is tied to PCB ground plane.

Table 10. Display analog output pins (continued)

Pin	Assignment	I/O	Voltage (a)	Description	Comments
AL32	VIDA1_MASSQUIET	-	-	Analog ground connection	It must be connected to noiseless board analog ground because it is sensitive pin for DAC output signal performance
AH30	VIDA1_IDUMP	O	-	Current return path for the DAC output	It is tied to PCB ground plane

a. For voltage values, please refer *Section 17.4: Triple HD video DACs on page 244*.

6.6 HDMI interface

Table 11. HDMI pins

Pin	Assignment	I/O	Voltage[(a)]	Description	Comments
AK25	TMDSTXCP	O	-	TMDS Control plus	
AM25	TMDSTXCN	O	-	TMDS Control minus	
AK26	TMDSTX0P	O	-	TMDS Data0 plus	
AJ26	TMDSTX0N	O	-	TMDS Data0 minus	
AJ27	TMDSTX1P	O	-	TMDS Data1 plus	
AH26	TMDSTX1N	O	-	TMDS Data1 minus	
AJ28	TMDSTX2P	O	-	TMDS Data2 plus	
AH27	TMDSTX2N	O	-	TMDS Data2 minus	
AL25	TMDSREF	-	-	TMDS voltage reference	Used by compensation cell to determine the current drive of output buffers. Pulled up externally to 3.3 V using a 50 Ω resistor.
AH28	HDMI_CEC	I/O	-	HDMI CEC line	

a. For voltage values, please contact your local ST representative to provide you specific internal document.

HDMI pins as PIO alternates

Assignment	I/O	Voltage[(a)]	Description	Comments
HDMI_PLUGIN	I	-	HDMI HOT PLUG detection input	PIO9[7]

6.7 Audio digital interface

For audio digital pins, refer to PIO10 and PIO11 alternate functions in *Alternate functions on PIO*.

6.8 Audio analog interface

Table 12. Audio analog pins

Pin	Assignment	I/O	Voltage (a)	Description	Comments
AM17	AUDA_LEFTOUTP	O	-	DAC left channel positive differential current output	
AL17	AUDA_LEFTOUTN	O	-	DAC left channel negative differential current output	
AL15	AUDA_RIGHTOUTP	O	-	DAC right channel positive differential current output	
AK15	AUDA_RIGHTOUTN	O	-	DAC right channel negative differential current output	
AM16	AUDA_VBGOUT	O		DAC output bandgap voltage	
AL16	AUDA_IREF	-	-	DAC output reference current	Connect an external 575 Ω 1% resistor to AUDA_AGND2V5

a. For voltage values, please refer *Section 17.3: Audio DAC on page 243*.

6.9 Serial ATA interface

Table 13. SATA pins

Pin	Assignment	I/O	Voltage (a)	Description	Comments
AJ20	SATATXP	O	-	SATA transmit plus	
AK18	-	-	-	No connect	
AH20	SATATXN	O	-	SATA transmit minus	
AK19	-	-	-	No connect	
AH21	SATARXP	I	-	SATA receive plus	
AJ19	-	-	-	No connect	
AG21	SATARXN	I	-	SATA receive minus	
AL18	-	-	-	No connect	
AH19	SATAREF	I/O	-	SATA external reference	It is an external 475 Ω resistor with the other end connected to AF18 pin (SATAVDD_PLL).

a. For voltage values, please refer *Section 17.7: SATA PHY electrical characteristics on page 248*.

6.10 FDMA interface

Table 14. FDMA pins

Pin	Assignment	I/O	Voltage	Description	Comments
K29	FDMAREQ[0]	I/O	3.3	FDMA request	
K30	FDMAREQ[1]	I/O	3.3	FDMA request	
K28	FDMAREQ[2]	I/O	3.3	FDMA request	
J27	FDMAREQ[3]	I/O	3.3	FDMA request	

6.11 Programmable inputs/outputs

Note: All PIO pins are rated at 4 mA sink/source.

Table 15. PIO pins

Pin	Assignment	I/O	Voltage	Description
AE31	PIO0[0]	I/O	3.3	Programmable input/output bank0
AE32	PIO0[1]			
AE30	PIO0[2]			
AD29	PIO0[3]			
AD31	PIO0[4]			
AD30	PIO0[5]			
AC29	PIO0[6]			
AC30	PIO0[7]			
AC28	PIO1[0]	I/O	3.3	Programmable input/output bank1
AB27	PIO1[1]			
AB29	PIO1[2]			
AB28	PIO1[3]			
AA27	PIO1[4]			
AA28	PIO1[5]			
Y27	PIO1[6]			
Y29	PIO1[7]			
Y28	PIO2[0]	I/O	3.3	Programmable input/output bank2
W29	PIO2[1]			
W30	PIO2[2]			
W28	PIO2[3]			
V29	PIO2[4]			
V31	PIO2[5]			
V30	PIO2[6]			
U31	PIO2[7]			
AF29	PIO3[0]	I/O	3.3	Programmable input/output bank3
AG28	PIO3[1]			
AF30	PIO3[2]			
AF28	PIO3[3]			
T30	PIO3[4]			
R29	PIO3[5]			
R31	PIO3[6]			
R30	PIO3[7]			

Table 15. PIO pins (continued)

Pin	Assignment	I/O	Voltage	Description
P29	PIO4[0]	I/O	3.3	Programmable input/output bank4
P30	PIO4[1]			
P28	PIO4[2]			
N27	PIO4[3]			
N29	PIO4[4]			
N28	PIO4[5]			
M27	PIO4[6]			
M28	PIO4[7]			
L27	PIO5[0]	I/O	3.3	Programmable input/output bank5
L29	PIO5[1]			
L28	PIO5[2]			
K27	PIO5[3]			
U30	PIO5[4]			
U32	PIO5[5]			
T31	PIO5[6]			
T32	PIO5[7]			
E4	PIO6[0]	I/O	3.3	Programmable input/output bank6
E2	PIO6[1]			
E3	PIO6[2]			
F5	PIO6[3]			
F3	PIO6[4]			
F4	PIO6[5]			
G4	PIO6[6]			
G3	PIO6[7]			
D1	PIO7[0]	I/O	3.3	Programmable input/output bank7
D2	PIO7[1]			
D3	PIO7[2]			
G5	PIO7[3]			
AK9	PIO7[4]			
AK8	PIO7[5]			
AJ6	PIO7[6]			
AH7	PIO7[7]			

Table 15. PIO pins (continued)

Pin	Assignment	I/O	Voltage	Description
AL8	PIO8[0]	I/O	3.3	Programmable input/output bank8
AK6	PIO8[1]			
AK7	PIO8[2]			
AF9	PIO8[3]			
AG8	PIO8[4]			
AH10	PIO8[5]			
AJ9	PIO8[6]			
AL9	PIO8[7]			
AK10	PIO9[0]	I/O	3.3	Programmable input/output bank9
AM8	PIO9[1]			
AJ7	PIO9[2]			
AG7	PIO9[3]			
AF7	PIO9[4]			
AH11	PIO9[5]			
AF8	PIO9[6]			
J29	PIO9[7]			
AF14	PIO10[0]	I/O	3.3	Programmable input/output bank10
AH14	PIO10[1]			
AJ14	PIO10[2]			
AK14	PIO10[3]			
AG13	PIO10[4]			
AJ10	PIO10[5]			
AJ11	PIO10[6]			
AG9	PIO10[7]			
AJ13	PIO11[0]	I/O	3.3	Programmable input/output bank11
AH13	PIO11[1]			
G30	PIO11[2]			
G29	PIO11[3]			
F27	PIO11[4]			
F29	PIO11[5]			
F28	PIO11[6]			
E28	PIO11[7]			

Table 15. PIO pins (continued)

Pin	Assignment	I/O	Voltage	Description
K5	PIO12[0]	I/O	3.3	Programmable input/output bank12
L4	PIO12[1]			
K3	PIO12[2]			
L6	PIO12[3]			
K4	PIO12[4]			
J3	PIO12[5]			
J2	PIO12[6]			
K6	PIO12[7]			
H3	PIO13[0]	I/O	3.3	Programmable input/output bank13
J4	PIO13[1]			
H1	PIO13[2]			
H2	PIO13[3]			
P5	PIO13[4]			
R2	PIO135]			
P3	PIO13[6]			
R4	PIO13[7]			
P4	PIO14[0]	I/O	3.3	Programmable input/output bank14
N5	PIO14[1]			
N4	PIO14[2]			
P6	PIO14[3]			
M5	PIO14[4]			
N6	PIO14[5]			
M6	PIO14[6]			
L5	PIO14[7]			
AM4	PIO15[0]	I/O	3.3	Programmable input/output bank15
AL4	PIO15[1]			
AJ5	PIO15[2]			
AL5	PIO15[3]			
AK5	PIO15[4]			
AH6	PIO15[5]			
H31	PIO15[6]			
H32	PIO15[7]			

Table 15. PIO pins (continued)

Pin	Assignment	I/O	Voltage	Description
E30	PIO16[0]	I/O	3.3	Programmable input/output bank16
E29	PIO16[1]			
D29	PIO16[2]			
D31	PIO16[3]			
D30	PIO16[4]			
J28	PIO16[5]			
H30	PIO16[6]			
G28	PIO16[7]			

6.12 External memory interface (EMI)

Note: The various configurations of the EMI (SRAM, FLASH, PCI) are shown in Section 7.4.

Table 16. EMI pins

Pin	Assignment	I/O	Voltage	Description	Comments
R3	NOTEMICSA	I/O	3.3	Peripheral chip select A	
T2	NOTEMICSB	I/O	3.3	Peripheral chip select B	
T1	NOTEMICSC	I/O	3.3	Peripheral chip select C	
U1	NOTEMICSD	I/O	3.3	Peripheral chip select D	
T3	NOTEMICSE	I/O	3.3	Peripheral chip select E	
AC5	NOTEMIBE[0]	I/O	3.3	External device databus byte enable	
AE1	NOTEMIBE[1]				
Y5	NOTEMIOE	O2	3.3	External device output enable	
AG4	NOTEMILBA	I/O	3.3	Flash device load burst address	
U3	NOTEMIBAA	I/O	3.3	Flash burst address advanced	
V3	EMITREADYORWAIT	I/O	3.3	External memory device target ready indicator	
AA6	EMIRDNOTWR	I/O	3.3	External read/write access indicator. Common to all devices.	

Table 16. EMI pins (continued)

Pin	Assignment	I/O	Voltage	Description	Comments
AM1	EMIDATA[0]	I/O	3.3	External common data bus	
AK2	EMIDATA[1]				
AF4	EMIDATA[2]				
AL2	EMIDATA[3]				
AK1	EMIDATA[4]				
AK4	EMIDATA[5]				
AH4	EMIDATA[6]				
AK3	EMIDATA[7]				
AL1	EMIDATA[8]				
AM3	EMIDATA[9]				
AL3	EMIDATA[10]				
AH3	EMIDATA[11]				
AM2	EMIDATA[12]				
AH5	EMIDATA[13]				
AJ3	EMIDATA[14]				
AJ2	EMIDATA[15]				

Table 16. EMI pins (continued)

Pin	Assignment	I/O	Voltage	Description	Comments
W4	EMIADDR[1]				
V4	EMIADDR[2]				
V2	EMIADDR[3]				
V5	EMIADDR[4]				
V6	EMIADDR[5]				
W6	EMIADDR[6]				
W3	EMIADDR[7]				
AB4	EMIADDR[8]				
AC3	EMIADDR[9]				
Y4	EMIADDR[10]				
Y6	EMIADDR[11]				
W5	EMIADDR[12]				
AA5	EMIADDR[13]	O	3.3	External common address bus	23-bit address[a]
AB6	EMIADDR[14]				
AE2	EMIADDR[15]				
AB5	EMIADDR[16]				
AC6	EMIADDR[17]				
AC4	EMIADDR[18]				
AG6	EMIADDR[19]				
AD4	EMIADDR[20]				
AD2	EMIADDR[21]				
AD3	EMIADDR[22]				
AJ4	EMIADDR[23]				
AF5	EMIADDR[24]				
AF3	EMIADDR[25]				
U2	EMIFLASHCLK	I/O	3.3	Flash clock	
AD6	EMIBUSREQ	I/O	3.3	Bus access request	For master/slave configuration
AE3	EMIBUSGNT	I/O	3.3	Bus access grant	
AG5	NANDWAIT		3.3		

a. No pull-up. External resistors to define mode at boot.

Table 17. EMI pins as PIO alternates

Signal	I/O	Voltage	Description	Comments
EMI_SS_BUS_FREE_ACCESSPEND/EMI_SS_BUS_FREE_OUT	I	3.3	Access Pending Flag	PIO15[2]
SPIBOOT_DATA_IN	I	3.3	SPI boot data in	PIO15[3]

Table 17. EMI pins as PIO alternates (continued)

Signal	I/O	Voltage	Description	Comments
SPIBOOT_DATA_OUT	O	3.3	SPI boot data out	PIO15[1]
SPIBOOT_CLOCK	O	3.3	SPI boot clock	PIO15[0]
SPIBOOT_CS	O	3.3	SPI boot chip select	PIO15[2]

Table 18. PCI pins as PIO alternates

Assignment	I/O	Voltage	Description	Comments
PCI_LOCK_IN	I	3.3	PCI lock function	PIO7[0], PIO15[5]
PCI_INT_FROM_DEVICE[0]	I	3.3	PCI interrupt input (when host)	PIO6[0], PIO15[3]
PCI_INT_FROM_DEVICE[1]	I	3.3	PCI interrupt input (when host)	PIO6[1]
PCI_INT_FROM_DEVICE[2]	I	3.3	PCI interrupt input (when host)	PIO6[2]
PCI_INT_TO_HOST	O	3.3	PCI interrupt output (when device)	PIO6[0], PIO15[3]
PCI_RESETN_FROM_HOST_TO_DEVICE	I	3.3	PCI reset input (when host)	PIO15[7]
PCI_SYSTEM_ERROR	O	3.3	PCI error flag	PIO15[4]
PCI_PME_IN	I	3.3	PCI pme function	PIO15[6]
PCI_BUS_GNT[1]	O	3.3	Bus access grant	PIO7[1]
PCI_BUS_GNT[2]	O	3.3	Bus access grant	PIO7[2]
PCI_BUS_REQ[1]	I	3.3	Bus access req	PIO6[5]
PCI_BUS_REQ[2]	I	3.3	Bus access req	PIO6[6]

6.13 Local memory interface

Table 19. LMI pins

Pin	Assignment	I/O	Voltage	Description	Comments
B17	LMICLK[0]	O	1.8	Clock to DDR0	
A17	NOTLMICLK[0]	O	1.8	Inverted clock to DDR0	
C3	LMICLK[1]	O	1.8	Clock to DDR1	
A2	NOTLMICLK[1]	O	1.8	Inverted clock to DDR1	
B9	NOTLMICS[0]	O	1.8	Chip select0	
D4	NOTLMICS[1]	O	1.8	Chip select1	
D9	NOTLMIRAS	O	1.8	Row address strobe	
C9	NOTLMICAS	O	1.8	Column address strobe	
D23	NOTLMIWE	O	1.8	Write enable	

Table 19. LMI pins (continued)

Pin	Assignment	I/O	Voltage	Description	Comments
G12	LMIADDR[0]	O	1.8	Address	
D22	LMIADDR[1]				
D14	LMIADDR[2]				
E21	LMIADDR[3]				
E13	LMIADDR[4]				
F20	LMIADDR[5]				
C15	LMIADDR[6]				
D19	LMIADDR[7]				
C14	LMIADDR[8]				
C19	LMIADDR[9]				
F22	LMIADDR[10]				
A16	LMIADDR[11]				
C17	LMIADDR[12]				
B16	LMIADDR[13]				

Table 19. LMI pins (continued)

Pin	Assignment	I/O	Voltage	Description	Comments
C18	LMIDATA[0]	I/O	1.8	Bidirectional data bus	
D27	LMIDATA[1]				
B18	LMIDATA[2]				
B28	LMIDATA[3]				
C28	LMIDATA[4]				
D18	LMIDATA[5]				
C27	LMIDATA[6]				
E19	LMIDATA[7]				
G21	LMIDATA[8]				
D26	LMIDATA[9]				
D20	LMIDATA[10]				
C26	LMIDATA[11]				
E26	LMIDATA[12]				
E20	LMIDATA[13]				
C25	LMIDATA[14]				
F21	LMIDATA[15]				
B4	LMIDATA[16]				
E11	LMIDATA[17]				
B3	LMIDATA[18]				
F12	LMIDATA[19]				
E12	LMIDATA[20]				
A3	LMIDATA[21]				
D11	LMIDATA[22]				
C4	LMIDATA[23]				
E6	LMIDATA[24]				
C10	LMIDATA[25]				
D6	LMIDATA[26]				
D10	LMIDATA[27]				
F11	LMIDATA[28]				
F6	LMIDATA[29]				
E10	LMIDATA[30]				
C7	LMIDATA[31]				

Table 19. LMI pins (continued)

Pin	Assignment	I/O	Voltage	Description	Comments
E23	LMIDATAMASK[0]	O	1.8	Data write mask	
D24	LMIDATAMASK[1]				
A8	LMIDATAMASK[2]				
B8	LMIDATAMASK[3]				
E27	LMIVREF[0]	I	1.8	SSTL reference voltage0	
F13	LMIVREF[1]	I	1.8	SSTL reference voltage1	
C23	LMICLKEN[0]	O	1.8	Memory clock enable	
E5	LMICLKEN[1]	O	1.8	Memory clock enable	
E7	ODT[0]	O	1.8	Memory on-die termination	
E22	ODT[1]	O	1.8	Memory on-die termination	
G24	LMI_COMP_REF	A	-	LMI compensation external resistor	
F24	LMI_COMP_GND	A	-	LMI compensation ground	
D15	LMIDUMMY[0]	A	-	LMI pcb track delay estimator	
C16	LMIDUMMY[1]	A	-	LMI pcb track delay estimator	
A25	LMIDQS[0]	I/O	1.8	Write/read data strobe	
C24	LMIDQS[1]				
C5	LMIDQS[2]				
D7	LMIDQS[3]				
B25	LMIDQSN[0]	I/O	1.8	Write/read data strobe	
B24	LMIDQSN[1]				
D5	LMIDQSN[2]				
C8	LMIDQSN[3]				
D13	LMIBA[0]	O	1.8	Bank select	
E14	LMIBA[1]				
B15	LMIBA[2]				

6.14 Ethernet

Note: This Ethernet interface is an alternative of PIO bits. By default, the PIO is selected. To enable the Ethernet interface, the PIO setting must be done at boot (refer to Chapter 19: Alternate functions on PIO on page 263 for programming details).

Table 20. MII interface pin mapping

Pad	I/O	Voltage	PIO mapping	Description	Comments
MIITXCLK	I	3.3	PIO9[2]	Timing reference for ETHMII_TXEN and ETHMII_TXD	
MIITX_EN	O	3.3	PIO8[2]	Indicates that the MAC is presenting nibbles on the MII for transmission	
MIITXD[3]	O	3.3	PIO8[1]	Data signals driven by the MAC	
MIITXD[2]	O	3.3	PIO8[0]		
MIITXD[1]	O	3.3	PIO7[7]		
MIITXD[0]	O	3.3	PIO7[6]		
MIIRXCLK	I	3.3	PIO8[5]	Timing reference for ETHMII_RXDV, ETHMII_RXER, and ETHMII_RXD	
MIIRX_DV	I	3.3	PIO7[4]	Receive data valid	
MIIRX_ER	I	3.3	PIO7[5]	Receive error	
MIIRXD[3]	I	3.3	PIO9[1]	Data signals that transition synchronously with respect to ETHMII_RXCLK	
MIIRXD[2]	I	3.3	PIO9[0]		
MIIRXD[1]	I	3.3	PIO8[7]		
MIIRXD[0]	I	3.3	PIO8[6]		
MIICRS	I	3.3	PIO9[4]	Asserted when either the transmit or receive medium is not idle	
MIICOL	I	3.3	PIO9[3]	Asserted on detection of a collision on the medium	
MIIMDC	O	3.3	PIO8[4]	Timing reference for transfer of information on the ETHMII_MDIO signals	
MIIMDIO	I/O	3.3	PIO8[3]	Management Data input/output signal	
MIIMDINT	I	3.3	PIO9[6]	Management data interrupt from PHY	
MIIPHYCLK	O	3.3	PIO9[5]	PHY clock	

Table 21. RMII interface pin mapping

Assignment	I/O	Voltage	PIO mapping	Description	Comments
RMIITX_EN	O	3.3	PIO8[2]	Indicates that the MAC is presenting nibbles on the MII for transmission	
RMIITXD[1]	O	3.3	PIO7[7]	Data signals driven by the MAC	
RMIITXD[0]	O	3.3	PIO7[6]		
RMIIRXD[1]	I	3.3	PIO8[7]	Data signals received by the MAC	
RMIIRXD[0]	I	3.3	PIO8[6]		
RMIICRS_DV	I	3.3	PIO7[4]	Asserted when either the transmit or receive medium is not idle	

Table 21. RMII interface pin mapping (continued)

Assignment	I/O	Voltage	PIO mapping	Description	Comments
RMIIRX_ER	I	3.3	PIO7[5]		
RMIIMDC	O	3.3	PIO8[4]	Timing reference for transfer of information on the ETHMII_MDIO signals	
RMIIMDIO	I/O	3.3	PIO8[3]	Management Data input/output signal	
RMIIMDINT	I	3.3	PIO9[6]	Management data interrupt from PHY	
RMIIREF_CLK	I/O	3.3	PIO9[5]	Reference clock	

6.15 USB 2.0 interface

Table 22. USB pins

Pin	Assignment	I/O	Voltage	Description	Comments
AK23	USB1DM	I/O	2.5	USB receive minus	
AJ23	USB1DP	I/O	2.5	USB receive plus	
AL24	USB2DM	I/O	2.5	USB receive minus	
AK24	USB2DP	I/O	2.5	USB receive plus	
AG22	REXT			External register	1.5 kΩ resistor

Table 23. USB pin mapping

Mapping	I/O	Voltage	Description	Assignment
USB1_PRT_OVCUR	I	3.3	USB 2.0 interface 1	PIO4[4], PIO12[5]
USB1_PRT_PWR	O	3.3		PIO4[5], PIO12[6]
USB2_PRT_OVCUR	I	3.3	USB 2.0 interface 2	PIO4[6]/PIO14[6]
USB2_PRT_PWR	O	3.3		PIO4[7]/PIO14[7]

Caution: In case of USB signals, the usual naming convention is not used. In order to align with the STi7105 ballout names, this manual mentions two instances of USB as USB1 and USB2 rather than USB0 and USB1. Therefore, in this manual the first instance of USB is USB1 and the second instance is USB2.

6.16 Peripherals

6.16.1 DAA

Table 24. DAA pins

Pin	Assignment	I/O	Voltage	Description	Comments
J31	DAA_C1A	I/O	3.3	DAA differential data[a]	
J30	DAA_C2A	I/O	3.3	DAA differential data[b]	

a. ISO-Link capacitors C1 and C2, (33 pF) should be as close to the line-side device as possible.

b. After satisfying the above, C1 and C2 should be as close to the embedded system-side DAA module as possible and no further than 6 inches away.

6.16.2 Asynchronous serial controller (ASC)

Table 25. ASC / SCIF pins

Assignment	I/O	Voltage	Description	Comments
ASC0				
UART0_RXD	I	3.3	ASC 0 receive signal	PIO0[1]
UART0_TXD	O	3.3	ASC 0 transmit signal	PIO0[0]
UART0_CTS	I	3.3	ASC 0 clear to send signal	PIO0[4]
UART0_RTS	O	3.3	ASC 0 request to send signal	PIO0[3]
UART0_NOT_OE	O	3.3		PIO0[2]
ASC1				
UART1_RXD	I	3.3	ASC 1 receive signal	PIO1[1]
UART1_TXD	O	3.3	ASC 1 transmit signal	PIO1[0]
UART1_CTS	I	3.3	ASC 1 clear to send signal	PIO1[4]
UART1_RTS	O	3.3	ASC 1 request to send signal	PIO1[3]
ASC2				
UART2_RXD	I	3.3	ASC 2 receive signal	PIO12[1], PIO4[1]
UART2_TXD	O	3.3	ASC 2 transmit signal	PIO12[0], PIO4[0]
UART2_CTS	I	3.3	ASC 2 clear to send signal	PIO12[2], PIO4[2]
UART2_RTS	O	3.3	ASC 2 request to send signal	PIO12[3], PIO4[3]
ASC3				
UART3_RXD	I	3.3	ASC 3 receive signal	PIO5[1]
UART3_TXD	O	3.3	ASC 3 transmit signal	PIO5[0]

Table 25. ASC / SCIF pins (continued)

Assignment	I/O	Voltage	Description	Comments
UART3_CTS	I	3.3	ASC 3 clear to send signal	PIO5[3]
UART3_RTS	O	3.3	ASC 3 request to send signal	PIO5[2]

6.16.3 Infrared transmitter/receiver

Table 26. Infrared transmitter/receiver pins

Assignment	I/O	Voltage	Description	Comments
IRB_IR_IN	I	3.3	IR data input	PIO3[0]
IRB_UHF_IN	I	3.3	UHF data input	PIO3[1]
IRB_IR_DATAOUT	O	3.3	IR data output	PIO3[2]
IRB_IR_DATAOUT_OD	O	3.3	IR data output. It is open drain.	PIO3[3]

6.16.4 Modem analog front-end interface (MAFE)

Table 27. MAFE pins

Assignment	I/O	Voltage	Description	Comments
MAFE_HC1	O	3.3	Indicates a control/status exchange	PIO1[2]
MAFE_DOUT	O	3.3	Line for serially transmitting samples	PIO1[3]
MAFE_DIN	I	3.3	Line for serially receiving samples	PIO1[0]
MAFE_SCLK	I	3.3	Modem system clock	PIO1[1]
MAFE_FS	I	3.3	Start of a sampling period latched on falling edges of SCLK	PIO1[5]

6.16.5 Pulse width modulator (PWM)

Table 28. PWM pins

Assignment	I/O	Voltage	Description	Comments
PWM 0				
PWM_OUT0	O	3.3	PWM 0	PIO13[0], PIO4[4]
PWM_CAPTURE_IN0	I			PIO4[3]
PWM 1				
PWM_OUT1	O	3.3	PWM 1	PIO13[1], PIO4[5]
PWM_CAPTURE_IN1	I	3.3		PIO4[7]
PWM_COMPARE_OUT1	O	3.3		PIO4[6]

6.16.6 Smartcard

Table 29. Smartcard pins

Assignment	I/O	Voltage	Description	Comments
Smartcard 0				
SC0_EXTCLKIN	I	3.3	External clock	PIO0[2]
SC0_CLKOUT	O	3.3	Clock for smartcard from 100 MHz system clock	PIO0[3]
SC0_DATAOUT	O	3.3	Serial data output	PIO0[0]
SC0_DATAIN	I	3.3	Serial data input	PIO0[1]
SC0_RESET	O	3.3	Serial data reset	PIO0[4]
SC0_COND_VCC	O	3.3	VCC control flag	PIO0[5]
SC0_COND_VPP	O	3.3	VPP control flag	PIO0[6]
SCO_DETECT	I	3.3	Detection flag	PIO0[7]
Smartcard 1				
SC1_EXTCLKIN	I	3.3	External clock	PIO1[2]
SC1_CLKOUT	O	3.3	Clock for smartcard from 100MHz system clock	PIO1[3]
SC1_DATAOUT	O	3.3	Serial data output	PIO1[0]
SC1_DATAIN	I	3.3	Serial data input	PIO1[1]
SC1_RESET	O	3.3	Serial data reset	PIO1[4]
SC1_COND_VCC	O	3.3	VCC control flag	PIO1[5]
SC1_COND_VPP	O	3.3	VPP control flag	PIO1[6]
SC1_DETECT	I	3.3	Detection flag	PIO1[7]

6.16.7 Synchronous serial controller (SSC)

Table 30. SSC pins

Assignment	I/O	Voltage	Description	Comments
SSC 0				
SSC0_SCL	I/O	3.3	SSC 0 serial clock	PIO2[2]
SSC0_MTSR/SSC0_MRST	I/O	3.3	SSC 0 data: master transmit, slave receive/master receive, slave transmit (half duplex mode for example I^2C)	PIO2[3]
SSC0_MRST	I/O	3.3	SSC 0 data: master receive, slave transmit (full duplex mode)	PIO2[4]
SSC 1				
SSC1_SCL	I/O	3.3	SSC 1 serial clock	PIO2[5]

Table 30. SSC pins (continued)

Assignment	I/O	Voltage	Description	Comments
SSC1_MTSR/SSC1_MRST	I/O	3.3	SSC 1 data: master transmit, slave receive/master receive, slave transmit (half duplex mode for example I^2C)	PIO2[6]
SSC1_MRST	I/O	3.3	SSC 1 data: master receive, slave transmit (full duplex mode)	PIO2[7]
SSC 2				
SSC2_SCL	I/O	3.3	SSC 2 serial clock	PIO3[4], PIO12[0], PIO13[4]
SSC2_MTSR/SSC2_MRST	I/O	3.3	SSC 2 data: master transmit, slave receive/master receive, slave transmit (half duplex mode for example I^2C)	PIO2[0], PIO3[5], PIO12[1], PIO13[5]
SSC 3				
SSC3_SCL	I/O	3.3	SSC 3 serial clock	PIO3[6], PIO13[2], PIO13[6]
SSC3_MTSR/SSC3_MRST	I/O	3.3	SSC3 data: master transmit, slave receive/master receive, slave transmit (half duplex mode for example I^2C)	PIO2[1], PIO3[7], PIO13[3], PIO13[7]

6.16.8 Key Scanner (KS)

Table 31. KS pins

Assignment	I/O	Voltage	Description	Comments
KEY_SCAN_OUT[0]	O	3.3	Key Scanner outputs	PIO7[0], PIO5[0]
KEY_SCAN_OUT[1]				PIO7[1], PIO5[1]
KEY_SCAN_OUT[2]				PIO7[2], PIO5[2]
KEY_SCAN_OUT[3]				PIO7[3], PIO5[3]
KEY_SCAN_IN[0]	I	3.3	Key Scanner inputs	PIO5[4]
KEY_SCAN_IN[1]				PIO5[5]
KEY_SCAN_IN[2]				PIO5[6]
KEY_SCAN_IN[3]				PIO5[7]

6.17 Pad reset conditions

Table 32 describes the pad reset conditions.

Table 32. Pad reset conditions

Ball/Signal name	Functional direction	Pad reset conditions		
		I/O	Reset value	Pull up/pull down
System				
SYSCLKIN	I	–	1	–
SYSCLKOSC	I/O	–	0	–
NOTASEBRK	I/O	I	1	Pull-up
TRIGGERIN	I	I	0	Pull-down
TRIGGEROUT	O	O	0	Pull-down
SYSITRQ[3:0]	I/O	I	0	Pull-down
NMI	I	I	0	Pull-down
WDOGRSTOUT	O	O	1	Pull-down
SYSCLKOUT	O	I	1	Pull-down
SYSCLKINALT	I	I	0	Pull-down
FDMAREQ[3:0]	I/O	I	0	–
NOTRESETIN	I	I	1	–
JTAG				
TDI	I	I	0	Pull-up
TMS	I	I	0	Pull-up
TCK	I	I	0	Pull-up
NOTTRST	I	I	1	Pull-up
TDO	O	O	1	–
EMI				
NOTEMICSA	I/O	I	1	Pull-up
NOTEMICSB	I/O	I	1	Pull-up
NOTEMICSC	I/O	I	1	Pull-up
NOTEMICSD	I/O	I	1	Pull-up
NOTEMICSE	I/O	I	1	Pull-up
NOTEMIBE[1:0]	I/O	I	1	Pull-up
NOTEMIOE	O	O	1	Pull-up
NOTEMILBA	I/O	I	1	Pull-up
NOTEMIBAA	I/O	I	1	Pull-up
EMIREADYORWAIT	I/O	I	0	Pull-down
NANDWAIT	I	I	1	Pull-up
EMIRDNOTWR	I/O	I	1	Pull-up

Table 32. Pad reset conditions (continued)

Ball/Signal name	Functional direction	Pad reset conditions		
		I/O	Reset value	Pull up/pull down
EMIDATA[15:0]	I/O	I	0	Pull-down
EMIADDR[16:1]	I/O	I	1	Pull-up
EMIADDR[25:17]	I/O	I	1	Pull-up
EMIFLASHCLK	I/O	I	0	Pull-down
EMIBUSREQ	I/O	I	0	Pull-down
EMIBUSGNT	I/O	O	0	Pull-down
PIO				
PIO0[7:0]	I/O	I	1	Weak pull-up
PIO1[7:0]	I/O	I	1	Weak pull-up
PIO2[7:0]	I/O	I	1	Weak pull-up
PIO3[7:0]	I/O	I	1	Weak pull-up
PIO4[7:0]	I/O	I	1	Weak pull-up
PIO5[7:0]	I/O	I	1	Weak pull-up
PIO6[7:0]	I/O	I	1	Weak pull-up
PIO7[7:4]	I/O	I	x	Weak pull-up
PIO7[3:0]	I/O	I	1	Weak pull-up
PIO8[7:6]	I/O	I	x	Weak pull-up
PIO8[5]	I/O	I	1	Weak pull-up
PIO8[4:0]	I/O	I	x	Weak pull-up
PIO9[7]	I/O	I	0	Weak pull-up
PIO9[6]	I/O	I	x	Weak pull-up
PIO9[5:2]	I/O	I	1	Weak pull-up
PIO9[1:0]	I/O	I	x	Weak pull-up
PIO10[7:0]	I/O	I	1	Weak pull-up
PIO11[7:0]	I/O	I	1	Weak pull-up
PIO12[7:0]	I/O	I	1	Weak pull-up
PIO13[7:0]	I/O	I	1	Weak pull-up
PIO14[7:0]	I/O	I	1	Weak pull-up
PIO15[3:0]	I/O	O	0	–
PIO15[7:6]	I/O	I	0	Weak pull-up
PIO15[5:4]	I/O	I	1	Weak pull-up

Table 32. Pad reset conditions (continued)

Ball/Signal name	Functional direction	Pad reset conditions		
		I/O	Reset value	Pull up/pull down
PIO16[7:5]	I/O	I	1	–
PIO16[4:0]	I/O	I	x	Weak pull-up

7 Basic chip operating modes and multiplexing scenarios

The STi7105 has one basic chip operating mode, however, other chip operating modes are supported through pad multiplexing.

Following interfaces include ball multiplexing:

- Ethernet interface, which can support MII and ReduceMII(RMII)
- External memory interface (EMI), valid in several operating modes, attached to various types of devices

7.1 Transport interfaces multiplexing

The PIO multiplexing used for transport interfaces can be configured in the following ways:

- serial transport stream inputs: up to four serial IN (mapping details in *Table 33)*
- parallel transport stream inputs/output: one parallel IN/OUT and two parallel IN (mapping details in *Table 34)*

Table 33. STi7105 Serial Transport Stream inputs mapping

Pin	Parameter	Interface	Details
PIO13[4]	Name	Serial transport stream input 0	TSIN0SER/DATA[7]
	Description		Transport stream0 serial data input
	Direction		I
	Configuration		No configuration is required
PIO13[5]	Name		TSIN0BYTECLK
	Description		Transport stream0 data clock input/output
	Direction		B
	Configuration		For OUTPUT selection: Config register: SYSTEM_CONFIG49[23:0] Config bus: PIO13_ALTFOP[2:0]_MUX_SEL_BUS[5]=0x000 For INPUT selection: No configuration is required
PIO13[6]	Name		TSIN0BYTECLKVALID
	Description		Transport stream0 data valid input
	Direction		I
	Configuration		No configuration is required
PIO13[7]	Name		TSIN0ERROR
	Description		Transport stream0 data error input
	Direction		I
	Configuration		No configuration is required
PIO14[0]	Name		TSIN0PACKETCLK
	Description		Transport stream0 packet clock input
	Direction		I
	Configuration		No configuration is required

Table 33. STi7105 Serial Transport Stream inputs mapping (continued)

Pin	Parameter	Interface	Details
PIO12[0]/ PIO15[4]	Name	Serial transport stream input 1	TSIN1SER/DATA[7]
	Description		Transport stream1 serial data input
	Direction		I
	Configuration		For INPUT selection: Config register: SYSTEM_CONFIG4[31:0] Config bus: when PIO12[0], SYSTEM_CONFIG4[9] = 0 when PIO15[4], SYSTEM_CONFIG4[9] = 1
PIO12[1]/ PIO15[1]	Name		TSIN1BYTECLK
	Description		Transport stream1 data clock input/output
	Direction		I
	Configuration		For INPUT selection: Config register: SYSTEM_CONFIG4[31:0] Config bus: when PIO12[1], SYSTEM_CONFIG4[9] = 0 when PIO15[1], SYSTEM_CONFIG4[9] = 1
PIO12[2]/ PIO15[2]	Name		TSIN1BYTECLKVALID
	Description		Transport stream1 data valid input
	Direction		I
	Configuration		For INPUT selection: Config register: SYSTEM_CONFIG4[31:0] Config bus: when PIO12[2], SYSTEM_CONFIG4[9] = 0 when PIO15[2], SYSTEM_CONFIG4[9] = 1
PIO12[3]/ PIO15[3]	Name		TSIN1ERROR
	Description		Transport stream1 data error input
	Direction		I
	Configuration		For INPUT selection: Config register: SYSTEM_CONFIG4[31:0] Config bus: when PIO12[3], SYSTEM_CONFIG4[9] = 0 when PIO15[3], SYSTEM_CONFIG4[9] = 1
PIO12[4]/ PIO15[0]	Name		TSIN1PACKETCLK
	Description		Transport stream1 packet clock input
	Direction		I
	Configuration		For INPUT selection: Config register: SYSTEM_CONFIG4[31:0] Config bus: when PIO12[4], SYSTEM_CONFIG4[9] = 0 when PIO15[0], SYSTEM_CONFIG4[9] = 1

Table 33. STi7105 Serial Transport Stream inputs mapping (continued)

Pin	Parameter	Interface	Details
PIO14[1]/ PIO6[0]	Name	Serial transport stream input 2	TSIN2SER/DATA[7]
	Description		Transport stream2 serial data input
	Direction		I
	Configuration		For INPUT selection: Config register: SYSTEM_CONFIG4[31:0] Config bus: when PIO6[0], SYSTEM_CONFIG4[10] = 0 when PIO14[1], SYSTEM_CONFIG4[10] = 1
PIO14[2]/ PIO6[1]	Name		TSIN2BYTECLK
	Description		Transport stream2 data clock input
	Direction		I
	Configuration		For INPUT selection: Config register: SYSTEM_CONFIG4[31:0] Config bus: when PIO6[1], SYSTEM_CONFIG4[10] = 0 when PIO14[2], SYSTEM_CONFIG4[10] = 1
PIO14[3]/ PIO6[2]	Name		TSIN2BYTECLKVALID
	Description		Transport stream2 data valid input
	Direction		I
	Configuration		For INPUT selection: Config register: SYSTEM_CONFIG4[31:0] Config bus: when PIO6[2], SYSTEM_CONFIG4[10] = 0 when PIO14[3], SYSTEM_CONFIG4[10] = 1
PIO14[4]/ PIO6[3]	Name		TSIN2ERROR
	Description		Transport stream2 data error input
	Direction		I
	Configuration		For INPUT selection: Config register: SYSTEM_CONFIG4[31:0] Config bus: when PIO6[3], SYSTEM_CONFIG4[10] = 0 when PIO14[4], SYSTEM_CONFIG4[10] = 1
PIO14[5]/ PIO6[4]	Name		TSIN2PACKETCLK
	Description		Transport stream2 packet clock input
	Direction		I
	Configuration		For INPUT selection: Config register: SYSTEM_CONFIG4[31:0] Config bus: when PIO6[4], SYSTEM_CONFIG4[10] = 0 when PIO14[5], SYSTEM_CONFIG4[10] = 1

Table 33. STi7105 Serial Transport Stream inputs mapping (continued)

Pin	Parameter	Interface	Details
PIO12[5]	Name	Serial transport stream Input 3	TSIN3SER/DATA[7]
	Description		Transport stream3 serial data input
	Direction		I
	Configuration		No configuration is required
PIO12[6]	Name		TSIN3BYTECLK
	Description		Transport stream3 data clock input/output
	Direction		I
	Configuration		No configuration is required
PIO12[7]	Name		TSIN3BYTECLKVALID
	Description		Transport STREAM3 data valid input
	Direction		I
	Configuration		No configuration is required
PIO13[0]	Name		TSIN3ERROR
	Description		Transport stream3 data error input
	Direction		I
	Configuration		No configuration is required
PIO13[1]	Name		TSIN3PACKETCLK
	Description		Transport stream3 packet clock input
	Direction		I
	Configuration		No configuration is required

Table 34. STi7105 Parallel Transport Stream inputs/output mapping

Pin	Parameter	Interface	Details
PIO13[4]	Name	Parallel transport stream input 0	TSIN0DATA[7]
	Description		Transport stream0 parallel data input
	Direction		I
	Configuration		No configuration is required
PIO13[5]	Name		TSIN0BYTECLK
	Description		Transport stream0 data clock input/output
	Direction		B
	Configuration		For OUTPUT selection: Config register: SYSTEM_CONFIG49[23:0] Config bus: PIO13_ALTFOP[2:0]_MUX_SEL_BUS[5]=0x000
PIO13[6]	Name		TSIN0BYTECLKVALID
	Description		Transport stream0 data valid input
	Direction		I
	Configuration		No configuration is required
PIO13[7]	Name		TSIN0ERROR
	Description		Transport stream0 data error input
	Direction		I
	Configuration		No configuration is required
PIO14[0]	Name		TSIN0PACKETCLK
	Description		Transport stream0 packet clock input
	Direction		I
	Configuration		No configuration is required

Table 34. STi7105 Parallel Transport Stream inputs/output mapping (continued)

Pin	Parameter	Interface	Details
PIO14[1]	Name	Parallel transport stream input 0	TSIN0DATA[6]
	Description		Transport stream0 parallel data input
	Direction		I
	Configuration		No configuration is required
PIO14[2]	Name		TSIN0DATA[5]
	Description		Transport stream0 parallel data input
	Direction		I
	Configuration		No configuration is required
PIO14[3]	Name		TSIN0DATA[4]
	Description		Transport stream0 parallel data input
	Direction		I
	Configuration		No configuration is required
PIO14[4]	Name		TSIN0DATA[3]
	Description		Transport stream0 parallel data input
	Direction		I
	Configuration		No configuration is required
PIO14[5]	Name		TSIN0DATA[2]
	Description		Transport stream0 parallel data input
	Direction		I
	Configuration		No configuration is required
PIO14[6]	Name		TSIN0DATA[1]
	Description		Transport stream0 parallel data input
	Direction		I
	Configuration		No configuration is required
PIO14[7]	Name		TSIN0DATA[0]
	Description		Transport stream0 parallel data input
	Direction		I
	Configuration		No configuration is required

Table 34. STi7105 Parallel Transport Stream inputs/output mapping (continued)

Pin	Parameter	Interface	Details
PIO12[0]	Name	Parallel transport stream input 1/ output 0	TSIN1DATA[7]/TSOUTDATA[7]
	Description		Transport STREAM1 parallel data input/output
	Direction		B
	Configuration		For OUTPUT selection: Config register: SYSTEM_CONFIG48[23:0] Config bus: PIO12_ALTFOP[2:0]_MUX_SEL_BUS[0]=0x000 PIO12_ALTFOP[2:0]_MUX_SEL_BUS[0]=0x001
PIO12[1]	Name		TSIN1BYTECLK/TSOUTBYTECLK
	Description		Transport stream1 data clock input/output
	Direction		B
	Configuration		For OUTPUT selection: Config register: SYSTEM_CONFIG48[23:0] Config bus: PIO12_ALTFOP[2:0]_MUX_SEL_BUS[1]=0x000 PIO12_ALTFOP[2:0]_MUX_SEL_BUS[1]=0x001
PIO12[2]	Name		TSIN1BYTECLKVALID/TSOUTBYTECLKVALID
	Description		Transport stream1 data valid input/output
	Direction		B
	Configuration		For OUTPUT selection: Config register: SYSTEM_CONFIG48[23:0] Config bus: PIO12_ALTFOP[2:0]_MUX_SEL_BUS[2]=0x000 PIO12_ALTFOP[2:0]_MUX_SEL_BUS[2]=0x001
PIO12[3]	Name		TSIN1ERROR/TSOUTERROR
	Description		Transport stream1 data error input/output
	Direction		B
	Configuration		For OUTPUT selection: Config register: SYSTEM_CONFIG48[23:0] Config bus: PIO12_ALTFOP[2:0]_MUX_SEL_BUS[3]=0x000 PIO12_ALTFOP[2:0]_MUX_SEL_BUS[3]=0x001
PIO12[4]	Name		TSIN1PACKETCLK
	Description		Transport stream1 packet clock input/output
	Direction		I
	Configuration		No configuration is required

Table 34. STi7105 Parallel Transport Stream inputs/output mapping (continued)

Pin	Parameter	Interface	Details
PIO12[5]	Name	Parallel transport stream input 1/ output 0	TSIN1DATA[6]/TSOUTDATA[6]
	Description		Transport stream1 parallel data input/output
	Direction		B
	Configuration		For OUTPUT selection: Config register: SYSTEM_CONFIG48[23:0] Config bus: PIO12_ALTFOP[2:0]_MUX_SEL_BUS[5]=0x000 PIO12_ALTFOP[2:0]_MUX_SEL_BUS[5]=0x001
PIO12[6]	Name		TSIN1DATA[5]/TSOUTDATA[5]
	Description		Transport stream1 serial data input/output
	Direction		B
	Configuration		For OUTPUT selection: Config register: SYSTEM_CONFIG48[23:0] Config bus: PIO12_ALTFOP[2:0]_MUX_SEL_BUS[6]=0x000 PIO12_ALTFOP[2:0]_MUX_SEL_BUS[6]=0x001
PIO12[7]	Name		TSIN1DATA[4]/TSOUTDATA[4]
	Description		Transport stream1 parallel data input/output
	Direction		B
	Configuration		For OUTPUT selection: Config register: SYSTEM_CONFIG48[23:0] Config bus: PIO12_ALTFOP[2:0]_MUX_SEL_BUS[7]=0x000 PIO12_ALTFOP[2:0]_MUX_SEL_BUS[7]=0x001
PIO13[0]	Name		TSIN1DATA[3]/TSOUTDATA[3]
	Description		Transport STREAM1 parallel data input
	Direction		B
	Configuration		For OUTPUT selection: Config register: SYSTEM_CONFIG49[23:0] Config bus: PIO13_ALTFOP[2:0]_MUX_SEL_BUS[0]=0x000 PIO13_ALTFOP[2:0]_MUX_SEL_BUS[0]=0x001
PIO13[1]	Name		TSIN1DATA[2]/TSOUTDATA[2]
	Description		Transport stream1 parallel data input
	Direction		B
	Configuration		For OUTPUT selection: Config register: SYSTEM_CONFIG49[23:0] Config bus: PIO13_ALTFOP[2:0]_MUX_SEL_BUS[1]=0x000 PIO13_ALTFOP[2:0]_MUX_SEL_BUS[1]=0x001

Table 34. STi7105 Parallel Transport Stream inputs/output mapping (continued)

Pin	Parameter	Interface	Details
PIO13[2]	Name		TSIN1DATA[1]/TSOUTDATA[1]
	Description		Transport stream1 parallel data input
	Direction		B
	Configuration		For OUTPUT selection: Config register: SYSTEM_CONFIG49[23:0] Config bus: PIO13_ALTFOP[2:0]_MUX_SEL_BUS[2]=0x000 PIO13_ALTFOP[2:0]_MUX_SEL_BUS[2]=0x001
PIO13[3]	Name		TSIN1DATA[0]/TSOUTDATA[0]
	Description		Transport stream1 parallel data input
	Direction		B
	Configuration		For OUTPUT selection: Config register: SYSTEM_CONFIG49[23:0] Config bus: PIO13_ALTFOP[2:0]_MUX_SEL_BUS[3]=0x000 PIO13_ALTFOP[2:0]_MUX_SEL_BUS[3]=0x001

Table 34. STi7105 Parallel Transport Stream inputs/output mapping (continued)

Pin	Parameter	Interface	Details
PIO14[1]/ PIO6[0]	Name	Parallel transport stream input 2	TSIN2SER/DATA[7]
	Description		Transport stream2 parallel data input
	Direction		I
	Configuration		For INPUT selection: Config register: SYSTEM_CONFIG4[31:0] Config bus: when PIO6[0], SYSTEM_CONFIG4[10] = 0 when PIO14[1], SYSTEM_CONFIG4[10] = 1
PIO14[2]/ PIO6[1]	Name		TSIN2BYTECLK
	Description		Transport stream2 data clock input
	Direction		I
	Configuration		For INPUT selection: Config register: SYSTEM_CONFIG4[31:0] Config bus: when PIO6[1], SYSTEM_CONFIG4[10] = 0 when PIO14[2], SYSTEM_CONFIG4[10] = 1
PIO14[3]/ PIO6[2]	Name		TSIN2BYTECLKVALID
	Description		Transport stream2 data valid input
	Direction		I
	Configuration		For INPUT selection: Config register: SYSTEM_CONFIG4[31:0] Config bus: when PIO6[2], SYSTEM_CONFIG4[10] = 0 when PIO14[3], SYSTEM_CONFIG4[10] = 1
PIO14[4]/ PIO6[3]	Name		TSIN2ERROR
	Description		Transport stream2 data error input
	Direction		I
	Configuration		For INPUT selection: Config register: SYSTEM_CONFIG4[31:0] Config bus: when PIO6[3], SYSTEM_CONFIG4[10] = 0 when PIO14[4], SYSTEM_CONFIG4[10] = 1
PIO14[5]/ PIO6[4]	Name		TSIN2PACKETCLK
	Description		Transport stream2 packet clock input
	Direction		I
	Configuration		For INPUT selection: Config register: SYSTEM_CONFIG4[31:0] Config bus: when PIO6[4], SYSTEM_CONFIG4[10] = 0 when PIO14[5], SYSTEM_CONFIG4[10] = 1

Table 34. STi7105 Parallel Transport Stream inputs/output mapping (continued)

Pin	Parameter	Interface	Details
PIO6[5]	Name	Parallel transport stream input 2	TSIN2DATA[6]
	Description		Transport stream2 parallel data input
	Direction		I
	Configuration		No configuration is required
PIO6[6]	Name		TSIN2DATA[5]
	Description		Transport stream2 parallel data input
	Direction		I
	Configuration		No configuration is required
PIO6[7]	Name		TSIN2DATA[4]
	Description		Transport stream2 parallel data input
	Direction		I
	Configuration		No configuration is required
PIO7[0]	Name		TSIN2DATA[3]
	Description		Transport stream2 parallel data input
	Direction		I
	Configuration		No configuration is required
PIO7[1]	Name		TSIN2DATA[2]
	Description		Transport stream2 parallel data input
	Direction		I
	Configuration		No configuration is required
PIO7[2]	Name		TSIN2DATA[1]
	Description		Transport stream2 parallel data input
	Direction		I
	Configuration		No configuration is required
PIO7[3]	Name		TSIN2DATA[0]
	Description		Transport stream2 parallel data input
	Direction		I
	Configuration		No configuration is required

7.2 Ethernet interface multiplexing in standard mode

The Ethernet interface can be configured in the following ways:

- MII mode
- RMII mode

The mapping is shown in *Table 35*.

Table 35. STi7105 Ethernet muxing details (in standard mode)

Pin	Parameter	Configuration0	Configuration1
		Ethernet MII mode	Ethernet RMII mode
	Configuration	CONTROL_CONFIG7[16] =1 CONTROL_CONFIG7[18] =1 CONTROL_CONFIG7[26:25] =00	CONTROL_CONFIG7[16] =1 CONTROL_CONFIG7[18] =0 CONTROL_CONFIG7[26:25] =01
ETHMII_TXCLK	Name	ETHMII_TXCLK	
	Description	Transmit clock	
	Direction	I	
ETHMII_TXEN	Name	ETHMII_TXEN	ETHRMII_TXEN
	Description	Transmit enable flag	Transmit enable flag
	Direction	O	O
ETHMII_TXD[3]	Name	ETHMII_TXD[3]	
	Description	Transmit data BIT3	
	Direction	O	
ETHMII_TXD[2]	Name	ETHMII_TXD[2]	
	Description	Transmit data BIT2	
	Direction	O	
ETHMII_TXD[1]	Name	ETHMII_TXD[1]	ETHRMII_TXD[1]
	Description	Transmit data BIT1	Transmit data BIT1
	Direction	O	O
ETHMII_TXD[0]	Name	ETHMII_TXD[0]	ETHRMII_TXD[0]
	Description	Transmit data BIT0	Transmit data BIT0
	Direction	O	O
ETHMII_RXCLK	Name	ETHMII_RXCLK	
	Description	Receive clock	
	Direction	I	
ETHMII_RXDV	Name	ETHMII_RXDV	ETHRMII_CRS_DV
	Description	Receive data valid flag	Receive data valid flag
	Direction	I	I
ETHMII_RXER	Name	ETHMII_RXER	ETHRMII_RXER
	Description	Receive data error flag	Receive data error flag
	Direction	I	I
ETHMII_RXD[3]	Name	ETHMII_RXD[3]	
	Description	Receive data BIT3	
	Direction	I	
ETHMII_RXD[2]	Name	ETHMII_RXD[2]	

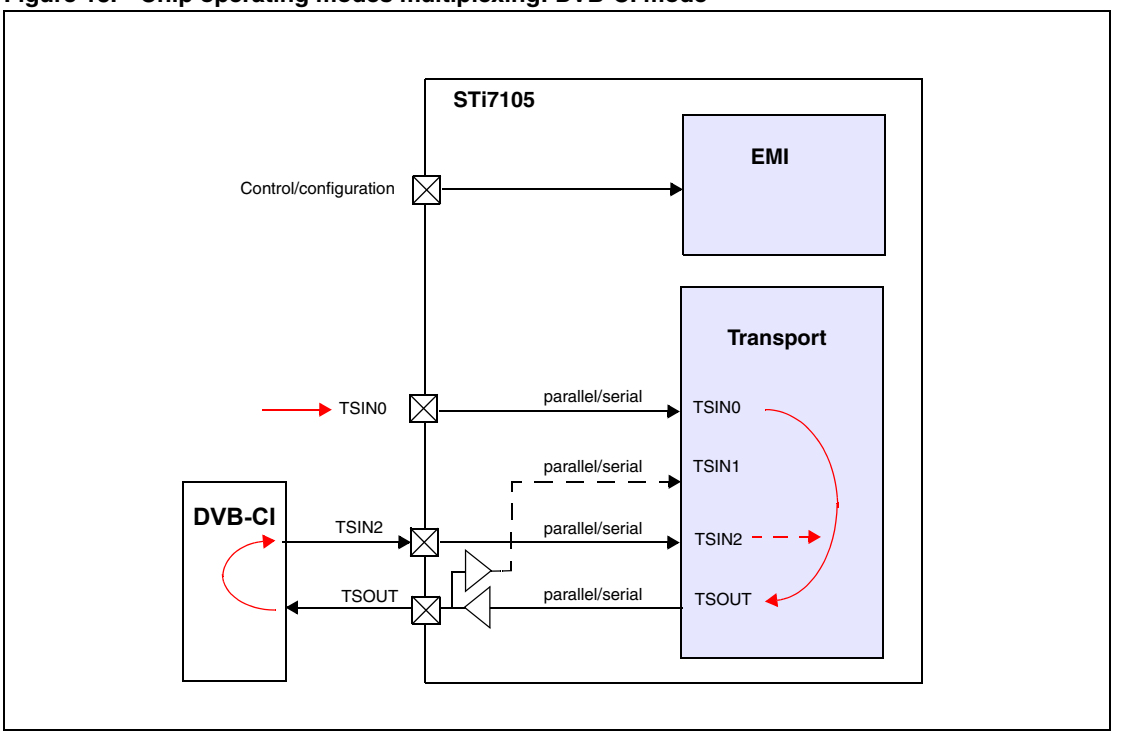
Table 35. STi7105 Ethernet muxing details (in standard mode) (continued)

Pin	Parameter	Configuration0	Configuration1
	Description	Receive data BIT2	
	Direction	I	
ETHMII_RXD[1]	Name	ETHMII_RXD[1]	ETHRMII_RXD[1]
	Description	Receive data BIT1	Receive data BIT1
	Direction	I	I
ETHMII_RXD[0]	Name	ETHMII_RXD[0]	ETHRMII_RXD[0]
	Description	Receive data BIT0	Receive data BIT0
	Direction	I	I
ETHMII_CRS	Name	ETHMII_CRS	
	Description	Carrier sense flag	
	Direction	I	
ETHMII_COL	Name	ETHMII_COL	
	Description	Carrier collision detect flag	
	Direction	I	
ETHMII_MDC	Name	ETHMII_MDC	ETHRMII_MDC
	Description	Management data clock	Management data clock
	Direction	O	O
ETHMII_MDIO	Name	ETHMII_MDIO	ETHRMII_MDIO
	Description	Management data	Management data
	Direction	B	B
ETHMII_MDINT	Name	ETHMII_MDINT	ETHRMII_MDINT
	Description	Management data interrupt	Management data interrupt
	Direction	I	I
ETHMII_PHYCLK	Name	ETHMII_PHYCLK	ETHRMII_PHYCLK
	Description	PHY clock	PHY clock
	Direction	O	O

7.3 DVB common interface (DVB-CI) transport mode

In the DVB common interface mode, the transport stream is demodulated by the front-end subsystem, sent to the external DVB-CI decryption module through the transport interface (in parallel mode) and sent back again (in parallel mode) to the STi7105.

Figure 18. Chip operating modes multiplexing: DVB-CI mode



Details of transport interface mapping on PIOs are provided in *Section 7.1: Transport interfaces multiplexing* and *Table 34.*

Refer to *Section 7.4.6: DVB-CI modes* for DVB-CI mapping on EMI pads.

7.4 External memory interface (EMI) operating modes

The EMI can support the following device types, each one associated with different pin mappings:

1. Peripheral/SRAM on *page 113*
2. Asynchronous NOR-FLASH on *page 113*
3. Synchronous NOR-FLASH on *page 114*
4. NAND-FLASH on *page 114*
5. Serial FLASH on *page 115*
6. DVB-CI on *page 115*
7. ATAPI-PIO on *page 116*
8. PCI on *page 116*
9. Multi-Chip; independent from all other modes (except PCI) on *page 117*

7.4.1 Peripheral/SRAM mode

Table 36. EMI peripheral/SRAM mode: pin mapping

EMI assignment	Peripheral/SRAM mode assignment	I/O	Voltage	Description
NOTEMICSE,D,C,B,A	NOTEMICSE,D,C,B,A	O	3.3	Peripheral chip select E,D,C,B,A
NOTEMIBE[1:0]	NOTEMIBE[1:0]	O	3.3	External device databus byte enable
NOTEMIOE	NOTEMIOE	O	3.3	External device output enable
EMITREADYORWAIT	EMITREADYORWAIT	I	3.3	External memory device target ready indicator
EMIRDNOTWR	EMIRDNOTWR	O	3.3	External read/write access indicator. Common to all devices.
EMIDATA[15:0]	EMIDATA[0]	I/O	3.3	External common databus
EMIADDR[25:1]	EMIADDR[25:1]	O	3.3	External common address bus

Note: EMINOTLBA, EMINOTBAA, EMINANDREADYNOTBUSY, and EMIFLASHCLK are not used.

7.4.2 Asynchronous NOR-Flash mode

Table 37. EMI asynchronous NOR-Flash mode: pin mapping

EMI assignment	Asynchronous NOR-Flash mode assignment	I/O	Voltage	Description
NOTEMICSE,D,C,B,A	NOTEMICSE,D,C,B,A	O	3.3	Chip select E,D,C,B,A
NOTEMIOE	NOTEMIOE	O	3.3	External device output enable
EMITREADYORWAIT	EMITREADYORWAIT	I	3.3	External memory device target ready indicator
EMIRDNOTWR	EMIRDNOTWR	O	3.3	External read/write access indicator. Common to all devices.
EMIDATA[15:0]	EMIDATA[15:0]	I/O	3.3	External common databus
EMIADDR[25:1]	EMIADDR[24:0]	O	3.3	External common address bus

Note: EMINOTLBA, EMINOTBAA, EMINANDREADYNOTBUSY, and EMIFLASHCLK are not used.

7.4.3 Synchronous NOR-Flash mode

Table 38. EMI synchronous NOR-Flash mode: pin mapping

EMI assignment	Synchronous NOR-Flash mode assignment	I/O	Voltage	Description
NOTEMICSE,D,C,B,A	NOTEMICSE,D,C,B,A	O	3.3	Chip select E,D,C,B,A
NOTEMIOE	NOTEMIOE	O	3.3	External device output enable
NOTEMILBA	NOTEMILBA	O	3.3	Flash device load burst address
NOTEMIBAA	NOTEMIBAA	O	3.3	Flash burst address advanced
EMITREADYORWAIT	EMITREADYORWAIT	I	3.3	External memory device target ready indicator
EMIRDNOTWR	EMIRDNOTWR	O	3.3	External read/write access indicator. common to all devices.
EMIDATA[15:0]	EMIDATA[15:0]	I/O	3.3	External common databus
EMIADDR[25:1]	EMIADDR[24:0]	O	3.3	External common address bus
EMIFLASHCLK	EMIFLASHCLK	I/O	3.3	Flash clock

7.4.4 NAND-Flash mode

Features

- Embeds a 1-bit error correcting code (ECC) hardware controller.
- Can support single level cell (SLC) NAND Flash devices from main Flash providers.
- Support of 16 Mbyte device per CS.
- Multiple Flash devices can be addressed, each EMI_CS being statically configured by software, such as EMI Flash CS. An external NOR is issued on READY_NOT_BUSY signals in that case.

Table 39. EMI NAND-Flash mode: pin mapping

EMI assignment	NAND-Flash mode assignment	I/O	Voltage	Description
NOTEMICSA	NAND_CS0	O	3.3	Chip select E,D,C,B,A
NOTEMICSB	NAND_CS1	O	3.3	
NOTEMICSC	NAND_CS2	O	3.3	
NOTEMICSD	NAND_CS3	O	3.3	
NOTEMICSE	NAND_CS4	O	3.3	
NOTEMIOE	NAND_REN	O	3.3	External device output enable
EMIRDNOTWR	NAND_WEN	O	3.3	External read/write access indicator

Table 39. EMI NAND-Flash mode: pin mapping (continued)

EMI assignment	NAND-Flash mode assignment	I/O	Voltage	Description
EMIDATA[15:0]	NAND_AD[15:0]	I/O	3.3	External common address/databus
EMIADDR[18]	NAND_ALE	O	3.3	
EMIADDR[17]	NAND_CLE	O	3.3	

Note: NOTEMIBE[1:0], NOTEMILBA, NOTEMIBAA, EMITREADYORWAIT, EMIADDR[25:19], EMIADDR[16:1], and EMIFLASHCLK are not used.

7.4.5 Serial-Flash mode

Table 40. EMI Serial-Flash pins as PIO alternates

Assignment	I/O	Voltage	Description	Comments
SPIBOOT_CLOCK	O	3.3		PIO15[0]
SPIBOOT_DATA_OUT	O	3.3		PIO15[1]
SPIBOOT_DATA_IN	I	3.3		PIO15[3]
SPIBOOT_CS	O	3.3		PIO15[2]

7.4.6 DVB-CI modes

The DVB-CI modes are only available on banks 2 and 3.

Table 41. EMI DVB-CI mode: pin mapping

EMI assignment	Peripheral/SRAM mode assignment	I/O	Voltage	Description
NOTEMICSD,C	DVBCI_NOTCEx	O	3.3	Peripheral chip select D,C
NOTEMIBE[0]	DVBCI_NOTIOWR	O	3.3	Write command
NOTEMIOE	DVBCI_NOTOE	O	3.3	Output enable
EMIRDNOTWR	DVBCI_NOTWE	O	3.3	Write enable DVBCI
NOTEMIBAA	DVBCI_NOTIORD	O	3.3	Read command
EMITREADYORWAIT	DVBCI_NOTWAIT	I	3.3	Wait signal
EMIDATA[7:0]	DVBCI_DATA[7:0]	I/O	3.3	External common databus
EMIADDR[15:1]	DVBCI_A[15:1]	O	3.3	Address bus

Note: EMI_NOTCSE/B/A, EMI_NOTBE[1], EMI_NOTLBA, EMI_NANDREADYNOTBUSY, EMI_DATA[15:8], EMI_ADDR[25:16], EMI_FLASHCLK are not used

7.4.7 ATAPI-PIO modes

The ATAPI-PIO modes are only available on banks 2 and 3.

Table 42. EMI ATAPI-PIO mode: pin mapping

EMI assignment	Peripheral/SRAM mode assignment	I/O	Voltage	Description
NOTEMICSD,C	ATAPI_NOTCEx	O	3.3	Peripheral chip select D,C
NOTEMIBE[0]	ATAPI_NOTDIOWR	O	3.3	Write command
NOTEMIBAA	ATAPI_NOTDIORD	O	3.3	Read command
EMITREADYORWAIT	ATAPI_IORDY	I	3.3	Wait signal
EMIDATA[15:0]	ATAPI_DATA[15:0]	I/O	3.3	External common databus
EMIADDR[20:19]	ATAPI_CS[1:0]	O	3.3	Chip select
EMIADDR[2:1]	ATAPI_A[2:1]	O	3.3	Address bus

*Note: NOTEMICSE/B/A, NOTEMIBE[1], NOTEMI*OE, *NOTEMI*LBA, *EMIADDR[25:21], EMIADDR[18:3], EMIFLASHCLK are not used.*

7.4.8 PCI mode

Table 43. EMI PCI mode: pin mapping

EMI assignment	Peripheral/SRAM mode assignment	I/O	Voltage	Description
NOTEMICSE	PCI_NOTFRAME	I/O	3.3	PCI frame
NOTEMIBE[1:0]	PCI_CBE[1:0]	I/O	3.3	PCI command/byte enable
EMIRDNOTWR	PCI_NOTPERR	I/O	3.3	PCI parity error flag
EMIDATA[15:0]	PCI_AD[15:0]	I/O	3.3	Common PCI address/data bus
EMIADDR[24:23]	PCI_CBE[3:2]	I/O	3.3	PCI command/byte enable
EMIADDR[22]	PCI_NOTDEVSEL	I/O	3.3	PCI device select
EMIADDR[20]	PCI_NOTSTOP	I/O	3.3	PCI target stop request
EMIADDR[19]	PCI_NOTIRDY	I/O	3.3	PCI initiator ready flag
EMIADDR[18]	PCI_NOTTRDY	I/O	3.3	PCI target ready flag
EMIADDR[17]	PCI_PAR	I/O	3.3	PCI parity flag
EMIADDR[16:1]	PCI_AD[31:16]	I/O	3.3	Common PCI address/data bus
EMIFLASHCLK	PCI_CLK	I/O	3.3	PCI clock
EMIBUSREQ	PCI_REQ[0]	I/O	3.3	PCI bus access request
EMIBUSGNT	PCI_GNT[0]	I/O	3.3	PCI bus access grant

Note: NOTEMICSD/C/B/A, NOTEMIOE, EMIADDR[25], EMIADDR[21], NOTEMILBA, and EMITREADYORWAIT are not used.

Caution: Memory read transfers from non-prefetchable memory are always signalled as 32 bits transfers (all byte enables active) by the STi7105. This should be taken into account when considering PCI devices to be used with STi7105.

Table 44. EMI PCI pins as PIO alternates

Assignment	I/O	Voltage	Description	Comments
PCI_BUS_REQ[1]	I	3.3	PCI bus access request	PIO6[5]
PCI_BUS_REQ[2]	I	3.3	PCI bus access request	PIO6[6]
PCI_BUS_GNT[1]	O	3.3	PCI bus access grant	PIO7[1]
PCI_BUS_GNT[2]	O	3.3	PCI bus access grant	PIO7[2]
PCI_LOCK_IN	I	3.3	PCI lock function	PIO7[0], PIO15[5]
PCI_PME_IN	I	3.3	PCI PME function	PIO15[6]
PCI_INT_FROM_DEVICE[0]	I	3.3	PCI interrupt input (when host)	PIO6[0]/PIO15[3]
PCI_INT_FROM_DEVICE[1]	I	3.3	PCI interrupt input (when host)	PIO6[1]
PCI_INT_FROM_DEVICE[2]	I	3.3	PCI interrupt input (when host)	PIO6[2]
PCI_INT_TO_HOST	O	3.3	PCI interrupt output (when device)	PIO15[3], PIO6[0]
PCI_RESETN_FROM_HOST_TO_DEVICE	I	3.3	PCI reset input (when host)	PIO15[7]
PCI_SYSTEM_ERROR	O	3.3	PCI error flag	PIO15[4]

7.4.9 Multi-chip mode

With the exception of PCI, this mode is independent from all other modes and uses dedicated balls.

Table 45. EMI multi-chip mode: pin mapping

EMI assignment	Peripheral/SRAM mode assignment	I/O	Voltage	Description
EMIBUSREQ	EMIBUSREQ	I/O	3.3	Bus access request
EMIBUSGNT	EMIBUSGNT	I/O	3.3	Bus access grant

EMI multi-chip mode: pins as PIO alternates

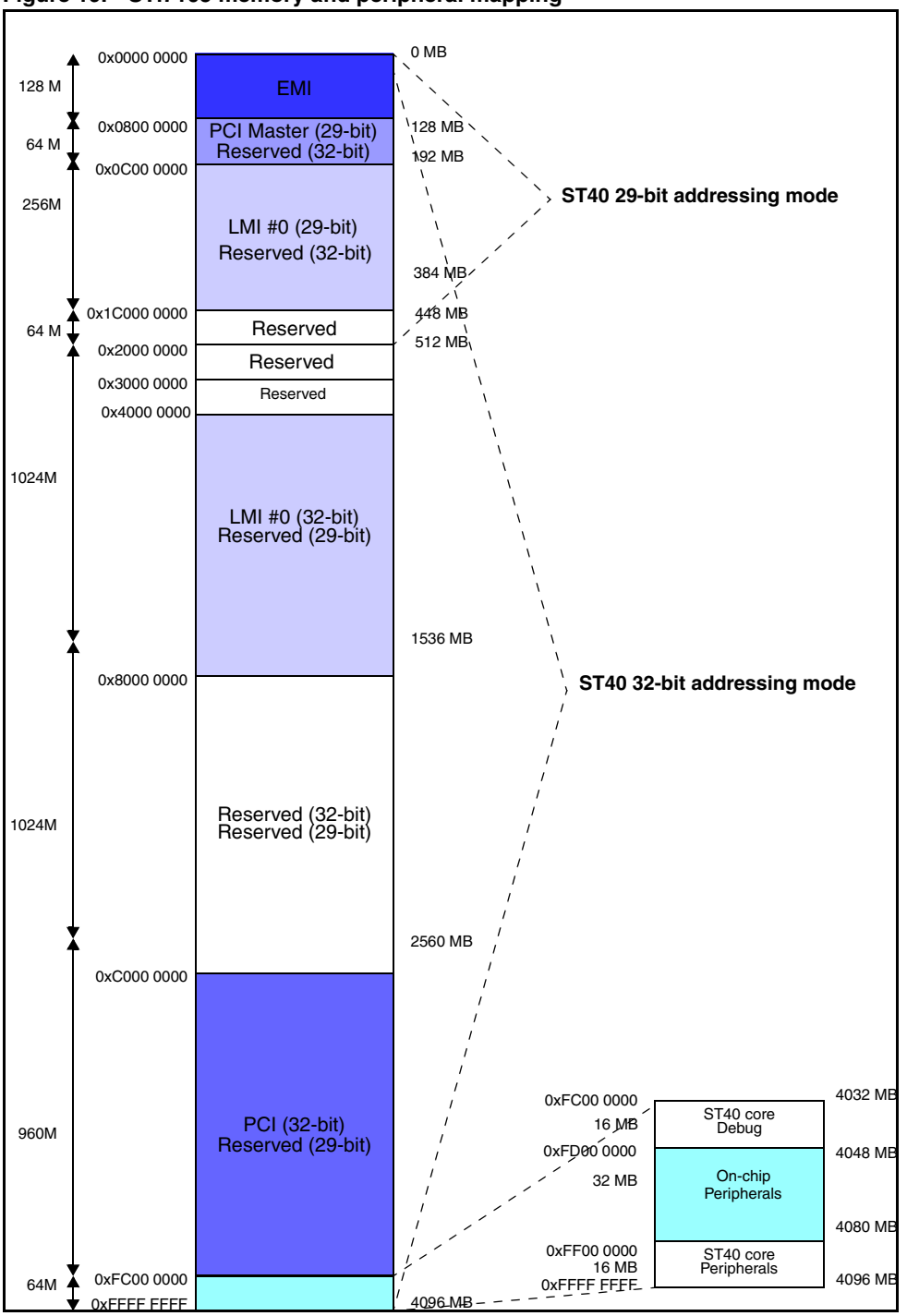
Assignment	I/O	Voltage	Description	Comments
EMI_SS_BUS_FREE_ACCESSPEND/ EMI_SS_BUS_FREE_OUT	I	3.3	Access pending flag	PIO15[2]

8 Memory map

The STi7105 memory space is populated with non-volatile memories, with external peripherals (EMI) at base address 0 (ST40 boots at address 0), and with DDR2-SDRAM devices (LMI) at base address 0x0C00 0000 (128 Mbytes) in 29-bit mode or at base address 0x4000 0000 (1024 Mbytes) in 32-bit mode.

The STi7105 on-chip peripherals are mapped in area 6 of the ST40 in 29-bit mode. The *Figure 19* shows the STi7105 memory and peripheral mapping.

Figure 19. STi7105 memory and peripheral mapping



Note: In SE mode, the ST40 Core Peripherals (P4) appear twice in the STBUS address map. The LMI base address is programmable.

8.1 Global Mapping

The internal peripherals addresses are located in ST40-300 P4 region. Grouping is done so that peripherals which belong to the same physical block have contiguous addresses, requiring only one address decoder in each physical block.

The *Table 46* gives the base address of the external interfaces and internal peripherals.

Table 46. Internal peripheral base addresses

Target Name	Start Offset	End Offset	Size	Description
EMI	0x0000 0000	0x07FF FFFF	128M	EMI
PCI_MASTER_29B	0x0800 0000	0x0BFF FFFF	64M	PCI Master, 29-bit mode
LMI0_HP_29B	0x0C00 0000	0x1BFF FFFF	256M	LMI #0 - HP, 29-bit mode
LMI0_LP_29B	0x0C00 0000	0x1BFF FFFF	256M	LMI #0 - LP, 29-bit mode
RESERVED	0x1C00 0000	0x3FFF FFFF	576M	Reserved
LMI0_HP_32B	0x4000 0000	0x7FFF FFFF	1024M	LMI #0 - HP, 32-bit mode
LMI0_LP_32B	0x4000 0000	0x7FFF FFFF	1024M	LMI #0 - LP, 32-bit mode
RESERVED	0x8000 0000	0xBFFF FFFF	1024M	Reserved
PCI_MASTER_32B	0xC000 0000	0xFBFF FFFF	960M	PCI Master, 32-bit mode
SH4 CORE DEBUG	0xFC00 0000	0xFCFF FFFF	16M	ST40 Core Debug
COMMs	0xFD00 0000	0xFD0F FFFF	1M	Comms config registers (details in *Table 47*)
SPARE0_PLUG	0xFD10 0000	0xFD10 0FFF	4K	Spare 0 plug
RESERVED	0xFD10 1000	0xFD10 17FF	2K	Reserved
PCMP1	0xFD10 1800	0xFD10 1FFF	4K	PCM player 1 port & config registers
PCMR0	0xFD10 2000	0xFD10 2FFF	4K	PCM reader port & config registers
CPXM	0xFD10 3000	0xFD10 3FFF	4K	CPXM registers
TVOUT_FDMA	0xFD10 4000	0xFD10 5FFF	8K	TVOUT FDMA (HDMI, PCM_p1,SPDIF_p, TTxT) (details in *Table 48*)
RESERVED	0xFD10 6000	0xFD10 FFFF	44K	Reserved
GMAC0	0xFD11 0000	0xFD11 7FFF	32K	Ethernet 0 config registers
RESERVED	0xFD11 8000	0xFD11 FFFF	32K	Reserved
SPARE1_PLUG	0xFD12 0000	0xFD12 7FFF	32K	Spare 1 plug
RESERVED	0xFD12 8000	0xFDFF FFFF	15200K	Reserved
CLKGENB	0xFE00 0000	0xFE00 0FFF	4K	Clock Generator B config registers
SYSC_A	0xFE00 1000	0xFE00 1FFF	4K	System config registers (GP Registers)
HD_DISPLAY	0xFE00 2000	0xFE00 2FFF	4K	HD display config registers

Table 46. Internal peripheral base addresses (continued)

Target Name	Start Offset	End Offset	Size	Description
SD_DISPLAY	0xFE00 3000	0xFE00 3FFF	4K	SD display config registers
RESERVED	0xFE00 4000	0xFE00 BFFF	32K	Reserved
RESERVED	0xFE00 C000	0xFE00 FFFF	16K	Reserved
T1_PIO	0xFE01 0000	0xFE01 FFFF	64K	T1 PIO - 10 Banks PIOs config registers
KEY_SCAN	0xFE02 0000	0xFE02 07FF	2K	Key scanning
RESERVED	0xFE02 0800	0xFE02 FFFF	62K	Reserved
TVOUT_CPU	0xFE03 0000	0xFE03 7FFF	32K	TVOUT Config Regs (Denc, VTGs, TVO_glue, FlexDVO, HD formatter, CEC) (details in *Table 49*)
RESERVED	0xFE03 8000	0xFE0F FFFF	800K	Reserved
USB2_1	0xFE10 0000	0xFE1F FFFF	1M	USB 2.0 #1 config registers
RESERVED	0xFE20 0000	0xFE20 7FFF	32K	Reserved
RESERVED	0xFE20 8000	0xFE20 8FFF	4K	Reserved
SATA	0xFE20 9000	0xFE20 9FFF	4K	SATA config registers
COMPO	0xFE20 A000	0xFE20 AFFF	4K	Compositor config registers
BLITTER	0xFE20 B000	0xFE20 BFFF	4K	Blitter display config registers
RESERVED	0xFE20 C000	0xFE20 D3FF	5K	Reserved
RESERVED	0xFE20 D400	0xFE20 FFFF	11K	Reserved
AUDIO_CONF	0xFE21 0000	0xFE21 0FFF	4K	Audio config registers
MBX0	0xFE21 1000	0xFE21 17FF	2K	Mailbox #0 (LX Delta_Mu) config registers
RESERVED	0xFE21 1800	0xFE21 1FFF	2K	Reserved
MBX1	0xFE21 2000	0xFE21 27FF	2K	Mailbox #1 (LX Delta_Mu) config registers
RESERVED	0xFE21 2800	0xFE21 2FFF	2K	Reserved
CLKGENA	0xFE21 3000	0xFE21 3FFF	4K	Clock Generator A config registers
RESERVED	0xFE21 4000	0xFE21 FFFF	48K	Reserved
FDMA_0	0xFE22 0000	0xFE22 FFFF	64K	FDMA_0 memory and config registers
PTI_0	0xFE23 0000	0xFE23 FFFF	64K	PTI_0 config registers
RESERVED	0xFE24 0000	0xFE24 0FFF	4K	Reserved
DVP	0xFE24 1000	0xFE24 1FFF	4K	DVP config registers
TSMERGER	0xFE24 2000	0xFE24 2FFF	4K	TSMerger config registers
RESERVED	0xFE24 3000	0xFE24 FFFF	52K	Reserved
RESERVED	0xFE25 0000	0xFE25 0FFF	4K	Reserved

Table 46. Internal peripheral base addresses (continued)

Target Name	Start Offset	End Offset	Size	Description
RESERVED	0xFE25 1000	0xFE25 FFFF	60K	Reserved
PTI_1	0xFE26 0000	0xFE26 FFFF	64K	PTI_1 config registers
RESERVED	0xFE27 0000	0xFE3F FFFF	1600K	Reserved
EMISS	0xFE40 0000	0xFE40 7FFF	32K	EMISS config registers (EMISS) (details in *Table 50*)
RESERVED	0xFE40 8000	0xFE40 FFFF	32K	Reserved
FDMA_1	0xFE41 0000	0xFE41 FFFF	64K	FDMA_1 config registers
FDMA_MUX	0xFE42 0000	0xFE42 0FFF	4K	FDMA Mux config registers
RESERVED	0xFE42 1000	0xFE53 FFFF	1148K	Reserved
DMU	0xFE54 0000	0xFE55 FFFF	128K	Delta Mu configuration registers
PCI_MASTER_REGS	0xFE56 0000	0xFE56 0FFF	4K	AHB-PCI config registers (on T3 I)
RESERVED	0xFE56 1000	0xFE5F FFFF	636K	Reserved
LX_DMU	0xFE60 0000	0xFE6F FFFF	1M	ST231 Delta Mu peripherals
EMIREG	0xFE70 0000	0xFE7F FFFF	1M	EMI configuration registers (details in *Table 50*)
LX_AUD	0xFE80 0000	0xFE8F FFFF	1M	ST231 audio peripherals
TSMERGER_T2	0xFE90 0000	0xFE90 0FFF	4K	TSMerger-Type2 space
LMI0_REG	0xFE90 1000	0xFE90 1FFF	4K	GPLMI0 control registers
RESERVED	0xFE90 2000	0xFE9F FFFF	1016K	Reserved
USB2_2	0xFEA0 0000	0xFEAF FFFF	1M	USB 2.0 #2 config registers
RESERVED	0xFEB0 0000	0xFEFF FFFF	4M	Reserved
SH4 CORE PERIPH	0xFF00 0000	0xFFFF FFFF	16M	ST40 core peripherals

Table 47. STi7105 Comms sub-blocks memory map (base address: 0xFD00 0000)

Region Name	Start Offset	End Offset	Size (Bytes)	Description
ILC3	0x00000	0x0FFF	1K	ILC
RESERVED	0x01000	0x07FFF	7K	Reserved
LPC	0x08000	0x08FFF	1K	LPC
RESERVED	0x09000	0x0FFFF	7K	Reserved
PWM0	0x10000	0x10FFF	1K	PWM0
RESERVED	0x11000	0x17FFF	7K	Reserved
IRB	0x18000	0x18FFF	1K	IRB group
RESERVED	0x19000	0x1FFFF	7K	Reserved

Table 47. STi7105 Comms sub-blocks memory map (base address: 0xFD00 0000) (continued)

Region Name	Start Offset	End Offset	Size (Bytes)	Description
PIO0	0x20000	0x20FFF	1K	PIO
PIO1	0x21000	0x21FFF	1K	
PIO2	0x22000	0x22FFF	1K	
PIO3	0x23000	0x23FFF	1K	
PIO4	0x24000	0x24FFF	1K	
PIO5	0x25000	0x25FFF	1K	
PIO6	0x26000	0x26FFF	1K	
PIO7	0x0101 0000	0x0101 0FFF	1K	
PIO8	0x0101 1000	0x0101 1FFF	1K	PIO
PIO9	0x0101 2000	0x0101 2FFF	1K	
PIO10	0x0101 3000	0x0101 3FFF	1K	
PIO11	0x0101 4000	0x0101 4FFF	1K	
PIO12	0x0101 5000	0x0101 5FFF	1K	
PIO13	0x0101 6000	0x0101 6FFF	1K	
PIO14	0x0101 7000	0x0101 7FFF	1K	
PIO15	0x0101 8000	0x0101 8FFF	1K	
PIO16	0x0101 9000	0x0101 9FFF	1K	
RESERVED	0x27000	0x2FFFF	9K	Reserved
UART0	0x30000	0x30FFF	1K	UART
UART1	0x31000	0x31FFF	1K	
UART2	0x32000	0x32FFF	1K	
UART3	0x33000	0x33FFF	1K	
RESERVED	0x34000	0x3FFFF	12K	Reserved
SSC0	0x40000	0x40FFF	1K	Synchronous Serial Controller
SSC1	0x41000	0x41FFF	1K	
SSC2	0x42000	0x42FFF	1K	
SSC3	0x43000	0x43FFF	1K	
RESERVED	0x44000	0x47FFF	4K	Reserved
RESERVED	0x48000	0x48FFF	1K	Reserved
RESERVED	0x49000	0x49FFF	1K	
RESERVED	0x4A000	0x57FFF	14K	Reserved
MAFE	0x58000	0x58FFF	1K	MAFE
RESERVED	0x59000	0x6FFFF	23K	Reserved
RESERVED	0x71000	0xFFFFF	143K	Reserved

Table 48. STi7105 TVOUT_FDMA sub-blocks memory map (base address: 0xFD10 4000)

Region Name	Start Offset	End Offset	Size (Bytes)	Description
HDMI_REG	0x0000	0x07FF	512	
RESERVED	0x0800	0x0BFF	256	Reserved
SPDIFPLAYER_REG	0x0C00	0x0CFF	64	
RESERVED	0x0E00	0x0FFF	128	Reserved
I2S2SPDIF_1	0x1000	0x13FF	256	
I2S2SPDIF_2	0x1400	0x17FF	256	
I2S2SPDIF_3	0x1800	0x1BFF	256	
I2S2SPDIF_4	0x1C00	0x1FFF	256	
HDCP	0x4800	0x48FF	64	
PCMPLAYER0_REG	0x4D00	0x4DFF	64	
TOP_GLUE_AUX	0x4E00	0x4EFF	64	

Table 49. STi7105 TVOUT_CPU sub-blocks memory map (base address: 0xFE03 0000)

Region Name	Start Offset	End Offset	Size (Bytes)	Description
DENC	0x0000	0x01FF	128	
AUX_VTG	0x0200	0x02FF	64	
MAIN_VTG	0x0300	0x03FF	64	
HDTVOUT_TOP_GLUE_MAIN	0x0400	0x05FF	64	
Flex-DVO0	0x0600	0x07FF	128	
HDTVOUT_HDF1	0x0800	0x08FF	64	HD formatter 1
HDTVOUT_HDF2	0x0900	0x09FF	64	HD formatter 2
HDTVOUT_HDF3	0x0A00	0x0AFF	64	HD formatter 3
HDTVOUT_HDF4	0x0B00	0x0BFF	64	HD formatter 4
CEC	0x0C00	0x0CFC	63	
RESERVED	0x1000	0x2FFF	8 K	

Table 50. STi7105 EMISS and EMI sub-blocks memory map

Region Name	Start Offset	End Offset	Size (Bytes)	Description
EMISS_ARBITER_REG	0xFE40 0000 + 0x1000	0xFE40 0000 + 0x13FF	256	EMI/PCI Arbiter registers
EMISS_PCI_BRIDGE_REG	0xFE40 0000 + 0x1400	0xFE40 0000 + 0x17FF	256	PCI STbus Bridge registers
EMI_CONF_REG	0xFE70 0000 + 0x0000	0xFE70 0000 + 0x0FFF	1K	EMI registers
EMI_NAND_REG	0xFE70 0000 + 0x1000	0xFE70 0000 + 0x1FFF	1K	EMI Nand Controller registers
EMI_SPI_REG	0xFE70 0000 + 0x2000	0xFE70 0000 + 0x2FFF	1K	EMI SPI Controller registers
RESERVED	0xFE70 0000 + 0x3000	0xFE70 0000 + 0xFFFF	13K	Reserved

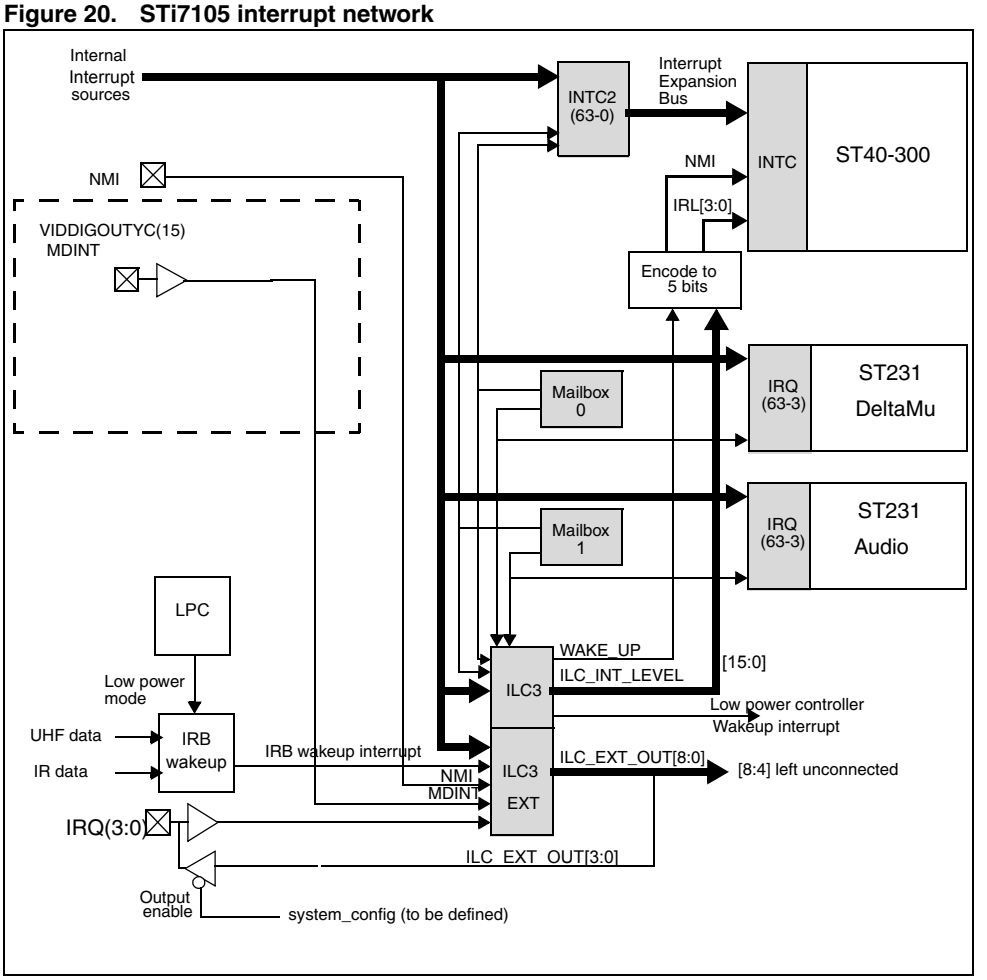
9 Interrupt networks

9.1 Interrupt network organization

The STi7105 has two interrupt networks. One network is associated with the ST40 CPU and the other network is associated with the DeltaMu-ST231 CPU when used as as an application processor.

The interrupt lines are routed to both ST40 and partially to DeltaMu-ST231. It is up to the software to handle the interrupts with ST40 or DeltaMu-ST231.

Figure 20. STi7105 interrupt network



9.1.1 STi7105 interrupt network

ILC3 interrupt level controller

The STi7105 interrupt network includes an ILC3 interrupt level controller. The ILC3 accepts 96 synchronous interrupt inputs and eight asynchronous interrupt inputs. The external

interrupts can have up to five programmable triggering conditions (active high, active low, falling edge, rising edge, or any edge).

The ILC3 maps any of these interrupts onto a group of 16 interrupt level outputs that are used in the STi7105 for internal and external interrupts and onto a group of four interrupt levels that are not used.

The ILC3 mapping is described in *Table 51* and *Table 52*.

Wake up by interrupt

The ILC3 also has an interrupt output dedicated to the wake-up process. A pulse stretcher receives a transition from the UHF and IR input pins and generates an interrupt connected to one of the external interrupt inputs.

Internal peripheral interrupts

Both the ST40 and the DeltaMu ST231 receive all the internal interrupt requests. It is up to the software to define the CPU that will serve each interrupt request.

All the internal interrupts are routed to the INTC2, ST231 Interrupt controller and ILC3. All the internal interrupts are level sensitive and active HIGH.

External interrupts inputs

The four external asynchronous interrupts and the MDINT interrupts (the Ethernet phy interrupt or fifth IRQ if the Ethernet/DVO pins are configured for Ethernet but the Ethernet phy is either not connected or does not use the MDINT) are routed to the ILC3 interrupt controller before reaching the ST40 and ST231 in order to synchronize and change the polarity if needed. The ST40 expects the interrupts to be active high. These interrupts are then output from the ILC3 to be routed toward the ST40 and DeltaMu ST231.

External interrupts outputs

The ILC3 has the capability to output a subset of the interrupts that are connected to it. Four of these interrupts are software selectable to be output externally for remote devices.

Control of the external interrupts direction

The direction of the external interrupts is controlled by the configuration register SYSTEM_CONFIG10.

Table 51. ILC3 internal interrupt mapping

Interrupt source		ILC3 mapping
Comms/PIO	PIO0_INTERRUPT	0
	PIO1_INTERRUPT	1
	PIO2_INTERRUPT	2
	PIO3_INTERRUPT	3
	PIO4_INTERRUPT	4
	PIO5_INTERRUPT	5
	PIO6_INTERRUPT	6

Table 51. ILC3 internal interrupt mapping (continued)

Interrupt source		ILC3 mapping
SSC	SSC0_INTERRUPT	7
	SSC1_INTERRUPT	8
	SSC2_INTERRUPT	9
	SSC3_INTERRUPT	10
Comms/UART	UART0_INTERRUPT	11
	UART1_INTERRUPT	12
	UART2_INTERRUPT	13
	UART3_INTERRUPT	14
Comms/MAFE	MAFE_INTERRUPT	15
Comms/PWM	PWM_INTERRUPT	16
Comms/IRB	IRB_INTERRUPT	17
Comms/TTXT	TTXT_INTERRUPT	18
Comms/DAA	DAA_INTERRUPT	19
DVP	DVP_INTERRUPT	20
Reserved	RESERVED	21
ClockGen	DCXO_INTERRUPT	22
PTI1	PTI1_INTERRUPT	23
MAILBOX	ST40_LX_DELTAMU_INTERRUPT	24
	LX_DELTAMU_ST40_INTERRUPT	25
	ST40_AUDIO_INTERRUPT	26
	LX_AUDIO_ST40_INTERRUPT	27
FDMA0/1	FDMA_1_MBOX_INTERRUPT	28
	FDMA_0_MBOX_INTERRUPT	29
Audio	I2S2SPDIF_INTERRUPT0	30
	SPDIFPLYR_INTERRUPT	31
	PCMRDR_INTERRUPT	32
	PCMPLYR1_INTERRUPT	33
	PCMPLYR0_INTERRUPT	34
Reserved	RESERVED	35
TVOUT/VTGs	AUX_VTG_INTERRUPT (1) OR AUX_VTG_INTERRUPT (0)	36
	MAIN_VTG_INTERRUPT (1) OR MAIN_VTG_INTERRUPT (0)	37
Main Video Display Pipe	MAIN_VDP_END_PROCESSING_IRQ	38
	MAIN_VDP_FIFO_EMPTY_IRQ	39

Table 51. ILC3 internal interrupt mapping (continued)

Interrupt source		ILC3 mapping
HDMI/HDCP	HDCP_INTERRUPT	40
	HDMI_INTERRUPT	41
	HDMI_CEC_IRQ	42
	HDMI_CEC_WAKEUP_INT	43
Blitter display	BDISP_AQ1_IRQP OR BDISP_AQ2_IRQP OR BDISP_AQ3_IRQP OR BDISP_AQ4_IRQP	44
RESERVED	RESERVED	45
	RESERVED	46
	RESERVED	47
PTI0	PTI0_INTERRUPT	48
RESERVED	RESERVED	52
USBH	EHCI_INTERRUPT	53
	OHCI_INTERRUPT	54
RESERVED	RESERVED	55
	RESERVED	56
RESERVED	RESERVED	57
TS Merger	TS_MERGER_INTERRUPT	58
Ethernet GMAC	PMT_INT	59
PCI	INT_PCI_DMA	60
BLITTER DISPLAY	BDISP_CQ1_IRQP OR BDISP_CQ2_IRQP	62
RESERVED	RESERVED	63

Table 52. ILC3 external interrupt mapping table

Interrupt source		ILC3 mapping
External Interrupts from external devices	EXT_INTERRUPT[0]	0
	EXT_INTERRUPT[1]	1
	EXT_INTERRUPT[2]	2
	EXT_INTERRUPT[3]	3
From pins through pulse stretcher	IRB_WAKEUP_INTERRUPT	4
NMI Pin	NMI_INTERRUPT	5
Ethernet PHY interrupt /SYSITRQ[4]	MDINT	6
From LPC timer	LOWPOWEROUT_FROM_LPC	7
From Pads through PIO alt (PCI wake-up interrupts)	PCI_PME_IN	8
FDMA0 requests line	selected FDMA_REQ among 32 FDMA DREQ lines	9

Table 52. ILC3 external interrupt mapping table (continued)

Interrupt source		ILC3 mapping
eSATA	SATA_IINTRQ_DMAC_0	10
	SATA_IINTRQ_HOSTC_0	11
Key Scanner	KEY_SCANNER_INTERRUPT	12
Ethernet Gmac	GMAC_MAC_INTR	13
Standalone 10 banks PIOs	STANDALONE_10_BANKS_PIO (10 ORED INTERRUPTS)	14
VDP AUX	AUX_VDP_END_PROCESSING_IRQ	15
	AUX_VDP_FIFO_EMPTY_IRQ	16
Compo Capture	COMPO_CAP_BF	17
Compo Capture	COMPO_CAP_TF	18
FDMA1 requests lines	SELECTED FDMA_REQ AMONG 32 FDMA DREQ LINES	19
Reserved	RESERVED	20
ClockGen A	IRQ_CLKOBS	21
DeltaMu	DELPHI_MBE_INTERRUPT	22
	DELPHI_PRE0_INTERRUPT	23
NAND Controller	INT_NAND	24
PCI	IRQ_PCI_ERROR	25
	IRQ_PCI_FROM_DEVICE[0]	26
	IRQ_PCI_FROM_DEVICE[1]	27
	IRQ_PCI_FROM_DEVICE[2]	28
	RESERVED	29
Audio	I2S2SPDIF_INTERRUPT1	30
	I2S2SPDIF_INTERRUPT2	31
	I2S2SPDIF_INTERRUPT3	32
Reserved	RESERVED	33
	RESERVED	34
	RESERVED	33
	RESERVED	
	RESERVED	95

9.1.2 ST40 interrupt network

Internal and external interrupts

The ST40-300 CPU has two types of interrupts.

External interrupts

- Non maskable interrupts (NMI)—external interrupt source.
- Interrupt request level INTerrupts (IRLINT)—four external interrupt sources IRL0 to IRL3 which can be configured as four independent interrupts or encoded to provide 15 external interrupt levels.

These interrupts are managed by the INTC interrupt controller integrated into the ST40-300 CPU core.

The four external asynchronous interrupts and the MDINT interrupts (that is, the Ethernet phy interrupt or fifth IRQ if the Ethernet phy is either not connected or does not use the MDINT) are routed to the ILC3 interrupt controller before reaching the ST40 and ST231 in order to synchronize and change the polarity if needed.

Internal peripheral interrupts

- On-chip peripherals interrupt sources.

These interrupts are managed by INTC and INTC2 which is an expansion to INTC.

All interrupts (except NMI) are assigned a priority level between 0 and 15: level 15 is the highest and level 1 the lowest, level 0 means that the interrupt is masked. The NMI is defined to have a fixed priority level of 16.

INTC controls the following interrupt sources:

- NMI, IRL[3...0] from external inputs
- ST40-P130 peripherals interrupts:
  - user debug interface (UDI)
  - timer unit (TMU0, 1)
  - real time clock (RTC)
  - serial controller interface (SCI)
  - watch dog timer (WDT)

The INTC2 controls all the on-chip peripherals interrupts and is connected to the INTC through an interrupt expansion bus.

The INTC2 accepts 16 groups of four interrupts (64 total), each group can be assigned a priority by software (INTPRIxx registers). Within each group (of four interrupts), there is a fixed priority, with interrupt four having the highest priority. All interrupts are synchronized in INTC2.

Interrupt service routine address

Whenever an interrupt occurs, the ST40 CPU branches to the interrupt handling vector address determined by adding the fixed offset 0x600 to the vector base address (VBR) register. Each interrupt type is assigned a code which is stored in the INTEVT (Interrupt Event) register when the interrupt occurs. This enables the interrupt service routine to identify the interrupt source type.

The interrupt controller is responsible for mapping each interrupt to its code (INTEVT).

Figure 21 displays the ST40-300 interrupt network, and *Table 53* describes the internal interrupts with their INTEVT code.

Figure 21. ST40 interrupt network

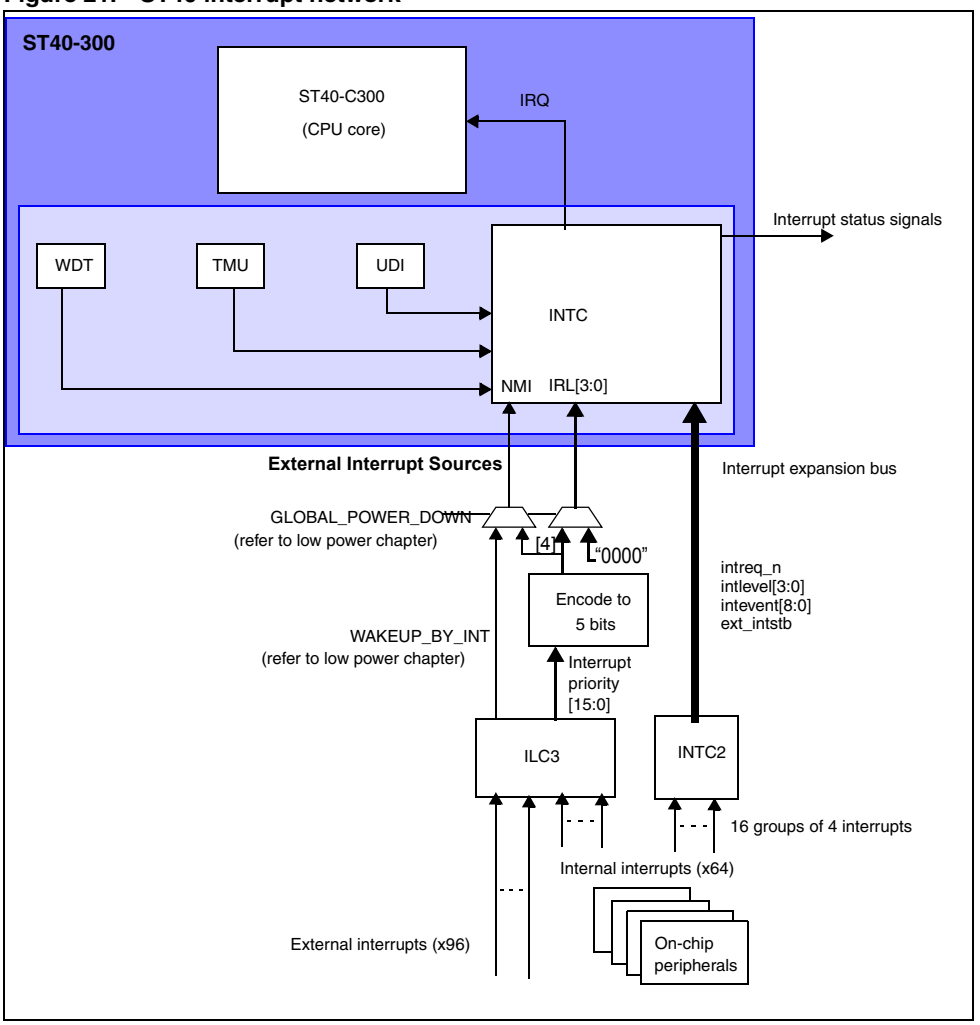


Table 53. ST40-300 P130 interrupts

Interrupt source		INTEVT code	IPR (bit numbers)	Interrupt priority (initial value)
NMI		0x1C0	-	16
IRL independent encoding	IRL0	0x240	IPRD[15:12]	15-0 (13)
	IRL1	0x2A0	IPRD[11:8]	15-0 (10)
	IRL2	0x300	IPRD[7:4]	15-0 (7)
	IRL3	0x360	IPRD[3:0]	15-0 (4)
IRL	level encoding	0x200~0x3C0	-	1-15
TMU0	TUNI0	0x400	IPRA[15:12]	15-0 (0)
TMU1	TUNI1	0x420	IPRA[11:8]	15-0 (0)

Table 53. ST40-300 P130 interrupts (continued)

Interrupt source		INTEVT code	IPR (bit numbers)	Interrupt priority (initial value)
TMU2	TUNI2	0x440	IPRA[7:4]	15-0 (0)
	TICPI2	0x460		
WDT	ITI	0x560	IPRB[15:12]	15-0 (0)
UDI	H-UDI	0x600	IPRC[3:0]	15-0 (0)

Table 54. ST40-300 on-chip peripheral interrupts

Group	Interrupt source		INTEVT code	IPR (bit numbers)	INTREQ/INTMSK (bit number)
group 0	AUDIO	I2S2SPDIF_INTERRUPT0	0xA00	INTPRI00[3:0]	INTREQ00[0]
		I2S2SPDIF_INTERRUPT1	0xA20		INTREQ00[1]
		I2S2SPDIF_INTERRUPT2	0xA40		INTREQ00[2]
		I2S2SPDIF_INTERRUPT3	0xA60		INTREQ00[3]
	eSATA	INTRQ_DMAC	0xA80	INTPRI00[7:4]	INTREQ00[4]
		INTRQ_HOSTC	0xB00		INTREQ00[5]
	DVP	DVP_INTERRUPT	0xB20		INTREQ00[6]
	Standalone 10 banks PIOs	STANDALONE_10_BANKS_PIO (10 ORED INTERRUPTS)	0xB40		INTREQ00[7]
	VDP AUX	AUX_VDP_END_PROCESSING_IRQ	0xB60	INTPRI00[11:8]	INTREQ00[8]
		AUX_VDP_FIFO_EMPTY_IRQ	0xB80		INTREQ00[9]
	Compo Capture	COMPO_CAP_BF	0xBA0		INTREQ00[10]
		COMPO_CAP_FF	0xBC0		INTREQ00[11]
	COMMs/PIO	PIO0_INTERRUPT	0xC00	INTPRI00[15:12]	INTREQ00[12]
		PIO1_INTERRUPT	0xC80	INTPRI00[19:16]	INTREQ00[13]
		PIO2_INTERRUPT	0xD00	INTPRI00[23:20]	INTREQ00[14]
group1	COMMs/PIO	PIO6_INTERRUPT	0x1000	INTPRI04[3:0]	INTREQ04[0]
		PIO5_INTERRUPT	0x1020		INTREQ04[1]
		PIO4_INTERRUPT	0x1040		INTREQ04[2]
		PIO3_INTERRUPT	0x1060		INTREQ04[3]
group2	SSC	SSC0_INTERRUPT	0x10E0	INTPRI04[7:4]	INTREQ04[7]
		SSC1_INTERRUPT	0x10C0		INTREQ04[6]
		SSC2_INTERRUPT	0x10A0		INTREQ04[5]
		SSC3_INTERRUPT	0x1080		INTREQ04[4]

Table 54. ST40-300 on-chip peripheral interrupts (continued)

Group	Interrupt source		INTEVT code	IPR (bit numbers)	INTREQ/INTMSK (bit number)
group3	COMMs/UART	UART0_INTERRUPT	0x1160	INTPRI04[11:8]	INTREQ04[11]
		UART1_INTERRUPT	0x1140		INTREQ04[10]
		UART2_INTERRUPT	0x1120		INTREQ04[9]
		UART3_INTERRUPT	0x1100		INTREQ04[8]
group4	COMMs/MAFE	MAFE_INTERRUPT	0x11E0	INTPRI04[15:12]	INTREQ04[15]
	COMMs/PWM	PWM_INTERRUPT	0x11C0		INTREQ04[14]
	COMMs/IRB	IRB_INTERRUPTS	0x11A0		INTREQ04[13]
		IRB_WAKEUP_INTERRUPT	0x1180		INTREQ04[12]
group5	COMMs/TTXT-DAA	TTXT_INTERRUPT	0x1260	INTPRI04[19:16]	INTREQ04[19]
		DAA_INTERRUPT	0x1240		INTREQ04[18]
	BLITTER DISPLAY	BDISP_AQ1_IRQP OR BDISP_AQ2_IRQP OR BDISP_AQ3_IRQP OR BDISP_AQ4_IRQP	0x1220		INTREQ04[17]
	RESERVED	RESERVED	0x1200		INTREQ04[16
group 6	TS merger	TS_MERGER_INTERRUPT	0x12E0	INTPRI04[23:20]	INTREQ04[23]
	Ethernet GMAC	PMT_INT	0x12A0		INTREQ04[21]
		GMAC_MAC_INTR	0x12C0		INTREQ04[22]
	PCI	INT_PCI_DMA	0x1280		INTREQ04[20]
group7	PTI1	PTI1_INTERRUPT	0x1360	INTPRI04[27:24]	INTREQ04[27]
	ClockGen	DCXO INTERRUPT	0x1340		INTREQ04[26]
	MAILBOXes	LX_AUDIO_ST40_INTERRUPT	0x1320		INTREQ04[25]
		LX_DELTAMU_ST40_INTERRUPT	0x1300		INTREQ04[24]
group8	USB2	EHCI1_INTERRUPT	0x13E0	INTPRI04[31:28]	INTREQ04[31]
		OHCI1_INTERRUPT	0x13C0		INTREQ04[30]
	FDMA0/1	FDMA_1_MBOX_INTERRUPT	0x13A0		INTREQ04[29]
		FDMA_0_MBOX_INTERRUPT	0x1380		INTREQ04[28]
group9	Audio	SPDIFPLYR_INTERRUPT	0x1460	INTPRI08[3:0]	INTREQ08[3]
		PCMRDR_INTERRUPT	0x1440		INTREQ08[2]
		PCMPLYR1_INTERRUPT (AUDIO SS)	0x1420		INTREQ08[1]
		PCMPLYR0_INTERRUPT (TVOUT SS)	0x1400		INTREQ08[0]

Table 54. ST40-300 on-chip peripheral interrupts (continued)

Group	Interrupt source		INTEVT code	IPR (bit numbers)	INTREQ/INTMSK (bit number)
group10	VIDEO DELTAMU	DELTAMU_MBE_INTERRUPT	0x14E0	INTPRI08[7:4]	INTREQ08[7]
		DELTAMU_PP_INTERRUPT	0x14C0		INTREQ08[6]
	NAND Controller	INT_NAND	0x14A0		INTREQ08[5]
	RESERVED	RESERVED	0x1480		INTREQ08[4]
group11	TVOUT/VTGs	AUX_VTG_INTERRUPT (1) OR AUX_VTG_INTERRUPT (0)	0x1560	INTPRI08[11:8]	INTREQ08[11]
		MAIN_VTG_INTERRUPT (1) OR MAIN_VTG_INTERRUPT (0)	0x1540		INTREQ08[10]
	VDP MAIN DISPLAY PIPE	MAIN_VDP_END_PROCESSING_IRQ	0x1520		INTREQ08[9]
		MAIN_VDP_FIFO_EMPTY_IRQ	0x1500		INTREQ08[8]
group12	HDMI/HDCP	HDCP_INTERRUPT	0x15E0	INTPRI08[15:12]	INTREQ08[15]
		HDMI_INTERRUPT	0x15C0		INTREQ08[14]
		HDMI_CEC_INT	0x15A0		INTREQ08[13]
		HDMI_CEC_WAKEUP_INT	0x1580		INTREQ08[12]
group13		RESERVED	0x1660	INTPRI08[19:16]	INTREQ08[19]
		RESERVED	0x1640		INTREQ08[18]
		RESERVED	0x1620		INTREQ08[17]
	PTI0	PTI0_INTERRUPT	0x1600		INTREQ08[16]
group14	RESERVED	RESERVED	0x16E0	INTPRI08[23:20]	INTREQ08[23]
	RESERVED	RESERVED	0x16C0		INTREQ08[22]
	RESERVED	RESERVED	0x16A0		INTREQ08[21]
	RESERVED	RESERVED	0x1680		INTREQ08[20]
group15	BLITTER DISPLAY	BDISP_CQ1_IRQP OR BDISP_CQ2_IRQP	0x1760	INTPRI08[27:24]	INTREQ08[27]
	RESERVED	RESERVED	0x1740		INTREQ08[26]
	USB1	EHCI_INTERRUPT	0x1720		INTREQ08[25]
		OHCI_INTERRUPT	0x1700		INTREQ08[24]
group16	RESERVED	RESERVED	0x17E0	INTPRI08[31:28]	INTREQ08[31]
	Key Scanner	KEY_SCANNER_INTERRUPT	0x17C0		INTREQ08[30]
		RESERVED	0x17A0		INTREQ08[29]
		RESERVED	0x1780		INTREQ08[28]

9.1.3 DeltaMU and LX_AUDIO ST231 interrupt network

The ST231 accepts 60 external interrupts (from 63 to 3). Interrupts 0 to 2 are Reserved to the ST231 internal timers. All the interrupts are maskable but with a single level of priority. Multiple level priority must be implemented in the software.

When used as an application processor, the DeltaMU ST231 processor receives a subset of the internal interrupts from the ST40 processor.

The interrupts are active high and are re-synchronized in the ST231 clk_bus clock domain.

When used as an application processor, the DeltaMU ST231 processor receives the same internal interrupts as ST40 processor except the interrupts generated by the DeltaMU coprocessors, the MES, ICAM3 interrupts, and Blitter Display interrupts.

The DeltaMu ST231 also receives the external interrupts through the ILC3 interrupt controller.

The AUDIO_LX receives audio peripherals and FDMA interrupts in order to manage audio applications without relying on the ST40 Host. Also, it executes soft modem (MAFE, DAA interrupts)

Table 55 describes the mapping of the interrupts on the DeltaMU ST231 interrupt controller.

Table 55. DeltaMU ST231 interrupts

Interrupt source		INT number
ST231 Timers	TIMER0_INTERRUPT	0
	TIMER1_INTERRUPT	1
	TIMER2_INTERRUPT	2
	RESERVED	3
Comms/PIO	PIO0_INTERRUPT	4
	PIO1_INTERRUPT	5
	PIO2_INTERRUPT	6
	PIO3_INTERRUPT	7
	PIO4_INTERRUPT	8
	PIO5_INTERRUPT	9
SSC	SSC0_INTERRUPT	10
	SSC1_INTERRUPT	11
	SSC2_INTERRUPT	12
	SSC3_INTERRUPT	13
Comms/UART	UART0_INTERRUPT	14
	UART1_INTERRUPT	15
	UART2_INTERRUPT	16
	UART3_INTERRUPT	17
Comms/MAFE	MAFE_INTERRUPT	18
Comms/PWM	PWM_INTERRUPT	19

Table 55. DeltaMU ST231 interrupts (continued)

Interrupt source		INT number
Comms/IRB	IRB_INTERRUPT	20
	IRB_WAKEUP_INTERRUPT	21
Comms/TTXT	TTXT_INTERRUPT	22
Comms/DAA	DAA_INTERRUPT	23
DVP	DVP_INTERRUPT	24
TS Merger	TS_MERGER_INTERRUPT	25
Ethernet GMAC	GMAC_MAC_INTR	26
	PMT_INT	27
ClockGen	DCXO_INTERRUPT	28
MAILBOX	ST40_TX_DELTAMU_INTERRUPT	29
PTI1	PTI1_INTERRUPT	30
FDMAs	FDMA_1_MBOX_INTERRUPT	31
	FDMA_0_MBOX_INTERRUPT	32
Audio	I2S2SPDIF_INTERRUPT0 OR I2S2SPDIF_INTERRUPT1 OR I2S2SPDIF_INTERRUPT2 OR I2S2SPDIF_INTERRUPT3	33
	SPDIFPLYR_INTERRUPT	34
	PCMRDR_INTERRUPT	35
	PCMPLYR1_INTERRUPT	36
	PCMPLYR0_INTERRUPT	37
RESERVED	RESERVED	38
TVOUT/VTGs	AUX_VTG_INTERRUPT (1) OR AUX_VTG_INTERRUPT (0)	39
	MAIN_VTG_INTERRUPT (1) OR MAIN_VTG_INTERRUPT (0)	40
Main Video Display Pipe	VDP_END_PROCESSING_IRQ	41
	VDP_FIFO_EMPTY_IRQ	42
HDMI/HDCP	HDCP_INTERRUPT	43
	HDMI_INTERRUPT	44
	HDMI_CEC_IRQ	45
	HDMI_CEC_WAKEUP_IRQ	46
BLITTER DISPLAY	BDISP_AQ1_IRQP OR BDISP_AQ2_IRQP OR BDISP_AQ3_IRQP OR BDISP_AQ4_IRQP	47

Table 55. DeltaMU ST231 interrupts (continued)

Interrupt source		INT number
RESERVED	RESERVED	48
	RESERVED	49
	RESERVED	50
PTI0	PTI0_INTERRUPT	51
RESERVED	RESERVED	54
RESERVED	RESERVED	55
USB1	EHCI0_INTERRUPT	56
	OHCI0_INTERRUPT	57
PADS	NMI_INTERRUPT	58
	RESERVED	59
External interrupts	EXT_INTERRUPT[0]	60
	EXT_INTERRUPT[1]	61
	EXT_INTERRUPT[2]	62
	EXT_INTERRUPT[3]	63

Caution: In case of USB signals, the usual naming convention is not used. In order to align with the STi7105 ballout names, this manual mentions two instances of USB as USB1 and USB2 rather than USB0 and USB1. Therefore, in this manual the first instance of USB is USB1 and the second instance is USB2.

The *Table 56* describes the mapping of the interrupts on the LX_AUDIO ST231 interrupt controller.

Table 56. LX_AUDIO ST231 interrupts

Interrupt source		INT number
ST231 timers	TIMER0_INTERRUPT	0
	TIMER1_INTERRUPT	1
	TIMER2_INTERRUPT	2
MAILBOX1	ST40_LX_AUDIO_INTERRUPT	3
RESERVED	RESERVED	17-4
Comms/MAFE	MAFE_INTERRUPT	18
RESERVED	RESERVED	22-19
Comms/DAA	DAA_INTERRUPT	23
RESERVED	RESERVED	30-24
Audio	RESERVED(CPXM_INTERRUPT)	31
	I2S2SPDIF_INTERRUPT	32
FDMA	FDMA_1_MBOX_INTERRUPT	33
	FDMA_0_MBOX_INTERRUPT	34

Table 56. LX_AUDIO ST231 interrupts (continued)

Interrupt source		INT number
Audio	SPDIFPLYR_INTERRUPT0	35
	SPDIFPLYR_INTERRUPT1	36
	SPDIFPLYR_INTERRUPT2	37
	SPDIFPLYR_INTERRUPT3	38
	PCMRDR_INTERRUPT	39
	PCMPLYR1_INTERRUPT	40
	PCMPLYR0_INTERRUPT	41
RESERVED	RESERVED	42-51
RESERVED	RESERVED	54
	RESERVED	55
RESERVED	RESERVED	56-62
Reserved	RESERVED	63

10 FDMA

10.1 Overview

The STi7105 integrates two multiple-channel general purpose DMA engines, FDMA0 and FDMA1. Each FDMA engine is a general purpose direct memory access controller capable of supporting 16 independent DMA channels. Their purpose is to move data efficiently from memory to memory, memory to peripheral, and peripheral to peripheral.

The FDMA supports free-running and paced transfers. The CPU sets up each DMA transfer by writing linked-lists of data structures in to main memory, then the CPU initializes the transfer by writing the pointer to the first node in the control word interface (CWI) of the FDMA. The FDMA then executes the necessary operations to complete the transfer and informs the CPU (through interrupts) after completion of the transfer.

The FDMA1 includes video stream parsing functionalities:

- video PES parsing and start-code detection (PES/SCD) for H264, VC1, AVS, and MPEG2
- dual PES parsing channel on same FDMA

10.1.1 FDMA0 and FDMA1 Partitioning

In STi7105, one FDMA is dedicated to serve real-time processes while the other FDMA handles the other processes, such as PES parsing, free-running, and non-critical paced channels.

The partitioning between FDMA0 and FDMA1 is as follows:

- FDMA0—real time paced channels: PCM players 0, 1, S/PDIF players, and SWTS (or playback)
- FDMA1—free-running channels, PES parsing, and non-real-time paced channels (that is, COMMS and PCI)

This partitioning is defined by software and is flexible. The Dreq crossbar-router, in front of the FDMAs, allows to route any paced peripheral Dreq signal to any FDMA Dreq input.

10.1.2 Peripheral and memory access

Each FDMA has two STBus Type-2 initiator ports. The Port0 (high priority port) has a direct connection to the paced peripherals. This direct connection minimizes the latency between the FDMA and peripherals. While defining the FDMA node, the Port0 is used to access the peripherals and Port1 (low priority port) is used to access the memory.

LMI can be accessed by FDMA0 and FDMA1.

10.1.3 FDMA processing power

The FDMA slim core frequency is configurable up to 450 MHz.

10.1.4 FDMA firmware

FDMA0 uses real-time firmware, and FDMA1 uses non-real-time firmware.

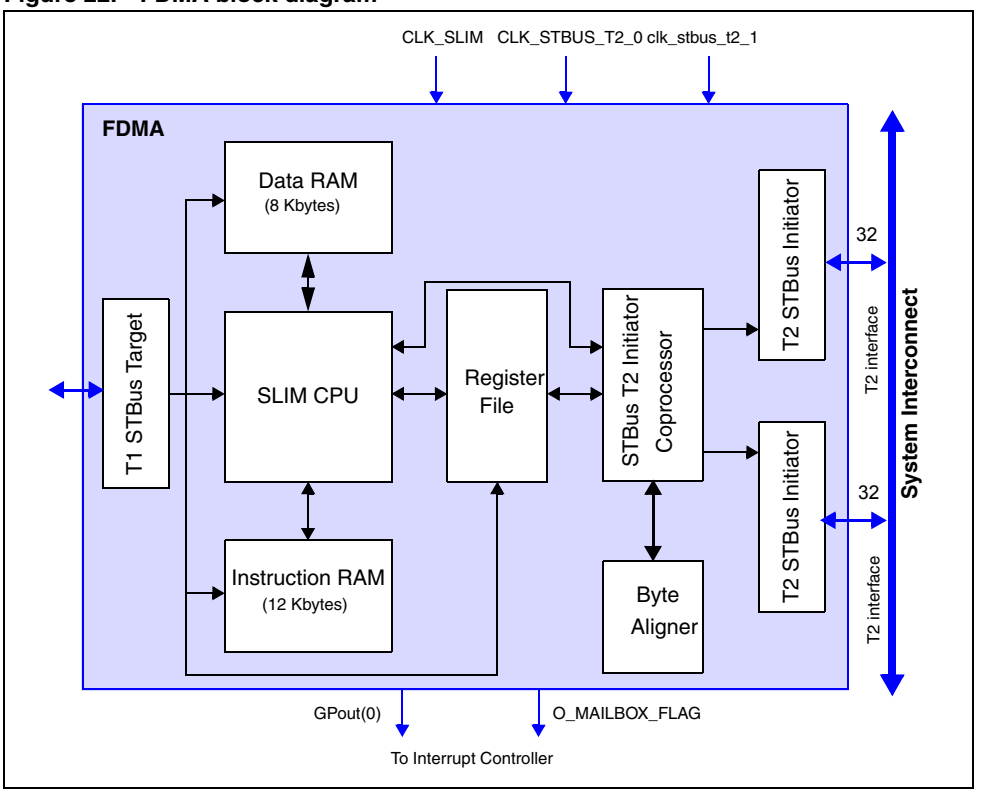
10.1.5 FDMA features

Following are the FDMA features:

- Support for 16 concurrent DMA channels
- Free-running transfer of aligned or unaligned data structure
  - Single location (0D)
  - Incrementing linear arrays (1D)
  - Incrementing rectangular arrays (2D)
- Transfer units of 1-32 bytes
- Up to 128 bytes message support
- Programmable opcode for paced transfer, support for up to 30 request generating peripherals (Dreq)
- Linked-list control allowing complex transfer sequence
- Video PES parsing (VC1, H264, MPEG2, AVS) on channel 0 and 1
- Audio compressed or PCM data output through S/PDIF player
- Hold off support per channel
- Secure/insecure transfer support
- NAND controller channel for AFM mode transfer to/from NAND devices

10.2 Block diagram

Figure 22. FDMA block diagram



Each FDMA comprises a SLIM CPU, an instruction memory, a data memory, peripherals, an STBus T1 target interface, and a SLIM STBus initiator coprocessor.

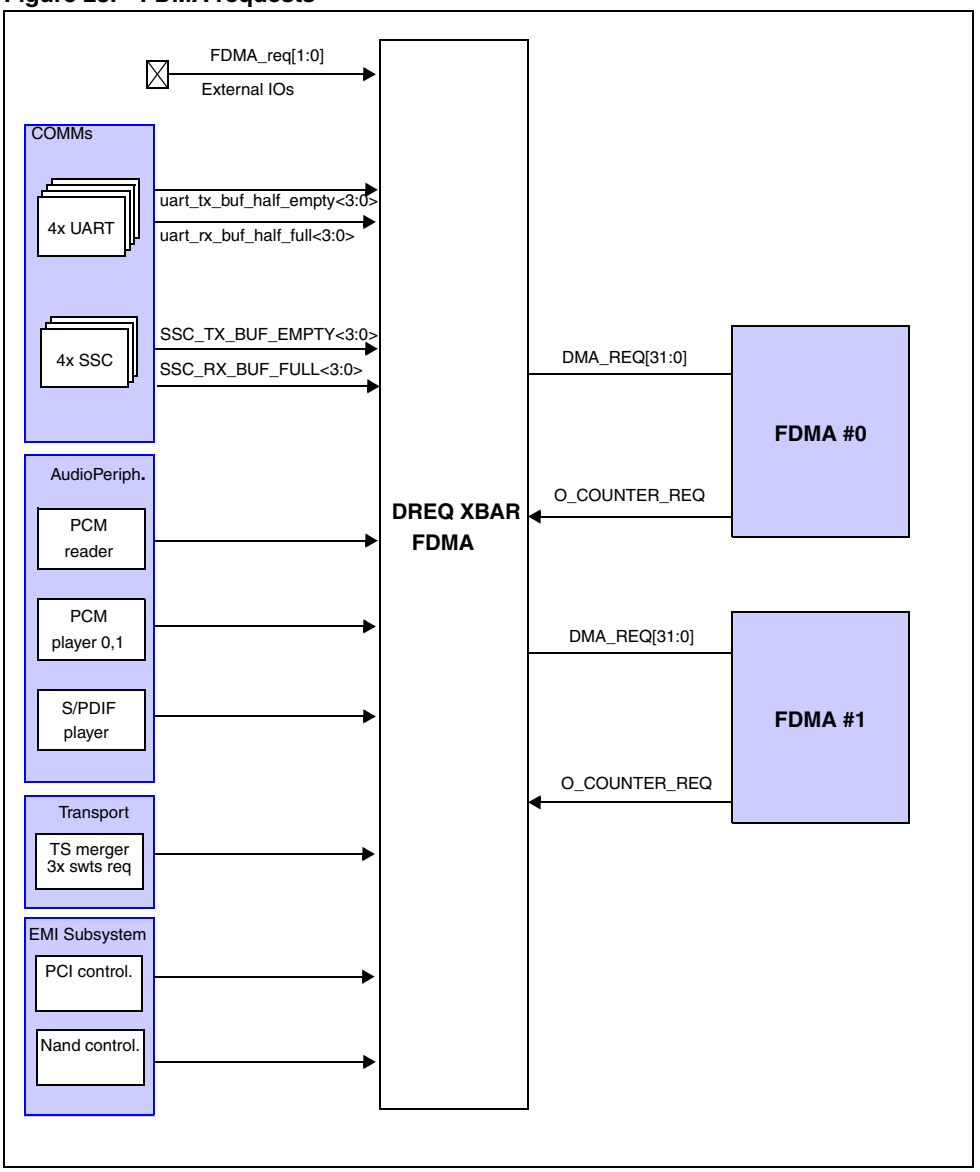
Each FDMA interfaces with the STBus interconnect through two STBus T2 initiator ports to execute the data transfers and through one STBus T1 target port to access the FDMA2 registers and memories.

Each STBus port has its own separate asynchronous clock input.

10.3 DMA requests

The FDMA receives a number of requests where pacing is required for flow control in the system. This signal is a simple high-level sensitive signal used in conjunction with a hold-off counter. The blocks generating a request signal are the audio peripherals (PCM players, PCM reader, and S/PDIF player), transport TSMerger (software stream), UARTs, SSCs, PCI controller, NAND controller and external DMA requests.

Figure 23. FDMA requests



The FDMA accepts up to 30 DMA requests or events that are used to drive the paced channels of the FDMA. Requests 0 and 31 are reserved for the counter request and are internally connected to the FDMA counter to provide timed DMA channels. Request #0 has the lowest priority and request #31 has the highest priority.

Table 57. FDMA request configuration

Unit	PACING SIGNAL	Xbar Input Index	FDMA #0	FDMA #1	FDMA DREQ line index	Opcode	Transfer Size	Comments
PCI controller	PCI_HALF_FULL	52	x		10	ST32	ST32 x4	
NAND controller	NAND_AFM_DATA_REQ	50		x	28	ST32	ST32 x1	Data request in Advanced Flex mode
	NAND_AFM_SEQ_REQ	49		x	27	LD32	LD32 xn	Sequence request in Advanced Flex mode
IRB/UHF	IRB_UHF_RX_BUFFER_FULL	46		x	19	LD4	LD4 x1	IRB requests
	IRB_UHF_RX_BUFFER_HALF 8FULL	45		x	18	LD4	LD4 x1	
TeleText DENC #0	TELETEXT_DREQ	42		x	30	ST4	ST4 x11	Ttxt FIFO is 2x48 bytes = 2 lines
HDMI S/PDIF Player	HDMI_SPDIF_DREQ	40	x		30	ST4	ST4 x4	Includes a 24 bytes FIFO
HDMI PCM Player #0	HDMI_PCM_DREQ	39	x		29	ST4	ST4 x20	Includes a 160 bytes FIFO
PCM reader	PCMIN_DREQ	37	x		27	LD4	LD4 x2	Includes a 8 bytes FIFO
PCM Player #1	PCMOUT1_DREQ	34	x		23	ST4	ST4 x20	Includes a 160 bytes FIFO
CSS/CPxM encryption	CPXM_ENCRYPT_OUT_DREQ	32	x		21	LD4	LD4 x32	128 bytes fifo
	CPXM_ENCRYPT_IN_DREQ	31	x		20	ST4	ST4 x32	
CSS/CPxM decryption	CPXM_DECRYPT_OUT_DREQ	30	x		19	LD4	LD4 x32	128 bytes fifo
	CPXM_DECRYPT_IN_DREQ	29	x		18	ST4	ST4 x32	
External DMA req	EXTDMAREQ1_DREQ	28	x		16	ST/LD32	ST/LD32 x4	
	EXTDMAREQ0_DREQ	27		x	21	ST/LD32	ST/LD32 x4	
	EXTDMAREQ2_DREQ	3	x		17	ST/LD32	ST/LD32 x4	
	EXTDMAREQ3_DREQ	4		x	20	ST/LD32	ST/LD32 x4	
UART#3 Tx	UART3_TX_HALF_EMPTY	26		x	16	ST4	ST4 x1	
UART#2 Tx	UART2_TX_HALF_EMPTY	25		x	15	ST4	ST4 x1	
UART#1 Tx	UART1_TX_HALF_EMPTY	24		x	14	ST4	ST4 x1	
UART#0 Tx	UART0_TX_HALF_EMPTY	23		x	13	ST4	ST4 x1	
UART#3 Rx	UART3_RX_HALF_FULL	22		x	12	LD4	LD4 x1	
UART#2 Rx	UART2_RX_HALF_FULL	21		x	11	LD4	LD4 x1	

Table 57. FDMA request configuration (continued)

Unit	PACING SIGNAL	Xbar Input Index	FDMA #0	FDMA #1	FDMA DREQ line index	Opcode	Transfer Size	Comments
UART#1 Rx	UART1_RX_HALF_FULL	20		x	10	LD4	LD4 x1	
UART#0 Rx	UART0_RX_HALF_FULL	19		x	9	LD4	LD4 x1	
SSC#3 Tx	SSC3_TX_BUF_EMPTY	17		x	7	ST4	ST4 x1	
SSC#2 Tx	SSC2_TX_BUF_EMPTY	16		x	6	ST4	ST4 x1	
SSC#1 Tx	SSC1_TX_BUF_EMPTY	15		x	5	ST4	ST4 x1	
SSC#0 Tx	SSC0_TX_BUF_EMPTY	14	x		15	ST4	ST4 x1	
SSC#3 Rx	SSC3_RX_BUF_FULL	12		x	3	LD4	LD4 x1	
SSC#2 Rx	SSC2_RX_BUF_FULL	11		x	2	LD4	LD4 x1	
SSC#1 Rx	SSC1_RX_BUF_FULL	10		x	1	LD4	LD4 x1	
SSC#0 Rx	SSC0_RX_BUF_FULL	9	x		14	LD4	LD4 x1	
TS Merger	SWTS0_REQ	7		x	24	ST32	ST32 x1	Software Transport Stream play through PTI4L.
	SWTS1_REQ	6		x	23	ST32	ST32 x1	
	SWTS2_REQ	5		x	22	ST32	ST32 x1	
HDMI AVI buffer	AVI_BUFF_EMPTY	2		x	26	ST4	ST4 x1	Should be handled by Host CPU not FDMA
FDMA #1 counter	FDMA1_COUNTER_REQ	1		x	0			Connects counter output to dreq #0
FDMA #0 counter	FDMA0_COUNTER_REQ	0	x		0			Connects counter output to dreq #0

Table 58. FDMA requests table

Request source	REQUEST SIGNAL	Request index	Description
FDMA# counter	O_COUNTER_REQ	31:0	FDMA internal counter output, used for timed DMA-channel.
FDMA# cross-bar	REQ_OUT[31:0]		
FDMA# counter	O_COUNTER_REQ		FDMA internal counter output, used for timed DMA-channel.

Note: # in Table 58 is 0 or 1.

10.4 Examples of DMA Data flow

The following figures describe various DMA data flows.

Figure 24. DMA data flows (I)

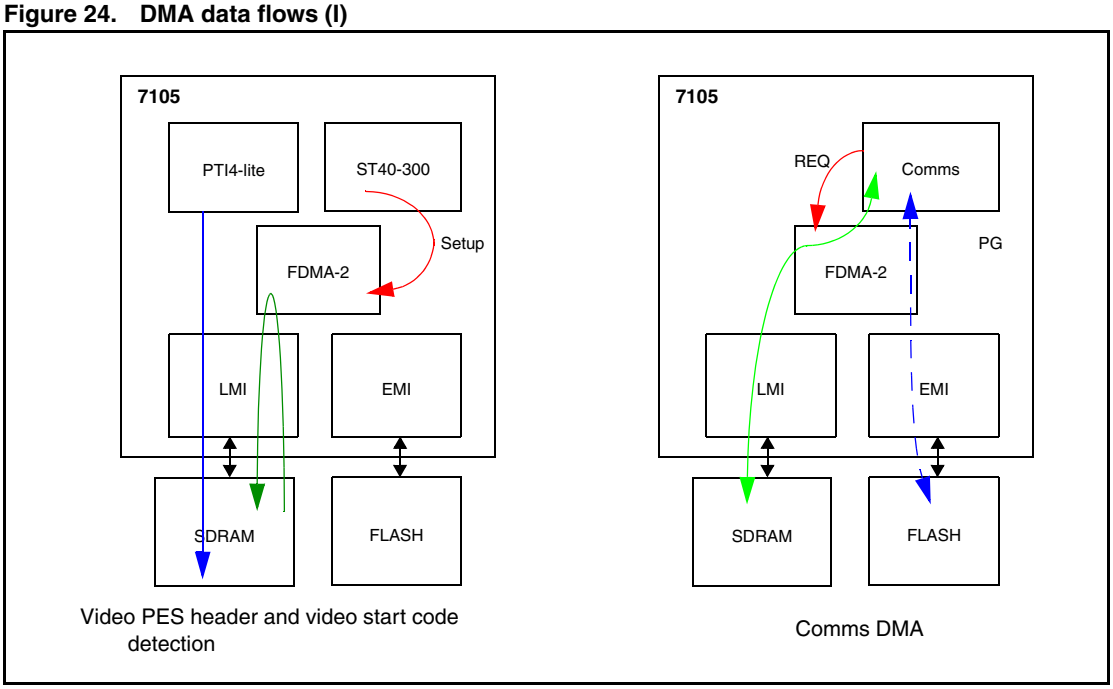
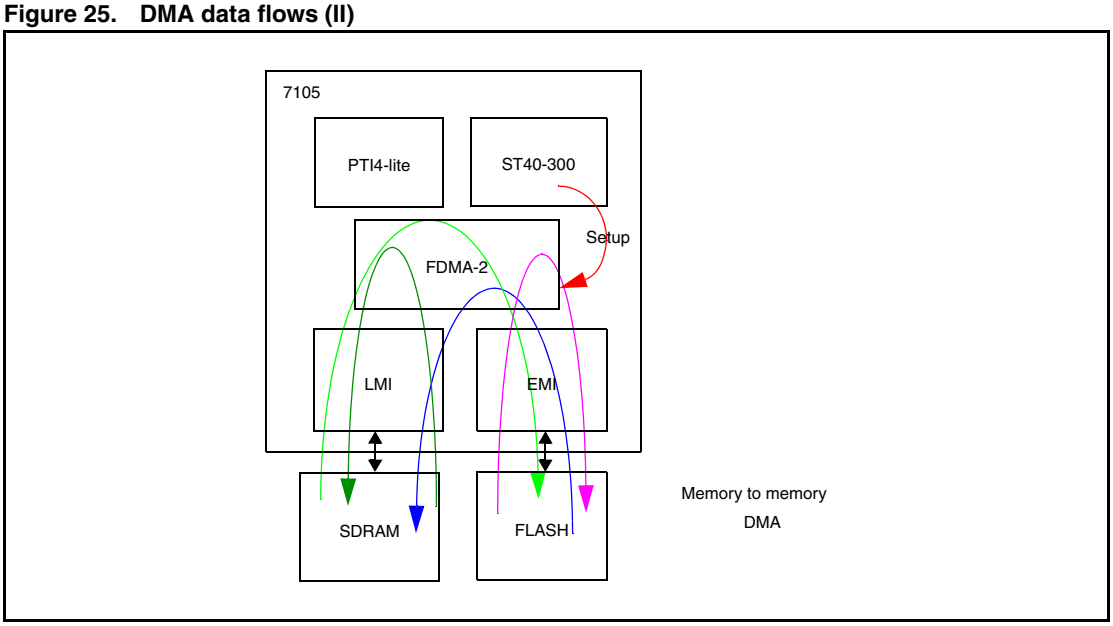


Figure 25. DMA data flows (II)



11 Clocking

The STi7105 includes four clock generator subsystems:

- ClockGen A: 2x PLLs main CPU, transport, and interconnect clocks
- ClockGen B: 2x FreqSynth: video, display, and peripheral clocks
- ClockGen C: 1x FreqSynth and audio clocks
- ClockGen D: 1x PLL memory clocks

11.1 Clock input/output pins

The SYSCLKIN/SYSCLKOSC pair is a crystal interface, a part of the SATA analog interface, integrating an oscillator requiring 30 MHz crystal. In addition to driving the SATA and two USB interfaces, the clock can be used as a reference clock to generate the Group A, B, C, and D clocks.

The SYSCLKINALT input provides an alternate reference clock for the Group A, B, C, and D clocks instead of using an oscillator clock inside the SATA Phy. The default state is to use the 30 MHz SATA clock, however, an alternate reference clock can be selected through a configuration register. The SYSCLKINALT pin is driven by either a 27 MHz fixed or voltage controllable oscillator or a fixed 30 MHz oscillator. A PWM output is provided as a part of an external VCXO configuration.

The internal clocks can be observed:

- ClockGen A through the TRIGGEROUT pad
- ClockGenB through the SYSCLKOUT pad
- ClockGen C frequency synthesizer #2 through the PIO10[3] pad
- ClockGen D through the LMICLKOUT pad

Encoder clock recovery

The STi7105 integrates a clock recovery module to recover the encoder clock. This module (DCXO) uses the digitally controllable frequency synthesizers and an integrated digital clock recovery module. This feature replaces the external VCXO functionality and allows the usage of a fixed oscillator. Nevertheless, the external VCXO functionality is still available.

When the external VCXO functionality is used, the VCXO oscillator must be connected to the SYSCLKINALT, and the SYSCLKIN is connected either to a fixed oscillator or to the VCXO oscillator.

When the DCXO is used the SYSCLKIN pin is connected to a fixed oscillator, and the SYSCLKINALT is connected either to the SYSCLKIN or left unconnected (in that case the SATA/USB 30 MHz clock is used).

The system counter inside the programmable transport interface (PTI), which is used to compare the arriving PCRs, is clocked by the recovered 27 MHz clock generated by the Clock Generator B.

Figure 26. STi7105 clocking scheme sources with optional external VCXO

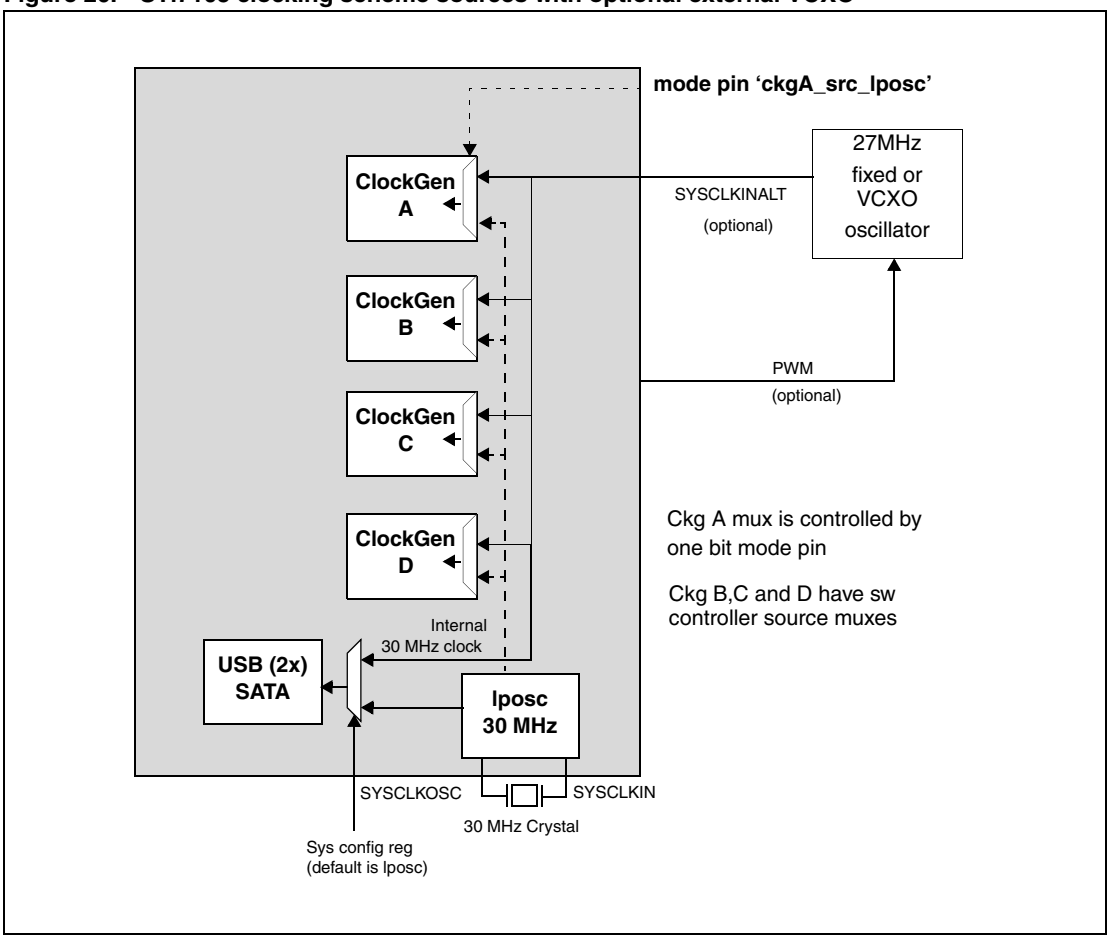


Table 59. STi7105 clocking scheme sources

ClockGen module	Reset default STi7105	Clock selection
A	Selection by modepin	STi7105 has mode pin to select default clock reference for ClockGen A
B	SATA/USB LP-Osc 30 MHz	ClockGen B config register
C	SATA/USB LP-Osc 30 MHz	Audio SS config register
D	SATA/USB LP-Osc 30 MHz	System config register
USB/SATA	SATA/USB LP-Osc 30 MHz	System config register

11.2 Clock domains

The *Table 60* describes the clocking of the functional units integrated in STi7105. Column S is the clock source, indicating A, B, C, D for ClockGen, or T for Tap.

Table 60. Functional blocks clocking

Block	Clock pin	Clock signal	S	Max frequency	Comment
TMC					
TMC	TCK	TCK	T	50 MHz	JTAG clock from pad
MAIN Interconnect and NOC					
STNoC		CLK_IC_STNOC	A	400 MHz	CPU processing clock
N_CPU		CLK_IC_IF_200	A	200 MHz	
N_PERIPH		CLK_IC_IF_100	A	100 MHz	
RESERVED		RESERVED			
N_DVP		CLK_IC_DISP_200	A		
N_DISPLAY		CLK_IC_DISP_200	A		
N_COMPO		CLK_IC_COMPO_200	A		
N_DMU		CLK_BLIT_PROC	A	266 MHz	
N_PCI		CLK_EMI_MASTER	A		
N_PCI_TS		CLK_IC_TS_200	A		
N_TS		CLK_IC_TS_200	A		
N_IF		CLK_IC_IF_100	A		
N_BDISP		CLK_IC_BDISP_200	A		
N_CPU_REG		CLK_IC_IF_100	A		
SYSTEM					
SYSCLKINALT	pad	SYSCLKINALT	IN	30 MHz	These are the clock sources, from the two possible inputs Clock from pad Clock from SATA/USB osc
LPOSC	ZI	CLK_LPOSC_30		30 MHz	
ClockGenA	CLK_STBUS	CLK_IC_IF_100	A	100 MHz	
	CLK_OSC_A	NOT USED			
	CLK_OSC_B	CLK_LPOSC_30		30 MHz	from SATA/USB oscillator
	CLK_OSC_C	SYSCLKINALT		27/30 MHz	direct from pad crystal
	CLK_OSC_D	NOT USED			

Table 60. Functional blocks clocking (continued)

Block	Clock pin	Clock signal	S	Max frequency	Comment
ClockGenB	CLK_IC	CLK_IC_IF_100	A		STBus clock
	CLK_OSC_A	NOT USED			
	CLK_OSC_B	CLK_LPOSC_30		30 MHz	from SATA/USB oscillator
	CLK_OSC_C	SYSCLKINALT		27/30 MHz	direct from pad crystal
	CLK_OSC_D	NOT USED			
ClockGen C	CLK_OSC_A	NOT USED			
	CLK_OSC_B	CLK_LPOSC_30		30 MHz	from SATA/USB oscillator
	CLK_OSC_C	SYSCLKINALT		27/30 MHz	direct from pad crystal
	CLK_OSC_D	NOT USED			
ClockGenD	CLK_OSC_A	NOT USED			
	CLK_OSC_B	CLK_LPOSC_30		30 MHz	from SATA/USB oscillator
	CLK_OSC_C	SYSCLKINALT		27/30 MHz	direct from pad crystal
	CLK_OSC_D	NOT USED			
MAIN CPU					
SH4-300	CLK_ST40_ICK	CLK_SH4_ICK	A	450 MHz	CPU processing clock
	CLK_ST40_PCK	CLK_IC_IF_100	A	100 MHz	Interface clock
Mailbox	CLK	CLK_IC_IF_100	A	100 MHz	Type 1 interconnect clock
DMA					
BlitterDisplay	IC_CK	CLK_IC_BDISP_200	A	200 MHz	Type 3 interconnect clock
	CPU_CK	CLK_IC_IF_100	A	100 MHz	Type 1 interconnect clock
	BDISP_CK	CLK_BLIT_PROC	A	266 MHz	Bdisp processing clock
FDMA0	CLK_SLIM	CLK_FDMA0	A	450 MHz	SLIM Processing clock
	CLK_STBUS_T2_0	CLK_IC_IF_100	A	100 MHz	High priority FDMA port
	CLK_STBUS_T2_1	CLK_IC_TS_200	A	200 MHz	Low priority FDMA port
	CLK_STBUS_T1	CLK_IC_IF_100	A	100 MHz	Type 1 interconnect clock

Table 60. Functional blocks clocking (continued)

Block	Clock pin	Clock signal	S	Max frequency	Comment
FDMA1	CLK_SLIM	CLK_FDMA1	A	450 MHz	SLIM Processing clock
	CLK_STBUS_T2_0	CLK_IC_IF_100	A	100 MHz	High priority FDMA port
	CLK_STBUS_T2_1	CLK_IC_TS_200	A	200 MHz	Low priority FDMA port
	CLK_STBUS_T1	CLK_IC_IF_100	A	100 MHz	Type 1 interconnect clock
DISPLAYS COMPOSITION					
HD Display	CLK_PROC	CLK_DISP_PIPE_200	A	200 MHz	Display pipeline processing clock
	CLK_SYS	CLK_IC_DISP_200	A	200 MHz	Type 3 interconnect clock
	CLK_PIX	CLK_DISP_HD	B	148.5 MHz	Display-to-Compositor pixel clock
	CLK_REG	CLK_IC_DISP_200	A	200 MHz	Type 1 interconnect clock
SD Display	CLK_DISP	CLK_DISP_PIPE_200	A	200 MHz	Display pipeline processing clock
	CLK_IC	CLK_IC_DISP_200	A	200 MHz	Type 3 interconnect clock
	CLK_PIXEL	CLK_DISP_ID or CLK_DISP_HD	B	13.5 MHz in SD and 148.5 MHz in HD (PIP)	Display-to-Compositor pixel clock
	CLK_REG	CLK_IC_DISP_200	A	200 MHz	Type 1 interconnect clock
Compositor	ST_CK	CLK_IC_COMPO_200	A	200 MHz	Type 3 Interconnect clock
	MAIN_CK	CLK_DISP_HD	B	148.5 MHz Max	Main mixer (HD) pixel clock
	AUX_CK	CLK_DISP_ID	B	108 MHz Max	Aux mixer (SD) pixel clock
	VP2_CK	CLK_DISP_ID	B	108 MHz Max	Video2 pixel clock (SD or HD)
	GDP3_CK	CLK_DISP_HD or CLK_DISP_ID (CLK_GDP3)	B	148.5 MHz	GDP3 pixel clock (HD or SD)

Table 60. Functional blocks clocking (continued)

Block	Clock pin	Clock signal	S	Max frequency	Comment
VIDEO OUTPUT STAGE					
DENC	CLK_IC	CLK_IC_IF_100	A	100 MHz	Type 1 interconnect clock
	PIX_CLK	CLK_PIX_SD	B	27MHz Max	DENC processing clock
	PIX_CLK_FROM_PAD	VIDINCLK FROM PAD	B	27 MHz	This clock is used by DVP in functional mode. Used for testing also.
RGB-to-YCbCr 601/709/240M	CLK_DISP_HD	CLK_DISP_HD	B	148.5 MHz	HD Display Clock
DWCS AWG	CLK_IC	CLK_IC_IF_100	A	100 MHz	Type 1 interconnect clock
	CLK_PIX	CLK_PIX_SD	B	27MHz	SD pixel input clock
UpSampler	CLK_DISP_HD	CLK_DISP_HD	B	148.5 MHz	HD pixel input clock
	CLK_PIXEL_SD	CLK_PIX_SD	B	27 MHz	SD pixel input clock
	CLK_PIXEL_HD	CLK_PIX_HD	B	148.5 MHz	Pixel output clock
VTG0	CLK_DISP	CLK_DISP_HD	B	148.5 MHz	HD display clock
VTG1	CLK_DISP	CLK_DISP_SD	B	13.5 MHz	ID display clock
HD Video DAC	CLK	CLK_PIX_HD	B	148.5 MHz	HD Video DAC sampling clock
SD Video DAC	CLK	CLK_PIX_SD	B	108 MHz	SD Video DAC sampling clock
AUDIO DECODING					
LX- Audio	CLK_CPU	CLK_LX_AUD_CPU	A	450 MHz Max	LX processing clock
	CLK_BUS	CLK_IC_100	A	100 MHz	Peripheral Interconnect clock
Audio Glue	CLK_IC	CLK_IC_IF_100	A	100 MHz	Peripheral Interconnect clock in audio peripherals
PCM player 1 see audio clocking scheme	CLK_STBUS	CLK_IC_IF_100	A	100 MHz	Interconnect clock
	CLK_PCM	CLK_PCM1	C	50 MHz Max	PCM oversampling clock (256xFs) = 256x 192kHz
PCM reader see audio clocking scheme	CLK_STBUS	CLK_IC_IF_100	A	100 MHz	Interconnect clock
	CLK_I2S	I2S_SCLK	C	5 MHz	PCM input serial clock

Table 60. Functional blocks clocking (continued)

Block	Clock pin	Clock signal	S	Max frequency	Comment
Audio DAC see audio clocking scheme	MCLK	CLK_PCM1	C	256 x Fs, 15 MHz Max	Oversampling clock (Fs = 48 kHz Max)
VIDEO DECODING					
DeltaMu ST231	CLK_CPU	CLK_LX_DMU_CPU	A	450 MHz	LX Processing clock
	CLK_BUS	CLK_IC_IF_100	A	100 MHz	Peripheral Interconnect clock
DeltaMu Hdw	CLK_VID	CLK_VID	A	225 MHz (clk_lx_dh_cpu/2)	DeltaMu Hdw processing clock
	CLK_BUS (CLK_IC_DELTA_200 ON SS)	CLK_BLIT_PROC	A	266 MHz	DeltaMu STBus initiator and target port clock
	CLK_PP	CLK_PP	B	150 MHz	DeltaMu Hdw Pre-processor clock
TRANSPORT					
TSMerger	CLK_SYSTEM	CLK_IC_TS_200	A	200 MHz	Interconnect clock
	CLK_27MHZ	CLK_PIX_SD	B	27 MHz	For free running and programmable counters (timestamp)
PTI	CLK_SYSTEM	CLK_IC_TS_200	A	200 MHz	200 MHzType 1 & 2 Interconnect clock
	CLK_TIMER	CLK_PIX_SD	B	27 MHz Max	PCR Timer clock for AV services
RESERVED	RESERVED	RESERVED		-	-
CONNECTIVITY					
GMAC	CLK100	CLK_IC_IF_100	A	100 MHz	Type 1 and 2 interconnect clock
	PAD	CLK_ETHERNET	A	75 MHz	potential clock for Ethernet interface
	PHY_TX_CLK PHY_TX_CLK_PS	PAD		75 MHz	Timing reference for MII RX interface (_ps is inverted clock)
	PHY_RX_CLK PHY_RX_CLK_PS	PAD		75 MHz	Timing reference for MII TX interface (_ps is inverted clock)
	PHY_RMII_CLK	CLK_ETHERNET (VIA PAD)	A	50 MHz	Clock to PHY in MII mode (output through PIOX(Y) pad) REF clock in RMII mode (input or output through PIOX(Y) pad)

Table 60. Functional blocks clocking (continued)

Block	Clock pin	Clock signal	S	Max frequency	Comment
USB2.0 Host	STBUS_CLOCK	CLK_IC_IF_100	A	100 MHz	Type 1 & 2 Interconnect clock
	CLOCK48	CLK_USB48	B	48 MHz	From USB FSyn pending confirmation that PHY will supply
	PHY_CLK_I	CLK_USB60		60 MHz	From USB PLL
	UTMI_PHY_CLK_I	CLK_PHY_USB60		60 MHz	From USB2.0 Phy
USB2.0 Phy	REFCLK_CUST	CLK_USB60		60 MHz	From USB PLL
	REFCLKBYPASS_CUST	TST_CLK_USB60		60 MHz	From pad for test
HDMI Frame formatter	STBUS_CLOCK	CLK_IC_IF_100	A	100 MHz	Type-1 interconnect clock
	PIX_CLOCK	CLK_DISP_HD	B	148.5 MHz Max	Pixel clock
	TMDS_CLOCK	CLK_TMDS_HDMI	B	148.5 MHz Max	TMDS clock is 1x or 2x pixel clock
	BCH_CLOCK	CLK_BCH_HDMI	B	148.5 MHz Max	BCH clock is 2x or 4x TMDS clock
PCM player 0	CLK_PCM	CLK_PCM0	C	50 MHz Max	PCM oversampling clock (256xFs, Fs = 192 kHz Max)
S/PDIF player	SPDIF_CLOCK	CLK_PCM2	C	15 MHz Max	S/PDIF clock 256xFs = 256 x 48 kHz
HDMI Analog	CKPXDLL	CLK_PLL_HDMI_PHY	B	148.5 MHz	From rejection PLL
	CKPX	CLK_TMDS_HDMI	B	74.25 MHz	From ClockGen B
DVP	ST_CK	CLK_IC_IF_200	A	200 MHz	Type 1 & 2 interconnect clock
	DVP_PIX2_CK	CLK_DVP	B	148.5 MHz in HD mode	D1 video stream clock provided by ClockGen B when in compositor capture mode
		VidInClk from pad	B	148.5 MHz in HD mode	D1 video stream clock

Table 60. Functional blocks clocking (continued)

Block	Clock pin	Clock signal	S	Max frequency	Comment
SATA HOST	CLK_STBUS	CLK_IC_IF_100	A	100 MHz	Type 1 & 2 interconnect clock
	CLK_RBC0	CLK_RBC0		75 MHz	Recovery clock, synchronous with received data (75 MHz) (provided by SATA PHY)
	CLK_ASIC	CLK_ASIC		75 MHz	Used into transport and link layer blocks (75 MHz) (provided by SATA PHY)
	CLK_RXOOB	CLK_SATA		30 MHz	Used to OOB detection and also used as possible reference clock for ClockGen B and C (provided by SATA PHY)
MEMORY INTERFACES					
EMI-PCI Subsystem	SYSTEM_CLOCK	CLK_EMI_MASTER	A	100 MHz	EMI & PCI can also be clocked from external pads, STBus side will be synchronized to SYSTEM_CLOCK
	PCI_CLOCK	CLK_PCI	A	33/66 MHz	
	DEVICE_CLK_IN	EMI_FLASHCLK (PAD)		50 MHz	EMI SS clock when in EMI clock slave mode or PCI clock when in PCI clock slave mode.
GPLMI0	MCLK	MCLK		400 MHz	From GPLMI0 padlogic after divider and DLL
GPLMI0PL	LMI_PL_MCLK	LMI_PL_MCLK	D	800 MHz	From PLL
RESERVED	RESERVED	RESERVED			
COMMS					
COMMs	CLK_IC	CLK_IC_IF_100	A	100 MHz	Type 1 & 2 interconnect clock
	LP_CLOCK	CLK_LPC	B	46.875 kHz	Low power clock
	CLK_DAA	CLK_DAA	B	32.768 MHz	DAA clock
	CLK_DSS	CLK_DSS	B	36.864 MHz	Smart card clock

11.3 CPUs and interconnect clock generation (ClockGen A)

The reference clock can be either an internal 30 MHz clock signal or a clock connected to the SYSCLKINALT pin. The reset value is defined by mode pin[0] value.

This ClockGen is responsible for clocking the following units.

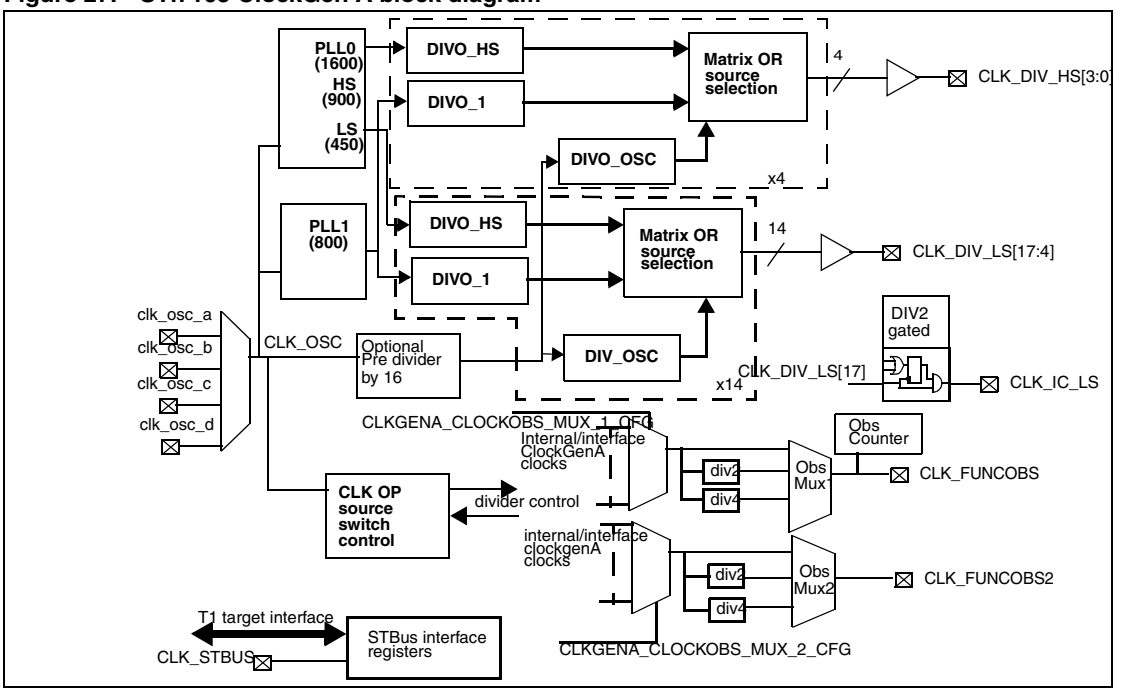
Table 61. ClockGen A mapping

Channel		30	900	450	800	
div#	**STi7105 Clk name**	**OSC**	**PLL0 HS**	**PLL0 LS**	**PLL1**	**Comment**
CLK_DIV_HS[0]	CLK_IC_STNOC		/3=300		/3=266 /2=400	
CLK_DIV_HS[1]	CLK_FDMA0		/3=300		/3=266 /2=400	
CLK_DIV_HS[2]	CLK_FDMA1					
CLK_DIV_HS[3]	NOT USED				/3=266 /4=200	
CLK_DIV_LS[4]	CLK_SH4_ICK	/32=0.95		/1=450		
CLK_DIV_LS[5]	CLK_IC_IF_100				/8=100	
CLK_DIV_LS[6]	CLK_LX_DMU_CPU			/1=450	/2=400	
CLK_DIV_LS[7]	CLK_LX_AUD_CPU			/1=450	/2=400	
CLK_DIV_LS[8]	CLK_IC_DISP_200				/4=200	
CLK_DIV_LS[9]	CLK_IC_BDISP_200				/4=200	
CLK_DIV_LS[10]	CLK_IC_TS_200				/4=200	
CLK_DIV_LS[11]	CLK_DISP_PIPE_200				/4=200	
CLK_DIV_LS[12]	CLK_BLIT_PROC				/3=266	DeltaMu IC at 266 MHz
CLK_DIV_LS[13]	CLK_ETHERNET_PHY			/6=75 /9=50 /18=25		
CLK_DIV_LS[14]	CLK_PCI				/12=66 /24=33	
CLK_DIV_LS[15]	CLK_EMI_MASTER					
CLK_DIV_LS[16]	CLK_IC_COMPO_200					
CLK_DIV_LS[17]	CLK_IC_IF_200					two outputs; full speed and half speed
CLK_IC_LS	not used					

11.3.1 Block diagram

At POR, all clocks are output at 30 MHz (x1 from USB/SATA osc). The *Figure 27* shows the STi7105 ClockGen A block diagram.

Figure 27. STi7105 ClockGen A block diagram



11.3.2 Clock–off and reduced power

Clocks in group A can be slowed to less than 1MHz, through register programming or low power signal from LPC, or stopped.

11.3.3 Clock observability

All the clocks of the ClockGen A can be observed on the TRIGGEROUT pad.

The CLOCK_OUT_SEL[5:0] bits of the CLKGNA_CLKOBS_MUX_*X*_CFG (where *X* = 1 and 2) configuration register is provided to select the clock which will be routed to the pad.

11.4 Video decoder, display, and Comms clock generation (ClockGen B)

This ClockGen is mainly responsible for generating the clocks used by the video display pipeline. This includes the following units:

- SD and HD displays
- compositor
- video output stage (formatters, HDMI, and DENC)
- HD and SD video DACs

In addition, ClockGen B also generates some processing clocks for the following units:

- comms—LPC/PWM

ClockGen B comprises two digitally controlled frequency synthesizers (FS0 and FS1). The reference clock can be either an internal 30 MHz clock (USB) signal or a clock connected to the SYSCLKINALT pin. The reset value is the SATA Phy clock.

The ClockGen B also includes a digital clock recovery module to recover the encoder clock.

The block diagram of ClockGen B is shown in *Figure 29*.

11.4.1 Clock signals

The *Table 62* lists the group B clocks with their maximum frequency.

Table 62. Clock generator B

Clock name	Maximum frequency (MHz)	Description
CLK_PIX_HD	148.5	HD pixel clock
CLK_PIX_SD	148.5	SD pixel clock (support HD format)
CLK_DISP_HD	148.5	HD display clock
CLK_DISP_ID	13.5	SD display clock
CLK_GDP3	148.5	GDP3 pixel clock (HD or SD)
CLK_656	148.5	DVO0 pixel clock
CLK_PP	150	Delta Preprocessors
CLK_DAA	32.768	DAA clock
CLK_DSS	36.864	DSS clock
CLK_LPC	46.875	Low Power Controller clock
CLK_TTXT	27	Teletext clock
CLK_SERLZR_HDMI	148.5	HDMI serializer clock
CLK_BCH_HDMI	148.5	HDMI BCH clock
CLK_TMDS_HDMI	148.5	HDMI TMDS clock
CLK_656_1	148.5	DVO1 pixel clock

The frequency of all the clocks is programmable. Especially, the video clocks must be set up with respect to the display standard in use.

The *Table 63* gives some programming examples with respect to the targeted application.

Table 63. Video clock domains by applications

Application			CLK_PIXEL_HD	CLK_DISP_HD	CLK_PIXEL_SD	CLK_DISP_ID	CLK_656	CLK_TMDS_HDMI	CLK_GDP3
Main (1080p60) & Aux	Main 1080p/60Hz or 720p/60Hz (HD) Aux: 480i / 576i (SD)	GDP3 on main	148.5	148.5	27	13.5	148.5	148.5	148.5
		GDP3 on aux	148.5	148.5	27	13.5	148.5	NA	13.5

Table 63. Video clock domains by applications

Application			CLK_PIXEL_HD	CLK_DISP_HD	CLK_PIXEL_SD	CLK_DISP_ID	CLK_656	CLK_TMDS_HDMI	CLK_GDP3
Main (HD) & Aux (HD)	Main 1080i/30Hz or 720p/60Hz (HD) Aux: 1080i/30 Hz or 720p/60Hz(HD) (no DACs outputs)	GDP3 on main	148.5	74.25	27	13.5	148.5	74.25	74.25
		GDP3 on aux	148.5	148.5	148.5	74.25	148.5	NA	74.25
Main & Aux	Main 1080i/30Hz or 720p/60Hz (HD) Aux: 480i / 576i (SD)	GDP3 on main	148.5	74.25	27	13.5	148.5	74.25	74.25
		GDP3 on aux	148.5	74.25	27	13.5	148.5	NA	13.5
Main & Aux	Main 480p/576p (ED) Aux: 480i / 576i (SD)	GDP3 on main	108	27	27	13.5	54	27	27
		GDP3 on aux	108	27	27	13.5	54	NA	13.5
Alternate (main to denc)	Main 480i/576i (SD) Aux: 480i / 576i (SD)	GDP3 on main	108	13.5	27	NA	27	27	13.5
Main & Aux SCART	Main 1080i/30Hz or 720p/60Hz (HD) Aux: 480i / 576i (SD)	GDP3 on main	108 (from FS0)	74.25	27	13.5	148.5	74.25	74.25
		GDP3 on aux	148.5	74.25	27	13.5	148.5	NA	13.5
Main & Aux pseudo-SCART	Main 480i/ 576i (SD) - TV (video + gfx) Aux: 480i / 576i (SD) - VCR (video only)	GDP3 on main	108	13.6	27	13.6	NA	NA	13.5
		GDP3 on aux	108	13.5	27	13.5	NA	NA	13.5

11.4.2 Clock generator B startup configuration

After the reset phase, the ClockGen B is by default configured with a 13.5 MHz display clock on both the Main and Auxiliary video outputs.

Table 64. Clock generator B default configuration

Clock name	Frequency (MHz)	Description
CLK_PIX_HD	148.5	HD pixel clock
CLK_PIX_SD	148.5	SD pixel clock
CLK_DISP_HD	13.5	HD display clock
CLK_DISP_ID	13.5	SD display clock
CLK_GDP3	148.5	GDP3 pixel clock (HD or SD)
CLK_656	148.5	DVO pixel clock
CLK_DVP	27	DVP clock
CLK_DAA	32.768	DAA clock
CLK_DSS	36.864	DSS clock

Table 64. Clock generator B default configuration (continued)

Clock name	Frequency (MHz)	Description
CLK_LPC	46.875	Low Power Controller clock
CLK_PP	27	DeltaMu Preprocessor clock must be re-programmed for 150 MHz frequency.
CLK_FSO_CHAN0	108	Clock to HDMI PII rejection
CLK_TMDS_HDMI	27	HDMI TMDS clock
CLK_656_1	13.5	DVO1 pixel clock

11.4.3 Clock frequency change

The clock generator always starts with the default configuration as defined in *Table 64*. Nevertheless, the frequency synthesizers FS0 and FS1 can be re-configured to produce different frequencies.

Clock generator programming—lock/unlock

To prevent any unwanted ClockGen reprogramming, a protection mechanism is provided using the CKGB_LOCK register. This register must be written first with the keyword 0xC0DE to authorize any ClockGen registers update. Writing another data to the CKGB_LOCK register locks all the ClockGen registers.

Clock ratio change without changing FS0 and FS1 programming

The clocks CLK_BCH_HDMI, CLK_TMDS_HDMI, Clk_656_1, CLK_PIX_HD, CLK_DISP_HD, CLK_656, CLK_GDP2, CLK_DISP_ID, and CLK_PIX_SD are generated from a master clock (from FS0 and FS1), which is then divided by programmable dividers (by 2, 4, 8, or 1024). These dividers can be redefined using the register CKGB_DISP_CFG without changing the FS0 and FS1 setup. The clock generator design ensures a glitch-free frequency change.

FS0 and FS1 frequency definition

The frequencies generated by FS0 and FS1 are defined by the registers CKGB_FS0/1_MDx, CKGB_FS0/1_PEx and CKGB_FS0/1_SDIVx and is given by the formula:

$$F_{out} = \frac{2^{15} \cdot F_{PLL}}{sdiv \times \left[\left(pe \cdot \left(1 + \frac{md}{32}\right)\right) - \left((pe - 2^{15}) \cdot \left(1 + \frac{md+1}{32}\right)\right)\right]}$$

with F_{PLL} = 216 MHz, if the reference clock is 27 MHz or with F_{PLL} = 240 MHz, if the reference clock is 30 MHz.

To avoid glitches at the frequency synthesizer output, only the MD, PE, and EN_PRG parameters can be changed. The other parameters can be changed but glitches will occur.

11.4.4 Clock frequency reduction

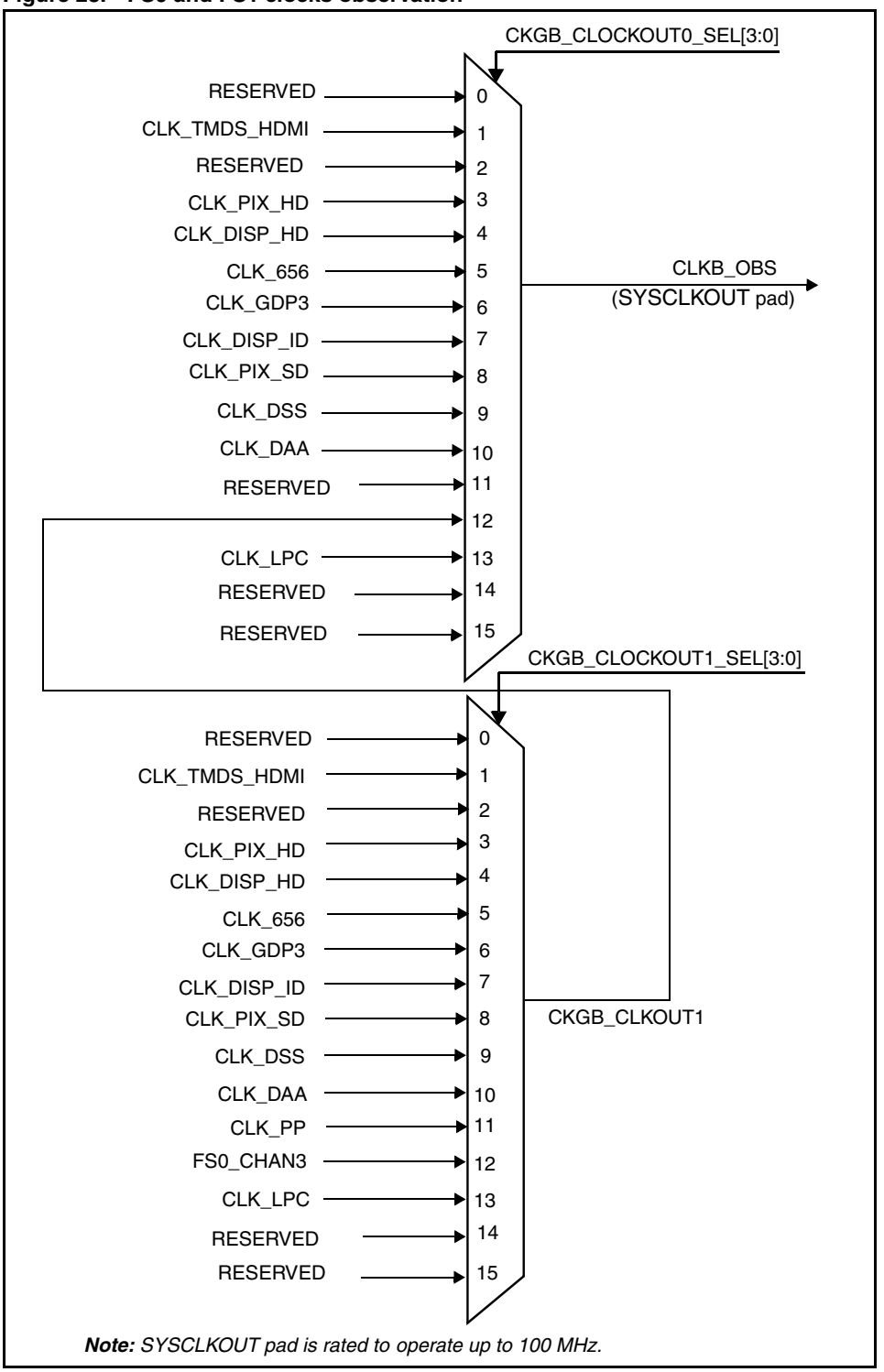
Most of the group B clocks can be divided to reduce the power consumption with the register CKGB_CLK_DIV without stopping the clocks.

11.4.5 Clocks observation

Any group B clock can be routed and observed on the SYSCLKOUT pad.

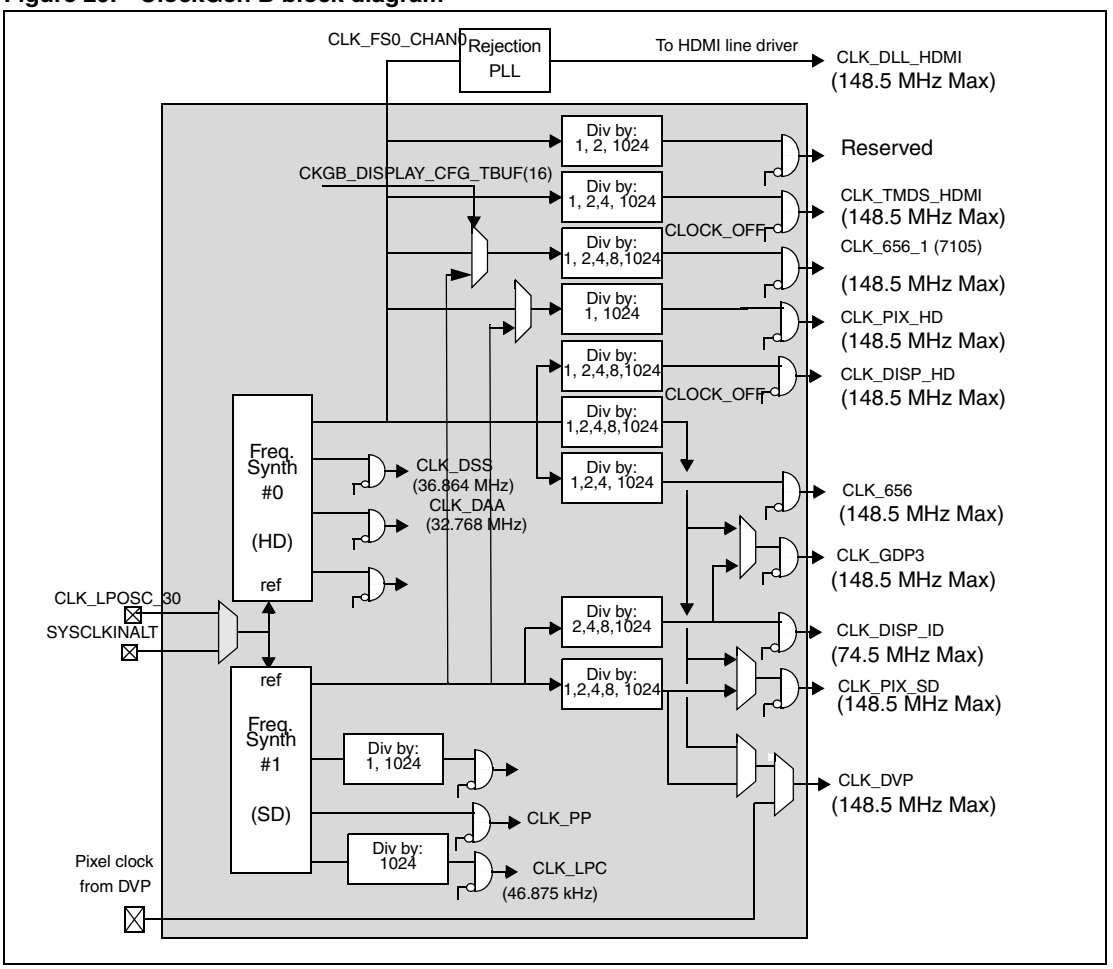
The configuration register CKGB_CLKOUT_SEL is provided to select the clock which will be routed to the pad.

Figure 28. FS0 and FS1 clocks observation



Note: *SYSCLKOUT pad is rated to operate up to 100 MHz.*

Figure 29. ClockGen B block diagram



11.4.6 Frequency synthesizers reference clock

The reference clock of two frequency synthesizers is selectable and can be chosen between the 30 MHz clock coming from the SATA Phy or from the pad SYSCLKINALT.

11.5 Audio clock generation (ClockGen C)

The ClockGen C is responsible for clocking the following units:

- multichannel PCM Player 0 (CLK_PCM0) connected to HDMI or external DACs (stereo)
- stereo PCM Player 1 (CLK_PCM1) connected to internal audio DACs and to HDMI stereo channels
- S/PDIF Player
- stereo audio DAC

The audio clock generator is a quad-frequency synthesizer which generates the 256 x Fs (audio sampling frequency) from which the I^2S serial clock, left-right clock and DAC oversampling clocks are derived.

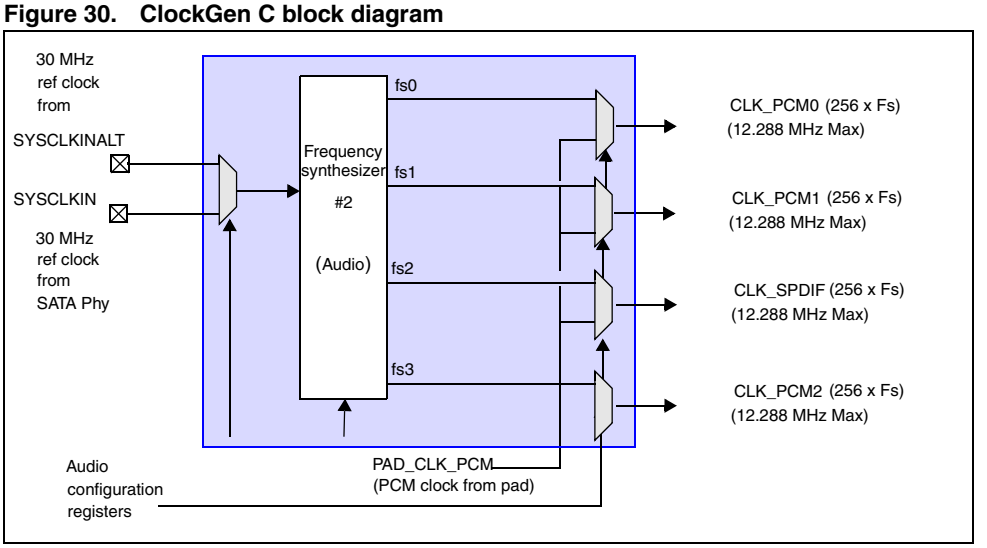
Typical audio sampling frequencies are: 32 kHz, 44.1 kHz, and 48 kHz for Set-top box applications, and can be up to 192 or 96 kHz for DVD applications.

The three audio players have independent clock generators issued from the same quad-frequency synthesizer. The frequency synthesizer channel#0 clocks the PCM player#0, the channel#1 clocks the PCM player#1, and the channel#2 clocks the S/PDIF player.

Refer to *Section 3.12: Audio subsystem on page 28* for a full overview of the Audio system clocking.

The *Figure 30* shows the block diagram of ClockGen C.

Figure 30. ClockGen C block diagram



11.5.1 Frequency synthesizer reference clock

The reference clock of the frequency synthesizer is selectable and can be chosen between the 30 MHz clock coming from the SATA Phy or from the pad SYSCLKINALT. The reset value is the SATA Phy clock.

11.6 LMI memory clocks (ClockGen D)

The ClockGen D supplies clocks to the LMI memory interface(s). This is a simple ClockGen with a PLL only, the dividing function, to generate the GPLMI IP Mclk, is done inside the LMI padlogic.

11.6.1 Clock signals

The *Table 65* lists group D clocks with their maximum and reset frequency.

Table 65. Clock Generator D

Clock name	Maximum frequency (MHz)	Reset frequency (MHz)	Description
CLK_LMI_PL	800	0	
CLK_LMI	400	0	Phase altered and divided by 2 version of CLK_LMI_PL

11.6.2 Reference clock

The reference clock can be either an internal 30 MHz clock signal or a clock connected to the SYSCLKINALT pin. The reset value is SYSCLKALTIN.

11.6.3 Clock frequency reduction

Flexible, CPU can reprogram the PLL controls.

11.7 MPEG clock recovery

The MPEG clock recovery is a mechanism to adjust the locally generated clocks with the encoder clock referenced in the program counter reference (PCR) located in the adaptation field of the incoming transport stream.

The STi7105 generates three local clocks from internal frequency synthesizers using a fixed and stable 27 MHz reference clock produced by a crystal.

These three clocks are:

- CLK_PIX_SD used for standard definition display
- CLK_PIX_HD used for high definition display
- CLK_PCM (256 x Fs, where Fs can take several possible values, such as 32 kHz, 44.1 kHz, and 48 kHz) used for audio output

11.7.1 Clock recovery principle

The mechanism assumes that these three clocks are related to each other.

The recovery is done as usual for the CLK_PIX_SD (generated by the frequency synthesizer FS#0) by comparing the 42 bits PCR value located in the adaptation field of the stream with the local system timer counter (STC) value when a packet arrives. This generates a potential correction that is applied to the CLK_PIX_SD frequency synthesizer. The frequency synthesizer is programmed with new setup values to slow or accelerate the clock.

Regarding the Audio PCM clock recovery, two counters are used.

- A PCM free-running counter, clocked by the PCM Audio frequency synthesizer FS#2.
- A reference counter, clocked by the SD video frequency synthesizer FS#0. The maximum value of this counter is programmable defining the time interval between two consecutive resets. This counter is used as a time-base.

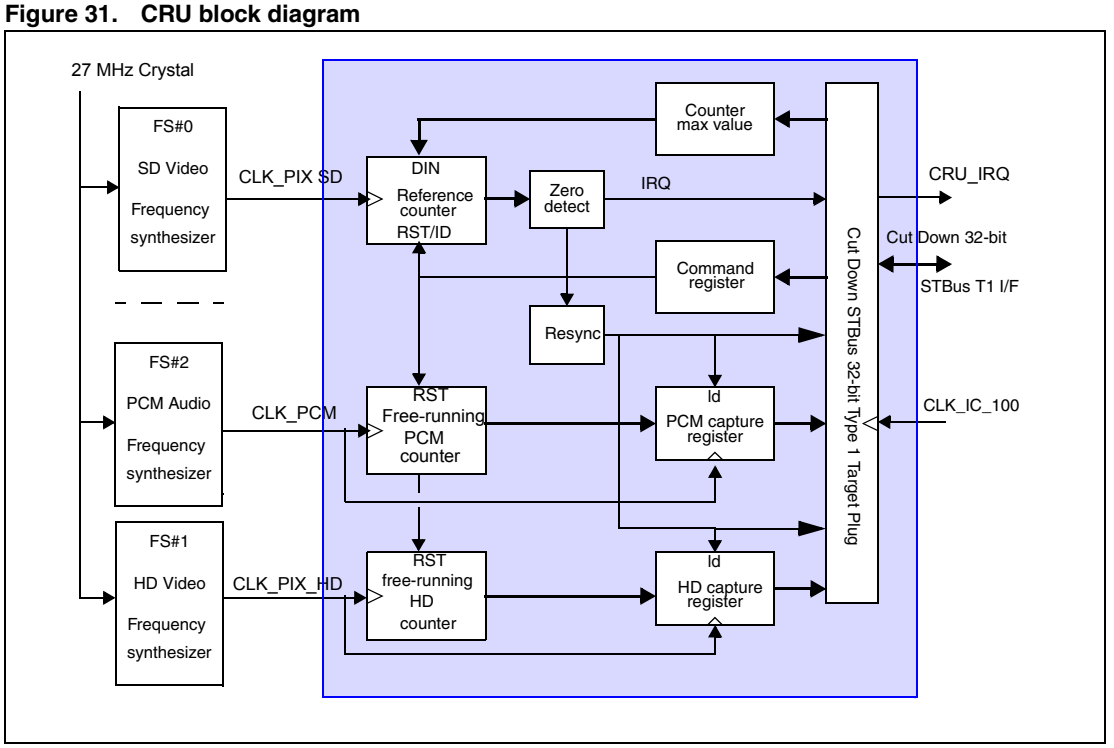
When the reference counter resets, the values of the free-running counter clocked off CLK_PCM is captured into a readable register. This event generates an interrupt to the CPU (CRU_IRQ). The CPU reads the value and compares it with the previously captured value. The difference between two adjacent values gives an indication of the correction to apply to the PCM audio frequency synthesizer FS#2.

The decision to correct the frequency synthesizer's setup is under the control of the software.

The same principle applies for the recovery of the CLK_PIX_HD. A free-running counter is clocked with the HD video frequency synthesizer FS#1. The same reference counter is used. When this counter resets then the output of the free-running counter clocked at CLK_PIX_HD is captured into a readable register.

The *Figure 31* shows the block diagram of clock recovery unit (CRU).

Figure 31. CRU block diagram



12 Power-On-Reset and system reset

12.1 Reset sources

The different reset sources are:

- Power-On-Reset (POR) signal, which is applied on the RESETN pad (with glitch suppression using a Schmitt type pad)
- watchdog reset generated by the ST40 internal Watchdog Timer (WDT)
- UDI reset sent through the ST40 debug port
- software reset from the ST40 to the ST231 CPU through the ST231 reset filters
- smartcard insertion
- long time-out reset (front-panel reset button)

The ST40 manual reset is not used, only the PMU_PRESET_N POR reset is used.

12.2 POR reset (cold reset) vs. system reset (warm reset)

In the POR sequence (cold reset), everything is reset including the clock generators and captured mode pins values.

In the system reset (warm reset) sequence, everything is reset except clock generators and a part of system configuration. The system reset sequence is executed when the reset source is watchdog, UDI, long-time-out reset, or smart card insertion.

The long-time-out reset can be performed with an interrupt generated from a PIO. The CPU can use this interrupt to identify a long-time-out reset, and then use the WDT to generate a system reset.

12.3 Reset test mode

The reset generator includes a test mode that allows to bypass all the stretchers, and to directly apply a reset signal simultaneously to all the units.

13 Mode pins

The *mode pins* are a group of pads configured in the input mode, and are dedicated to capture values during the power-on-reset sequence that are used to configure certain defined functionalities. The captured values are viewed in the SYSTEM_STATUS1 register.

The mode pins are captured at the rising-edge of the RST_N signal during the reset phase, and are made available to the system to define operating modes, such as ClockGen boot configuration. The *Table 66* describes the mapping of the mode pins on PIO pads.

Table 66. Mode pins mapping

Bit	Bit field	Controlled unit	Controlling Pad
MODE[0]	**Ref clock selection for Clockgen A** 0: SYSCLKINALT (Ext) 1: Osc (SATA)	ClockGen A	MIIMDIO [PIO8(3)]
MODE[2:1]	**PLL0 startup configuration**(1) 00: Fin/Fout–27/900 MHz 01: Fin/Fout–27/604.8 MHz 10: Fin/Fout–30/900 MHz 11: Fin/Fout–30/600 MHz	ClockGen A	[PIO16(1,0)]
MODE[4:3]	**PLL1 startup configuration**(1) 00: Fin/Fout–27/799.2 MHz 01: Fin/Fout–27/399.6 MHz 10: Fin/Fout–30/800 MHz 11: Fin/Fout–30/400 MHz	ClockGen A	MIIMDINT: MIIMDC [PIO9(6):PIO8(4)]
MODE[6:5]	**Reset bypasses**(2) CPU_RST_OUT_BYPASS[1]: bypass of (LX_Audio+LXDelphi) reset loop back CPU_RST_OUT_BYPASS[0]: bypass of (SH4+LX_Audio+LXDelphi) reset loop back	Reset generator	[PIO16(3:2)]
MODE[7]	**Resetout mode** (see SYSTEM_CONFIG9, long_reset_mode bit)(3)	Reset generator	MIITX_EN [PIO8(2)]
MODE[9:8]	**BOOT mode selection**: 00: SH4-300 boot first 01: ST231 DeltaMu boot first 10: ST231 Audio boot first	ST40, ST231 Audio, ST231 DeltaMu, request filtering	MIIRXD[3:2] [PIO9(1:0)]
MODE[10]	**Reserved** (Do not connect)	Reserved	MIIRX_DV [PIO7(4)]
MODE[11]	**nand_addr_short_not_long**(4)	Nand Controller	MIIRX_ER [PIO7(5)]
MODE[12]	**Serial Flash usage**: 0: ATMEL 1: ST Flash	EMI4	MIIRXD[0] PIO8(6)
MODE[13]	**Boot device port size at boot:** (4) 0: 16 bits 1: 8 bits	EMI4 and Nand Controller	[PIO16(4)]

Table 66. Mode pins mapping (continued)

Bit	Bit field	Controlled unit	Controlling Pad
MODE[14]	**emiss_slave_not_master**	EMI subsystem	MIIRXD[1] [PIO8(7)]
MODE[16:15]	**Boot Device**: 00: NOR Flash (EMI controller) 01: Nand Flash (Nand Controller) 10: Serial Flash (SPI controller) 11: Reserved	EMI subsystem	MIITXD[1:0] [PIO7(7:6)]
MODE[17]	**emiss_clock_slave_not_master**	EMI subsystem	MIITXD[2] [PIO8(0)]
MODE[18]	**nand_page_large_not_small**(4)	Nand Controller	MIITXD[3] [PIO8(1)]

1. It allows to setup ClockGen A PLL0 and PLL1 configurations (freq input /freq output) without relying on software. The ClockGen A registers CLKGENA_CLKOPSRC_SWITCH_CFG/CFG2 have to be configured to switch the source of STi7105 clocks from oscillator (default mode after reset) to PLL. The usage of mode pins allows to speed-up the ClockGen A configuration. By the time the software changes the CLKGENA_CLKOPSRC_SWITCH_CFG/CFG2 setting, the PLL may already be locked (so normally that allows to mask the PLL lock time). For more details, please contact your local ST representative to access ClockGen A functional specifications.
2. Allows to bypass the CPUs handshake in the chain of the reset generator. After boot, the modepin value can be bypassed by using the SYSTEM_CONFIG9[28:27] register (this register is not reset in case of watchdog reset, also it takes the value of the two modepins at reset). A typical usage of this system config bit is to bypass the ST231 resetout. Infact, the ST40 may change the boot address of the ST231 (by default 0x0). To allow the ST231 to take into account this new boot address it must be reset again through a config register (SYSTEM_CONFIG29). In that case, you do not propagate the resetout of the ST231 to the others IPs which may have already been configured.
3. It selects the resetout mode (SYS_WDOGRSTOUT pin):

   In Long ResetOut mode, the reset value guarantees a 200 ms reset out for the resetout.

   In Short ResetOut mode, resetout lasts 100 us.

   The resetout period is loaded during reset (RST_CONF) on the SYSTEM_CONFIG9[25:0] register (being the resetout period value depending on the mode pin 7 value). This register is not reset in case of watchdog reset and it can be reprogrammed after reset to allow for a resetout period of 2.48 s.
4. The Nand controller selects among the different memory types based on the three input signals: nand_page_large_not_small, nand_add_short_not_long, and nand_data_8_not_16. Refer *Table 67*.

Table 67. Memory type based on static input pins

Type select signal			Type	Comment
nand_page_large_not_small	**nand_add_short_not_long**	**nand_data_8_not_16**		
0	0	1	3	small page devices
0	0	0	4	
0	1	1	1	
0	1	0	2	
1	0	1	7	large page devices
1	0	0	8	
1	1	1	5	
1	1	0	6	

System configuration registers reset

Some System configuration registers are not affected by a system reset. They keep the value which was written either during the POR reset or by the software.

These registers are:

- mode pins value captured during the POR sequence
- reset generator configuration—resetout duration, CPUresetout bypass(1:0)
- boot mode
- boot size—boot Flash bus width (8 or 16 bits)

14 Low power control

Power down mode in the STi7105 consists of having some or almost all clocks running 1024 times as slow as their normal speed. This reduces power consumption dramatically and still enables some software to be running, also, it enables the chip to be woken up fairly quickly without having to reboot the application.

Note: Certain precautions must be taken to achieve this: In particular, the DDR SDRAM must be put into self-refresh mode prior to entering this mode, and at wake up there must be no access to DDR until the DDR and associated PadLogic have been restored to their normal mode of operation. If the LMI clock is slowed down (to less than 100 MHz), the DDL of the LMI padlogic will no longer be operational. It will also be necessary to update the refresh interval.

Additionally, a standby mode is provided whereby some clocks can be completely switched off. This can be a power saving feature for applications where functionalities clocked by a dedicated clock will never be needed.

The standby mode includes different mechanisms: switch-off clocks by programming the ClockGen or some bits of the system configuration module (for the EMI and DDR self-refresh), standby, and sleep modes in the ST40.

The ST40 also supports two main low power modes: sleep and standby (see *ST40 sleep and standby modes overview on page 175*).

The EMI clock cannot be switched off with the ClockGen. Both IPs support the powerdown protocol: this is managed by a simple hand-shake between the system configuration register (under control of the CPU) and the two IPs. This mechanism allows the EMI clock to be switched off selectively.

The same mechanism is used to send the DDR into self-refresh mode (powerdown protocol between the LMI Core and the system config module).

14.1 Entering low power modes

Method 1.1: by programming configuration bits in the ClockGen

Using configuration bits of the ClockGen, some clocks can selectively be slowed down (divided by 1024) to enter power down mode whilst others keep their nominal speed. Refer to the ClockGen specifications.

Note: Standby mode (clocks halted) is also controllable through configuration bits of the ClockGen.

Method 1.2: using the low power controller (LPC) module

A global power down command can be issued by using the low power alarm (LPA) timer of the LPC module (part of STi7105 COMMs). Refer to *Figure 32 on page 174*.

All clocks, for which the 1024 divider ratio is available inside the two ClockGens, will be slowed down: the 1024 division is not currently implemented for the following clocks:

- In the ClockGen A:
  - CLK_EMI_MASTER_A (EMI clock @ 100 MHz)
  - CLK_ETHERNET_A (Ethernet clock @ 100 MHz)
- In the ClockGen B:
  - CLK_DSS (DSS clock @ 36.768 MHz)
  - CLK_DAA (DAA clock @ 32.768 MHz)
  - CLK_EMI_MASTER_B (EMI clock @ 100 MHz)
  - CLK_ETHERNET_B (Ethernet clock @ 100 MHz)

Power Down mode is entered upon programming of the LPA timer.

Note: 1 The usage of the LPA Counter is not compatible with use as a WatchDog Timer. Refer to the LPC specification for details.

2 Standby mode (clocks completely switched off) cannot be entered through the LPC.

3 The only way to slow down the clocks for which the 1024 divider ratio is not implemented inside the ClockGen, is to bypass the PLL (By doing this it is possible to reach frequencies in the range of a few MHz), or to use the clockgen configuration registers to reduce the clock frequency generated by the PLL. Refer to clockgen specifications for details.

Method 1.3: using a global power down control bit

A global power down command (all clocks slowed down) can be issued by setting the appropriate configuration bit located in the CONF block register (refer to the System Configuration bit SYSTEM_CONFIG7[23]). Global standby mode (clocks completely switched off) cannot be entered this way.

14.2 Exiting low power modes

Method 2.1: through configuration bits in the ClockGen

If power down is entered by Method 1.1 above, it can clear the bits that are already set in ClockGen while exiting.

Note: This is also valid for standby mode (that is, when clocks were halted through ClockGen configuration).

Method 2.2: through the LPC

If power down is entered by Method 1.2 above: when the LPA counter reaches zero, the LPC releases the global power down command and the ClockGen exits power down mode. The duration of the countdown is user programmable, and can be programmed from a few milliseconds to up to 271 days after LPA has been programmed (LPA counter is 40 bits clocked at 46.87 kHz).

Method 2.3: upon detection of activity on the UHF or IRB inputs

This generates an interrupt (IRB_WAKEUP_INTERRUPT) to the ILC3, which, assuming it has first been programmed accordingly, treats it as a wake up request that it routes to the LPC and also to the CONF module (to clear the global powerdown bit). Refer to *Figure 32 on page 174*.

Note: ***IMPORTANT****: the IRB_WAKE_UP interrupt routed to the ILC3 will be generated only if the global power down command is received by the wake-up interrupt generator module. This implies that the LPC must be programmed (METH 1.2). Of course this has also the effect of slow down by 1024 the frequency clocks.*

If power down is entered by method 1.2: the LPC, when it receives the wake up request from the ILC, clears the global power down command that goes to the ClockGen and normal speed is restored.

If power down is entered by method 1.3: the global powerdown control bit in the CONF block, when it receives the wake up request from the ILC, clears the global power down command that goes to the ClockGen and normal speed is restored.

If power down is entered by method 1.1: the configuration bits in the ClockGen must be set back to their normal value. This can be done by an interrupt routine. However, if DDR is not operational (because it was sent in self-refresh) this means the interrupt servicing routine is stored in the ST40 cache or stored in external Flash, if EMI is not switched off.

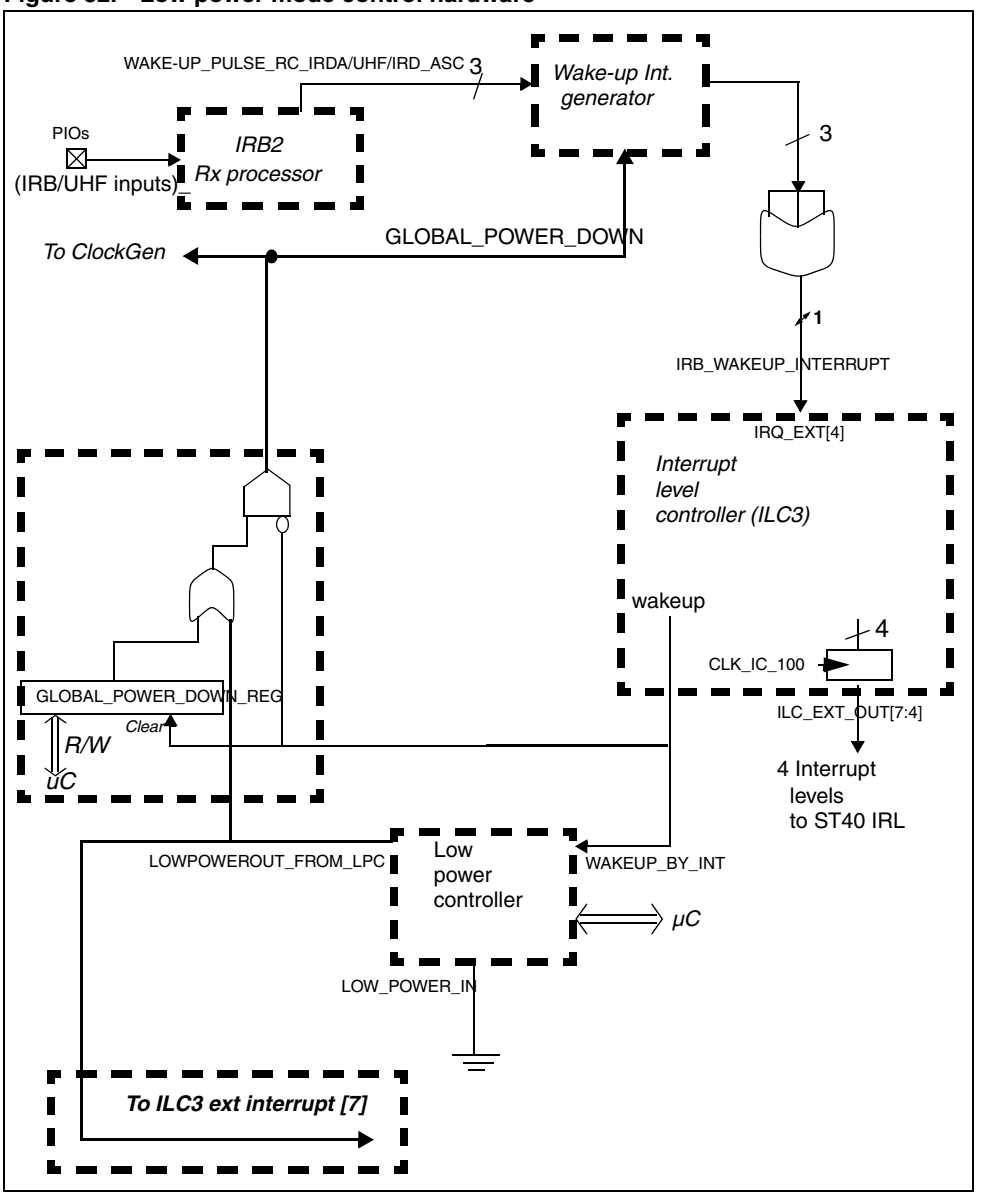
In the case that the interrupt going to the ILC3 upon detection of IRB/UHF activity can be treated as a normal interrupt, servicing it then consists of restoring the ClockGen configuration bits.

Note: *The same interrupt can be also used to wake-up the ST40 from sleep or standby mode since four interrupt levels provided by the ILC3 are connected to the ST40 IRL.*

Method 2.4: upon firing of any selected interrupt

This is just an extension of the latter case. In fact if the condition that the relevant interrupt handler is not located in DDR is fulfilled, then any source can be programmed to trigger the interrupt routine that will clear configuration bits in the ClockGen if power down was entered in that way (method 1.1), or clear the LPA counter to restore normal operation if power down was controlled from the LPC (method 1.2).

Figure 32. Low power mode control hardware



14.3 DDR self-refresh

To send the DDR in self-refresh the CPU needs to write a bit in the system config register:

SYSTEM_CONFIG11: **GP-LMI / LMI padlogic config control register**

bit[12] **LMIPL_PLL_POWERDOWN**: PLL power down

This write operation activates the powerdown protocol for the LMI Core (a powerdown request is received by the LMI). The LMI core completes all of the outstanding operations, it

puts the DDR in self-refresh mode and then answers with a powerdown grant. This can be monitored by means of a status bit in the system conf register:

SYSTEM_STATUS4: LMI padlogic status register, bit[0] **LMI_PWRD_ACK**: LMI power acknowledge

As soon the acknowledge is received the LMI clock can be switched off or slowed down using the methods described before.

After exiting from low power mode the DLLs inside the LMI padlogic must be reset by means of a soft reset using the sys conf bit and the lock condition must be reached:

SYSTEM_CONFIG11: GP-LMI / LMI padlogic config control register

bit[27] **RST_N_LMI:** LMI sub system reset. Active Low

Note: This procedure has the effect of resetting the LMI core. This implies that the LMI core configuration must be re-done.

The software needs to guarantee that no access is performed to the LMI during powerdown and until LMI and padlogic are restored to the normal mode of operation.

14.4 EMI and PCI clocks stopping

The clocks of these three IPs can be switched off with the same mechanism used to put the DDR into self-refresh (that is, by means of the powerdown protocol executed between the system config and the two IPs). For that case the system config bits to be used are:

- SYSTEM_CONFIG32: **Power down config register**
  - bit[1] **EMI_POWER_DOWN_REQ**: Power down request for EMI module
  - bit[2] **PCI_POWER_DOWN_REQ**: Power down request for PCI module

- SYSTEM_STATUS15: **Power down status register**
  - bit[1] **POWER_DOWN_ACK_EMI**: EMI power down acknowledge
  - bit[2] **POWER_DOWN_ACK_PCI**: PCI power down acknowledge

14.5 ST40 sleep and standby modes overview

The ST40-300 ISA includes a sleep instruction that can be used to suspend operation of the core to the point where the clocks can be stopped. The ST40-300 top also provides signals to inform an SoC level power or clock controller when it is safe to remove the clock and to determine whether the CSP clock should be stopped or not.

Note: The STi7105 ClockGenA does not allow the ST40 clocks to be switched off because of the missing hand-shake with the ST40. ST40 clocks can only be slowed-down.

Sleep mode

On executing the sleep instruction the ST40-300 core will flush the instructions in the pipeline and complete all outstanding STBus transactions on the initiator port. Once this has been completed the CPU will assert the EXT_ST40_CORE_PDACK signal to indicate that the clock to the core can be removed.

The actual gating of the clock provided to the core is expected to be performed at the SoC level from the clock controller itself in response to the EXT_ST40_CORE_PDACK signal being asserted. This is done to allow the entire clock tree to be stopped and therefore to maximize the dynamic power-saving.

Note: The STi7105 ClockGenA does not allow the ST40_ICK clock to be switched off because of the missing hand-shake with the ST40.

The CSP also provides a mechanism to enter sleep mode as directed by a system level clock or power controller. In this case the CSP is instructed to enter sleep mode by the system level assertion of the EXT_ST40_CSP_PDREQ signal. At this point the CSP will complete all outstanding STBus requests that it has received. Once the CSP is idle it will internally switch the relevant wake-up control signals to operate correctly with the CSP clock removed and will then assert EXT_ST40_CSP_PDACK to indicate that it is safe to stop the clock to the CSP.

The actual gating of the clock provided to the CSP is expected to be performed at the SoC level from the clock controller itself in response to the EXT_ST40_CSP_PDACK signal being asserted. This is done to allow the entire clock tree to be stopped and therefore to maximize the dynamic power-saving.

Note: 1 Neither the core nor the CSP will signal readiness to have their clocks removed until all outstanding transactions are completed. Consequently, a pending access to a non-responding peripheral will prevent the ST40-300 entering sleep mode. The system designer must ensure that other initiators and targets in the system are shut down in a manner that ensures all transactions can be completed safely.

2 The STi7105 ClockGenA does not allow the ST40_PCK clock to be switched off because of the missing hand-shake with the ST40.

Exiting sleep mode

Two conditions will cause the ST40 core to exit sleep mode.

- An interrupt on the NMI, IRL, through the interrupt expansion interface or generated by one of the CSP peripherals (if the CSP is still being clocked).
- Either a manual or power-on reset. This can be applied either through the relevant pins on the core, the UDI, or by the watchdog timer.

De-asserting EXT_ST40_CSP_PDREQ will not cause the CSP or core to resume from sleep and will be ignored. When a return from sleep mode is requested the CSP will de-assert the EXT_ST40_CSP_PDACK signal to indicate to the system level clock controller that it is ready for its clock to be started.

Note: Before starting the CSP clock the system level clock controller should de-assert EXT_ST40_CSP_PDREQ to prevent the CSP from re-entering sleep mode.

Once it has started to receive a clock the CSP will return to functional mode and will assert the STBus default grant signal to indicate it can start to accept transactions from the STBus.

The CSP will also internally signal to the core that it is to wake-up from sleep mode, at which point the core will de-assert its EXT_ST40_CORE_PDACK and wait until the core clock is re-started by the clock controller therefore allowing the core to continue with execution of instructions.

Note: There is no mechanism in place to prevent the CSP from transitioning into sleep even if the CPU is in functional mode. An operation where the core is being clocked and the CSP is powered down is not supported and should be avoided except during the transition to and from sleep mode.

15 System config module

15.1 Brief overview

The System Config is a module that holds general purpose configuration registers. It can also be used to read back some system configurations.

Register addresses are shown as *SystemConfigBaseAddress* + Offset

The *SystemConfigBaseAddress* is: 0xFE00 1000

15.1.1 Register summary

Table 68. Register summary

Address offset	Register	Description	Reference
0x0000	DEVICE_ID	Device identifier	*on page 180*
0x0004	EXTRA_DEVICE_ID	Reserved	*on page 180*
Status registers			
0x0008	SYSTEM_STATUS0	USB/SATA PHY status register	*on page 181*
0x000C	SYSTEM_STATUS1	Mode pin status captured during power-on-reset	*on page 181*
0x0010	SYSTEM_STATUS2	OSC status register	*on page 182*
0x0014	SYSTEM_STATUS3	LMI-PADLOGIC (LMI_SYS) status register	*on page 182*
0x0018	SYSTEM_STATUS4	LMI-PADLOGIC (LMI_SYS) status register	*on page 183*
0x001C	SYSTEM_STATUS5	ClockGen D Jitter estimator capture pattern monitor	*on page 183*
0x0020	SYSTEM_STATUS6	ClockGen D Jitter estimator beat edge monitor	*on page 184*
0x0024	SYSTEM_STATUS7	Compensation status registers	*on page 184*
0x0028	SYSTEM_STATUS8	ClockGenD Jitter estimator beat edge counter monitor	*on page 185*
0x002C	SYSTEM_STATUS9	HDMI PLL status register	*on page 185*
0x0030	SYSTEM_STATUS10	USB/LMI PLI Bist counter status register	*on page 186*
0x0034	SYSTEM_STATUS11	Reserved	*on page 186*
0x0038	SYSTEM_STATUS12	Thermal sensor status register	*on page 187*
0x003C	SYSTEM_STATUS13	Reserved	*on page 187*
0x0040	SYSTEM_STATUS14	Reserved	*on page 188*
0x0044	SYSTEM_STATUS15	Power down status register	*on page 188*
Configuration registers			
0x0100	SYSTEM_CONFIG0	Transport config register	*on page 189*
0x0104	SYSTEM_CONFIG1	HDMI PHY compensation code register	*on page 190*

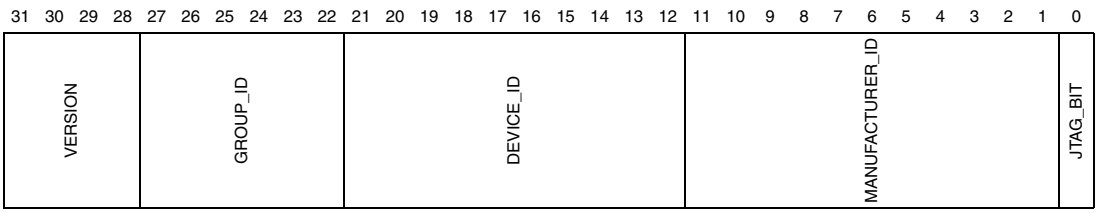
Address offset	Register	Description	Reference
0x0108	SYSTEM_CONFIG2	HDMI PHY configuration register	on page 191
0x010C	SYSTEM_CONFIG3	DAC /HDMI config register	on page 192
0x0110	SYSTEM_CONFIG4	USB / Delta -Mu config register	on page 193
0x0114	SYSTEM_CONFIG5	EMI/PCI config register	on page 194
0x0118	SYSTEM_CONFIG6	Vidout config register	on page 195
0x011C	SYSTEM_CONFIG7	COMMS /Ethernet config register	on page 196
0x0120	SYSTEM_CONFIG8	SH4 boot control config register	on page 198
0x0124	SYSTEM_CONFIG9	ResetGen config register (only sensitive to preset)	on page 199
0x0128	SYSTEM_CONFIG10	ITRQ pads control pin config register	on page 200
0x012C	SYSTEM_CONFIG11	LMI padlogic config register	on page 200
0x0130	SYSTEM_CONFIG12	LMI padlogic config register	on page 201
0x0134	SYSTEM_CONFIG13	LMI padlogic config register	on page 203
0x0138	SYSTEM_CONFIG14	LMI padlogic config register	on page 204
0x13C	SYSTEM_CONFIG15	Key scan / FDMA config register	on page 204
0x0140	SYSTEM_CONFIG16	Comms SSC configuration register	on page 205
0x0144	SYSTEM_CONFIG17	CPXM config control register	on page 206
0x0148	SYSTEM_CONFIG18	pad state config control register	on page 207
0x014C	SYSTEM_CONFIG19	PIO 0 alternate function control register	on page 207
0x0150	SYSTEM_CONFIG20	PIO 1 alternate function control register	on page 208
0x0154	SYSTEM_CONFIG21	PIO 2 alternate function control register	on page 208
0x0158	SYSTEM_CONFIG22	Compensation config registers	on page 209
0x015C	SYSTEM_CONFIG23	Compensation config registers	on page 210
0x0160	SYSTEM_CONFIG24	Osc config register	on page 211
0x0164	SYSTEM_CONFIG25	PIO 3 alternate function control register	on page 211
0x0168	SYSTEM_CONFIG26	ST230 Lx - AUDIO boot	on page 212
0x016C	SYSTEM_CONFIG27	ST230 Lx - AUDIO reset control and periph address	on page 212
0x0170	SYSTEM_CONFIG28	ST230 DELTA - MU boot	on page 213
0x0174	SYSTEM_CONFIG29	ST230 DELTA -MU reset control and periph address	on page 213
0x0178	SYSTEM_CONFIG30	Reserved	on page 214
0x017C	SYSTEM_CONFIG31	EMI config register	on page 214
0x0180	SYSTEM_CONFIG32	Power Down config register	on page 215
0x0184	SYSTEM_CONFIG33	SOFT_JTAG register for the USB2.0 tap controller	on page 216

Address offset	Register	Description	Reference
0x0188	SYSTEM_CONFIG34	PIO 4 alternate function control register	*on page 216*
0x018C	SYSTEM_CONFIG35	PIO 5 alternate function control register	*on page 217*
0x0190	SYSTEM_CONFIG36	PIO 6 alternate function control register	*on page 217*
0x0194	SYSTEM_CONFIG37	PIO 7 alternate function control register	*on page 218*
0x0198	SYSTEM_CONFIG38	LMI config register	*on page 218*
0x019C	SYSTEM_CONFIG39	Reserved	*on page 219*
0x01A0	SYSTEM_CONFIG40	Clock select config register	*on page 219*
0x01A4	SYSTEM_CONFIG41	Thermal sensor config register	*on page 220*
0x01A8	SYSTEM_CONFIG42	LMI config register	*on page 220*
0x01AC	SYSTEM_CONFIG43	LMI config register	*on page 221*
0x01B0	SYSTEM_CONFIG44	Reserved	*on page 221*
0x01B4	SYSTEM_CONFIG45	Reserved	*on page 222*
0x01B8	SYSTEM_CONFIG46	PIO 8 alternate function control register	*on page 222*
0x01BC	SYSTEM_CONFIG47	PIO 9 alternate function control register	*on page 223*
0x01C0	SYSTEM_CONFIG48	PIO 12 alternate function control register	*on page 223*
0x01C4	SYSTEM_CONFIG49	PIO 13 alternate function control register	*on page 224*
0x01C8	SYSTEM_CONFIG50	PIO 15 alternate function control register	*on page 224*
0x01CC	SYSTEM_CONFIG51	LMI config register	*on page 225*
0x01D0	SYSTEM_CONFIG52	LMI config register	*on page 226*
0x01D4	SYSTEM_CONFIG53	Reserved	*on page 226*
0x01D8	SYSTEM_CONFIG54	Reserved	*on page 227*
0x01DC	SYSTEM_CONFIG55	LMI config	*on page 227*
INTC2 registers			
0x0300	INTC2_PRIORITY00	Reserved	*on page 228*
0x0304	INTC2_PRIORITY04	Reserved	*on page 228*
0x0308	INTC2_PRIORITY08	Reserved	*on page 229*
0x0320	INTC2_REQUEST00	Reserved	*on page 229*
0x0324	INTC2_REQUEST04	Reserved	*on page 229*
0x0328	INTC2_REQUEST08	Reserved	*on page 230*
0x0340	INTC2_MASK00	Reserved	*on page 230*
0x0344	INTC2_MASK04	Reserved	*on page 230*
0x0348	INTC2_MASK08	Reserved	*on page 231*
0x0360	INTC2_MASK_CLEAR00	Reserved	*on page 231*
0x0364	INTC2_MASK_CLEAR04	Reserved	*on page 231*

Address offset	Register	Description	Reference
0x0368	INTC2_MASK_CLEAR08	Reserved	*on page 232*
0x0380	INTC2_MODE	Reserved	*on page 232*

15.1.2 Device ID register descriptions

DEVICE_ID Device ID register



Address: *SystemConfigBaseAddress* + 0x0000

Type: R

Reset: 0x2D43E041(1)

Description: JTAG deviceID

[31:28] **VERSION**

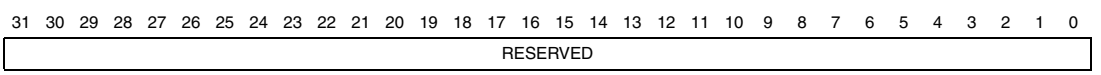
[27:22] **GROUP_ID**

[21:12] **DEVICE_ID**

[11:1] **MANUFACTURER_ID**

[0] **JTAG_BIT**

EXTRA_DEVICE_ID Reserved



Address: *SystemConfigBaseAddress* + 0x0004

Type: R

Reset: 0xXXXX

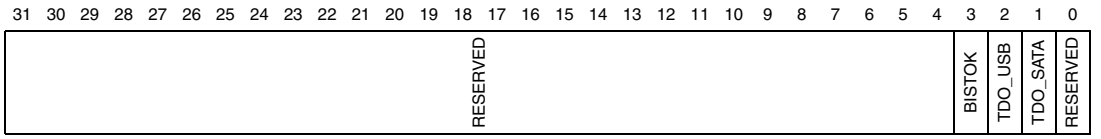
Description: Reserved

[31:0] **RESERVED**

1. This reset value is for cut 3.0. The reset value is 0x1D43E041 for cut 2.0 and 0x0D43E041 for cut 1.0.

15.1.3 System status register description

SYSTEM_STATUS0 USB/SATA PHY status register



Address: *SystemConfigBaseAddress* + 0x0008

Type: R

Reset: 0x0000

Description: USB/SATA Phy status

[31:4] **RESERVED**

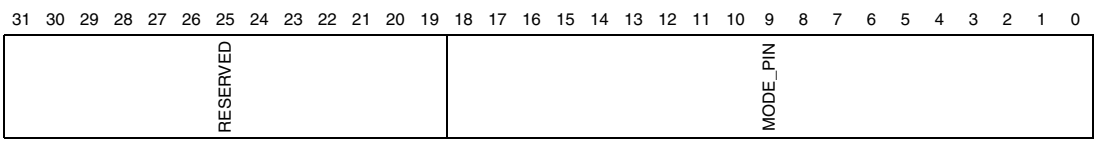
[3] **BISTOK**: High level means that bist is running into USB PHY device and no error is detected.

[2] **TDO_USB**: USB2 PHY TDO signal.

[1] **TDO_SATA**: SATA PHY TDO signal.

[0] **RESERVED**

SYSTEM_STATUS1 Mode pins values register



Address: *SystemConfigBaseAddress* + 0x000C

Type: R

Reset: Undefined(1)

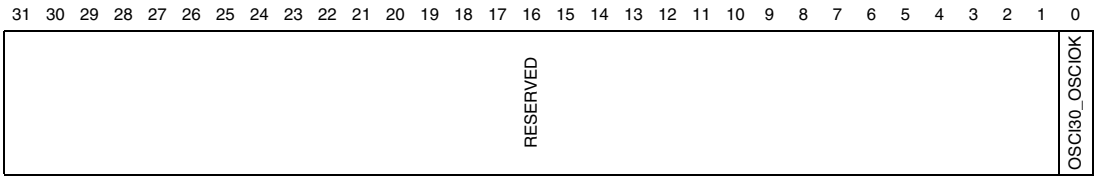
Description: Mode pins values

[31:19] **RESERVED**

[18:0] **MODE_PIN**: Mode pins are captured during the power-on-reset period.

1. Reset value depends on modepins value

SYSTEM_STATUS2 OSC status register



Address: *SystemConfigBaseAddress* + 0x0010

Type: R

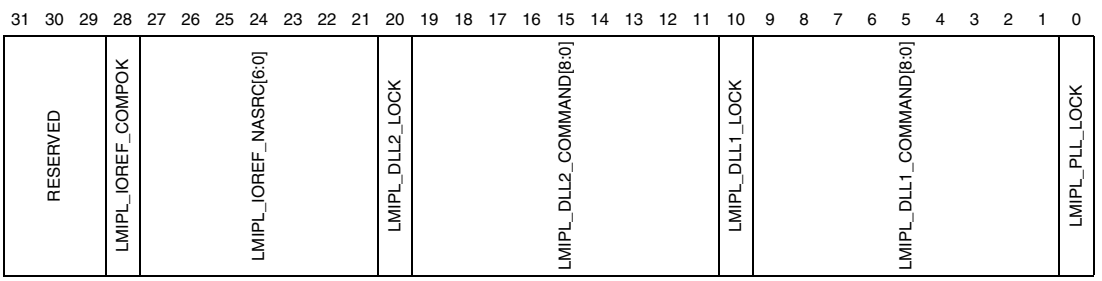
Reset: 0x00000000

Description: OSC status

[31:1] **RESERVED**

[0] **OSCI30_OSCIOK**:
1: OSCI 30 MHz oscillation stable (ZI output enabled)
0: OSCI 30 MHz oscillation unstable

SYSTEM_STATUS3 LMI status register



Address: *SystemConfigBaseAddress* + 0x0014

Type: R

Reset: 0xXXXX(1)

Description: LMI status

[31:29] **RESERVED**

[28] **LMIPL_IOREF_COMPOK**: Can be high only in normal mode and when a new measured code is available on the ASRC lines. When macrocell turns from any other mode to normal mode, delay constraints are applied to COMPOK signal.

[27:21] **LMIPL_IOREF_NASRC[6:0]:** Input code to be copied on the AxSRC lines by the compensation cell in Read mode.

[20] **LMIPL_DLL2_LOCK:** DLL2 lock.
1: DDL2 is locked 0: DDL2 is unlocked

1. From LMI Padlogic

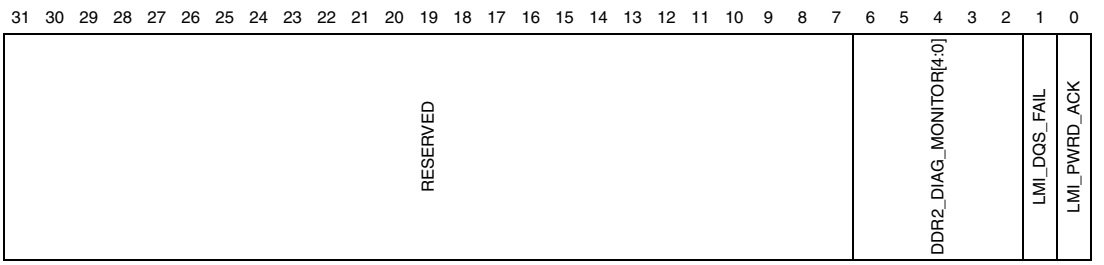
[19:11] **LMIPL_DLL2_COMMAND[8:0]:** DLL2 command. Reports the command currently being generated by DLL2.

[10] **LMIPL_DLL1_LOCK:** DLL1 lock.
1: DDL1 is locked 0: DDL1 is unlocked

[9:1] **LMIPL_DLL1_COMMAND[8:0]:** DLL1 command. Reports the command currently being generated by DLL1.

[0] **LMIPL_PLL_LOCK:** LMIPL PLL lock signal.
1: LMI PLL is locked 0: LMI PLL is unlocked

SYSTEM_STATUS4 LMI padlogic status register



Address: *SystemConfigBaseAddress* + 0x0018

Type: R

Reset: 0x00000000

Description: LMI padlogic config status

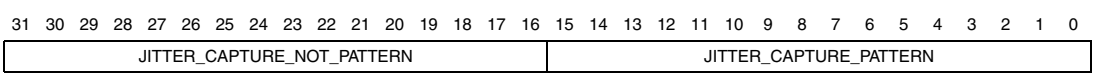
[31:7] **RESERVED**

[6:2] **DDR2_DIAG_MONITOR[4:0]:** For future development.

[1] **LMI_DQS_FAIL:**
1: Notification for DQS spurious/missing behavior

[0] **LMI_PWRD_ACK:**
1: LMI power acknowledge

SYSTEM_STATUS5 Clockgen D Jitter estimator capture pattern monitor



Address: *SystemConfigBaseAddress* + 0x001C

Type: R

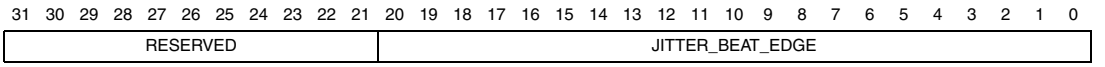
Reset: 0x00000000

Description: ClockGenD Jitter estimator capture pattern monitor

[31:16] **JITTER_CAPTURE_NOT_PATTERN**

[15:0] **JITTER_CAPTURE_PATTERN**

SYSTEM_STATUS6 Clockgen D Jitter estimator beat edge monitor



Address: *SystemConfigBaseAddress* + 0x0020

Type: R

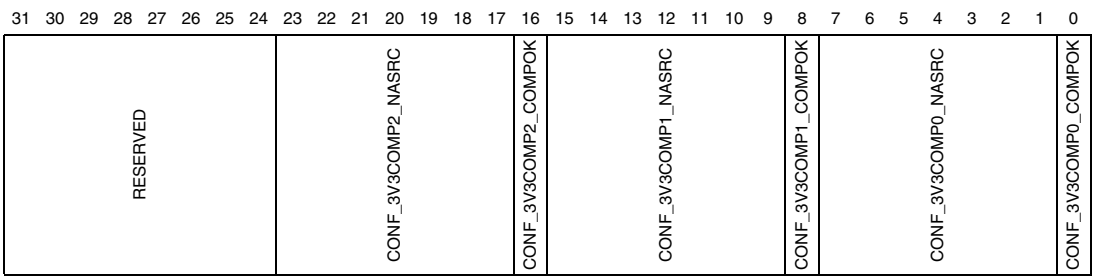
Reset: 0x00000000

Description: ClockGenD Jitter estimator beat edge monitor

[31:21] **RESERVED**

[20:0] **JITTER_BEAT_EDGE**

SYSTEM_STATUS7 Compensation status register



Address: *SystemConfigBaseAddress* + 0x0024

Type: R

Reset: 0x00000000

Description: Compensation status

[31:24] **RESERVED**

[23:17] **CONF_3V3COMP2_NASRC**: 3V3 compensation 2: NASRC code

[16] **CONF_3V3COMP2_COMPOK**: 3V3 compensation 2: COMPOK signal

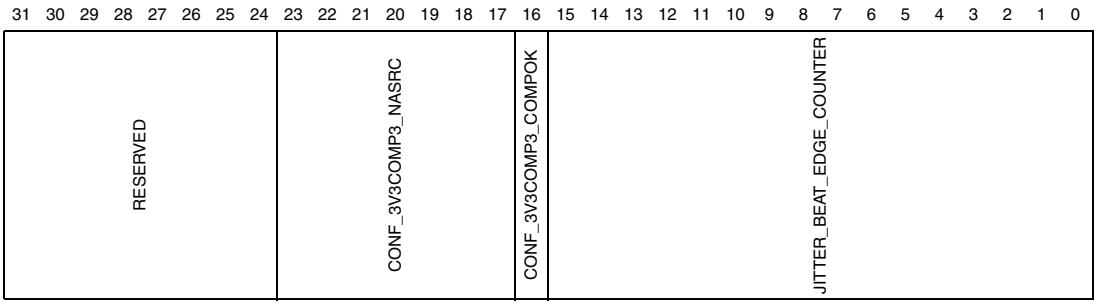
[15:9] **CONF_3V3COMP1_NASRC**: 3V3 compensation 1: NASRC code

[8] **CONF_3V3COMP1_COMPOK**: 3V3 compensation 1: COMPOK signal

[7:1] **CONF_3V3COMP0_NASRC**: 3V3 compensation 0: NASRC code

[0] **CONF_3V3COMP0_COMPOK**: 3V3 compensation 0: COMPOK signal

SYSTEM_STATUS8 ClockGenD Jitter estimator beat edge counter monitor



Address: *SystemConfigBaseAddress* + 0x0028

Type: R

Reset: 0x00000000

Description: ClockGenD Jitter estimator beat edge pattern monitor

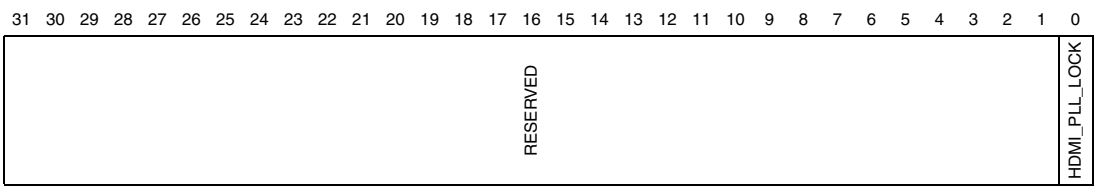
[31:24] **RESERVED**

[23:17] **CONF_3V3COMP3_NASRC**: 3V3 compensation 3: nasrc code

[16] **CONF_3V3COMP3_COMPOK**: 3V3 compensation 3: compok signal

[15:0] **JITTER_BEAT_EDGE_COUNTER**

SYSTEM_STATUS9 HDMI PLL status register



Address: *SystemConfigBaseAddress* + 0x002C

Type: R

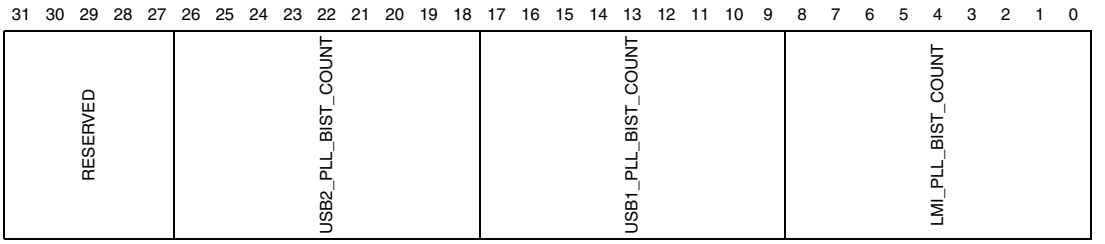
Reset: 0x00000000

Description: HDMI PLL status

[31:1] **RESERVED**

[0] **HDMI_PLL_LOCK:** Used to check lock condition of HDMI rejection PLL.
1: HDMI rejection PLL is locked 0: HDMI rejection PLL is unlocked

SYSTEM_STATUS10 USB/LMI PLI Bist counter status register



Address: *SystemConfigBaseAddress* + 0x0030

Type: R

Reset: 0x00000000

Description: Reserved

[31:27] **RESERVED**

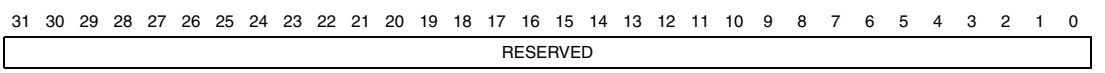
[26:18] **USB2_PLL_BIST_COUNT:** Value of USB2 PLL Bist counter value

[17:9] **USB1_PLL_BIST_COUNT:** Value of USB1 PLL Bist counter value

[8:0] **LMI_PLL_BIST_COUNT:** Value of LMI PLL Bist counter value

Caution: In case of USB signals, the usual naming convention is not used. In order to align with the STi7105 ballout names, this manual mentions two instances of USB as USB1 and USB2 rather than USB0 and USB1. Therefore, in this manual the first instance of USB is USB1 and the second instance is USB2.

SYSTEM_STATUS11 Reserved



Address: *SystemConfigBaseAddress* + 0x0034

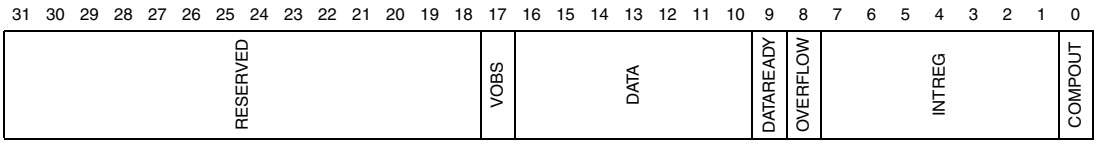
Type: R

Reset: 0xXXXX

Description: Reserved

[31:0] **RESERVED**

SYSTEM_STATUS12 Thermal sensor status register



Address: *SystemConfigBaseAddress* + 0x0038

Type: R

Reset: 0x00000000

Description: Thermal sensor status

[31:18] **RESERVED**

[17] **VOBS:** Reserved to debug - not connected in application.

[16:10] **DATA:** Output data.

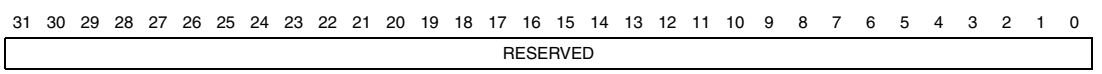
[9] **DATAREADY:** Set to '1' every 32 clock cycles when conversion is over, valid for 1 clock period, held at '0' as long as the bandgap has not started.

[8] **OVERFLOW:** Overflow of digital adder, corresponds to the upper limit of the temperature range after calibration.

[7:1] **INTREG:** Reserved to debug - not connected in application.

[0] **COMPOUT:** Reserved to debug - not connected in application.

SYSTEM_STATUS13 Reserved



Address: *SystemConfigBaseAddress* + 0x003C

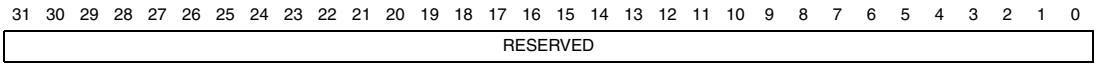
Type: R

Reset: 0x00000000

Description: Reserved

[31:0] **RESERVED**

SYSTEM_STATUS14 Reserved



Address: *SystemConfigBaseAddress* + 0x0040

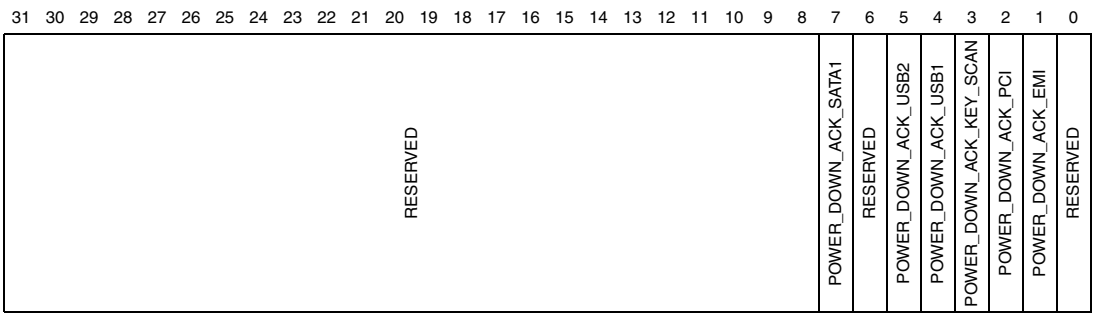
Type: R

Reset: 0x00000000

Description: Reserved

[31:0] **RESERVED**

SYSTEM_STATUS15 Power down status register



Address: *SystemConfigBaseAddress* + 0x0044

Type: R

Reset: 0x00000000

Description: Power down status

[31:8] **RESERVED**

[7] **POWER_DOWN_ACK_SATA1:**
1: SATA host power down acknowledge

[6] **RESERVED**

[5] **POWER_DOWN_ACK_USB2:**
1: USB2 host power down acknowledge.

[4] **POWER_DOWN_ACK_USB1:**
1: USB1 host power down acknowledge

[3] **POWER_DOWN_ACK_KEY_SCAN:**
1: Key scanner power down acknowledge

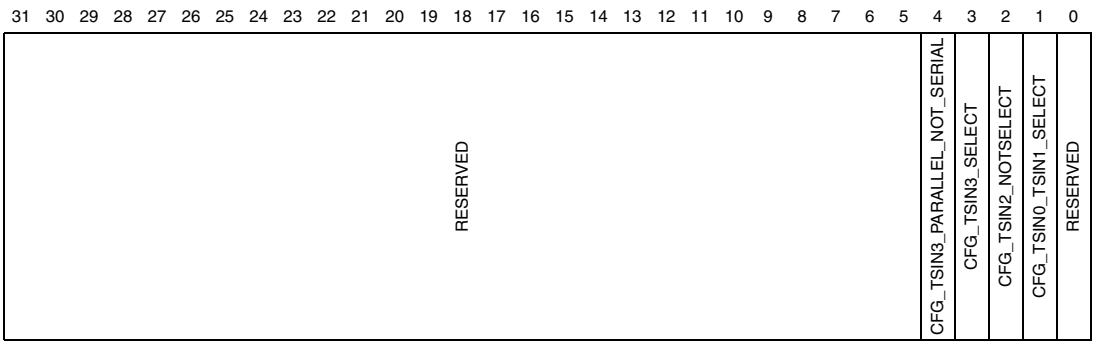
[2] **POWER_DOWN_ACK_PCI:**
1: PCI power down acknowledge

[1] **POWER_DOWN_ACK_EMI**:
1: EMI power down acknowledge

[0] **RESERVED**

15.1.4 System configuration register description

SYSTEM_CONFIG0 **Transport stream config register**



Address: *SystemConfigBaseAddress* + 0x0100

Type: RW

Reset: 0x00000000

Description: Transport stream config register

[31:5] **RESERVED**

[4] **CFG_TSIN3_PARALLEL_NOT_SERIAL**:
1: TSIN3 is in parallel mode 0: TSIN3 is in serial mode

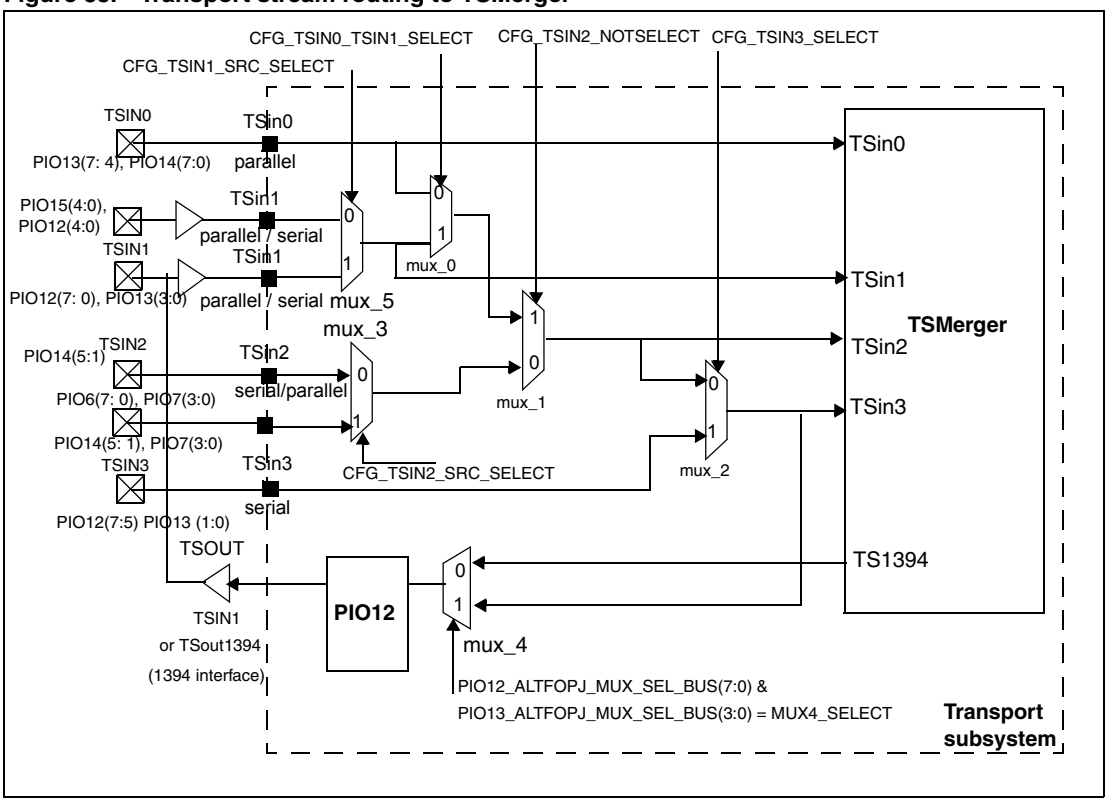
[3] **CFG_TSIN3_SELECT**:
1: TSIN3 of TS_Merger receives TSIN3
0: TSIN3 of TS_Merger receives output of mux_1 (that is, TSIN0, TSIN1, OR TSIN2 depending upon CFG_TSIN0_TSIN1_SELECT and CFG_TSIN2_NOTSELECT)

[2] **CFG_TSIN2_NOTSELECT**:
1: input TSIN2 of TSMerger receives output of mux_0 (i.e. TSIN0 or TSIN1 depending of CFG_TSIN0_TSIN1_SELECT)
0: input TSIN2 of TSMerger recieves TSIN2

[1] **CFG_TSIN0_TSIN1_SELECT**:
1: TSIN1 routed through mux_0 to input 1 of mux_1
0: TSIN0 routed through mux_0 to input 1 of mux_1

[0] **RESERVED**

Figure 33. Transport stream routing to TSMerger



Note: CFG_TSIN3_PARALLEL_NOT_SERIAL is an extra programming required to select parallel mode. On reset, the TSIN3 stream by default is in serial mode. Since, on PIO TSIN3 can be selected both in parallel and serial mode, therefore, to receive TSIN3 in parallel mode this bit must be first programmed to 1. Then, serial not parallel configuration inside TSmerger will also be required to process TSIN3 in serial/parallel mode.

SYSTEM_CONFIG1 HDMI PHY compensation config register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
USER_COMP																															

Address: *SystemConfigBaseAddress* + 0x0104

Type: RW

Reset: 0x00000000

Description: HDMI PHY compensation config register

[31:0] **USER_COMP:** External compensation code command to be applied to the HDMI phy.

SYSTEM_CONFIG2 HDMI / HDMI phy config register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	HDMI_AUDIO_SRC_SEL	HDMI_CEC_RX_ENABLE	CLK_BCH_HDMI_DIVSEL	HDMI_HOT_PLUG_ENABLE	HDMI_POFF_ENABLE	HDMI_PHY_PREEMPWDTHEXT	HDMI_PHY_PREEMPWDTH[2:0]			HDMI_PHY_PREEMPSTR[1:0]		HDMI_PHY_PREEMPON	PROG[1:0]		COMPENSATION_BYPASS	USER_COMP[47:32]															

Address: *SystemConfigBaseAddress* + 0x0108

Type: RW

Reset: 0x0000

Description: HDMI PHY config register

[31] **RESERVED**

[30] **HDMI_AUDIO_SRC_SEL:**
1: Audio SRC is 8-channel PCM out 0: Audio SRC is 2-channel stereo

[29] **HDMI_CEC_RX_ENABLE:**
1: Indicates usage of HDMI_CEC_RX is enabled 0: Indicates disabled

[28] **CLK_BCH_HDMI_DIVSEL**

[27] **HDMI_HOT_PLUG_ENABLE:**
1: Enables mapping of HDMI_HOT_PLUG_IN on PIO

[26] **HDMI_POFF_ENABLE:**
1: Enables power off on HDMI 0: Disables POFF

[25] **HDMI_PHY_PREEMPWDTHEXT**

[24:22] **HDMI_PHY_PREEMPWDTH[2:0]**

[21:20] **HDMI_PHY_PREEMPSTR[1:0]**

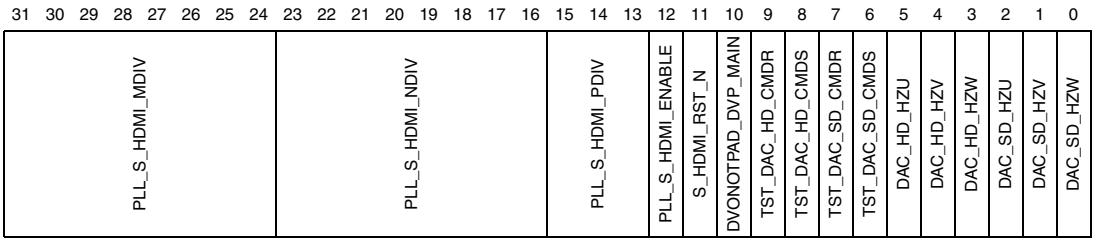
[19] **HDMI_PHY_PREEMPON**

[18:17] **PROG[1:0]:** Programs the output buffer speed for PROGB/PROGA.
x0: Speed set up to 1.6 Gbps 01: Speed set up to 800 Mbps
1: Speed set up to 400 Mbps

[16] **COMPENSATION_BYPASS:** Selects internally generated compensation bits or external compensation code.
1: Provides compensation bits generated by Pivot compensation cell
0: Provides external bits generated by USER_COMP to compensation cell

[15:0] **USER_COMP[47:32]:** External compensation command bit.

SYSTEM_CONFIG3 Video DAC / HDMI config register



Address: *SystemConfigBaseAddress* + 0x010C

Type: RW

Reset: 0x32644000

Description: DAC config

[31:24] **PLL_S_HDMI_MDIV[7:0]:** Sets the dividing factor of the 8-bit programmable input divider.

[23:16] **PLL_S_HDMI_NDIV[7:0]:** Sets the dividing factor of the 8-bit programmable loop divider.

[15:13] **PLL_S_HDMI_PDIV[2:0]**: Sets the dividing factor of the 3-bit programmable output divider.

[12] **PLL_S_HDMI_ENABLE**: This signal determines the mode of operation of the rejection PLL.
0: PLL is powered down 1: Rejection PLL is powered up

[11] **S_HDMI_RST_N:**
0: HDMI serializer reset is asserted 1: HDMI serializer is de-asserted

[10] **DVONOTPAD_DVP_MAIN:**
0: DVP video input coming from pads 1: DVP video input coming from DVO

[9] **TST_DAC_HD_CMDR:** Functions with CMDR signals. Can be used to force DAC HD O/P.

[8] **TST_DAC_HD_CMDS:** Functions with CMDS signal. Can be used to force DAC HD O/P.

[7] **TST_DAC_SD_CMDR:** Functions with CMDR signals. Can be used to force DAC SD O/P.

[6] **TST_DAC_SD_CMDS**: Functions with CMDS signal. Can be used to force DAC SD O/P.

[5] **DAC_HD_HZU**:
1: Disables the DAC HD output current and puts the O/P in high impedance mode, but leaves the reference circuitry powered for fast recovery to active mode.

[4] **DAC_HD_HZV**:
1: Disables the DAC HD output current and puts the O/P in high impedance mode, but leaves the reference circuitry powered for fast recovery to active mode.

[3] **DAC_HD_HZW**:
1: Disables the DAC HD output current and puts the O/P in high impedance mode, but leaves the reference circuitry powered for fast recovery to active mode.

[2] **DAC_SD_HZU**:
1: Disables the DAC SD output current and puts the O/P in high impedance mode, but leaves the reference circuitry powered for fast recovery to active mode.

[1] **DAC_SD_HZV**:
1: Disables the DAC SD output current and puts the O/P in high impedance mode, but leaves the reference circuitry powered for fast recovery to active mode.

[0] **DAC_SD_HZW**:
1: Disables the DAC SD output current and puts the O/P in high impedance mode, but leaves the reference circuitry powered for fast recovery to active mode.

SYSTEM_CONFIG4 STBus / USB config control register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															USBPHY_INEDGECTRL2	USB_INDCSHIFT2	USBPHY_INEDGECTRL1	USB_INDCSHIFT1	CFG_USB2_OVRCURR_ENABLE	CFG_USB1_OVRCURR_ENABLE	CFG_TSIN2_SRC_SELECT	CFG_TSIN1_SRC_SELECT	RESERVED	USB_PHY_XTAL_VALID	USB2_PRT_OVCURR_SEL	USB1_PRT_OVCURR_SEL	USB2_PRT_OVCURR_POL	USB1_PRT_OVCURR_POL	PLI_CLOCK_STOP	USB_HOST_SOFT_RESET_ENABLE	ENABLE_TID_DELTAMU

Address: *SystemConfigBaseAddress* + 0x0110

Type: RW

Reset: 0x00000126

Description: STBus/ USB Config

[31:17] **RESERVED**

[16] **USBPHY_INEDGECTRL2:**
1: USBPHY_INEDGECTRL2 is active 0: USBPHY_INEDGECTRL2 is inactive

[15] **USB_INDCSHIFT2**
1: USBPHY_INDCSHIFT2 is active 0: USBPHY_INDCSHIFT2 is inactive

[14] **USBPHY_INEDGECTRL1:**
1: USBPHY_INEDGECTRL1 is active 0: USBPHY_INEDGECTRL1 is inactive

[13] **USB_INDCSHIFT1:**
1: USBPHY_INDCSHIFT1 is active 0: USBPHY_INDCSHIFT1 is inactive

[12] **CFG_USB2_OVRCURR_ENABLE:**
1: USB2_overcurrent is enabled 0: Disabled

[11] **CFG_USB1_OVRCURR_ENABLE:**
1: USB1_overcurrent is enabled 0: Disabled

[10] **CFG_TSIN2_SRC_SELECT:**
1: TSin2 is from PIO14 0: TSin2 is from PIO6

[9] **CFG_TSIN1_SRC_SELECT:**
1: TSin1 is selected from PIO15 0: TSin1 is from PIO12

[8] **RESERVED**

[7] **USB_PHY_XTAL_VALID:**
1: OSC input to USB PHY is stable 0: OSC input is invalid

[6] **USB2_PRT_OVCURR_SEL:**
1: USB2_PRT_OVCURR_IN is from PIO14[6] 0: From PIO4[6]

[5] **USB1_PRT_OVCURR_SEL:**
1: USB1_PRT_OVCURR_IN is from PIO12[5] 0: From PIO4[4]

[4] **USB2_PRT_OVCURR_POL:**
1: USB2_PRT_OVCURR is active high 0: USB2_PRT_OVCURR is sensed active low

[3] **USB1_PRT_OVCURR_POL:**
1: USB1_PRT_OVCURR is active high 0: USB1_PRT_OVCURR is sensed active low

[2] **PLI_CLOCK_STOP:**
1: Stops the PLL1600 clock output to LMI padlogic

[1] **USB_HOST_SOFT_RESET_ENABLE:**
1: Allows soft reset of USB host (active low)

[0] **ENABLE_TID_DELTAMU:**
1: Enables TID[3:0] generation for DeltaMu Rasta STBUS plug2

SYSTEM_CONFIG5 EMI / PCI config register

31 30	29	28	27 26	25	24	23	22	21	20	19	18	17	16 15 14 13 12	11 10	9 8	7	6	5 4	3	2	1	0
RESERVED	PCI_DEVICE_NOT_HOST_ENABLE	PCI_CLOCK_MASTER_NOT_SLAVE	RESERVED	PCI_LOCK_IN_SEL	PCI_SYS_ERROR_ENABLE	PCI_RESETN_ENABLE	PCI_INT_TO_HOST_ENABLE	PCI_INT0_FROM_DEVICE	PCI_INT1_FROM_DEVICE	PCI_INT2_FROM_DEVICE	RESERVED	PCI_LOCK_IN_ENABLE	RESERVED	FMI_PULLUP_DISABLE[1:0]	FMI_GEN_CFG[1:0]	RESERVED	FMI_BUSFREE_ACCESS_ENABLE	RESERVED	RESERVED	RESERVED	RESERVED	DVBCI_MODE_ENABLE

Address: *SystemConfigBaseAddress* + 0x0114

Type: RW

Reset: 0x04000040

Description: EMI / PCI config

[31:30] **RESERVED**

[29] **PCI_DEVICE_NOT_HOST_ENABLE:**
1: PCI is a device 0: PCI is a host

[28] **PCI_CLOCK_MASTER_NOT_SLAVE:**
1: PCI clock is master 0: PCI clock is slave

[27:26] **RESERVED**

[25] **PCI_LOCK_IN_SEL:**
1: PCI_LOCK_IN is from PIO15[5] 0: PCI_LOCK_IN is from PIO7[0]

[24] **PCI_SYS_ERROR_ENABLE:**
1: Indicates PCI_SYSTEM_ERROR enabled 0: ISs disabled

[23] **PCI_RESETN_ENABLE:**
1: Indicates PCI_RESETN_FROM_HOST_TO_DEVICE is enabled
0: Indicates PCI_RESETN_FROM_HOST_TO_DEVICE is disabled

[22] **PCI_INT_TO_HOST_ENABLE:**
1: Indicates INT_PCI_TO_HOST enabled 0: Indicates INT_PCI_TO_HOST is disabled

[21] **PCI_INT0_FROM_DEVICE:**
1: Indicates PCI_INT_FROM_DEVICE[0] is enabled 0: Indicates disabled

[20] **PCI_INT1_FROM_DEVICE:**
1: Indicates PCI_INT_FROM_DEVICE[1] is enabled 0: Indicates disabled

[19] **PCI_INT2_FROM_DEVICE:**
1: Indicates PCI_INT_FROM_DEVICE[2] is enabled 0: Indicates disabled

[18] **RESERVED**

[17] **PCI_LOCK_IN_ENABLE:**
1: Indicates usage of PCI_LOCK_IN is enabled 0: indicates disabled

[16:12] **RESERVED**

[11:10] **FMI_PULLUP_DISABLE[1:0]:**
1: Pullup is disabled 0: Pullup is enabled

[9:8] **FMI_GEN_CFG[1:0]:** Decides whether re-timing stages are used or not in FMI padlogic

[7] **RESERVED**

[6] **FMI_BUSFREE_ACCESS_ENABLE:**
1: EMI_BUS_FREE_ACCESSPENDING_IN enabled 0: Indicates disabled

[5:4] **RESERVED**

[3] **RESERVED**

[2] **RESERVED**

[1] **RESERVED**

[0] **DVBCI_MODE_ENABLE:**
1: Indicates DVB-CI mode is enabled 0: DVBCI mode is disabled

SYSTEM_CONFIG6 Video-out config control register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																OLD_FASHIONED_DVO1	AUX_NOT_MAIN_DVO1	REF_NO_SYNCH_DVO1	H_NOT_V_DVO1	SPDIF_CHANNEL_SEL		PCMPLYR0_OUT_SEL			OLD_FASHIONED_DVO0	AUX_NOT_MAIN_DVO0	REF_NO_SYNCH_DVO0	H_NOT_V_DVO0	BOT_NOT_TOP_INVERSION	AUDIO_SYNC_MAIN_NOT_AUX	PIP_MODE

Address: *SystemConfigBaseAddress* + 0x0118

Type: RW

Reset: 0x0000

Description: Video-out config

[31:16] **RESERVED**

[15] **OLD_FASHIONED_DVO1:**
1: H/V reference and synch are from main 0: H/V reference and synch are from VTG1

[14] **AUX_NOT_MAIN_DVO1:**
1: H/V reference is taken from AUX channel 0: H/V reference is taken from main channel

[13] **REF_NO_SYNCH_DVO1:**
1: Input from pad is H/V reference 0: Input is H/V sync for DVO1

[12] **H_NOT_V_DVO1:**
1: H ref/sync is selected 0: V ref/sync is selected for DVO1

[11:10] **SPDIF_CHANNEL_SEL:**
00: SPDIF_CH0 is selected 01: SPDIF_CH1 is selected
10: SPDIF_CH2 is selected 11: SPDIF_CH3 is selected

[9:7] **PCMPLYR0_OUT_SEL:**
000: PCM channel 0 is routed to PCM_READER

[6] **OLD_FASHIONED_DVO0:**
1: H/V reference and synch are from main 0: H/V reference and synch are from VTG0

[5] **AUX_NOT_MAIN_DVO0:**
1: H/V reference is taken from AUX channel 0: H/V reference is taken from main channel

[4] **REF_NO_SYNCH_DVO0:**
1: Input from pad is H/V reference 0: Input is H/V sync for DVO0

[3] **H_NOT_V_DVO0:**
1: H ref/sync is selected 0: V ref/sync is selected for DVO0

[2] **BOT_NOT_TOP_INVERSION:**
1: Inversion is enabled 0: Inversion is disabled

[1] **AUDIO_SYNC_MAIN_NOT_AUX:**
1: Audio synch is taken from VTG_MAIN 0: Audio synch is taken from VTG_AUX

[0] **PIP_MODE:**
1: Video2 plug of compositor is routed to main mixer else on AUX mixer

SYSTEM_CONFIG7 Comms/Ethernet config control register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				ENMII	PHY_INTF_SELECT		RESERVED	GLOBAL_POWER_DOWN	DAA_CONFIG_CTRL	RESERVED	MAC_SPEED_SEL	RESERVED	RMII_MODE	MIIM_DIO_SELECT	ETHERNET_INTERFACE_ON	RESERVED				DAA_SERIAL_MODE	SC1_COND_VCC_ENABLE	SC_DETECT_VPP_POL	IRB_DATA_OUT_POL_OD	SC0_DETECT_VCC_POL	SC0_COND_VCC_ENABLE	SC0_NOT_SC1_SELECT	SCCLK1_NOT_CLKDSS	SCCLK0_NOT_CLKDSS	SC1_DETECT_VCC_POL	UART2_CTS_SRC_SELECT	UART2_RXD_SRC_SELECT	SCIF_PIO_OUTEN	

Address: *SystemConfigBaseAddress* + 0x011C

Type: RW

Reset: 0x08081000

Description: COMMS/Ethernet config

[31:28] **RESERVED**

[27] **ENMII:**
1: MII mode 0: Reverse MII mode

[26:25] **PHY_INTF_SELECT:** Selects the type of Ethernet mode
00: MII mode (Default) 01: Reserved
1x: Reserved

[24] **RESERVED**

[23] **GLOBAL_POWER_DOWN:**
1: Activate low power 0: Normal mode

[22] **DAA_CONFIG_CTRL:** DAA configuration control

[21] **RESERVED**

[20] **MAC_SPEED_SEL:**
1: Indicates that the MAC is running at 100 Mbps speed
0: Indicates that the MAC is running at 10 Mbps speed
Remark: Useless if RMII interface is not activated (SYSTEM_CONFIG7[18]). MAC speed does not need to be specified in MII mode.

[19] **RESERVED**

[18] **RMII_MODE:**
1: RMII interface activated 0: MII interface activated

[17] **MIIM_DIO_SELECT:**
1: MIIM_DIO from external input, else from GMAC

[16] **ETHERNET_INTERFACE_ON:**
1: Ethernet on (pads enables controlled by MAC) 0: All MII pads in input mode

[15:13] **RESERVED**

[12] **DAA_SERIAL_MODE:** DAA serial interface mode select pin
1: Sets a start pulse on FSYNC at the beginning of the transition
0: Sets a low level on FSYNC at the beginning of the transition

[11] **SC1_COND_VCC_ENABLE:** Enables control of smart card VCC upon detection of smart card removal or insertion.This bit is overridden by PDES_SC_MUXOUT, which is driven by a configuration bit in the PDES.
1: Alternate PIO output pin SC_NOT_SETVCC is controlled according to input SC_DETECT
0: Alternate PIO output pin SC_NOT_SETVCC is driven permanently low

[10] **SC_DETECT_VPP_POL:**
1: Output pin SC_NOT_SETVPP is inverted of PDES_SC_SETVPP
0: Output pin SC_NOT_SETVPP is PDES_SC_SETVPP

[9] **IRB_DATA_OUT_POL_OD:** Selection of polarity of IRB output signal routed as alternate function IRB_DATA_OUT_OD to PIO_3[6] (normally configured as open-drain)
0: IRB_DATA_OUT_OD has same polarity as IRB_DATA_OUT
1: Polarity of IRB_DATA_OUT_OD is inverted

[8] **SC0_DETECT_VCC_POL:**
1: Output pin SC_NOT_SETVPP is inverted 0: Output pin SC_NOT_SETVPP is not inverted

[7] **SC0_COND_VCC_ENABLE:** Enables control of smart card VCC upon detection of smart card removal or insertion.This bit is overridden by PDES_SC_MUXOUT, which is driven by a configuration bit in the PDES.
1: Alternate PIO output pin SC_NOT_SETVCC is controlled according to input SC_DETECT
0: Alternate PIO output pin SC_NOT_SETVCC is driven permanently low

[6] **SC0_NOT_SC1_SELECT:**
1: Smartcard 0 is selected 0: Smartcard1 is selected

[5] **SCCLK1_NOT_CLKDSS:** Smartcard clock muxing selection.
1: Smart card clock sourced from smart card clock generator (COMMS): SCCLKGEN1_CLK_OUT
0: Smart card clock sourced from CLK_DSS (CLKgen B)

[4] **SCCLK0_NOT_CLKDSS:** Smartcard clock muxing selection.
1: Smart card clock sourced from smart card clock generator (COMMS): SCCLKGEN0_CLK_OUT
0: Smart card clock sourced from CLK_DSS (CLKgen B)

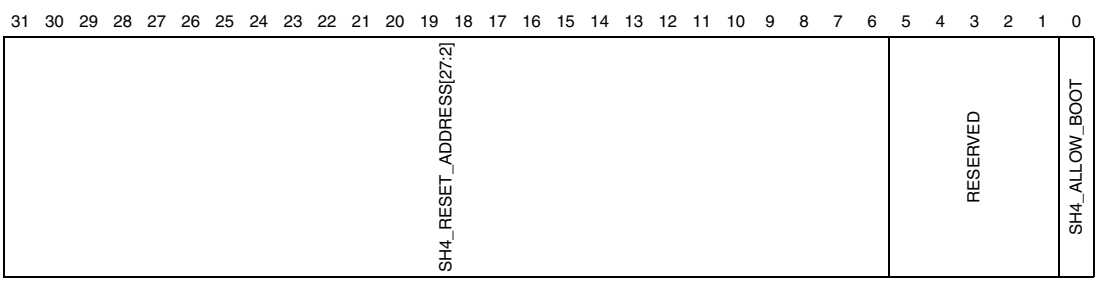
[3] **SC1_DETECT_VCC_POL:**
1: Output pin SC1_NOT_SETVCC is inverted
0: Output pin SC1_NOT_SETVCC is un-inverted

[2] **UART2_CTS_SRC_SELECT:**
1: UART2_CTS is from PIO12[2] 0: From PIO4[2]

[1] **UART2_RXD_SRC_SELECT:**
1: UART2_RXD is from PIO12[1] 0: From PIO4[1]

[0] **SCIF_PIO_OUTEN:**
1: SCIF output enable 0: Used as regular PIO

SYSTEM_CONFIG8 SH4 boot config control register



Address: *SystemConfigBaseAddress* + 0x0120

Type: RW

Reset: 0x01(1)

Description: This register configures the ST40 boot process. Bit 0 controls the ST40 boot request upon reset. Its value depends on the mode_pins (9:8) captured during the reset period.

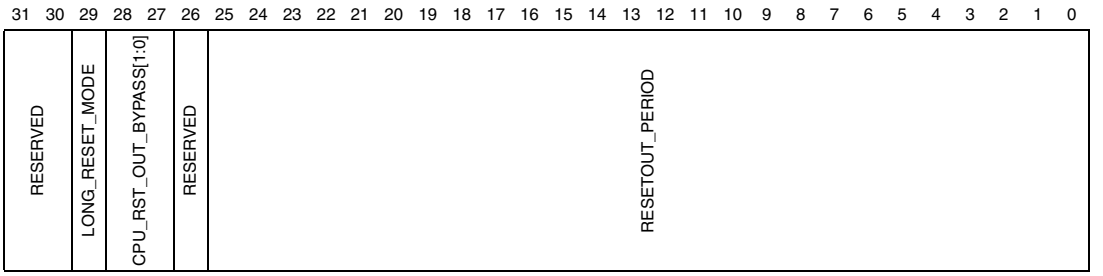
[31:6] **SH4_RESET_ADDRESS[27:2]:** NDS compliance.

1. 0x01 when MODE[9:8]=00; ST40 boots, 0x00 for other values of MODE[9:8]

[5:1] **RESERVED**

[0] **SH4_ALLOW_BOOT**: SH4 request filter control.
1: Request enabled
0: Request bypassed

SYSTEM_CONFIG9 Reset Gen config control register



Address: *SystemConfigBaseAddress* + 0x0124

Type: RW

Reset: 0xXXXX(1)

Description: Reset Gen config

[31:30] **RESERVED**

[29] **LONG_RESET_MODE:** ResetOut mode. Reset value from mode pin (7)

[28:27] **CPU_RST_OUT_BYPASS[1:0]:**
CPU_RST_OUT_BYPASS (1): bypass of (LX_Audio+LXDelphi) reset loop back
CPU_RST_OUT_BYPASS (0): bypass of (SH4+LX_Audio+LXDelphi) reset loop back
Reset value from mode pin (6:5).

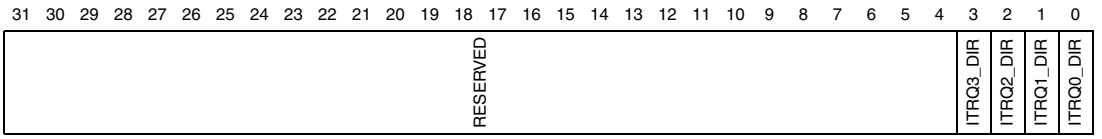
[26] **RESERVED**

[25:0] **RESETOUT_PERIOD**: Period of ResetOut in 27MHz cycles.
In Long ResetOut mode, the reset value guarantees a 200 ms reset out.
In short ResetOut mode, reset out lasts 100 us.
This dynamic of this register allows for a max reset out of 2.48 s.
Reset value: 0x5265C0 in long ResetOut mode(a), 0x000A8C in short ResetOut mode

a. Long ResetOut mode is selected when the CONF input mode_pin(7) is set to 1.

1. Depends on mode pin

SYSTEM_CONFIG10 ITRQ pins config control register



Address: *SystemConfigBaseAddress* + 0x0128

Type: RW

Reset: 0x000F

Description: ITRQ pins config

[31:4] **RESERVED**

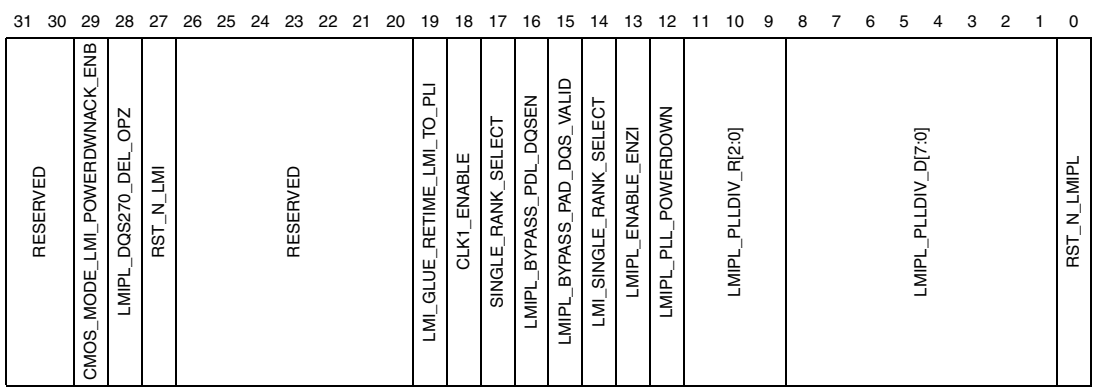
[3] **ITRQ3_DIR**:
1: ITRQ3 is configured as input 0: ITRQ3 is configured as output

[2] **ITRQ2_DIR**:
1: ITRQ2 is configured as input 0: ITRQ2 is configured as output

[1] **ITRQ1_DIR**: 1: ITRQ1 is configured as input 0: ITRQ1 is configured as output

[0] **ITRQ0_DIR**: ITRQ0 pin direction:
0: ITRQ0 configured as output 1: ITRQ0 configured as input

SYSTEM_CONFIG11 GP-LMI / LMI padlogic config control register



Address: *SystemConfigBaseAddress* + 0x012C

Type: RW

Reset: 0x00000D28

Description: LMI padlogic config

[31:30] **RESERVED**

[29] **CMOS_MODE_LMI_POWERDWNACK_ENB**
1: CMOS mode power mode is enabled 0: CMOS mode power mode is disabled

[28] **LMIPL_DQS270_DEL_OPZ**: Selects dqs270_del as 3T/4 or T/2 (1=T/2)

[27] **RST_N_LMI:**
1: LMI sub system reset. Active Low.

[26:20] **RESERVED**

[19] **LMI_GLUE_RETIME_LMI_TO_PLI:**
1: Re-time is done 0: No re-time

[18] **CLK1_ENABLE:**
1: clk1 is enabled 0: clk1 is disabled

[17] **SINGLE_RANK_SELECT:**
1: Single rank is selected 0: Dual rank (default)

[16] **LMIPL_BYPASS_PDL_DQSEN**:
1: Bypasses PDL component of DQS_EN_DEL timing.

[15] **LMIPL_BYPASS_PAD_DQS_VALID**:
1: Bypasses dummy pad component of DQS_EN_DEL timing.

[14] **LMI_SINGLE_RANK_SELECT:**
1: Single rank is selected 0: Dual rank is selected

[13] **LMIPL_ENABLE_ENZI**:
1: Overrides ENZI disable when MODEZI = 0 (differential input mode).

[12] **LMIPL_PLL_POWERDOWN:** PLL power down
0: Normal mode 1: Power down mode

[11:9] **LMIPL_PLLDIV_R[2:0]:** Default values for PLL output clock at 666 MHz
Values for PLL output clock at 800 MHz:
LMIPL0_PLLDIV_R(2:0) = 100

[8:1] **LMIPL_PLLDIV_D[7:0]:** Default values for PLL output clock at 666 MHz
Values for PLL output clock at 800 MHz:
LMIPL0_PLLDIV_R[2:0] = 100

[0] **RST_N_LMIPL**: LMISYS_PL reset. Active low.

SYSTEM_CONFIG12 GP-LMI / LMI padlogic config control register

31	30	29	28	27	26	25	24	23	22	21 20 19 18 17 16 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONF_LMIPL_FUNC_OTHERS_PD	CONF_LMIPL_FUNC_OTHERS_PU	CONF_LMIPL_FUNC_CMDDQSNCKN_PD	CONF_LMIPL_FUNC_CMDDQSNCKN_PU	LMIPL_IOREF_TQ	LMIPL_IOREF_DDR_COMP	LMIPL_IOREF_ACCURATE	LMIPL_IOREF_FREEZE	LMIPL_IOREF_COMPTQ	LMIPL_IOREF_COMPEN	LMIPL_IOREF_RASRC[6:0]	LMIPL_FUNC_TQ_VREF	LMIPL_FUNC_USEPAD_VREF	LMIPL_FUNC_ODTB	LMIPL_FUNC_ODTA	LMIPL_FUNC_MODEZI	LMIPL_FUNC_ZOUTPROGA_CMD	LMIPL_FUNC_ZOUTPROGA_CK	LMIPL_FUNC_ZOUTPROGA_DQDQSDM	LMIPL_FUNC_PROGB_CMD	LMIPL_FUNC_PROGB_CK	LMIPL_FUNC_PROGB_DQDQSDM	LMIPL_FUNC_PROGA_CMD	LMIPL_FUNC_PROGA_CK	LMIPL_FUNC_PROGA_DQDQSDM	LMIPL_FUNC_DDR

Address: *SystemConfigBaseAddress* + 0x0130

Type: RW

Reset: 0xA200180F

Description: GP-LMI / LMI padlogic config

[31] **CONF_LMIPL_FUNC_OTHERS_PD (func_pdn_active_hi):** Other pads than CMD, DQSN, CKN pulldown command.

[30] **CONF_LMIPL_FUNC_OTHERS_PU (func_pu_active_high):** Other pads than CMD, DQSN, CKN pullup command.

[29] **CONF_LMIPL_FUNC_CMDDQSNCKN_PD (func_pdn_active_lo):** CMD, DQSN, CKN pad pulldown command.

[28] **CONF_LMIPL_FUNC_CMDDQSNCKN_PU (func_pu_active_lo):** CMD, DQSN, CKN pad pullup command.

[27] **LMIPL_IOREF_TQ:**
1: IDDQ mode select.

[26] **LMIPL_IOREF_DDR_COMP:**
1: Controls PSW compensation signal.

[25] **LMIPL_IOREF_ACCURATE:**
1: Accurate mode select.

[24] **LMIPL_IOREF_FREEZE:**
1: Freezes compensation code.

[23] **LMIPL_IOREF_COMPTQ:** Operating mode.

[22] **LMIPL_IOREF_COMPEN:** Operating mode.

[21:15] **LMIPL_IOREF_RASRC[6:0]:** Input code.

[14] **LMIPL_FUNC_TQ_VREF:** TQ setting for VREFIN pad control.

[13] **LMIPL_FUNC_USEPAD_VREF:** Use PAD setting for VREFIN pad.

[12] **LMIPL_FUNC_ODTB:**

[11] **LMIPL_FUNC_ODTA:** ODTA / ODTB controlling On Die Termination
00: Disabled 01: RTT2 = 150 Ω
10: RTT2 = 150 Ω 11: RTT1 = 75 Ω

[10] **LMIPL_FUNC_MODEZI:** Receiver mode select (I/O MODEZI)
0: Differential 2.5V receiver for DDR1 or Differential 1.8V receiver for DDR2
1: 2.5V Digital CMOS receiver for DDR1 or 1.8V Digital CMOS receiver for DDR2

[9] **LMIPL_FUNC_ZOUTPROGA_CMD (func_zoutproga_abc):** Outputs buffer impedance (I/O ZOUTPROGA).

[8] **LMIPL_FUNC_ZOUTPROGA_CK (func_zoutproga_k):** Outputs buffer impedance (I/O ZOUTPROGA).

[7] **LMIPL_FUNC_ZOUTPROGA_DQDQSDM (func_zoutproga_d):** Outputs buffer impedance(I/O ZOUTPROGA).
0: 25 Ω (Strong SSTL2)
1: 40 Ω (Weak SSTL2)

[6] **LMIPL_FUNC_PROGB_CMD (func_progb_abc):** PROGB for CMD pads.

[5] **LMIPL_FUNC_PROGB_CK (func_progb_k):** PROGB for CK/CKN pads.

[4] **LMIPL_FUNC_PROGB_DQDQSDM (func_progb_d):** PROGB for DQ/DQS/DQSN/DM pads.

[3] **LMIPL_FUNC_PROGA_CMD (func_proga_abc):** PROGA for CMD pads.

[2] **LMIPL_FUNC_PROGA_CK (func_proga_k):** PROGA for CK/CKN pads.

[1] **LMIPL_FUNC_PROGA_DQDQSDM (func_proga_d):** PROGA for DQ/DQS/DQSN/DM pads.

[0] **LMIPL_FUNC_DDR:** DDR mode
0: DDR1 operation mode (2.5V) 1: DDR2 operation mode (1.8V)

SYSTEM_CONFIG13 GP-LMI / LMI padlogic config control register

31–23	22	21	20–19–18	17	16–15–14–13–12–11–10–9–8	7–6–5–4	3	2	1	0
RESERVED	LMIPL_FORCE_DQS_VALID_MINUS_HALF	LMIPL_FORCE_ODT_INT_MINUS_HALF	RESERVED	LMIPL0_SEL_OEN_DEL	LMIPL0_DLL1_USR_CMD[8:0]	LMIPL0_DLL1_LOCK_CON[3:0]	LMIPL0_DLL1_INT_CMD_CON	LMIPL0_DLL1_EXT_CMD_CON	LMIPL0_PDL_CLK_OPZ_DLL1	LMIPL0_DLL1_SOFT_RST

Address: *SystemConfigBaseAddress* + 0x0134

Type: RW

Reset: 0x00000000

Description: LMI padlogic config

[31:23] **RESERVED**

[22] **LMIPL_FORCE_DQS_VALID_MINUS_HALF:** Utilizes negative shift of DDR 0.5 CAS latency in DDR2 mode for dqs270_valid timing.
0: Aligned 1: T/2

[21] **LMIPL_FORCE_ODT_INT_MINUS_HALF:** Utilizes negative shift of DDR 0.5 CAS latency in DDR2 mode for odt_int timing.
0: Aligned 1: T/2

[20:18] **RESERVED**

[17] **LMIPL0_SEL_OEN_DEL:** DATA/DM output enable timing options (T/4 resolution).

[16:8] **LMIPL0_DLL1_USR_CMD[8:0]:** Allows user control of DLL1 delay.

[7:4] **LMIPL0_DLL1_LOCK_CON[3:0]:** Defines lock condition for DLL1.

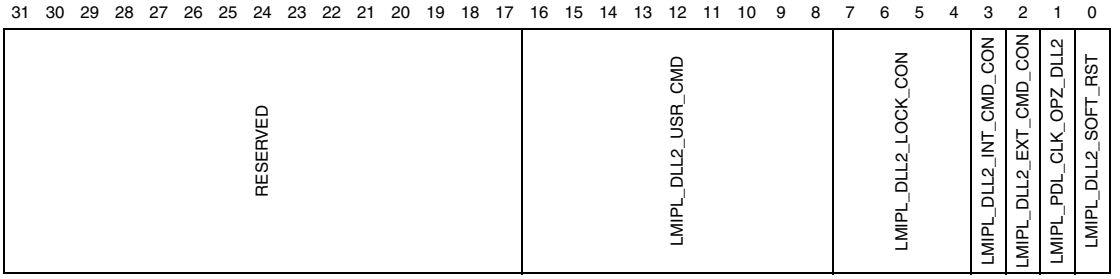
[3] **LMIPL0_DLL1_INT_CMD_CON:** Controls which internal delay command is used for DLL1.

[2] **LMIPL0_DLL1_EXT_CMD_CON:** Controls which external delay command is used for DLL1.

[1] **LMIPL0_PDL_CLK_OPZ_DLL1:** Selects CLK_COMMAND inputs for DLL1 PDLs (LOW = PDL output, HIGH = DLL output).

[0] **LMIPL0_DLL1_SOFT_RST:** DLL1 soft reset.

SYSTEM_CONFIG14 LMI padlogic config control register



Address: *SystemConfigBaseAddress* + 0x0138

Type: RW

Reset: 0x0000

Description: LMI Padlogic config

[31:17] **RESERVED**

[16:8] **LMIPL_DLL2_USR_CMD:** Allows user control of DLL2 delay.

[7:4] **LMIPL_DLL2_LOCK_CON:** Defines lock condition for DLL2.

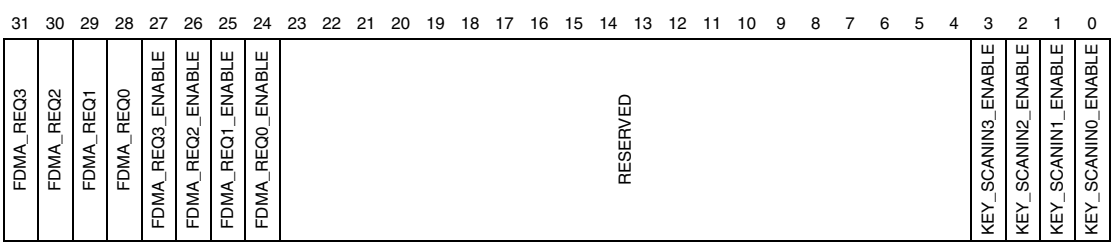
[3] **LMIPL_DLL2_INT_CMD_CON:** Controls which internal delay command is used for DLL2.

[2] **LMIPL_DLL2_EXT_CMD_CON:** Controls which external delay command is used for DLL2.

[1] **LMIPL_PDL_CLK_OPZ_DLL2:** Selects CLK_COMMAND inputs for DLL2 PDLs (LOW = PDL output, HIGH = DLL output).

[0] **LMIPL_DLL2_SOFT_RST:** DLL2 soft reset.
1: DLL2 soft reset is active 0: DLL2 soft reset is inactive

SYSTEM_CONFIG15 FDMA and key scan config register



Address: *SystemConfigBaseAddress* + 0x013C

Type: RW

Reset: 0x000000

Description: FDMA and key scan config

[31] **FDMA_REQ3:** Internal FDMA req 3 ORed with external FDMA req 3

[30] **FDMA_REQ2:** Internal FDMA req 2 ORed with external FDMA req 2

[29] **FDMA_REQ1:** Internal FDMA req 1ORed with external FDMA req 1

[28] **FDMA_REQ0:** Internal FDMA req 0 ORed with external FDMA req 0

[27] **FDMA_REQ3_ENABLE:** External FDMA req 3 enable

[26] **FDMA_REQ2_ENABLE:** External FDMA req 2 enable

[25] **FDMA_REQ1_ENABLE:** External FDMA req 1 enable

[24] **FDMA_REQ0_ENABLE:** External FDMA req 0 enable

[23: 4] **RESERVED**

[3] **KEY_SCANIN3_ENABLE:**
1: Indicates key_scanin3 enabled 0: Indicates key_scanin3 disabled

[2] **KEY_SCANIN2_ENABLE:**
1: Indicates key_scanin2 enabled 0: Indicates key_scanin2 disabled

[1] **KEY_SCANIN1_ENABLE:**
1: Indicates key_scanin1 enabled 0: Indicates key_scanin1 disabled

[0] **KEY_SCANIN0_ENABLE:**
1: Indicates key_scanin0 enabled 0: Indicates key_scanin0 disabled

SYSTEM_CONFIG16 Comms SSC configuration register

31–20	19–18	17–16	15–14	13	12–11	10–9	8–7	6–4	3	2–1	0
RESERVED	SSC3_SCLK_IN	SSC3_MTSR_IN_SEL[1:0]	SSC3_MRST_IN_SEL[1:0]	RESERVED	SSC2_SCLK_IN[1:0]	SSC2_MTSR_IN_SEL[1:0]	SSC2_MRST_IN_SEL[1:0]	RESERVED	SSC1_MRST_IN_SEL	RESERVED	SSC0_MRST_IN_SEL

Address: *SystemConfigBaseAddress* + 0x0140

Type: RW

Reset: 0x000000

Description: Comms SSC config

[31:20] **RESERVED**

[19:18] **SSC3_SCLK_IN:**
00: Invalid 01: ssc3_sclk_in from PIO3[6]
10: ssc3_sclk_in from PIO13[2] 11: ssc3_sclk_in from PIO13(6)

[17:16] **SSC3_MTSR_IN_SEL[1:0]:**
00: ssc3_mtsr_in from PIO2[1] 01: ssc3_mtsr_in from PIO3[7]
10: ssc3_mtsr_in from PIO13[3] 11: ssc3_mtsr_in from PIO13[7]

[15:14] **SSC3_MRST_IN_SEL[1:0]:**
00: ssc3_mrst_in from PIO2[1] 01: ssc3_mrst_in from PIO3(7)
10: ssc3_mrst_in from PIO13[3] 11: ssc3_mrst_in from PIO13(7)

[13] **RESERVED**

[12:11] **SSC2_SCLK_IN[1:0]:**
0x: ssc2_sclk_in from PIO3[4] 10: ssc2_sclk_in from PIO12[0]
11: ssc2_sclk_in from PIO13[4]

[10:9] **SSC2_MTSR_IN_SEL[1:0]:**
00: ssc2_mtsr_in from PIO2[0] 01: ssc2_mtsr_in from PIO3[5]
10: ssc2_mtsr_in from PIO12[1] 11: ssc2_mtsr_in from PIO13[5]

[8:7] **SSC2_MRST_IN_SEL[1:0]:**
00: ssc2_mrst_in from PIO2[0] 01: ssc2_mrst_in from PIO3[5]
10: ssc2_mrst_in from PIO12[1] 11: ssc2_mrst_in from PIO13[5]

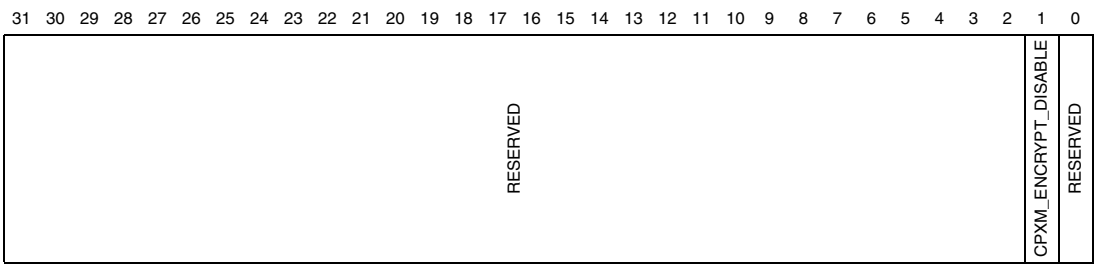
[6:4] **RESERVED**

[3] **SSC1_MRST_IN_SEL:**
1: ssc1_mrst_in is from PIO2[7] 0: ssc1_mrst_in is from PIO2[6]

[2:1] **RESERVED**

[0] **SSC0_MRST_IN_SEL:**
1: ssc0_mrst_in is from PIO2[4] 0: ssc0_mrst_in is from PIO2[3]

SYSTEM_CONFIG17 CPXM CPRM enable configuration register



Address: *SystemConfigBaseAddress* + 0x0144

Type: RW

Reset: 0x00000002

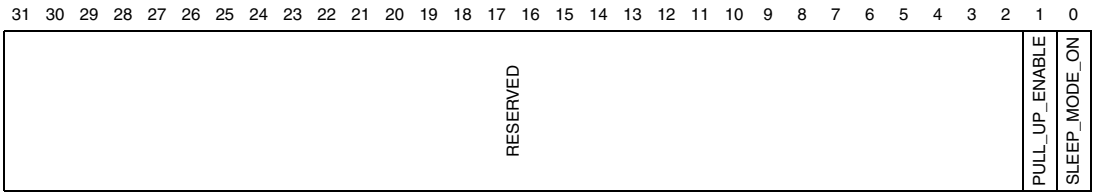
Description: CPXM CPRM encode enable config

[31:2] **RESERVED**

[1] **CPXM_ENCRYPT_DISABLE:**
1: CPXM_ENCRYPT is disabled 0: Enabled only if CPXM feature is enabled

[0] **RESERVED**

SYSTEM_CONFIG18 PAD State control register



Address: *SystemConfigBaseAddress* + 0x0148

Type: RW

Reset: 0x0000

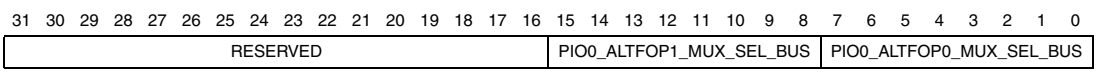
Description: Pad state config

[31:2] **RESERVED**

[1] **PULL_UP_ENABLE:**
1: Indicates pad pullup is active 0: Indicates pull up is de-active

[0] **SLEEP_MODE_ON:**
1: Indicates sleep mode control switched on 0: Indicates switched off

SYSTEM_CONFIG19 Alternate function output control for PIO 0



Address: *SystemConfigBaseAddress* + 0x014C

Type: RW

Reset: 0x0000

Description: PIO0 alternate function output config

[31:16] **RESERVED**

[15:8] **PIO0_ALTFOP1_MUX_SEL_BUS**

[7:0] **PIO0_ALTFOP0_MUX_SEL_BUS**

Note:

Alternate 1: PIO0_ALTFOPJ_MUX_SEL_BUS(n) = 00 [(j = 0,1); (n = 0,1,2,3,4,5,6,7)]
Alternate 2: PIO0_ALTFOPJ_MUX_SEL_BUS(n) = 01 [(j = 0,1); (n = 0,1,2,3,4,5,6,7)]
Alternate 3: PIO0_ALTFOPJ_MUX_SEL_BUS(n) = 10 [(j = 0,1); (n = 0,1,2,3,4,5,6,7)]
Alternate 4: PIO0_ALTFOPJ_MUX_SEL_BUS(n) = 11 [(j = 0,1); (n = 0,1,2,3,4,5,6,7)]

SYSTEM_CONFIG20 Alternate function output control for PIO 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PIO1_ALTFOP1_MUX_SEL_BUS								PIO1_ALTFOP0_MUX_SEL_BUS							

Address: *SystemConfigBaseAddress* + 0x0150

Type: RW

Reset: 0x00000000

Description: Alternate Function PIO1 Output Control

[31:16] **RESERVED**

[15:8] **PIO1_ALTFOP1_MUX_SEL_BUS**

[7:0] **PIO1_ALTFOP0_MUX_SEL_BUS**

Note:

Alternate 1: PIO1_ALTFOPj_MUX_SEL_BUS(n) = 00 [(j = 0,1); (n = 0,1,2,3,4,5,6,7)]

Alternate 2: PIO1_ALTFOPj_MUX_SEL_BUS(n) = 01 [(j = 0,1); (n = 0,1,2,3,4,5,6,7)]

Alternate 3: PIO1_ALTFOPj_MUX_SEL_BUS(n) = 10 [(j = 0,1); (n = 0,1,2,3,4,5,6,7)]

Alternate 4: PIO1_ALTFOPj_MUX_SEL_BUS(n) = 11 [(j = 0,1); (n = 0)]

SYSTEM_CONFIG21 Alternate function output control for PIO 2

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PIO2_ALTFOP1_MUX_SEL_BUS								PIO2_ALTFOP0_MUX_SEL_BUS							

Address: *SystemConfigBaseAddress* + 0x0154

Type: RW

Reset: 0x00000000

Description: PIO2 alternate function output config

[31:16] **RESERVED**

[15:8] **PIO2_ALTFOP1_MUX_SEL_BUS**

[7:0] **PIO2_ALTFOP0_MUX_SEL_BUS**

Note:

Alternate 1: PIO2_ALTFOPj_MUX_SEL_BUS(n) = 00 [(j = 0,1); (n = 0,1,2,3,4,5,6,7)]

Alternate 2: PIO2_ALTFOPj_MUX_SEL_BUS(n) = 01 [(j = 0,1); (n = 0,1,2,3,4,5,6,7)]

Alternate 3: PIO2_ALTFOPj_MUX_SEL_BUS(n) = 10 [(j = 0,1); (n = 0,1,2,3,4,5,6,7)]

Alternate 4: PIO2_ALTFOPj_MUX_SEL_BUS(n) = 11 [(j = 0,1); (n = 0,1,2,3,4,5,6,7)]

SYSTEM_CONFIG22 Compensation config register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					CONF_3V3COMP2_RASRC				CONF_3V3COMP2_FREEZE	CONF_3V3COMP2_COMPTQ	CONF_3V3COMP2_COMPEN	CONF_3V3COMP1_RASRC							CONF_3V3COMP1_FREEZE	CONF_3V3COMP1_COMPTQ	CONF_3V3COMP1_COMPEN	CONF_3V3COMP0_RASRC							CONF_3V3COMP0_FREEZE	CONF_3V3COMP0_COMPTQ	CONF_3V3COMP0_COMPEN

Address: *SystemConfigBaseAddress* + 0x0158

Type: RW

Reset: 0x00000000

Description: Compensation config

[31:30] **RESERVED**

[29:23] **CONF_3V3COMP2_RASRC:** 3V3 COMPENSATION 2: Input code

[22] **CONF_3V3COMP2_FREEZE:** 3V3 COMPENSATION 2: Freezes ASRC code to its last value

[21] **CONF_3V3COMP2_COMPTQ:**

[20] **CONF_3V3COMP2_COMPEN:** 3V3 COMPENSATION 2: Operating mode (comptq/compen)
00: Normal mode 01: HZ mode
11: Read mode

[19:13] **CONF_3V3COMP1_RASRC:** 3V3 COMPENSATION 1: Input code

[12] **CONF_3V3COMP1_FREEZE:** 3V3 COMPENSATION 1: Freezes ASRC code to its last value

[11] **CONF_3V3COMP1_COMPTQ:**

[10] **CONF_3V3COMP1_COMPEN:** 3V3 COMPENSATION 1: Operating mode (comptq/compen)
00: Normal mode 01: HZ mode
11: Read mode

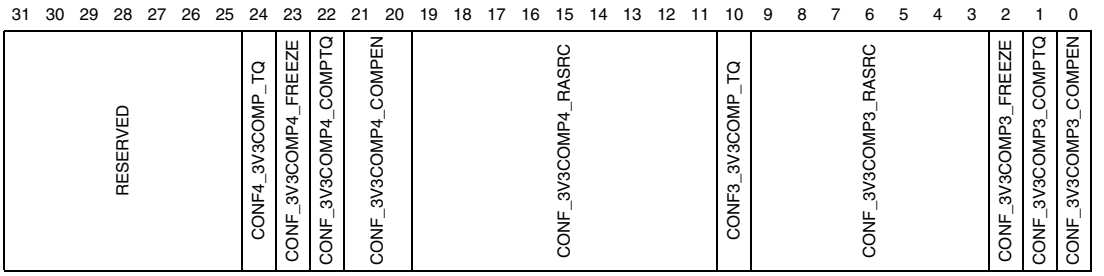
[9:3] **CONF_3V3COMP0_RASRC:** 3V3 COMPENSATION 0: Input code

[2] **CONF_3V3COMP0_FREEZE:** 3V3 COMPENSATION 0: Freezes ASRC code to its last value

[1] **CONF_3V3COMP0_COMPTQ:**

[0] **CONF_3V3COMP0_COMPEN:** 3V3 COMPENSATION 0: Operating mode (comptq/compen)
00: Normal mode 01: HZ mode
11: Read mode

SYSTEM_CONFIG23 Compensation config register



Address: *SystemConfigBaseAddress* + 0x015C

Type: RW

Reset: 0x00000000

Description: Compensation config

[31:25] **RESERVED**

[24] **CONF4_3V3COMP_TQ:** Drives the 4 compensations TQ pin 1 to put the cells in IDDQ mode

[23] **CONF_3V3COMP4_FREEZE:** 3V3 COMPENSATION 4: Freezes ASRC code to its last value

[22] **CONF_3V3COMP4_COMPTQ:**

[21:20] **CONF_3V3COMP4_COMPEN:** 3V3 COMPENSATION 4: Operating mode (comptq/compen)
00: Normal mode 01: HZ mode
11: Read mode

[19:11] **CONF_3V3COMP4_RASRC:** 3V3 COMPENSATION 4: Input code

[10] **CONF3_3V3COMP_TQ:** Drives the 4 compensations TQ pin
1: Puts the cells in IDDQ mode

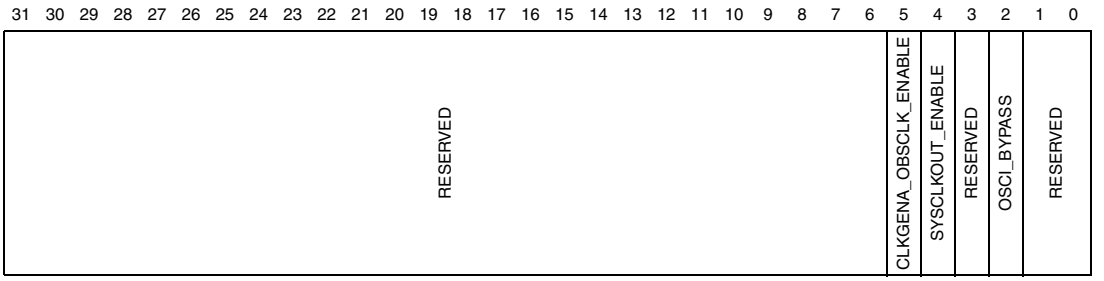
[9:3] **CONF_3V3COMP3_RASRC:** 3V3 COMPENSATION 3: Input code

[2] **CONF_3V3COMP3_FREEZE:** 3V3 COMPENSATION 3: Freeze ASRC code to its last value

[1] **CONF_3V3COMP3_COMPTQ:**

[0] **CONF_3V3COMP3_COMPEN:** 3V3 COMPENSATION 3: Operating mode (comptq/compen)
00: Normal mode 01: HZ mode
11: Read mode

SYSTEM_CONFIG24 OSC config register



Address: *SystemConfigBaseAddress* + 0x0160

Type: RW

Reset: 0x0000000C

Description: Oscillator config

[31:6] **RESERVED**

[5] **CLKGENA_OBSCLK_ENABLE:**
1: ClockGenA clk output is enabled 0: Disabled

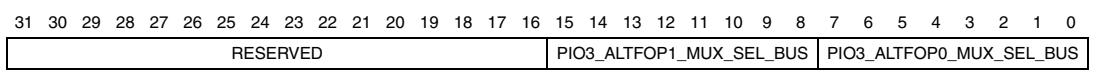
[4] **SYSCLKOUT_ENABLE:**
1: ClockGenB clk output is enabled 0: Disabled

[3] **RESERVED**

[2] **OSCI_BYPASS:**
1: OSC is not bypassed 0: OSC is bypassed

[1:0] **RESERVED**

SYSTEM_CONFIG25 Alternate function output control for PIO 3



Address: *SystemConfigBaseAddress* + 0x0164

Type: RW

Reset: 0x0000

Description: PIO3 alternate function output register

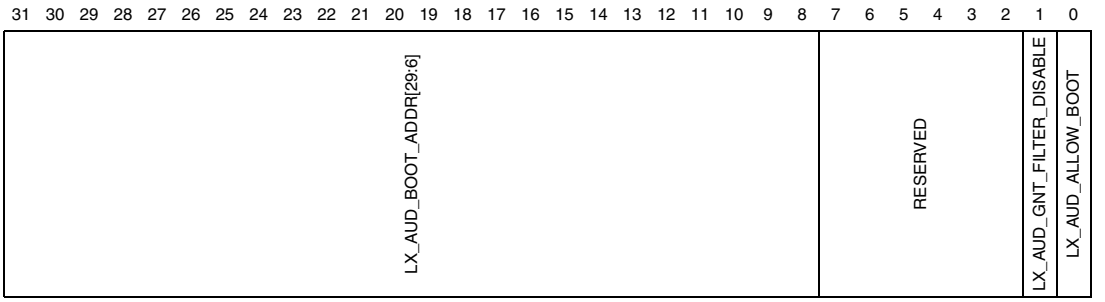
[31:16] **RESERVED**

[15:8] **PIO3_ALTFOP1_MUX_SEL_BUS**

[7:0] **PIO3_ALTFOP0_MUX_SEL_BUS**

Note: Alternate 1: PIO3_ALTFOPj_MUX_SEL_BUS(n) = 00 [(j = 0,1); (n = 0,1,2,3,4,5,6,7)]
Alternate 2: PIO3_ALTFOPj_MUX_SEL_BUS(n) = 01 [(j = 0,1); (n = 0,1,2,3,4,5,6,7)]
Alternate 3: PIO3_ALTFOPj_MUX_SEL_BUS(n) = 10 [(j = 0,1); (n = 0,1,2,3,4,5,6,7)]
Alternate 4: PIO3_ALTFOPj_MUX_SEL_BUS(n) = 11 [(j = 0,1); (n = 0,1,2,3,4,5,6,7)]

SYSTEM_CONFIG26 LX audio config register



Address: *SystemConfigBaseAddress* + 0x0168

Type: RW

Reset: 0xXXXX(1)

Description: LX Audio config

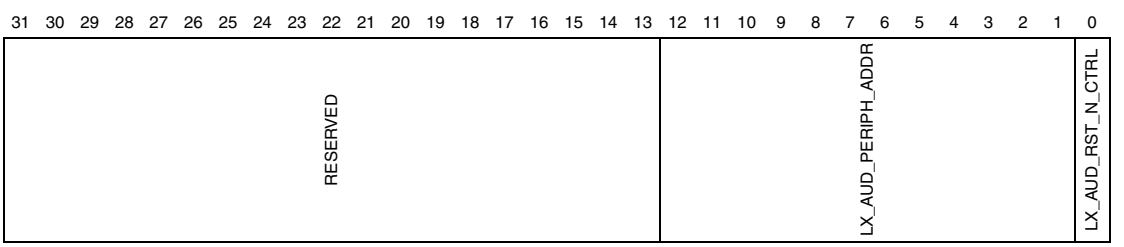
[31:8] **LX_AUD_BOOT_ADDR[29:6]:** ST230 AUDIO boot address.

[7:2] **RESERVED**

[1] **LX_AUD_GNT_FILTER_DISABLE:**
1: Filter is disabled

[0] **LX_AUD_ALLOW_BOOT:** ST230 AUDIO request filter.
1: Request enabled 0: Request bypassed

SYSTEM_CONFIG27 LX audio config register



Address: *SystemConfigBaseAddress* + 0x016C

Type: RW

Reset: 0x1FD0

Description: LX Audio config

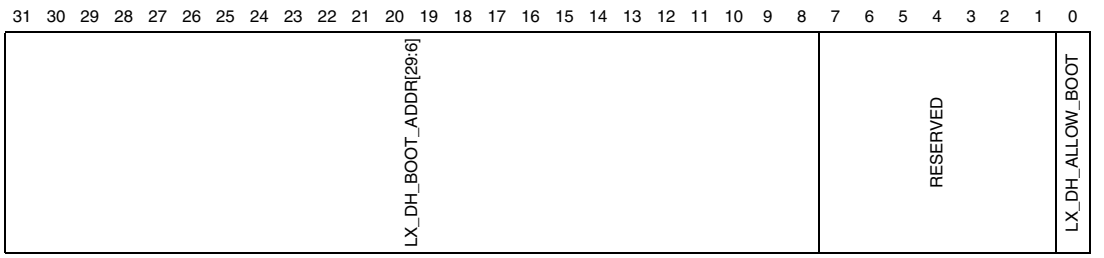
[31:13] **RESERVED**

[12:1] **LX_AUD_PERIPH_ADDR:** ST230 AUDIO peripheral address.

1. Depends on mode pins; Reset value is 1, when MODE[9:8]=10 AND LX_AUDIO_BOOT_ENABLE=1, and reset value is 0, For other values of MODE[9:8] and LX_AUDIO_BOOT_ENABLE

[0] **LX_AUD_RST_N_CTRL:** ST230 AUDIO reset active low control bit.
0: Reset of ST230 driven by hardware reset 1: Reset of ST230 fixed to active state

SYSTEM_CONFIG28 LX Delta Rasta config register



Address: *SystemConfigBaseAddress* + 0x0170

Type: RW

Reset: 0xXXXX(1)

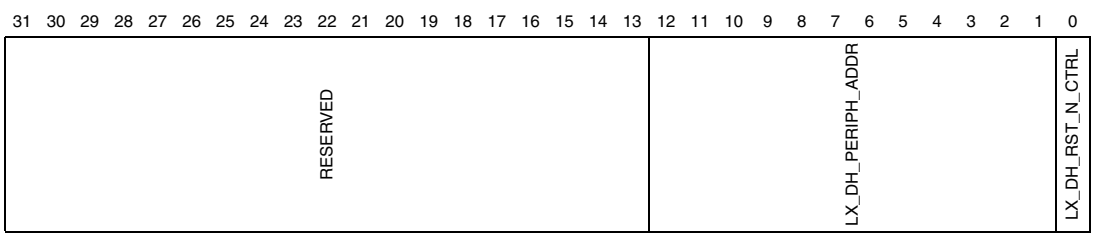
Description: LX Delta Rasta config

[31:8] **LX_DH_BOOT_ADDR[29:6]:** ST230 DELPHI boot address.

[7:1] **RESERVED**

[0] **LX_DH_ALLOW_BOOT**:
ST230 DELPHI request filter:
1: Request enabled 0: Request bypassed

SYSTEM_CONFIG29 LX Delta Rasta config register



Address: *SystemConfigBaseAddress* + 0x0174

Type: RW

Reset: 0x1FCC

Description: LX Delta Rasta config

[31:13] **RESERVED**

1. Depends on Mode pins. Reset value is:

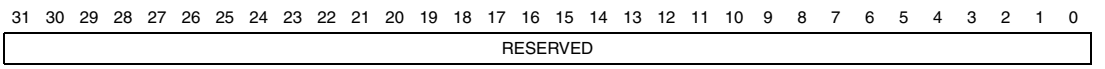
1: When MODE[9:8]=01 AND LX_DELTA_BOOT_ENABLE=1

0: For other values of MODE[9:8] and LX_DELTA_BOOT_ENABLE

[12:1] **LX_DH_PERIPH_ADDR**: ST230 DELPHI peripheral address.

[0] **LX_DH_RST_N_CTRL**: ST230 DELPHI reset active low control bit.
0: Reset of ST230 driven by hardware reset 1: Reset of ST230 fixed to active state

SYSTEM_CONFIG30 Reserved



Address: *SystemConfigBaseAddress* + 0x0178

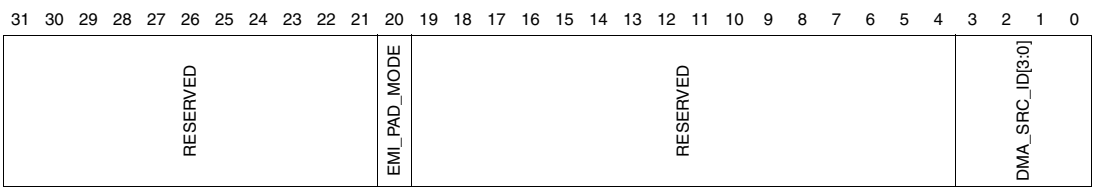
Type: RW

Reset: 0x0000

Description: Reserved

[31:0] **RESERVED**

SYSTEM_CONFIG31 EMI config register



Address: *SystemConfigBaseAddress* + 0x017C

Type: RW

Reset: 0x0000

Description: EMI config

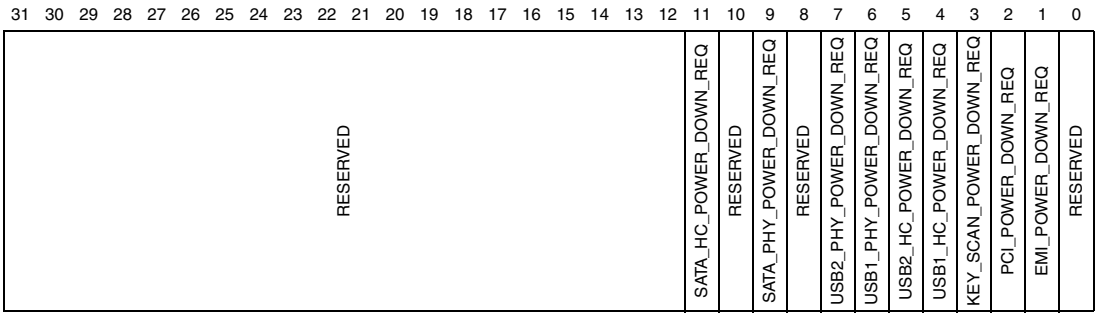
[31:21] **RESERVED**

[20] **EMI_PAD_MODE:**
0: TTL bi-directional mode (EMI) 1: PCI mode

[19:4] **RESERVED**

[3:0] **DMA_SRC_ID[3:0]:** DMA source ID.

SYSTEM_CONFIG32 Power down config register



Address: *SystemConfigBaseAddress* + 0x0180

Type: RW

Reset: 0x0B35

Description: Power down config

[31:12] **RESERVED**

[11] **SATA_HC_POWER_DOWN_REQ:**
1: SATA host power down 0: SATA host power up

[10] **RESERVED**

[9] **SATA_PHY_POWER_DOWN_REQ:**
1: Power down request for SATA PHY module

[8] **RESERVED**

[7] **USB2_PHY_POWER_DOWN_REQ:**
1: USB2 phy is in power down 0: USB2 phy is power up

[6] **USB1_PHY_POWER_DOWN_REQ:**
1: USB1 phy is in power down 0: USB1 phy is power up

[5] **USB2_HC_POWER_DOWN_REQ:**
1: Power down request for USB2 HC module

[4] **USB1_HC_POWER_DOWN_REQ:**
1: Power down request for USB1 HC module

[3] **KEY_SCAN_POWER_DOWN_REQ:**
1: Power down request for Key scanner module

[2] **PCI_POWER_DOWN_REQ:**
1: Power down request for PCI module is active

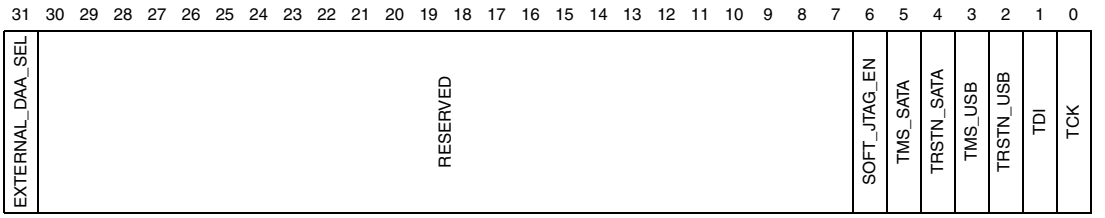
[1] **EMI_POWER_DOWN_REQ**:
1: Power down request for EMI module is active

[0] **RESERVED**

Note: 1 Due to the reset value of bit 0, 2 ,4,5,9, and 11 the PCI and USB PHY's and SATA HC+PHY are switched off by default.

2 USB PHY's power down are active low.

SYSTEM_CONFIG33 SOFT_JTAG register (USB) config register



Address: *SystemConfigBaseAddress* + 0x0184

Type: RW

Reset: 0x00000000

Description: SOFT_JTAG register (USB) config

[31] **EXTERNAL_DAA_SEL**

[30:7] **RESERVED**

[6] **SOFT_JTAG_EN:** High level means that USB2.0 or SATA TAP is managed by SOFT_JTAG register; Low level means JTAG is through PAD.

[5] **TMS_SATA:** TEST mode select for SATA TAP only

[4] **TRSTN_SATA:** Asynchronous reset for SATA TAP only.

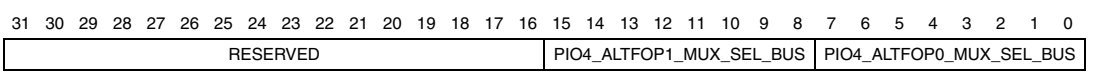
[3] **TMS_USB:** Test mode select USB2.0 TAP only.

[2] **TRSTN_USB:** Asynchronous reset USB2.0 TAP only.

[1] **TDI:** Test data input for the USB2.0 TAP or SATA TAP.

[0] **TCK:** Test clock for the USB2.0 TAP or SATA TAP.

SYSTEM_CONFIG34 Alternate function PIO output control for PIO 4



Address: *SystemConfigBaseAddress* + 0x0188

Type: RW

Reset: 0x00000000

Description: PIO4 alternate function output config

[31:16] **RESERVED**

[15:8] **PIO4_ALTFOP1_MUX_SEL_BUS**

[7:0] **PIO4_ALTFOP0_MUX_SEL_BUS**

Note: Alternate 1 : PIO4_ALTFOPj_MUX_SEL_BUS(n) = 00 [(j = 0,1); (n = 0,1,2,3,4,5,6,7)]

Alternate 2 : PIO4_ALTFOPj_MUX_SEL_BUS(n) = 01 [(j = 0,1); (n = 0,1,2,3,4,5,6,7)]

Alternate 3 : PIO4_ALTFOPj_MUX_SEL_BUS(n) = 10 [(j = 0,1); (n = 0,1,2,3,4,5,6,7)]

Alternate 4 : PIO4_ALTFOPj_MUX_SEL_BUS(n) = 11 [(j = 0,1); (n = 0,1,2,3,4,5,6,7)]

SYSTEM_CONFIG35 Alternate function PIO output control for PIO 5

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PIO5_ALTFOP1_MUX_SEL_BUS								PIO5_ALTFOP0_MUX_SEL_BUS							

Address: *SystemConfigBaseAddress* + 0x018C

Type: RW

Reset: 0x0000

Description: PIO5 alternate function output config

[31:16] **RESERVED**

[15:8] **PIO5_ALTFOP1_MUX_SEL_BUS**

[7:0] **PIO5_ALTFOP0_MUX_SEL_BUS**

Alternate 1 : PIO5_ALTFOPj_MUX_SEL_BUS(n) = 00 [(j = 0,1); (n = 0,1,2,3,4,5,6,7)]

Alternate 2 : PIO5_ALTFOPj_MUX_SEL_BUS(n) = 01 [(j = 0,1); (n = 0,1,2,3,4,5,6,7)]

Alternate 3 : PIO5_ALTFOPj_MUX_SEL_BUS(n) = 10 [(j = 0,1); (n = 0,1,2,3,4,5,6,7)]

Alternate 4 : PIO5_ALTFOPj_MUX_SEL_BUS(n) = 11 [(j = 0,1); (n = 0,1,2,3,4,5,6,7)]

SYSTEM_CONFIG36 Alternate Function PIO Output Control for PIO 6

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PIO6_ALTFOP1_MUX_SEL_BUS								PIO6_ALTFOP0_MUX_SEL_BUS							

Address: *SystemConfigBaseAddress* + 0x0190

Type: RW

Reset: 0x0000

Description: PIO6 alternate function output config

[31:16] **RESERVED**

[15:8] **PIO6_ALTFOP1_MUX_SEL_BUS**

[7:0] **PIO6_ALTFOP0_MUX_SEL_BUS**

Note:

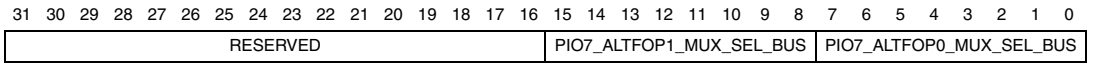
Alternate 1 : PIO6_ALTFOPj_MUX_SEL_BUS(n) = 00 [(j = 0,1); (n = 0,1,2,3,4,5,6,7)]

Alternate 2 : PIO6_ALTFOPj_MUX_SEL_BUS(n) = 01 [(j = 0,1); (n = 0,1,2,3,4,5,6,7)]

Alternate 3 : PIO6_ALTFOPj_MUX_SEL_BUS(n) = 10 [(j = 0,1); (n = 0,1,2,3,4,5,6,7)]

Alternate 4 : PIO6_ALTFOPj_MUX_SEL_BUS(n) = 11 [(j = 0,1); (n = 0,1,2,3,4,5,6,7)]

SYSTEM_CONFIG37 Alternate function PIO output control for PIO 7



Address: *SystemConfigBaseAddress* + 0x0194

Type: RW

Reset: 0x00000000

Description: PIO7 alternate function output config

[31:16] **RESERVED**

[15:8] **PIO7_ALTFOP1_MUX_SEL_BUS**

[7:0] **PIO7_ALTFOP0_MUX_SEL_BUS**

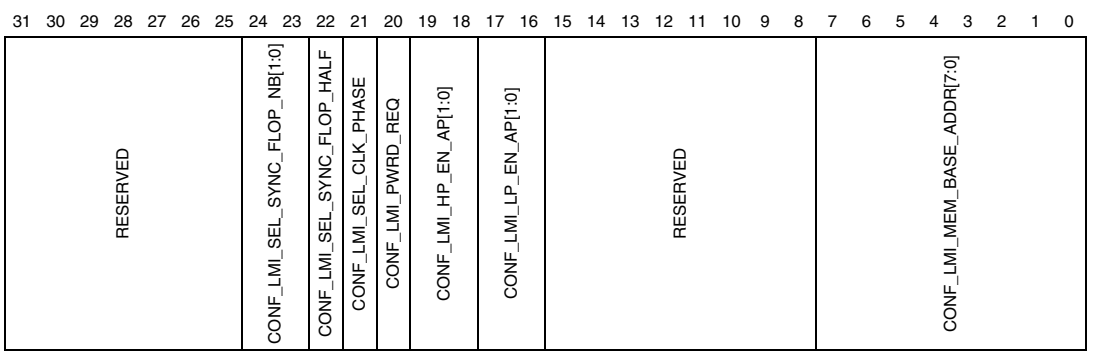
Alternate 1 : PIO7_ALTFOPj_MUX_SEL_BUS(n) = 00 [(j = 0,1); (n = 0,1,2,3,4,5,6,7)]

Alternate 2 : PIO7_ALTFOPj_MUX_SEL_BUS(n) = 01 [(j = 0,1); (n = 0,1,2,3,4,5,6,7)]

Alternate 3 : PIO7_ALTFOPj_MUX_SEL_BUS(n) = 10 [(j = 0,1); (n = 0,1,2,3,4,5,6,7)]

Alternate 4 : PIO7_ALTFOPj_MUX_SEL_BUS(n) = 11 [(j = 0,1); (n = 0,1,2,3,4,5,6,7)]

SYSTEM_CONFIG38 LMI / LMI padlogic config register



Address: *SystemConfigBaseAddress* + 0x0198

Type: RW

Reset: 0x0000000C

Description: LMI / LMI padlogic config

[31:25] **RESERVED**

[24:23] **CONF_LMI_SEL_SYNC_FLOP_NB[1:0]:** Selection of the number of flops used in the synchronizer to prevent metastability.

00: two flops are used

01: three flops are used

10 : four flops are used

11: one flop is used; For test/characterization only

[22] **CONF_LMI_SEL_SYNC_FLOP_HALF:** Selection of the clk_m clock or clk_m180 used for the first resync. flop used to prevent metastability :
0: both rising and falling edges of clk_m are used
1: only rising edge of clk_m is used

[21] **CONF_LMI_SEL_CLK_PHASE:** Selection of the clock edges used in FIFO control:
0: both rising and falling edges of clk_m are used
1: only rising edges of clk_m is used

[20] **CONF_LMI_PWRD_REQ:** LMI power down request.

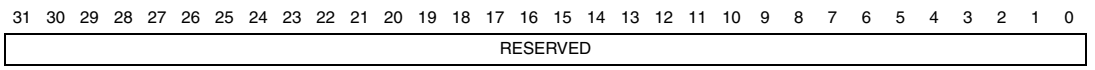
[19:18] **CONF_LMI_HP_EN_AP[1:0]:** Enables read with autoprecharge on lmi0 high priority port.

[17:16] **CONF_LMI_LP_EN_AP[1:0]:** Enables read with autoprecharge on lmi0 low priority port.

[15:8] **RESERVED**

[7:0] **CONF_LMI_MEM_BASE_ADDR[7:0]:** LMI memory base address.
29-bit LMI base address : 0x0C
32-bit LMI base address : 0x40

SYSTEM_CONFIG39 Reserved



Address: *SystemConfigBaseAddress* + 0x019C

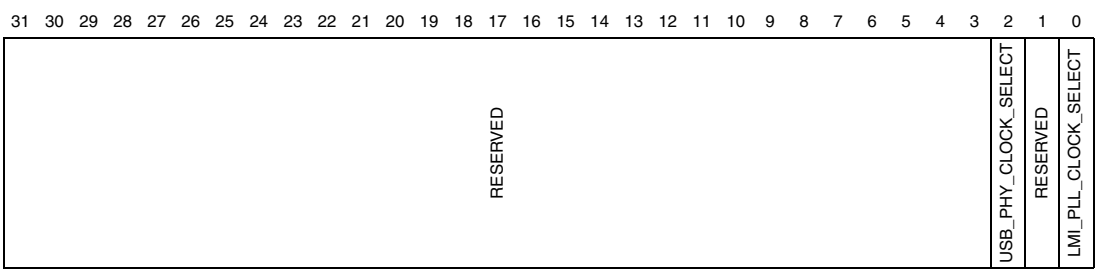
Type: RW

Reset: 0x0000

Description: Reserved

[31:0] **RESERVED**

SYSTEM_CONFIG40 Clock select config register



Address: *SystemConfigBaseAddress* + 0x01A0

Type: RW

Reset: 0x00000004

Description: Clock select config

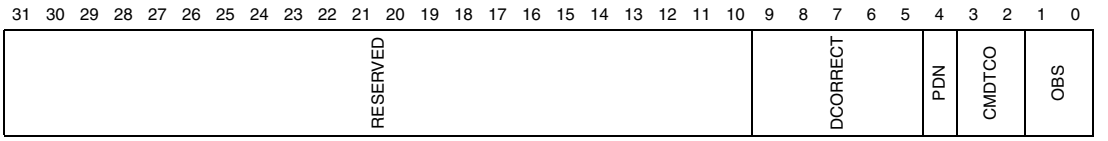
[31:3] **RESERVED**

[2] **USB_PHY_CLOCK_SELECT:** Select clock for USB PHY.
0: Clock from SATA OSC 1: Clock from alternate pad

[1] **RESERVED**

[0] **LMI_PLL_CLOCK_SELECT:** Select clock for LMI Pll imput.
0: Clock from alternate pad 1: Clock from SATA OSC

SYSTEM_CONFIG41 Thermal sensor config register



Address: *SystemConfigBaseAddress* + 0x01A4

Type: RW

Reset: 0x00000008

Description: Thermal sensor config

[31:10] **RESERVED**

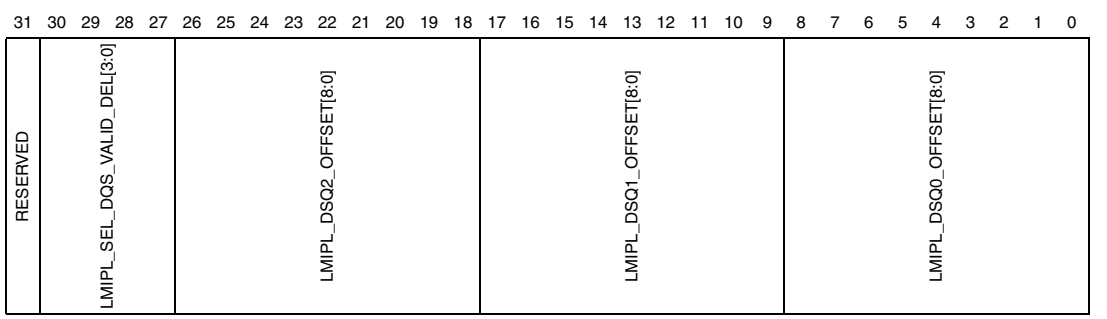
[9:5] **DCORRECT:** Digital code to correct systematic offset by addition to the digital output.

[4] **PDN:** Power Down
0: Power down mode 1: Normal mode; asynchronous

[3:2] **CMDTCO:** Reserved to debug. To be fixed to 10 in application.

[1:0] **OBS:** Reserved to debug. To be fixed to 00 in application.

SYSTEM_CONFIG42 LMI / LMI padlogic config register



Address: *SystemConfigBaseAddress* + 0x01A8

Type: RW

Reset: 0x0000

Description: LMI padlogic config register

[31] **RESERVED**

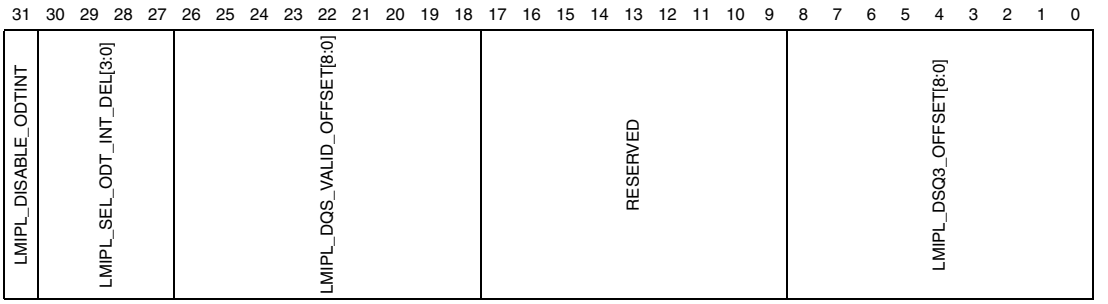
[30:27] **LMIPL_SEL_DQS_VALID_DEL[3:0]:** 'dqs_valid' timing options (T/4 resolution).

[26:18] **LMIPL_DSQ2_OFFSET[8:0]:** Offset command for DQS[2] PDL.

[17:9] **LMIPL_DSQ1_OFFSET[8:0]:** Offset command for DQS[1] PDL.

[8:0] **LMIPL_DSQ0_OFFSET[8:0]:** Offset command for DQS[0] PDL.

SYSTEM_CONFIG43 LMI / LMI Padlogic config register



Address: *SystemConfigBaseAddress* + 0x01AC

Type: RW

Reset: 0x0000

Description: LMI / LMI Padlogic config

[31] **LMIPL_DISABLE_ODTINT:** Disables Internal ODT function (as in DDR1 mode).

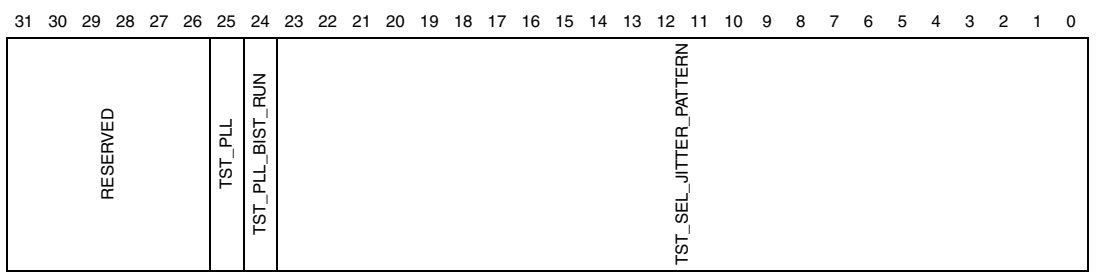
[30:27] **LMIPL_SEL_ODT_INT_DEL[3:0]:** Internal odt timing options (T/4 resolution).

[26:18] **LMIPL_DQS_VALID_OFFSET[8:0]:** Offset command for 'dqs_en_del' PDL.

[17:9] **RESERVED**

[8:0] **LMIPL_DSQ3_OFFSET[8:0]:** Offset command for DQS[3] PDL.

SYSTEM_CONFIG44 ClockgenD Jitter estimator



Address: *SystemConfigBaseAddress* + 0x01B0

Type: RW

Reset: 0x00000000

Description: ClockGen D Jitter estimator config

[31:26] **RESERVED**

[25] **TST_PLL**

[24] **TST_PLL_BIST_RUN**

[23:0] **TST_SEL_JITTER_PATTERN**

SYSTEM_CONFIG45 Reserved

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED

Address: *SystemConfigBaseAddress* + 0x01B4

Type: RW

Reset: 0x00000000

Description: Reserved

[31:0] **RESERVED**

SYSTEM_CONFIG46 Alternate function PIO output control for PIO 8

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PIO8_ALTFOP1_MUX_SEL_BUS								PIO8_ALTFOP0_MUX_SEL_BUS							

Address: *SystemConfigBaseAddress* + 0x01B8

Type: RW

Reset: 0x0000

Description: PIO8 alternate function output config

[31:16] **RESERVED**

[15:8] **PIO8_ALTFOP1_MUX_SEL_BUS**

[7:0] **PIO8_ALTFOP0_MUX_SEL_BUS**

Note:

Alternate 1 : PIO8_ALTFOPj_MUX_SEL_BUS(n) = 00 [(j = 0,1); (n = 0,1,2,3,4,5,6,7)]

Alternate 2 : PIO8_ALTFOPj_MUX_SEL_BUS(n) = 01 [(j = 0,1); (n = 0,1,2,3,4,5,6,7)]

Alternate 3 : PIO8_ALTFOPj_MUX_SEL_BUS(n) = 1x [(j = 0,1); (n = 0,1,2,3,4,5,6,7)]

SYSTEM_CONFIG47 Alternate function PIO output control for PIO 9

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PIO9_ALTFOP1_MUX_SEL_BUS								PIO9_ALTFOP0_MUX_SEL_BUS							

Address: *SystemConfigBaseAddress* + 0x01BC

Type: RW

Reset: 0x0000

Description: PIO9 alternate function output config

[31:16] **RESERVED**

[15:8] **PIO9_ALTFOP1_MUX_SEL_BUS**

[7:0] **PIO9_ALTFOP0_MUX_SEL_BUS**

Note:

Alternate 1 : PIO9_ALTFOPj_MUX_SEL_BUS(n) = 00 [(j = 0,1); (n = 0,1,2,3,4,5,6,7)]

Alternate 2 : PIO9_ALTFOPj_MUX_SEL_BUS(n) = 01 [(j = 0,1); (n = 0,1,2,3,4,5,6,7)]

Alternate 3 : PIO9_ALTFOPj_MUX_SEL_BUS(n) = 1x [(j = 0,1); (n = 0,1,2,3,4,5,6,7)]

SYSTEM_CONFIG48 Alternate function PIO output control for PIO 12

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PIO12_ALTFOP2_MUX_SEL_BUS								PIO12_ALTFOP1_MUX_SEL_BUS								PIO12_ALTFOP0_MUX_SEL_BUS							

Address: *SystemConfigBaseAddress* + 0x01C0

Type: RW

Reset: 0x0000

Description: PIO12 alternate function output config

[31: 24] **RESERVED**

[23 : 16] **PIO12_ALTFOP2_MUX_SEL_BUS**

[15 : 8] **PIO12_ALTFOP1_MUX_SEL_BUS**

[7 : 0] **PIO12_ALTFOP0_MUX_SEL_BUS**

Note:

Alternate 1 : PIO12_ALTFOPj_MUX_SEL_BUS(n) = 000 [(j = 0,1,2); (n = 0,1,2,3,4,5,6,7)]

Alternate 2 : PIO12_ALTFOPj_MUX_SEL_BUS(n) = 001 [(j = 0,1,2); (n = 0,1,2,3,4,5,6,7)]

Alternate 3 : PIO12_ALTFOPj_MUX_SEL_BUS(n) = 010 [(j = 0,1,2); (n = 0,1,2,3,4,5,6,7)]

Alternate 4 : PIO12_ALTFOPj_MUX_SEL_BUS(n) = 011 [(j = 0,1,2); (n = 0,1,2,3,4,5,6,7)]

Alternate 5 : PIO12_ALTFOPj_MUX_SEL_BUS(n) = 1xx [(j = 0,1,2); (n = 0,1,2,3,4,5,6,7)]

SYSTEM_CONFIG49 Alternate function PIO output control for PIO 13

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PIO13_ALTFOP2_MUX_SEL_BUS								PIO13_ALTFOP1_MUX_SEL_BUS								PIO13_ALTFOP0_MUX_SEL_BUS							

Address: *SystemConfigBaseAddress* + 0x01C4

Type: RW

Reset: 0x0000

Description: PIO13 alternate function output config

[31: 24] **RESERVED**

[23 : 16] **PIO13_ALTFOP2_MUX_SEL_BUS**

[15 : 8] **PIO13_ALTFOP1_MUX_SEL_BUS**

[7 : 0] **PIO13_ALTFOP0_MUX_SEL_BUS**

Note:

Alternate 1 : PIO13_ALTFOPj_MUX_SEL_BUS(n) = 000 [(j = 0,1,2); (n = 0,1,2,3,4,5,6,7)]

Alternate 2 : PIO13_ALTFOPj_MUX_SEL_BUS(n) = 001 [(j = 0,1,2); (n = 0,1,2,3,4,5,6,7)]

Alternate 3 : PIO13_ALTFOPj_MUX_SEL_BUS(n) = 010 [(j = 0,1,2); (n = 0,1,2,3,4,5,6,7)]

Alternate 4 : PIO13_ALTFOPj_MUX_SEL_BUS(n) = 011 [(j = 0,1,2); (n = 0,1,2,3,4,5,6,7)]

Alternate 5 : PIO13_ALTFOPj_MUX_SEL_BUS(n) = 1xx [(j = 0,1,2); (n = 0,1,2,3,4,5,6,7)]

SYSTEM_CONFIG50 Alternate function PIO output control for PIO 15

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PIO15_ALTFOP1_MUX_SEL_BUS								PIO15_ALTFOP0_MUX_SEL_BUS							

Address: *SystemConfigBaseAddress* + 0x01C8

Type: RW

Reset: 0x00000400

Description: PIO15 alternate function output config

[31:16] **RESERVED**

[15:8] **PIO15_ALTFOP1_MUX_SEL_BUS**

[7:0] **PIO15_ALTFOP0_MUX_SEL_BUS**

Note:

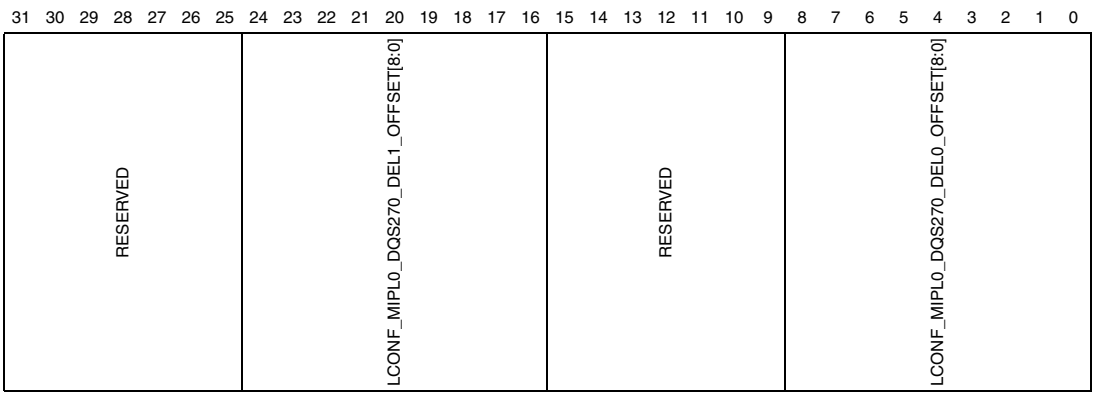
Alternate 1 : PIO15_ALTFOPj_MUX_SEL_BUS(n) = 00 [(j = 0,1); (n = 0,1,2,3,4,5,6,7)]

Alternate 2 : PIO15_ALTFOPj_MUX_SEL_BUS(n) = 01 [(j = 0,1); (n = 0,1,2,3,4,5,6,7)]

Alternate 3 : PIO15_ALTFOPj_MUX_SEL_BUS(n) = 1x [(j = 0,1); (n = 0,1,2,3,4,5,6,7)]

Note: PIO10, PIO11 and PIO14 do not require any alternate function output muxing as they are dedicated.

SYSTEM_CONFIG51 LMI / LMI Padlogic config register



Address: *SystemConfigBaseAddress* + 0x01CC

Type: RW

Reset: 0x0000

Description: LMI / LMI Padlogic config

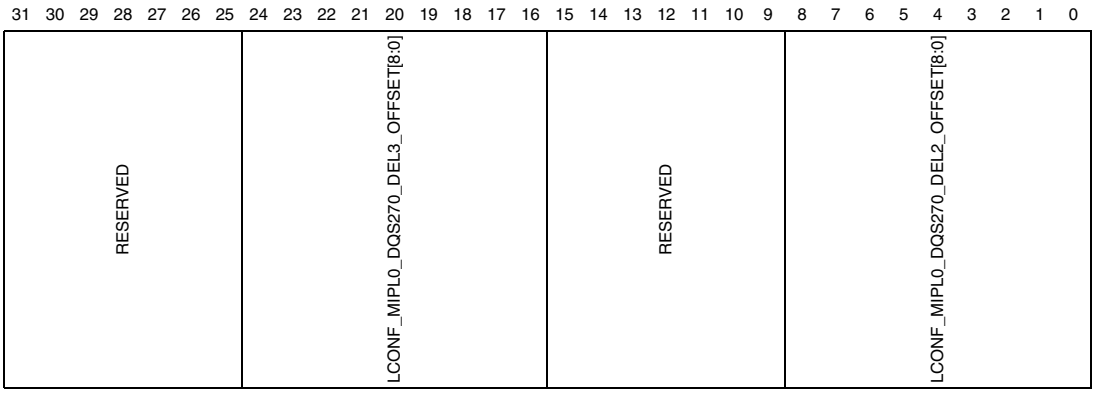
[31:25] **RESERVED**

[24:16] **LCONF_MIPL0_DQS270_DEL1_OFFSET[8:0]:** Offset command for ‘dqs270_del1’ PDL.

[15:9] **RESERVED**

[8:0] **LCONF_MIPL0_DQS270_DEL0_OFFSET[8:0]:** Offset command for ‘dqs270_del0’ PDL.

SYSTEM_CONFIG52 LMI / LMI Padlogic config register



Address: *SystemConfigBaseAddress* + 0x01D0

Type: RW

Reset: 0x0000

Description: LMI / LMI Padlogic config

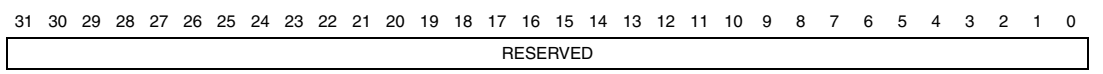
[31:25] **RESERVED**

[24:16] **LCONF_MIPL0_DQS270_DEL3_OFFSET[8:0]:** Offset command for 'dqs270_del1' PDL.

[15:9] **RESERVED**

[8:0] **LCONF_MIPL0_DQS270_DEL2_OFFSET[8:0]:** Offset command for 'dqs270_del0' PDL.

SYSTEM_CONFIG53 Reserved



Address: *SystemConfigBaseAddress* + 0x01D4

Type: RW

Reset: 0x00000000

Description: Reserved

[31:0] **RESERVED**

SYSTEM_CONFIG54 Reserved

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

Address: *SystemConfigBaseAddress* + 0x01D8

Type: RW

Reset: 0x00000000

Description: Reserved

[31:0] **RESERVED**

SYSTEM_CONFIG55 LMI / LMI Padlogic config register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		LMIPL_USERMODE_PDL_DQS_VALID	LMIPL_USERMODE_PDL_DQS270_DEL	LMIPL_USERMODE_PDL_DQS	LMIPL_USER_COMMAND_DQS_VALID									RESERVED				LMIPL_RETIME_PLI_LMI	LMIPL_PHASE_SHIFT[1:0]		LMIPL_LOWER_16BIT_ONLY	LMIPL_FILTER_SHIFT_PARAM[2:0]			LMIPL_DUMMY_PCB_TRACE	LMIPL_DOUBLE_WIDTH	LMIPL_DDR2_DIAG_CONTROL[4:0]					

Address: *SystemConfigBaseAddress* + 0x01DC

Type: RW

Reset: 0x00002000

Description: LMI / LMI Padlogic config

[31:30] **RESERVED**

[29] **LMIPL_USERMODE_PDL_DQS_VALID:**
0: T/4 DLL1 command routed to dqs_valid PDL
1: user_command_dqs_valid<8:0> routed to dqs_valid PDL

[28] **LMIPL_USERMODE_PDL_DQS270_DEL:**
0: 3T/4 (or T/2) DLL2 command routed to dqs270_del<3:0> PDLs
1: dll2_usr_cmd<8:0> routed to dqs270_del<3:0> PDLs

[27] **LMIPL_USERMODE_PDL_DQS:**
0: T/4 DLL command routed to dqs<3:0> PDLs
1: dll1_usr_cmd<8:0> routed to dqs<3:0> PDLs

[26:18] **LMIPL_USER_COMMAND_DQS_VALID:** User command for forcing delay of dqs_valid PDL(also diagnostics).

[17:14] **RESERVED**

[13] **LMIPL_RETIME_PLI_LMI:** Active high retiming stage enable for lmisys_pl.

[12:11] **LMIPL_PHASE_SHIFT[1:0] :** Shift padlogic clock in T/4 increments; needs clk_pll stopped when rst_n released.

[10] **LMIPL_LOWER_16BIT_ONLY:** 16/32-bit mode switch; High = 16-bit mode.

[9:7] **LMIPL_FILTER_SHIFT_PARAM[2:0]:** Programmable filter characteristic.

[6] **LMIPL_DUMMY_PCB_TRACE:** Active high to enable dummy PCB trace option.

[5] **LMIPL_DOUBLE_WIDTH:** Enable half speed LMI-PLI interface.

[4:0] **LMIPL_DDR2_DIAG_CONTROL[4:0]:** For future development. Tied off.

15.1.5 INTC2 registers description

INTC2_PRIORITY00 INTC2 priority 00 register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

Address: *SystemConfigBaseAddress* + 0x0300

Type: RW

Reset: 0

Description: INTC2 priority 00 register

[31:0] **RESERVED**

INTC2_PRIORITY04 INTC2 priority 04 register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

Address: *SystemConfigBaseAddress* + 0x0304

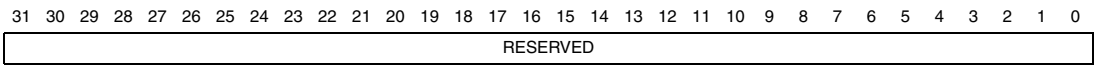
Type: RW

Reset: 0

Description: INTC2 priority 04 register

[31:0] **RESERVED**

INTC2_PRIORITY08 INTC2 priority 08 register



Address: *SystemConfigBaseAddress* + 0x0308

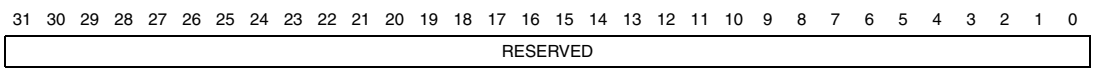
Type: RW

Reset: 0

Description: INTC2 priority 08 register

[31:0] **RESERVED**

INTC2_REQUEST00 INTC2 request 00 register



Address: *SystemConfigBaseAddress* + 0x0320

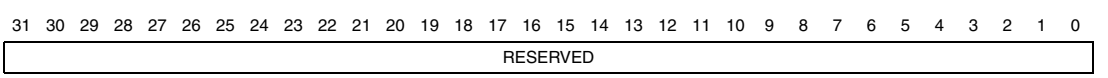
Type: RW

Reset: 0

Description: INTC2 request 00 register

[31:0] **RESERVED**

INTC2_REQUEST04 INTC2 request 04 register



Address: *SystemConfigBaseAddress* + 0x0324

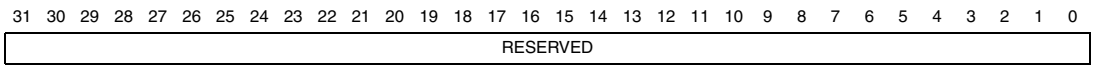
Type: RW

Reset: 0

Description: INTC2 request 04 register

[31:0] **RESERVED**

INTC2_REQUEST08 INTC2 request 08 register



Address: *SystemConfigBaseAddress* + 0x0328

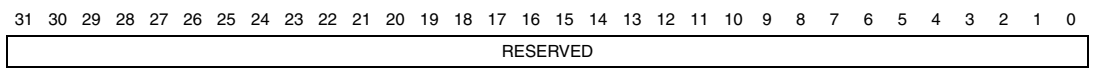
Type: RW

Reset: 0

Description: INTC2 request 08 register

[31:0] **RESERVED**

INTC2_MASK00 INTC2 mask 00 register



Address: *SystemConfigBaseAddress* + 0x0340

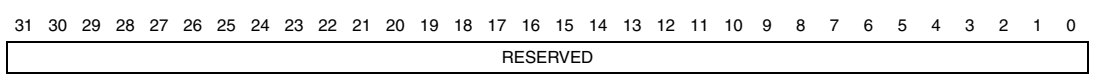
Type: RW

Reset: 0

Description: INTC2 mask 00 register

[31:0] **RESERVED**

INTC2_MASK04 INTC2 mask 04 register



Address: *SystemConfigBaseAddress* + 0x0344

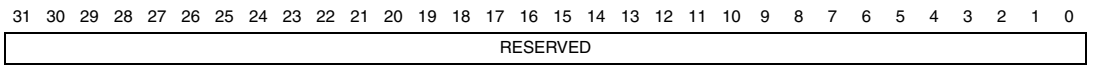
Type: RW

Reset: 0

Description: INTC2 mask 04 register

[31:0] **RESERVED**

NTC2_MASK08 INTC2 mask 08 register



Address: *SystemConfigBaseAddress* + 0x0348

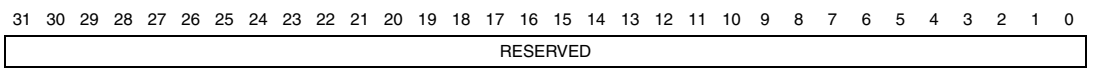
Type: RW

Reset: 0

Description: INTC2 mask 08 register

[31:0]	**RESERVED**

INTC2_MASK_CLEAR00 INTC2 mask clear 00 register



Address: *SystemConfigBaseAddress* + 0x0360

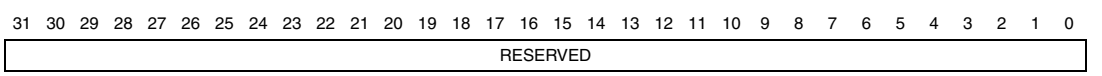
Type: RW

Reset: 0

Description: INTC2 mask clear 00 register

[31:0] **RESERVED**

INTC2_MASK_CLEAR04 INTC2 mask clear 04 register



Address: *SystemConfigBaseAddress* + 0x0364

Type: RW

Reset: 0

Description: INTC2 mask clear 04 register

[31:0] **RESERVED**

INTC2_MASK_CLEAR08 INTC2 mask clear 08 register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

Address: *SystemConfigBaseAddress* + 0x0368

Type: RW

Reset: 0

Description: INTC2 mask clear 08 register

[31:0] **RESERVED**

INTC2_MODE INTC2 mode register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

Address: *SystemConfigBaseAddress* + 0x0380

Type: RW

Reset: 0

Description: INTC2 mode register

[31:0] **RESERVED**

16 External circuitry recommendations

16.1 Power supplies

16.1.1 Decoupling recommendations

It is recommended to:

1. connect all balls of the same group (with the same names) together
2. add decoupling capacitors between each VDD and GND group, respectively:
   - VDD3V3 group and GND3V3 group
   - AVDD2V5 group and AGND2V5 group
   - VDD1V8_2V5 group and LMI_GND1V8 group
   - DVDD1V2 group and DGND1V2 group

The decoupling capacitor values must be carefully considered and fully simulated prior to the board design cycle.

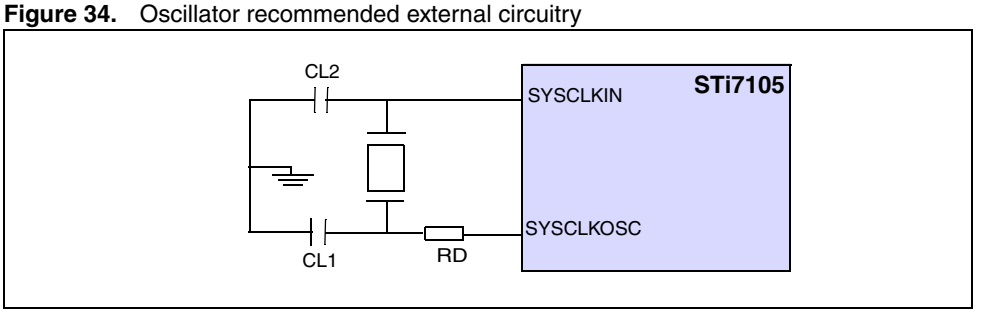
16.1.2 Power-up recommendations

There is no specific recommendation for power-up sequence.

16.2 System

The SYS oscillator recommended external circuitry is shown in *Figure 34*.

Figure 34. Oscillator recommended external circuitry



Two differential signals (VDDSENSE and GNDSENSE) are used to provide loopback information on the core supply voltage to an external voltage regulator.

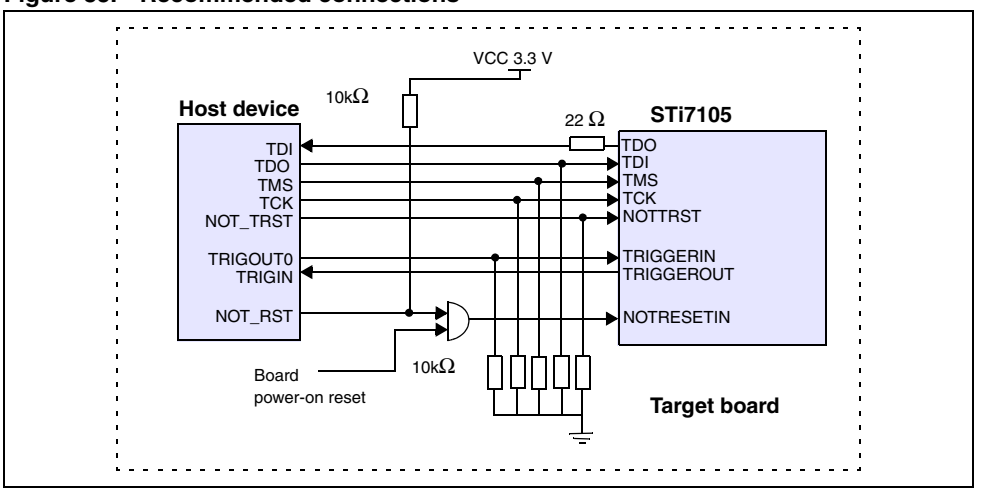
Most of the signals have internal pull-up or pull-down, and do not require an external resistor when not in use. Refer to the 'I/O value' field of the *Table 32* for details.

For the electrical specifications, please contact your local ST representative to access SATA application notes describing oscillators electrical specifications.

16.3 JTAG

The JTAG recommended connections are shown in *Figure 35.*

Figure 35. Recommended connections



Note: If there is a lot of noise on the clock line, a capacitor in the range 10 to 100 pF can be fitted between TCK and ground near the target STi7105, however, this may limit the maximum TAP clock rate.

16.4 Display analog output interface

16.4.1 Video DACs description

There are two identical sets of triple video DACs for HD and SD output. Both are triple high performance 10-bit digital to analog converters, and consist of three 10-bit DAC modules joined together. A reference circuit controlled by one external resistor sets the full-scale output for each DAC set. Each DAC is able to drive 10 mA.

The blocks are powered by 2.5 V analog and 1.2 V digital supplies, with separate analog and digital grounds.

The blocks require an external precision resistor (Rref) to provide a bandgap reference. The Rref optimum value is 7.81 kΩ +/- 1%.

The blocks' analog current sources provide a voltage output range of 1.4 V with an optimum linearity through an external precision resistor (Rload). The Rload optimum value is 140 Ω +/- 1%.

The exact calculation for the voltage output range is:

Vout = Din * 0.0625 * [(Rext-Mass_quiet)/Rref]*Rload

where:

- Din—Code value in decimal
- Rext-Mass_quiet—VbandGap(=1.2214 V)
- Rref—reference resistor; optimum value is 7.81 kΩ
- Rload—load resistor (=140 Ω)

16.4.2 Power mode

Each DAC has two power modes—normal mode and high-impedance mode—that are controlled by the SYSTEM_CONFIG3 system configuration register.

The high impedance mode allows fast recovery from the low power consumption state, and can be used to reduce power during line and frame refresh.

Each DAC takes 100 ns time interval to switch from normal mode to high-impedance mode, and vice-versa.

16.4.3 Video DACs output-stage adaptation and amplification

Please contact your local ST representative to access application notes describing video DACs output stage adaptation and amplification.

16.5 HDMI interface

Please contact your local ST representative to access application notes describing HDMI PCB design guidelines.

16.6 Audio digital interface

Please contact your local ST representative to access application notes describing audio digital interface.

16.7 Audio analog interface

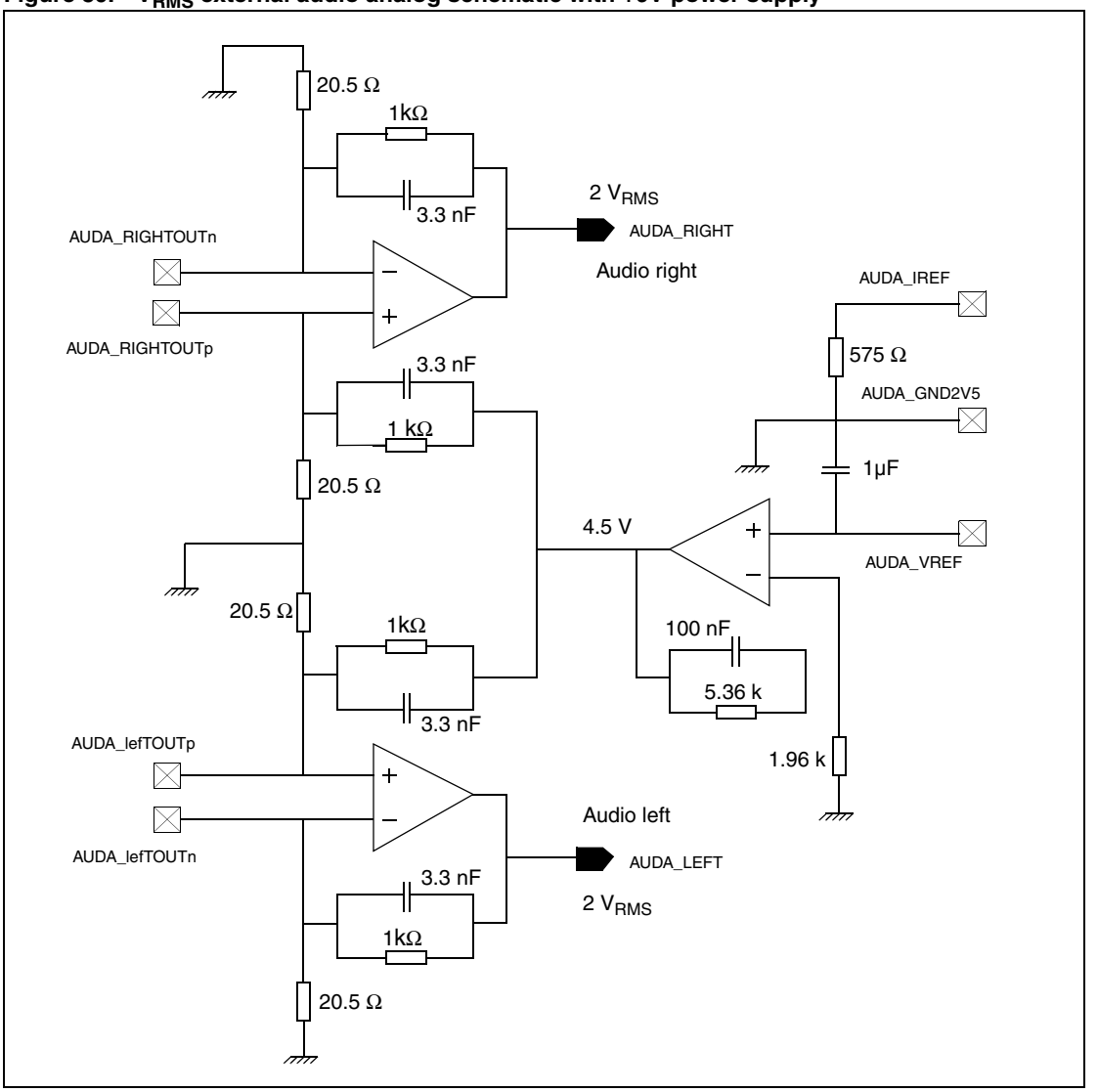
The audio DAC provides differential current source outputs for each channel. The use of a differential mode interface circuit is recommended to achieve the best signal to noise ratio performance. A single-ended mode interface circuit can be used, by grounding pins AUDA_LEFTOUTN and AUDA_RIGHTOUTN, but this is not recommended as the resulting signal to noise ratio is less than 90 dB.

An external 1% resistor R_{REF} should be connected between AUDA_IREF and AUDA_GND2V5. A typical value for R_{REF} is 575 Ω, to get proper band gap functionality.

An external 10 µF capacitance should be connected between AUDA_VREF and AUDA_GND2V5.

Figure 36 describes an audio output stage to deliver a 2 VRMS signal.

Figure 36. V_{RMS} external audio analog schematic with +9V power supply



16.8 Programmable inputs/outputs

There is no specific external circuitry recommendations for this interface.

16.9 External memory interface (EMI)

The EMI is designed to be connected to up to:

- 1 PCI/33 MHz slot + 4 TTL/100 MHz/40 pF slots
- 1 PCI/66 MHz slot + 3 TTL/100 MHz/30 pF slots

16.10 Local memory interface

Apart from the direct signal connections between the LMI and the DDR memories (refer to *Figure 37* and *Figure 38* for details), several extra connections are required.

An external resistor of 121 KΩ +/- 1% is to be connected between LMI_COMP_REF AND LMI_COMP_GND to enable the internal pad drive compensation mechanism.

The two voltage reference signals LMIVREF[0]/LMIVREF[1] are to be connected together to the memories' VREF signals and to a resistor pair whose pedestal is connected to VDD1V8_2V5 and LMI_GND1V8.

The LMIDUMMY[0]/LMIDUMMY[1] signals act as a PCB track delay estimator, and have to be connected through a dummy PCB trace. If all signal lengths are equal to an ideal TL_{signal}, TL_{dummy} is also equal to this TL_{signal}. If this is not the case, the ideal TL_{dummy} length is defined by the following equation:

$$TL_{dummy} = 0.5 \times \{(TL_{LMICLK[0]} + TL_{NOTLMICLK[0]} + TL_{LMICLK[1]} + TL_{NOTLMICLK[1]}) / 4 + (TL_{LMIDQS[0]} + TL_{LMIDQSN[0]} + TL_{LMIDQS[1]} + TL_{LMIDQSN[1]} + TL_{LMIDQS[2]} + TL_{LMIDQSN[2]} + TL_{LMIDQS[3]} + TL_{LMIDQSN[3]}) / 8\}$$

For further information on LMI PCB design guidelines, please contact your local ST representative.

Figure 37. LMI: connections to a (single rank/2 x16 devices) DDR 32-bit configuration

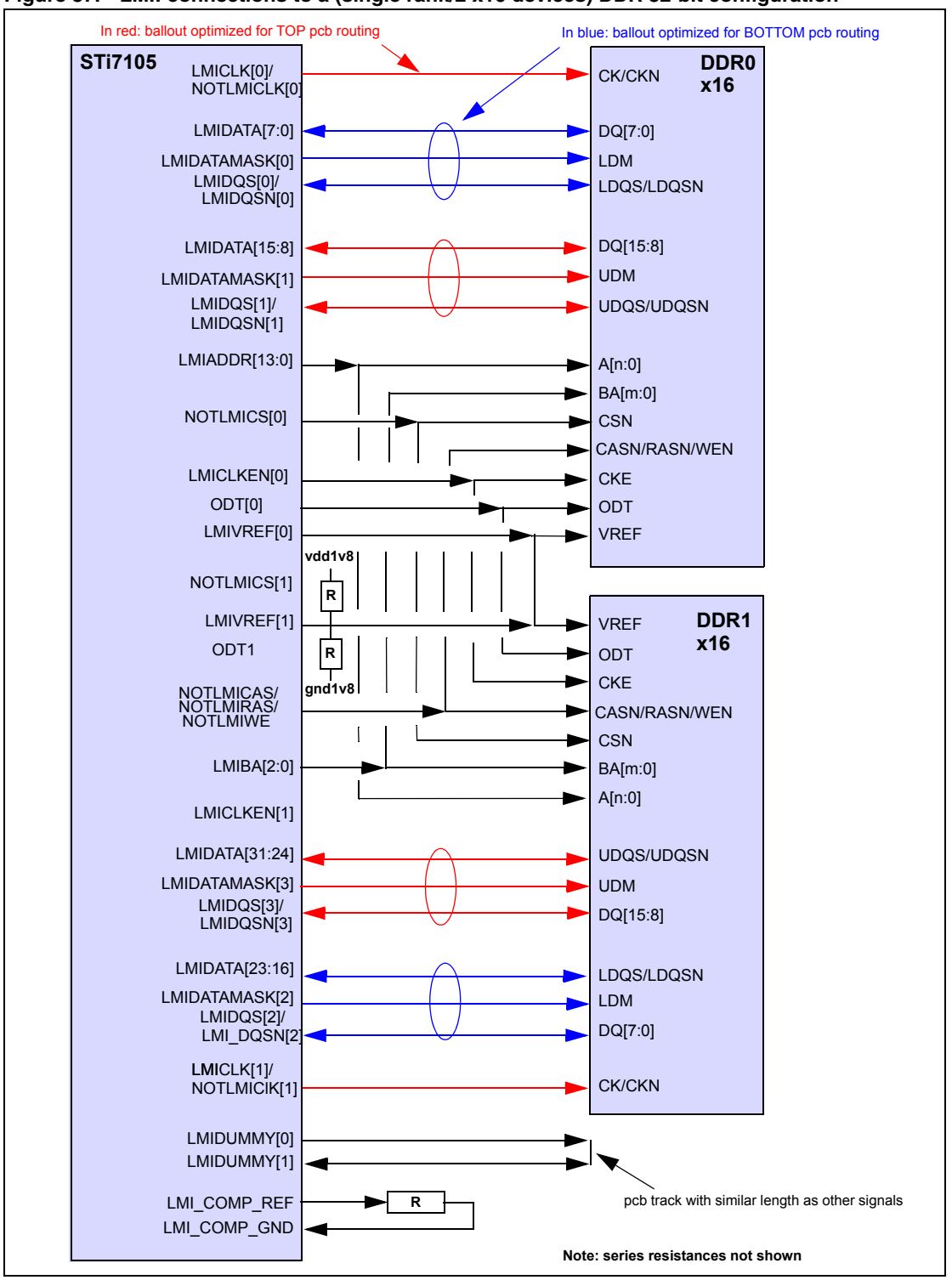
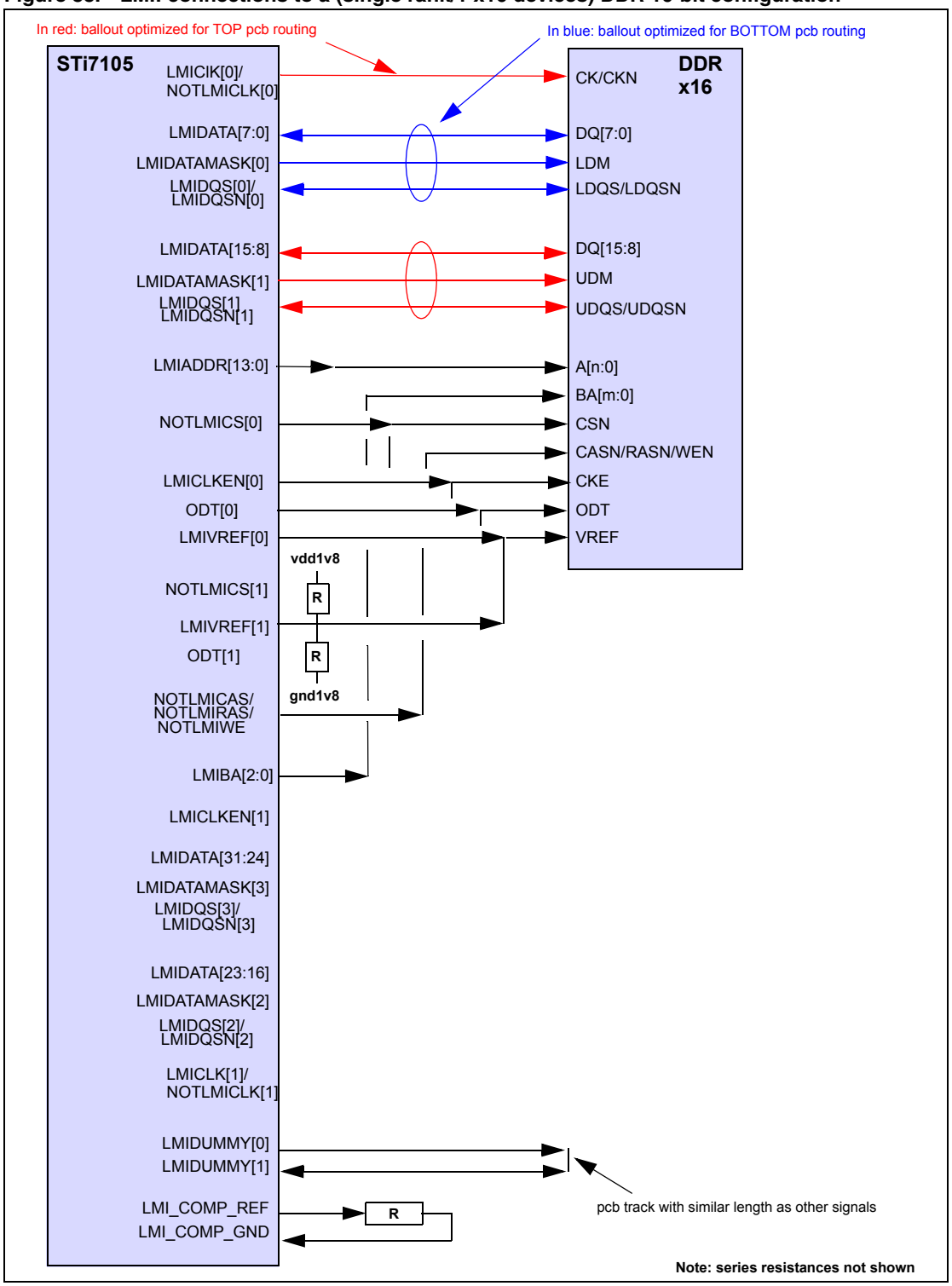


Figure 38. LMI: connections to a (single rank/1 x16 devices) DDR 16-bit configuration



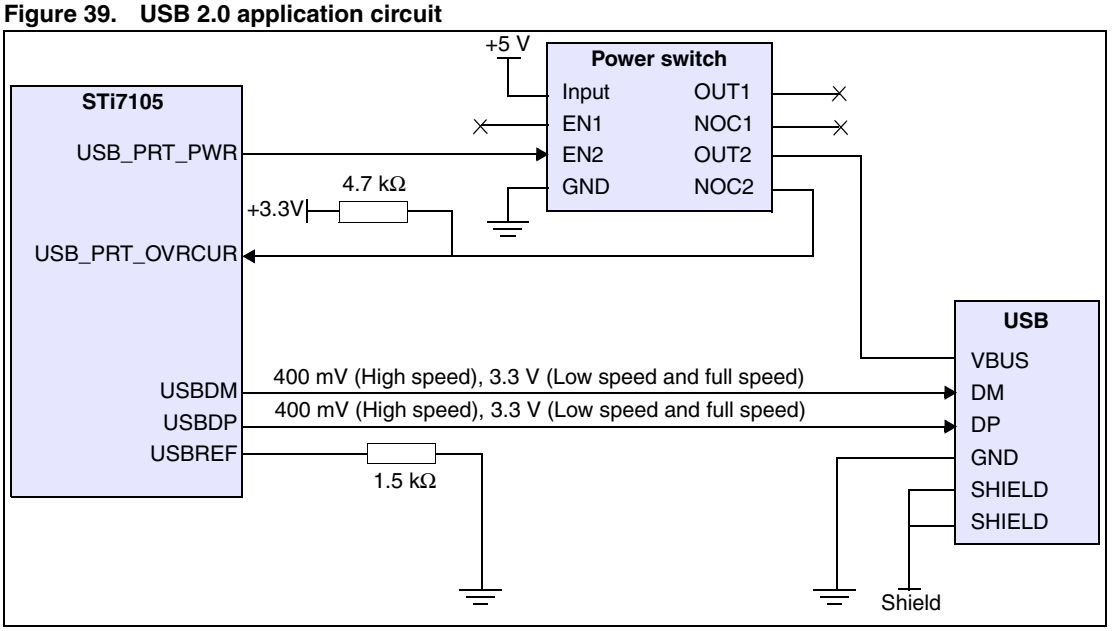
16.11 Ethernet interface

Some mode pins are mapped on some Ethernet interface signals. Pull-up or pull-down resistors have to be added depending upon the chosen reset configuration. Refer to *Mode pins* for details.

16.12 USB interface

The USB external recommended connections are shown in *Figure 39.*

Figure 39. USB 2.0 application circuit



For PCB design guidelines, refer to the 'USB PCB design guidelines' specific document (ADCS #7991152). For access to this ST internal document please contact your local ST representative.

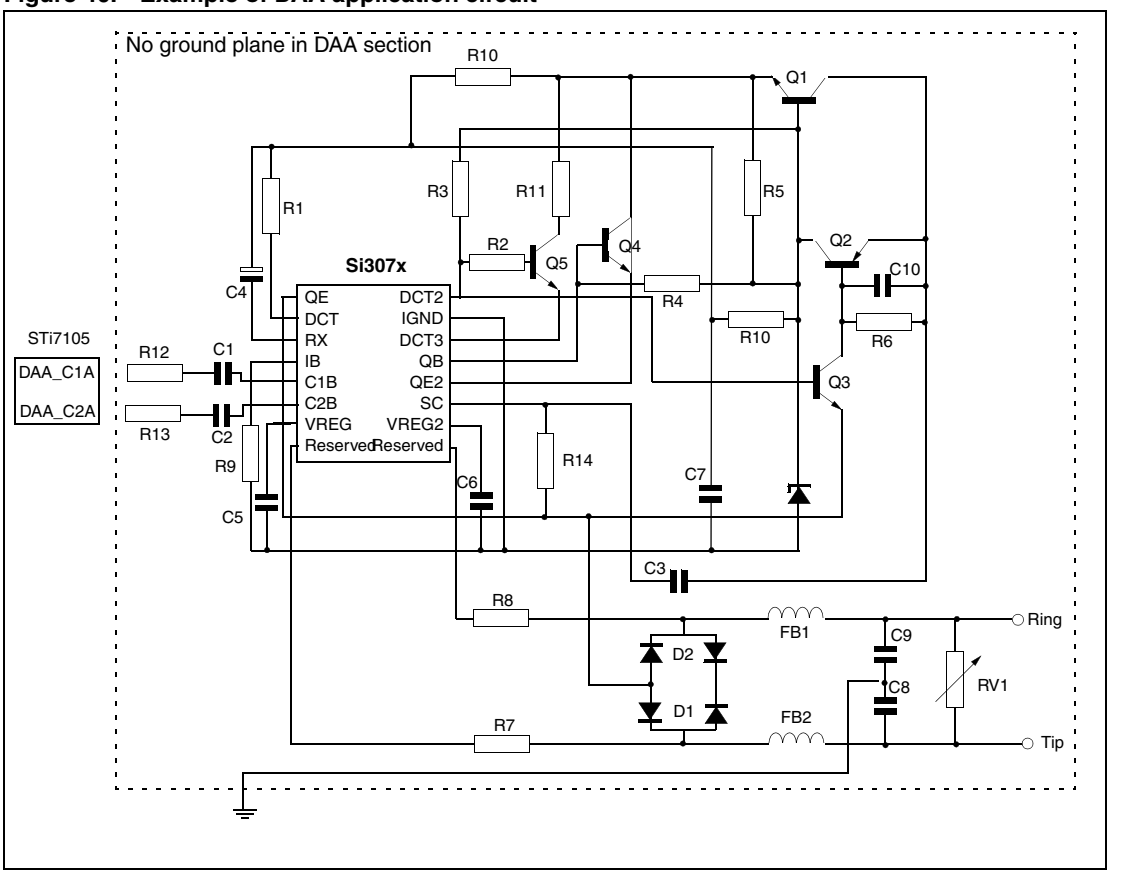
16.13 SATA

Please contact your local ST representative to access application notes describing SATA PCB design guidelines.

16.14 Peripherals

The DAA external recommended connections are shown in *Figure 40.*

Figure 40. Example of DAA application circuit



Note: The ISO-Link capacitors C1 and C2, (33 pF) should be as close to the line-side device as possible.They should also be as close to the embedded system-side DAA module as possible and no further than 6 inches away.

17 Electrical specifications

Values in this chapter are provisional and may change after characterization

17.1 Absolute maximum ratings

Table 69. Absolute maximum ratings

Symbol	Parameter	Min	Typ	Max	Units
$VDD3V3_{max}$	Digital 3.3 V maximum voltage	-0.6		3.9	V
$VDD2V5_{max}$	Analog 2.5 V maximum voltage	-0.5		3.3	V
$VDD1V8\_2V5_{max}$	Digital 1.8 V maximum voltage	-0.5		3.3	V
$VDD1V2_{max}$	Digital 1.2 V maximum voltage	-0.5		1.4	V
V_{ESD_HBM}	Electrostatic discharge voltage (HBM modem)			1000	V
V_{ESD_CDM}	Electrostatic discharge voltage (CDM modem)			250	V
T_{STG}	Storage temperature	- 60		150	°C

17.2 Operating conditions

Table 70. Operating conditions

Symbol	Parameter	Min	Typ	Max	Units
VDD3V3	Digital 3.3 V operating voltage	3.0	3.3	3.6	V
VDD2V5	Analog 2.5 V operating voltage	2.25	2.5	2.75	V
VDD1V8	Digital 1.8 V operating voltage	1.7	1.8	1.9	V
VDD1V2	Digital 1.2 V operating voltage	1.14	1.2	1.26	V
I_{3V3}	Digital 3.3 V current			TBD	A
I_{2V5}	Analog 2.5 V current			TBD	A
I_{1V8}	Digital 1.8 V current			TBD	A
I_{1V2}	Digital 1.2 core current			TBD	A
C_L	Load capacitance per pin			100	pF
TA	Operating ambient temperature	0		70	°C
PD_{FP}	Full-Power consumption		TBD		W
PD_{LP}	Low-Power consumption		TBD		W
R_{THJAa}	Junction-to-ambient thermal resistance		TBD		°C/W

17.3 Audio DAC

17.3.1 Electrical characteristics

Absolute maximum ratings

The *Table 71* describes absolute maximum ratings for audio DAC.

Table 71. Absolute maximum ratings

Symbol	Parameter	Min	Typ	Max	Units
ANA1_VDD2V5	Analog power supply			4	V
AUDA_DVDD1V2	Digital power supply			2	V
T_{stg}	Storage temperature	- 60		150	°C

Operating conditions

The *Table 72* describes operating conditions for audio DAC.

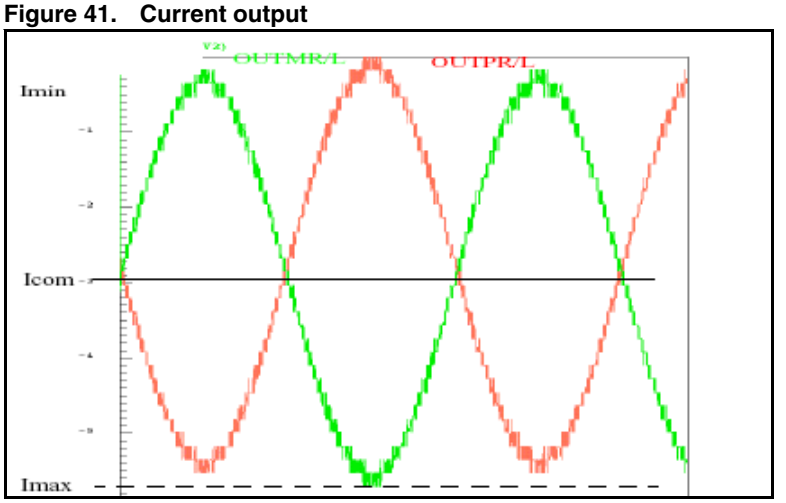
Table 72. Operating conditions

Symbol	Parameter	Min	Typ	Max	Units
AUDA_DVDD1V2	Digital power supply	1	1.2	1.4	V
T_{oper}	Operating Temperature	-40	27	125	°C
I_D	Digital Supply Current		2		mA
ANA1_VDD2V5	Analog power supply	2.25	2.5	2.75	V
I_A	2.5 Analog Supply Current			TBD	mA
I_{PD}	Supply Current in Power Down Mode			10	µA

Output current

In case of no input data, the DAC provides a common mode output current (Icom), as shown in *Figure 41*.

Figure 41. Current output



The output current is fixed by internal reference current or can be fixed externally.

Table 73. Audio DAC output current

Parameter	Imin	Icom	Imax	Unit
Output current	0	$\frac{0.8}{Rext}$	$\frac{1.613}{Rext}$	A

17.4 Triple HD video DACs

The *Table 74* describes absolute maximum ratings for triple video DACs.

Table 74. Absolute maximum rating

Symbol	Parameter	Min	Typ	Max	Unit
VIDA1_VCCA1/ VIDA2_VCCA1	Analog power supply for current matrix & bias blocks 2.75 V			2.75	V
VIDA1_VCCA2/ VIDA2_VCCA2	Analog power supply for level shifters			2.75	V
T_{stg}	Storage temperature	-60		150	degrees

The *Table 75* describes operating conditions for triple video DACs.

Table 75. Operating conditions

Symbol	Parameter	Min	Typ	Max	Unit
VIDA1_VCCA1/ VIDA2_VCCA1	Analog power supply for current matrix & bias blocks 2.75 V	2.25	2.5	2.75	V
VIDA1_VCCA2/ VIDA2_VCCA2	Analog power supply for level shifters	2.25	2.5	2.75	V
T_{op}	Operating junction temperature	-40	25	125	degrees

The *Table 76* describes static electrical performance of TriDAC.

Table 76. Static electrical performance Rref = 7.81 kΩ; Rload = 140 Ω

Symbol	Parameter	Min	Typ	Max	Unit
Nb	DAC resolution		10		bits
PonAnalog	Power consumption analog/ active(1)		110	133	mW
PonDigital	Power consumption digital/ active(2)		3.0	3.9	mW
PHZ	Power consumption / HZ mode(3)		12.7	15.6	mW
POFF	Power consumption / Off mode(4)		2.5	102.0	µW
INL	Integral non linearity		+/- 0.4	+/- 1.0	LSB
DNL	Differential non linearity		+/- 0.2	+/- 0.5	LSB
DAC to DAC matching	DAC to DAC matching(5)		+/- 0.5	+/- 3	
Compliance	Output compliance 0 V < Vout < 1.4 V			0.03	LSB
Iout Rref = 7.81 kΩ	DAC output current	0 (code min)		10.0 (code max)	mA
Full scale Gain Error	Full scale gain error (6)			+/7	%
Rout	DAC output resistance @ DC	100			kΩ

1. Typical consumption at 2.5 V/1.2 V supply; and Max. at 2.75 V/1.32 V supply
2. Typical consumption at 2.5 V/1.2 V supply; and Max. at 2.75 V/1.32 V supply
3. Independent of dk activity
4. Transistor off-stage leakage only
5. Under ideal supply conditions
6. This value includes the 1% variation of reference resistor (Rref) and 1% of load resistor (Rload)

The *Table 77* describes dynamic electrical performance of video DACs.

Table 77. Dynamic electrical performance Rref = 7.81 kΩ; Rload = 140 Ω

Symbol	Parameter	Min	Typ	Max	Unit
F_CLK	Clock speed			160	MHz
BDW	Output 3 dB bandwidth @ Fclk=160 MHz	DC to 30			MHz
THD	Total harmonic distortion Fin =4 MHz, F_clk =160 MHz	-44.27	-46.47		dB
SFDR	Spurious free dynamic range Fin=4 MHz, Fclk=160 MHz Output full scale	-44.88	-47.79		dB
PSRR (dVout/dVvcca)	Power supply rejection ratio @ 1 Hz (full scale)	-50	-55		dB
	Power supply rejection ratio @1 MHz(full scale)	-22	-25		dB

17.5 DAA electrical characteristics

The *Table 78* describes absolute maximum ratings for DAA.

Table 78. Absolute maximum ratings

Symbol	Parameter	Conditions	Min	Max	Units
V_1	Input voltage on IO pin with respect to GND		–	3.6	V

17.6 DDR electrical characteristics

17.6.1 Limiting values

The *Table 79* describes the limiting values for DDR.

Table 79. DDR limiting values

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VDDE	1.8 V pad supply voltage	DDR II mode	1.7	1.8	1.9	V
		DDR I mode	2.25	2.5	2.75	V
VREF(DC)	Input reference voltage connected on REFSSTL (corresponding to supply VDDE)	(1)	(0.49 * VDDE)	(0.5 * VDDE)	(0.51 * VDDE)	V
VTT	Termination voltage	(2)	VREF - 0.04	VREF	VREF +0.04	V

1. The value of VREF is expected to be (0.49-0.51) x VDDE of the transmitting device and VREF is expected to track variations in VDDE.
2. Peak to peak AC noise on VREF may not exceed +/-2% of VREF(DC). VTT of transmitting device must track VREF of receiving device.

17.6.2 Output buffer DC characteristics

Table 80. Output buffer DC characteristics

Symbol	Mode of I/O buffer	Parameter	Conditions	Min	Typ	Max	Unit
Iol	DDRI	Output minimum DC current sink	Vol = 0.36V(1)	16.2	-	-	mA
Ioh		Output minimum DC current source	Voh = VDDE - 0.36V	-16.2	-	-	mA
Iol	DDRII	Output minimum DC current sink	Vol = 0.28V	13.4	-	-	mA
Ioh		Output minimum DC current source	Voh = VDDE - 0.28V(2)	-13.4	-	-	mA

1. SSTL2 classII specification with ZOUTPROGA set low.
2. SSTL_18 specification with ZOUTPROGA set low.

17.6.3 Input buffer DC specifications

Table 81. Input buffer DC characteristics for DDRI

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VREF	Voltage reference	-	0.49 * VDDE = 1.1	0.5 * VDDE = 1.25	0.51 * VDDE = 1.4	V
Vil (DC)	DC input logic low	-	-0.3	-	VREF - 0.15	V
Vih (DC)	DC input logic high	-	VREF + 0.15	-	VDDE + 0.3	V
Vil (AC)	AC input logic low	-	-	-	VREF - 0.31	V
Vih(AC)	AC input logic high	-	VREF + 0.31	-	-	V

Table 82. Input buffer DC characteristics for DDRII

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VREF	Voltage reference	-	0.49 * VDDE = 0.833	0.5 * VDDE = 0.9	0.51 * VDDE = 0.969	V
Vil (DC)	DC input logic low	-	-0.3	-	VREF - 0.125	V
Vih (DC)	DC input logic high	-	VREF + 0.125	-	VDDE + 0.3	V
VTT (DC)	Termination voltage		VREF - 0.04	-	VREF + 0.04	V
Vil (AC)	AC input logic low	-	-	-	VREF - 0.25	V
Vih(AC)	AC input logic high	-	VREF + 0.25	-	-	V

17.7 SATA PHY electrical characteristics

17.7.1 Absolute maximum ratings

Table 83 describes the absolute maximum ratings.

Table 83. Absolute maximum ratings

Symbol	Parameter	Min	Max	Unit
SATAVDDR	Supply Voltage (1.2 V nom.)		1.35	V
SATAVDDT				
SATAVDD_PLL				
SATAVDD2_PLL	Supply Voltage (2.5 V)		2.75	V
V_{INL}	Input low level	TBD		V
V_{INH1}	Input high level (oscillator and pll 2v5 inputs)		2.75	V
V_{INH2}	Input high level (all other inputs)		1.35	V

17.7.2 Operating conditions

Table 84 describes the operating conditions.

Table 84. Operating conditions

Symbol	Parameter	Min	Typ	Max	Units
SATAVDDR	1v2 supply voltage range	1.08	1.20	1.32	V
SATAVDDT					
SATAVDD_PLL					
SATAVDD2_PLL	Supply Voltage (2.5 V)	2.25	2.50	2.75	V
	Supply ripple (1MHz to 3GHz)			50	mV(pk-pk)
TJ	Operating junction temperature	-40		125	°C

17.7.3 General electrical specifications

Table 85 describes the general electrical specifications.

Table 85. General electrical specifications

Symbol	Parameter	Min	Typ	Max	Unit
Rref	External reference resistor (from refers pin to the vdd_pll pin)	-1%	475	+1%	Ohm
$TUI_{SATASAS1}$	Unit Interval for SATA/SAS gen1 (1.5 Gbps)		666.67		ps
F_{SSC}	Spread spectrum modulation frequency	30		33	kHz
SSC_{TOL}	Spread spectrum modulation deviation	-5000		+0	ppm
$V_{cm,ac}$	AC coupled common mode voltage	0		2000	mV
Z_{diff}	Nominal differential impedance		100		
$t_{settle,cm}$	Common mode transient settle time (SATA gen1 only)			10	ns
V_{trans}	Sequencing transient voltage	-2.0		2.0	V

17.8 External memory interface (EMI)

The EMI pads are TTL/PCI dual-mode. TTL electrical specifications are shown in *Table 86* and PCI electrical specifications in *Table 87*.

Table 86. TTL-mode 3V3 EMI pads DC specifications

Symbol	Parameter	Min	Typical	Max	Units	Notes
V_{IH}	Input logic 1 voltage	2.0		VDD3V3 + 0.5	V	
V_{IL}	Input logic 0 voltage	-0.5		0.8	V	
V_{OH}	Output logic 1 voltage	VDD3V3 - 0.2			V	(1)
V_{OL}	Output logic 0 voltage			0.2	V	(2)
R_{PU}	Equivalent pull-up resistance		50		kΩ	
R_{PD}	Equivalent pull-down resistance		50		kΩ	
I_{IN}	Input leakage current (input pin)			4	µA	(3)
C_{IN}	Input capacitance			10	pF	

1. I_{OUT} = -8 mA
2. I_{OUT} = 8 mA
3. $0 \leq V_{in} \leq$VDD3V3

Table 87. PCI-mode 3V3 EMI pads DC specifications

Symbol	Parameter	Min	Typical	Max	Units	Notes
V_{IH}	Input logic 1 voltage	0.5*VDD3V3		VDD3V3 + 0.5	V	
V_{IL}	Input logic 0 voltage	-0.5		0.3*VDD3V3	V	
V_{OH}	Output logic 1 voltage	0.9*VDD3V3			V	(1)
V_{OL}	Output logic 0 voltage			0.1*VDD3V3	V	(2)
R_{PU}	Equivalent pull-up resistance		50		kΩ	
R_{PD}	Equivalent pull-down resistance		50		kΩ	
I_{IN}	Input leakage current (input pin)			4	µA	(3)
C_{IN}	Input capacitance			10	pF	

1. I_{OUT} = -0.5 mA
2. I_{OUT} = 1.5 mA
3. $0 \leq V_{in} \leq$VDD3V3

17.9 USB

Table 88 describes the operating conditions of USB.

Table 88. USB operating conditions

Symbol	Parameter	Min	Typ	Max	Unit
USB1_VDD3V3	Analog supply voltage	3.0	3.3	3.6	V
USB2_VDD3V3					
USB_VDD1V2	Digital supply voltage	1.1	1.2	1.3	V
USB_VDD2V5	Analog supply voltage	2.3	2.5	2.7	V
V_{LFS-cm}	Low and full speed mode input common mode level	800		2500	mV
V_{HS-cm}	High speed mode input common mode level	-50	200	500	mV
$V_{chirp-cm}$	Chirp mode input common mode level	-50		600	mV
V_{diff}	Differential input signal amplitude	100	400	1100	mV

18 Timing interfaces

18.1 Digital audio interface

18.1.1 Digital PCM reader input interface

Digital PCM Player timing waveform

The *Figure 42* shows the timing waveforms of the digital Audio PCM input to the PCM reader.

Figure 42. Digital PCM audio input timing waveforms

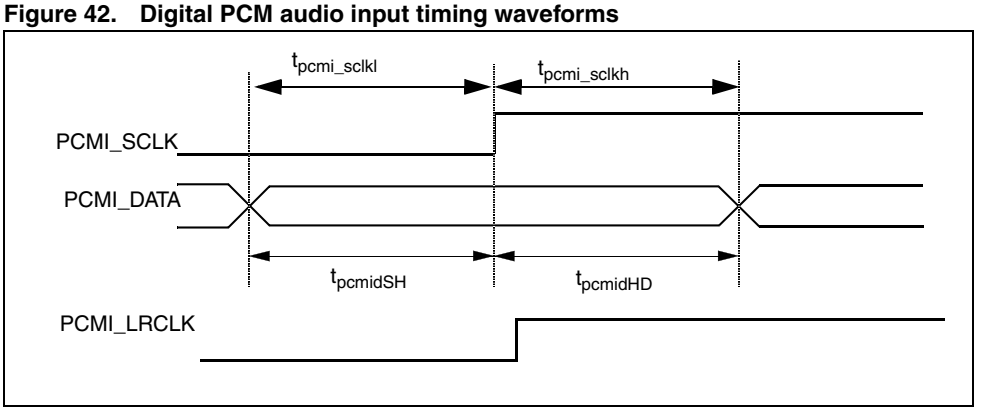


Table 89. Digital audio PCM input timing parameters

Symbol	Parameter	Min	Max	Units
f_{pcmi_sclk}	PCMI_SCLK max frequency	--	32	MHz
t_{pcmi_sclkl}	PCMI_SCLK low pulse	12	--	ns
t_{pcmi_sclkh}	PCMI_SCLK high pulse	12	--	ns
$t_{pcmidSH}$	PCMI_data setup time to PCMI_SCLK rising edge	5	--	ns
$t_{pcmidHD}$	PCMI_data hold time from PCMI_SCLK rising edge	5	--	ns

18.2 Digital PCM player output interface

18.2.1 PCM player output timing waveform

The *Figure 43* shows the timing waveforms of the PCM player output interface.

Figure 43. PCM player timing output waveforms

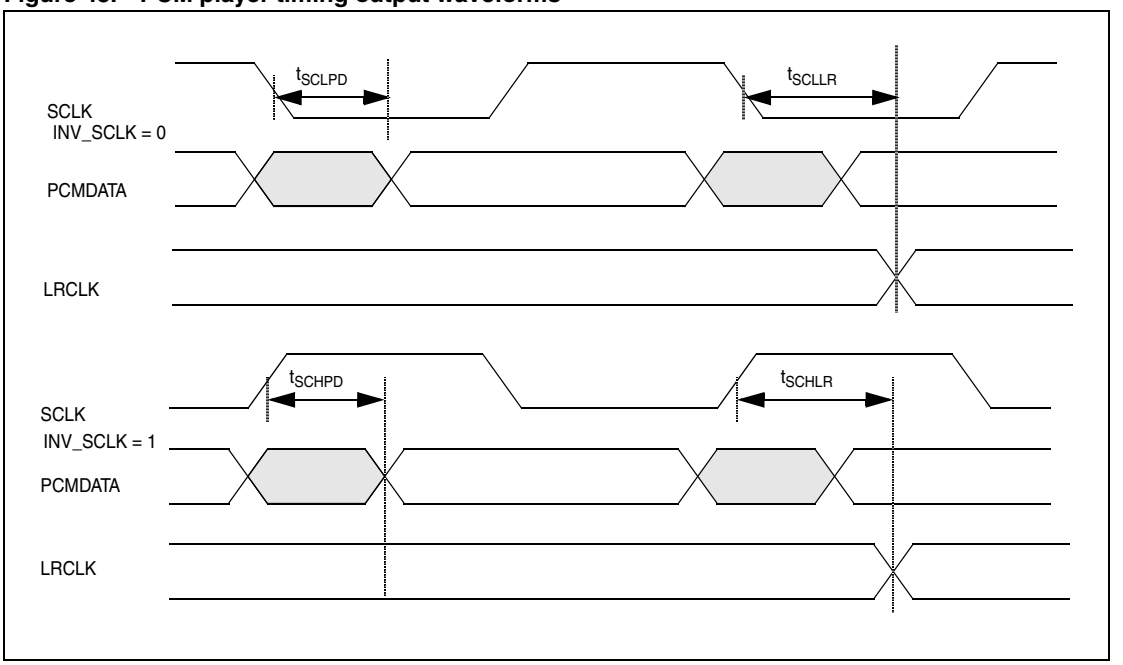


Table 90. PCM player output timing parameters

Symbol	Parameter	Min	Max	Units
t_{SCLPD}	SCLK low to PCMDATA valid	--	10	ns
t_{SCLLR}	SCLK low to LRCLK	--	10	ns
t_{SCHPD}	SCLK high to PCMDATA valid	--	50	ns
t_{SCHLR}	SCLK high to LRCLK	--	50	ns
PCM_{jitter}	Dedicated PCMCLK pin jitter			

18.3 Transport stream input AC specification

18.3.1 Parallel transport stream input interface

The *Figure 44* shows the timing waveforms of parallel transport stream input interface.

Figure 44. Parallel transport stream input timing waveform

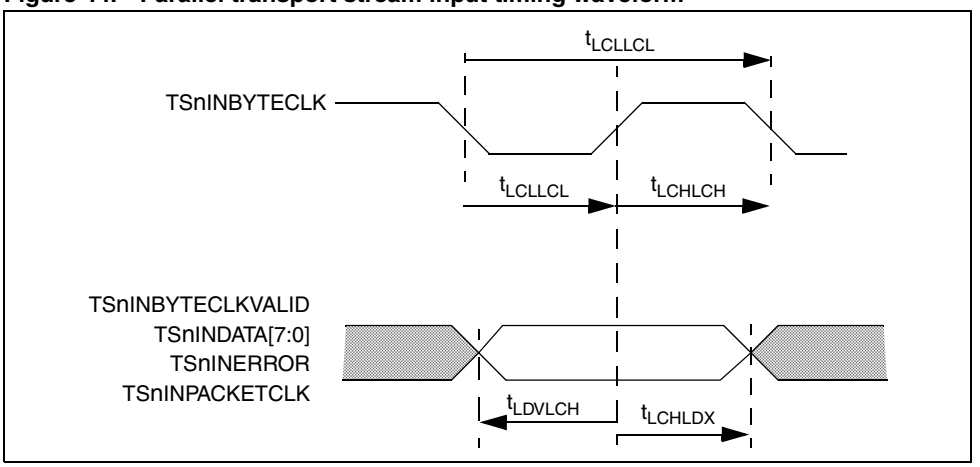


Table 91. Parallel transport stream input timing parameter

Symbol	Parameter	Min	Mon	Max	Units
t_{LCLLCL}	TSnINBYTECLK period	37	--	--	ns
t_{LCHLCH}	TSnINBYTECLK pulse width high	10	--	--	ns
t_{LCLLCL}	TSnINBYTECLK pulse width low	10	--	--	ns
t_{LDVLCH}	TSnIN signals valid to TSnINBYTECLK high	4	--	--	ns
t_{LCHLDX}	TSnIN signals hold after TSnINBYTECLK high	0	--	--	ns

18.3.2 Serial transport stream input interface

The *Figure 45* shows the timing waveforms of serial transport stream input interface.

Figure 45. Serial transport stream input timing waveform

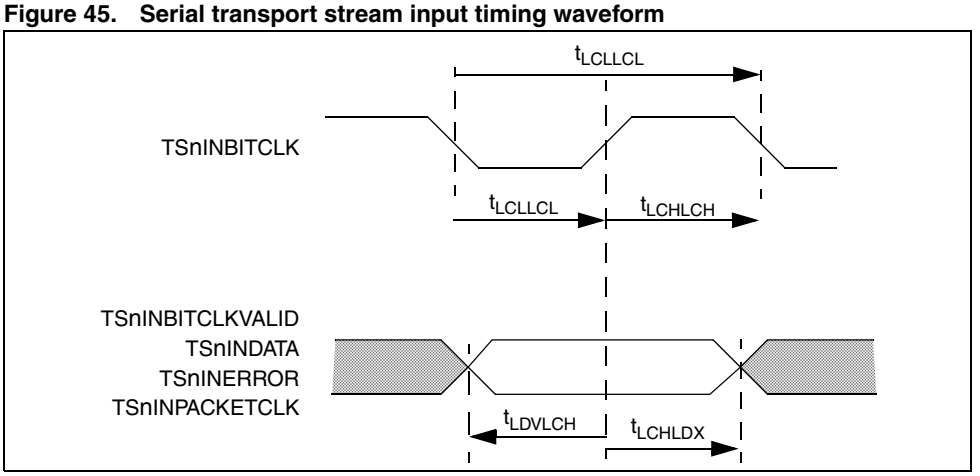


Table 92. Serial transport stream input timing parameter

Symbol	Parameter	Min	Mon	Max	Units
t_{LCLLCL}	TSnINBITCLK period	10	--	--	ns
t_{LCHLCH}	TSnINBITCLK pulse width high	3	--	--	ns
t_{LCLLCL}	TSnINBITCLK pulse width low	3	--	--	ns
t_{LDVLCH}	TSnIN signals valid to TSnINBITCLK high	3	--	--	ns
t_{LCHLDX}	TSnIN signals hold after TSnINBITCLK high	0	--	--	ns

18.4 Transport stream output AC specification

The *Figure 46* shows the timing waveforms of transport stream output interface.

Figure 46. Transport stream output timing

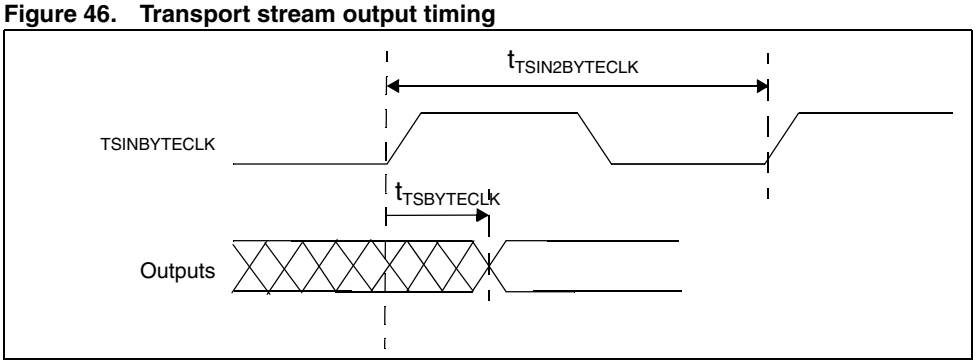


Table 93. Transport stream output port timings

Symbol	Parameter	Min	Max	Units
$t_{TSINBYTECLK}$	TSINBYTECLK clock period	10		ns
$t_{TSBYTECLK}$	Output delay to TSINBYTECLK		0	ns
t_{ACHACH}	TSnINOUTBYTECLK pulse width high	40		ns
t_{ACLLAL}	TSnINOUTBYTECLK pulse width low	40		ns

18.5 JTAG interfaces AC specification

Input clocks: TCK (rising edge)

Inputs: TDI, TMS

Figure 47. JTAG interface timing

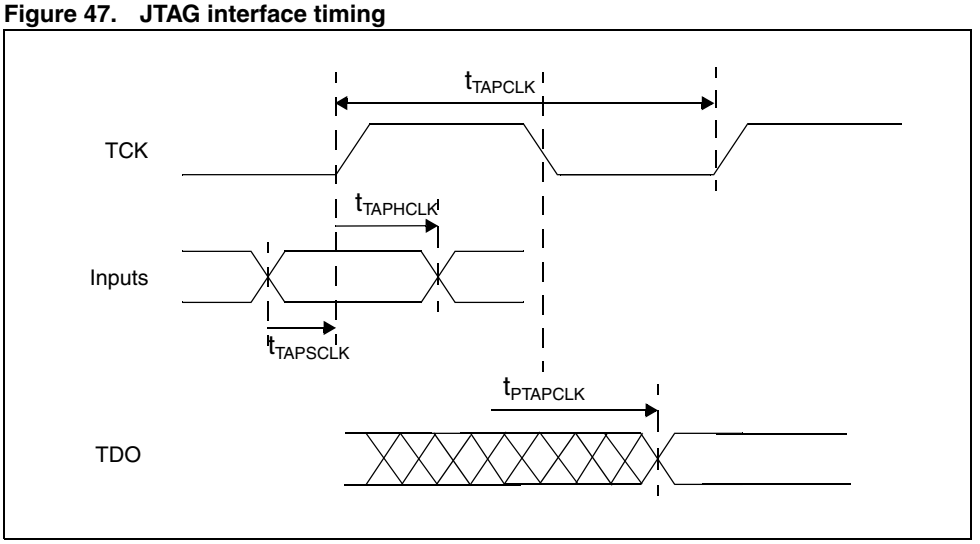


Table 94. JTAG input/output port timings

Symbol	Parameter	Min	Max	Units
Input clock	TCK period	20		ns
tTAPHCLK	Inputs setup to TCK rising edge	5		ns
tTAPSCLK	Inputs hold to TCK rising sdge	5		ns
tPTAPCLK	Output delay to TCK falling edge		15	ns

18.6 EMI timings

All of the outputs come from a multiplexer controlled by the clock. It is assumed that the EMI will be programmed so that all the outputs will be changed on the falling edge of the clock.

Following tables assume an external load of 25 pF on every EMI pad.

18.6.1 Synchronous devices

All synchronous transactions originate and terminate at flip flops within the padlogics. Outputs are generated with respect to the falling edge of the bus clock, and inputs are sampled with respect to the rising edge.

EMI-Clock: EMISFLASH

EMI-outputs: EMIADDR[*], EMIDATA[*], NOTEMICS*, NOTEMIBE, NOTEMIOE, NOTEMILBA, NOTEMIBAA, EMIRDNOTWR

EMI-inputs: EMIDATA[*], EMIREADYORWAIT

Figure 48. EMI synchronous device timing

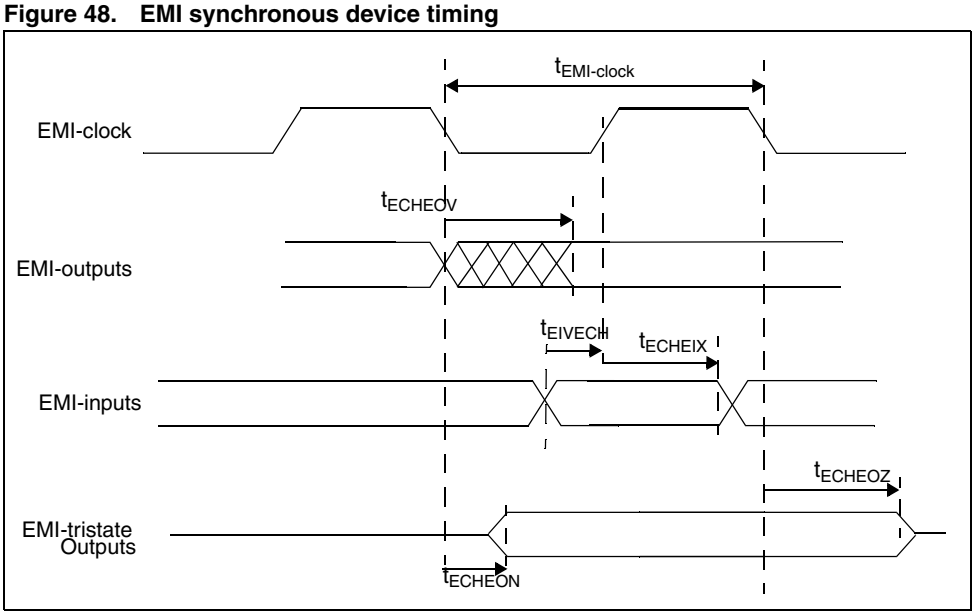


Table 95. EMI / SFLASH synchronous interface parameters

Symbol	Parameter	Min	Max	Units
Input clock	EMISFLASHCLK period	33		ns
t_{ECHEOV}	Bus clock falling edge to valid data	0	4	ns
t_{EIVECH}	Input valid to rising clock edge (input setup time)	5.5		ns
t_{ECHEIX}	Rising clock edge to input invalid (input hold time)	0		ns
t_{ECHEON}	Falling clock edge to data valid (after tristate output)	2		ns
t_{ECHEOZ}	Falling clock edge to data valid (before tri-state output)		-3	ns

These values are static offsets within a bus cycle, they should be read in conjunction with the waveforms in *external memory interface* (EMI), which are cycle accurate only.

Asynchronous memory/peripherals

The EMI strobes are programmed in terms of internal clock phases, that is to say with half cycle resolution. The clock to output delay for all outputs (address, data, strobes) are closely matched with a skew tolerance of -3 ns / +3 ns (assuming an external load of 25 pF on pads).

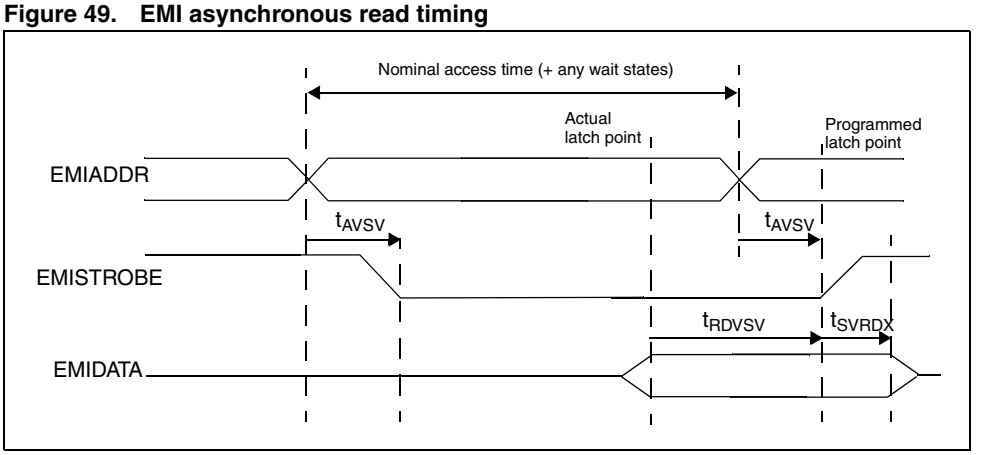
The input latch point for a read access is determined by the number of programmed EMI subsystem clock cycles for the latch point. The correction allows the latch point to be measured from the edge of an active chip select, that has been programmed to rise at the programmed read latch point.

Time between the address bus switching and a chip select or data bus output switching is n programmed phases +/- 3 ns. That is, worst case, the chip select or data is maximum of 3 ns after the address, or worst case the chip select or data is 3 ns before the address.

For a read cycle, the data is latched by the STi7105 at the programmed number of EMI subsystem clock cycles from the end of the access plus a latch point correction time, which is effectively the read setup time. The latch point correction time (read setup time) is a minimum of 5 ns + skew tolerance correction of the output signal used as a reference. This is 5 +/- 3 ns, thus the minimum read setup time relative to a strobe is 8 ns. This ensures the read hold time is always a minimum of 0 ns, guaranteed by design.

Asynchronous access - READ

Figure 49. EMI asynchronous read timing



Asynchronous access - WRITE

Figure 50. EMI asynchronous write timing

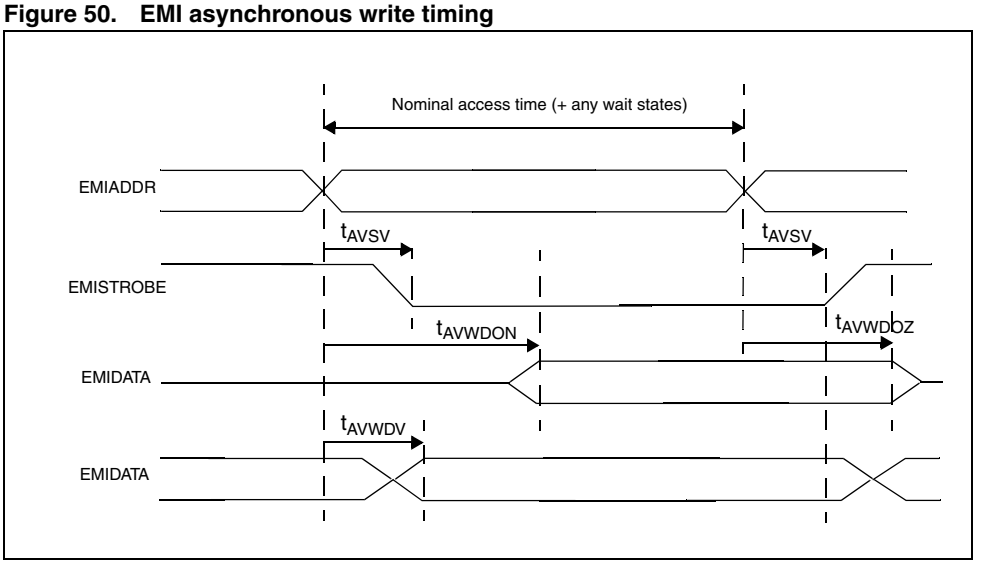


Table 96. EMI / Asynchronous memory/peripherals interface parameters

Symbol	Parameter	Min	Max	Units	Note
t_{AVSV}	Address valid to output strobe valid	-1.5	3	ns	(1)
t_{RDVSV}	Read data valid to strobe valid (read setup time)	8		ns	(2)
t_{SVRDX}	Read data hold time after strobe valid (read hold time)	0		ns	(3)
t_{AVWDON}	Address valid to write data valid (after tristate output)	3		ns	(4)
t_{AVWDOZ}	Address valid to write data valid (before tristate output)		-4.5	ns	
t_{AVWDV}	Address valid to write data valid	-2	2	ns	

1. Skew plus nominal N programmed EMI subsystem clock cycles of strobe delay.
2. Skew from nominal programmed read latch point.
3. Minimum values are guaranteed by design.
4. Skew from nominal programmed phases of data drive delay.

Table 96 assumes an external load of 25 pF on EMI pads.

18.7 LMI DDR2-SDRAM timings

The DDR2 interface is compliant to the Jedec DDR2 specs (DDR2-800 grade).

18.8 PIO output AC specification

Reference clock in this case means the last transition of any PIO signal.

Note: There are two different sets of PIO timings, one for the SSC (I^2C) outputs and one for all other PIO outputs.

Figure 51. PIO timing

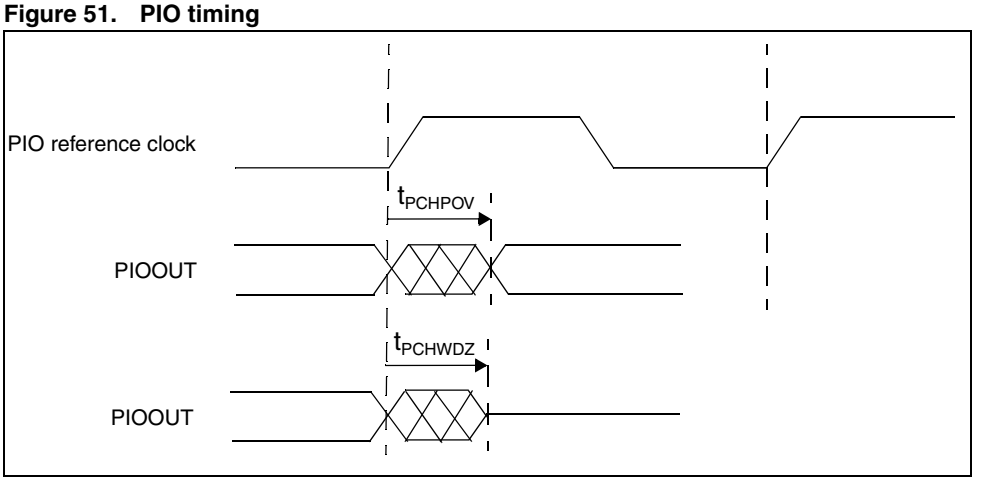


Table 97. PIO timings: SSC (I^2C bus)

Symbol	Parameter	Min	Max	Units
t_{PCHPOV}	PIO_REFCLOCK high to PIO output valid	-20.0	0.0	ns
t_{PCHWDZ}	PIO tristate after PIO_REFCLOCK high	-20.0	5.0	ns
t_{PIOr}	Output rise time	3.0	30.0	ns
t_{PIOf}	Output fall time	3.0	30.0	ns

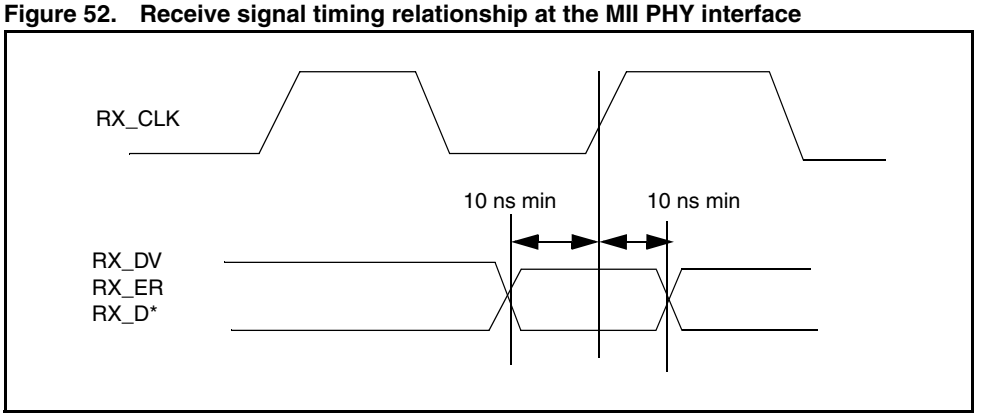
18.9 Ethernet interface

18.9.1 MII interface

MII receive interface

The *Figure 52* shows the timing waveform for the Receive MII interface.

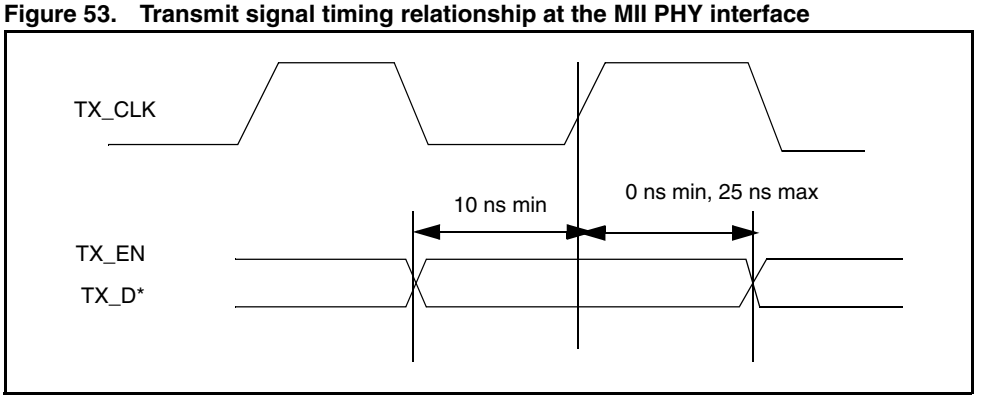
Figure 52. Receive signal timing relationship at the MII PHY interface



MII transmit interface

The *Figure 53* shows the timing waveform for the Transmit MII interface.

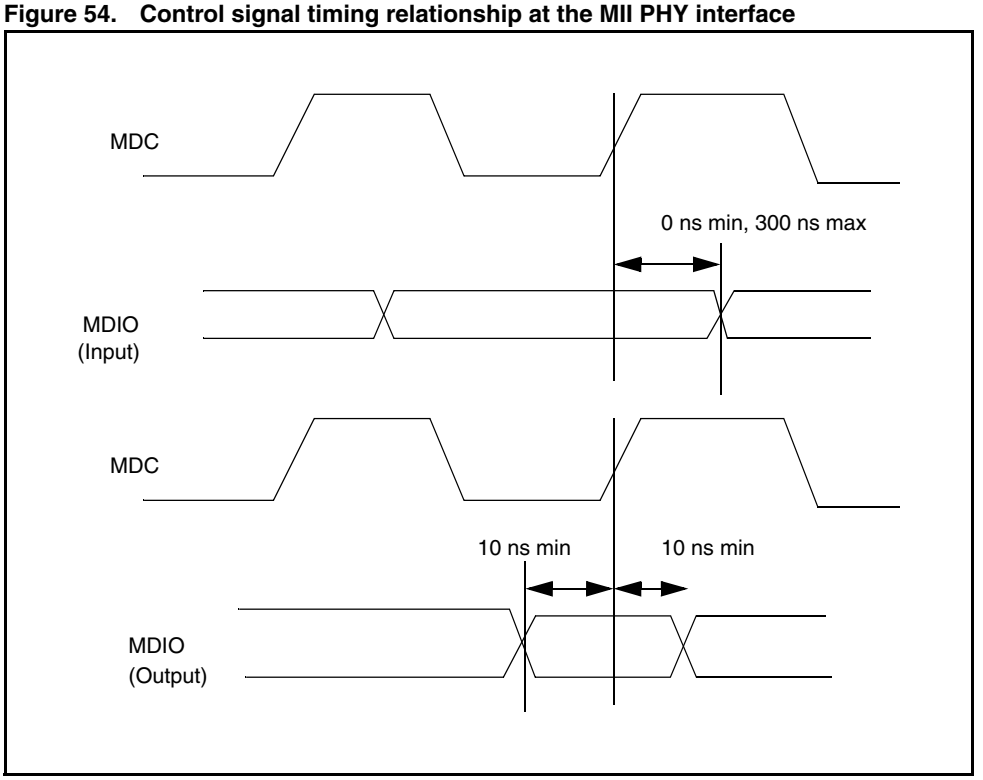
Figure 53. Transmit signal timing relationship at the MII PHY interface



MII control interface

The *Figure 54* shows the timing waveform for the MII control interface.

Figure 54. Control signal timing relationship at the MII PHY interface



18.9.2 RMII interface

RMII timing parameters

The *Table 98* describes RMII timings parameters.

Table 98. RMII timing parameters

Parameter	Min	Typ	Max	Units
REF_CLK Frequency		50		MHz
REF_CLK Duty Cycle	35		65	%
TXD[1:0], TX_EN,RXD[1:0], CRS_DV, RX_ER (Data Setup to REF_CLK rising edge)	4			ns
TXD[1:0], TX_EN,RXD[1:0], CRS_DV, RX_ER (Data hold from REF_CLK rising edge)	2			ns

19 Alternate functions on PIO

19.1 Alternate functions

To improve flexibility and to allow the STi7105 to fit into different set-top box application architectures, the input and output signals from some of the peripherals and functions are not directly connected to the pins of the device. Instead, they are assigned to the alternate function inputs and outputs of a PIO port bit, or an I/O pin. This allows the pins to be configured with their default function if the associated input or output is not required in that particular application.

Some pins have several alternate functions, for inputs and outputs, or both. *Table 99* to *Table 115* list the different alternate functions.

Inputs connected to the alternate function input are permanently connected to the input pin. The output signal from a peripheral is only connected when the PIO bit is configured into either push-pull or open drain driver alternate function mode.

Some alternate function signals are available on more than one PIO port.

The STi7105 uses 7 PIO banks (PIO#0 to PIO#6) that are controlled by the COMMS IP and 10 banks that are driven by a standalone PIO module called STD_PIO.

The STi7105 embeds two types of PIOs alternate functions.

- Functions that are enabled by a register located inside the COMMS (or STD_PIO module).
- Functions that are enabled by a register located inside the system config module. This configuration is required for the pins where the alternate functions are enabled already at reset (by default the pins controlled by the COMMS are in the PIO mode and not alternate).

In addition to the multiplexing on the PIO pins, the STi7105 uses other pin multiplexing to provide different signal options depending upon the device application. For these other multiplexing options see *Section 7: Basic chip operating modes and multiplexing scenarios on page 98*.

Figure 55. I/O port pins (alternate functions controlled by COMMS or STD_PIO)

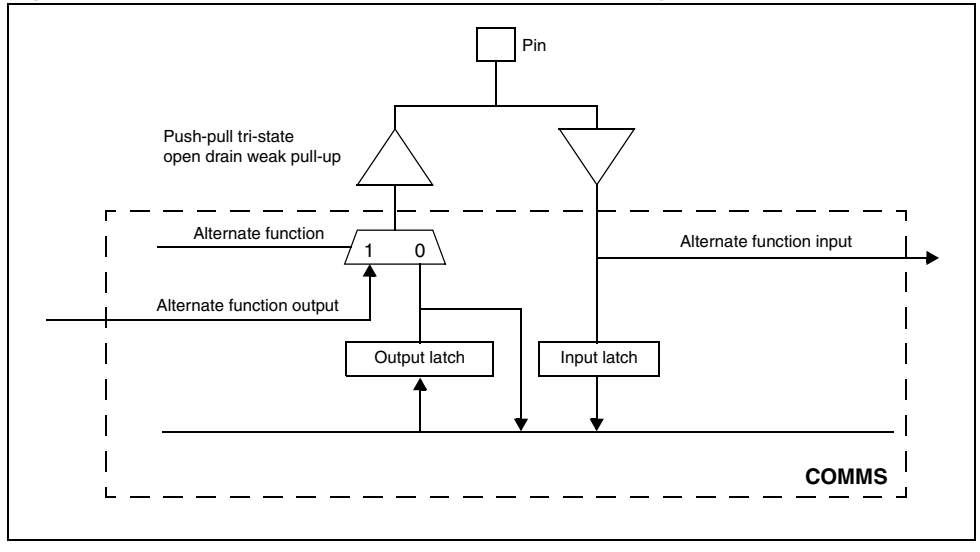
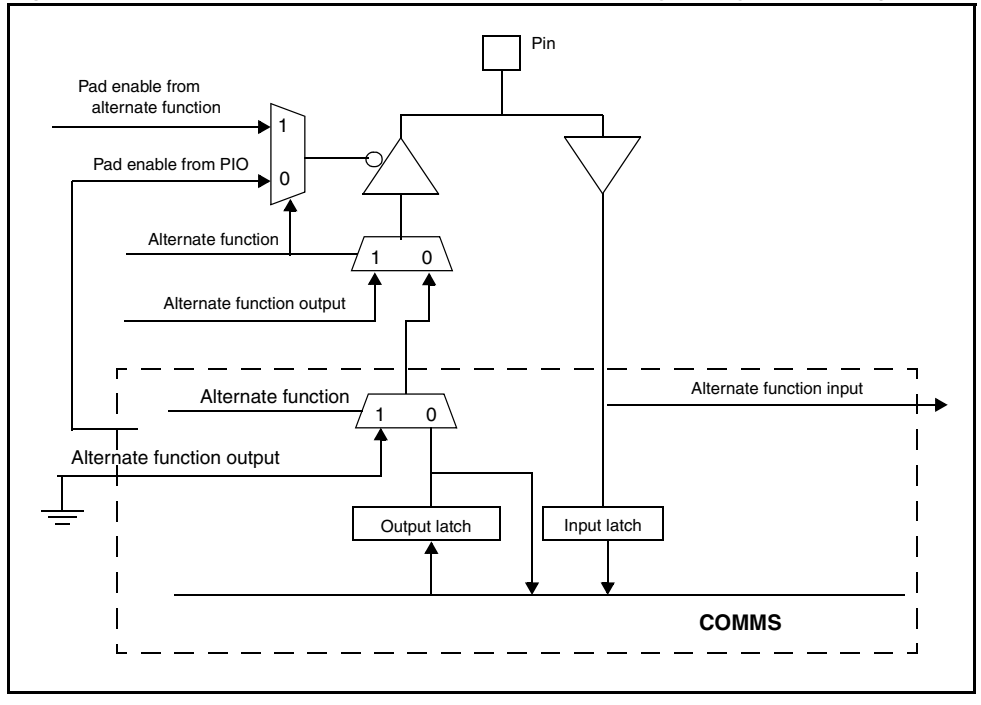


Figure 56. I/O port pins (alternate functions controlled by the System Config bit)



Note: In case of alternate functions controlled by the System Config bit, the enabling of the pad is driven by the alternate function itself when in the alternate mode or by the COMMS (or STD_PIO) signals when in the PIO mode.

19.2 PIO0 alternate functions

PIO0 is on COMMS block. It provides:

- first digital video output extension (8 to 16-bit) DVO0
- second digital video output (24-bit) DVO1
- smartcard interfaces SC0 and SC1
- UART0 interfaces

Table 99. PIO0 alternate functions

PIO0	Config register: SYSTEM_CONFIG19[15:0]					
	Config bus: PIO0_ALTFOP[1:0]_MUX_SEL_BUS[7:0]					
PIN	**Parameter**	**Alternate 1**	**Alternate 2**	**Alternate 3**	**Alternate 4**	**Alternate 5**
		Digital video output 1	**Digital video output 0**	**Smart card 0**	**UART 0**	**Reserved**
PIO0[0]	Name	DVO1[0]	DVO0[16]	SC0_DATAOUT	UART0_TXD	RESERVED
	Description	Second DVO output	First DVO output	Smartcard 0	UART 0	RESERVED
	Direction	O	O	O	O	RESERVED
	Configuration	SYSTEM_CONFIG19[8,0]=00	SYSTEM_CONFIG19[8,0]=01	SYSTEM_CONFIG19[8,0]=10	SYSTEM_CONFIG19[8,0]=11	RESERVED
PIO0[1]	Name	DVO1[1]	DVO0[17]	SC0_DATAIN	UART0_RXD	RESERVED
	Description	Second DVO output	First DVO output	Smartcard 0	UART 0	RESERVED
	Direction	O	O	I	I	RESERVED
	Configuration	SYSTEM_CONFIG19[9,1]=00	SYSTEM_CONFIG19[9,1]=01	Not required	Not required	RESERVED
PIO0[2]	Name	DVO1[2]	DVO0[18]	SC0_EXTCLKIN	UART0_NOT_OE	RESERVED
	Description	Second DVO output	First DVO output	Smartcard 0	UART 0	RESERVED
	Direction	O	O	I	O	RESERVED
	Configuration	SYSTEM_CONFIG19[10,2]=00	SYSTEM_CONFIG19[10,2]=01	Not required	SYSTEM_CONFIG19[10,2]=11	RESERVED
PIO0[3]	Name	DVO1[3]	DVO0[19]	SC0_CLKOUT	UART0_RTS	RESERVED
	Description	Second DVO output	First DVO output	Smartcard 0	UART 0	RESERVED
	Direction	O	O	O	O	RESERVED
	Configuration	SYSTEM_CONFIG19[11,3]=00	SYSTEM_CONFIG19[11,3]=01	SYSTEM_CONFIG19[11,3]=10	SYSTEM_CONFIG19[11,3]=11	RESERVED

Table 99. PIO0 alternate functions (continued)

PIO0	Config register: SYSTEM_CONFIG19[15:0]					
	Config bus: PIO0_ALTFOP[1:0]_MUX_SEL_BUS[7:0]					
PIN	**Parameter**	**Alternate 1**	**Alternate 2**	**Alternate 3**	**Alternate 4**	**Alternate 5**
		Digital video output 1	**Digital video output 0**	**Smart card 0**	**UART 0**	**Reserved**
PIO0[4]	Name	DVO1[4]	DVO0[20]	SC0_RESET	UART0_CTS	RESERVED
	Description	Second DVO output	First DVO output	Smartcard 0	UART 0	RESERVED
	Direction	O	O	O	I	RESERVED
	Configuration	SYSTEM_CONFIG19[12,4]=00	SYSTEM_CONFIG19[12,4]=01	SYSTEM_CONFIG19[12,4]=10	Not required	RESERVED
PIO0[5]	Name	DVO1[5]	DVO0[21]	SC0_COND_VCC		RESERVED
	Description	Second DVO output	First DVO output	Smartcard 0		RESERVED
	Direction	O	O	O		RESERVED
	Configuration	SYSTEM_CONFIG19[13,5]=00	SYSTEM_CONFIG19[13,5]=01	SYSTEM_CONFIG19[13,5]=10		RESERVED
PIO0[6]	Name	DVO1[6]	DVO0[22]	SC0_COND_VPP		RESERVED
	Description	Second DVO output	First DVO output	Smartcard 0		RESERVED
	Direction	O	O	O		RESERVED
	Configuration	SYSTEM_CONFIG19[14,6]=00	SYSTEM_CONFIG19[14,6]=01	SYSTEM_CONFIG19[14,6]=10		RESERVED
PIO0[7]	Name	DVO1[7]	DVO0[23]	SC0_DETECT		RESERVED
	Description	Second DVO output	First DVO output	Smartcard 0		RESERVED
	Direction	O	O	I		RESERVED
	Configuration	SYSTEM_CONFIG19[15,7]=00	SYSTEM_CONFIG19[15,7]=01	Not required		RESERVED

19.3 PIO1 alternate functions

PIO1 is on COMMS block. It provides:

- second Digital Video Output (24-bit) DVO1
- smart card interface SC1
- MAFE interface
- UART interfaces

Table 100. PIO1 alternate functions

PIO1	Config register: SYSTEM_CONFIG20[15:0]				
	Config bus: PIO0_ALTFOP[1:0]_MUX_SEL_BUS[7:0]				
PIN	**Parameter**	**Alternate 1**	**Alternate 2**	**Alternate 3**	**Alternate 4**
		Digital video output 1	**MAFE I/F**	**Smartcard 1**	**UART 1**
PIO1[0]	Name	DVO1[8]	MAFE_DIN	SC1_DATAOUT	UART1_TXD
	Description	Second DVO output	MAFE	Smartcard 1	UART 1
	Direction	O	I	O	O
	Configuration	SYSTEM_CONFIG20[8,0]=00	Not required	SYSTEM_CONFIG20[8,0]=10	SYSTEM_CONFIG20[8,0]=11
PIO1[1]	Name	DVO1[9]	MAFE_SCLK	SC1_DATAIN	UART1_RXD
	Description	Second DVO output	MAFE	Smartcard 1	UART 1
	Direction	O	I	I	I
	Configuration	SYSTEM_CONFIG20[9,1]=00	Not required	Not required	Not required
PIO1[2]	Name	DVO1[10]	MAFE_HC1	SC1_EXTCLKIN	
	Description	Second DVO output	MAFE	Smartcard 1	
	Direction	O	O	I	
	Configuration	SYSTEM_CONFIG20[10,2]=00	SYSTEM_CONFIG20[10,2]=01	Not required	
PIO1[3]	Name	DVO1[11]	MAFE_DOUT	SC1_CLKOUT	UART1_RTS
	Description	Second DVO output	MAFE	Smartcard 1	UART 1
	Direction	O	O	O	O
	Configuration	SYSTEM_CONFIG20[11,3]=00	SYSTEM_CONFIG20[11,3]=01	SYSTEM_CONFIG20[11,3]=10	SYSTEM_CONFIG20[11,3]=11

Table 100. PIO1 alternate functions (continued)

PIO1	Config register: SYSTEM_CONFIG20[15:0]				
	Config bus: PIO0_ALTFOP[1:0]_MUX_SEL_BUS[7:0]				
PIN	**Parameter**	**Alternate 1**	**Alternate 2**	**Alternate 3**	**Alternate 4**
		Digital video output 1	**MAFE I/F**	**Smartcard 1**	**UART 1**
PIO1[4]	Name	DVO1[12]		SC1_RESET	UART1_CTS
	Description	Second DVO output		Smartcard 1	UART 1
	Direction	O		O	I
	Configuration	SYSTEM_CONFIG20[12,4]=00		SYSTEM_CONFIG20[12,4]=10	Not required
PIO1[5]	Name	DVO1[13]	MAFE_FS	SC1_COND_VCC	
	Description	Second DVO output	MAFE	Smartcard 1	
	Direction	O	I	O	
	Configuration	SYSTEM_CONFIG20[13,5]=00	Not required	SYSTEM_CONFIG20[13,5]=00	
PIO1[6]	Name	DVO1[14]		SC1_COND_VPP	
	Description	Second DVO output		Smartcard 1	
	Direction	O		O	
	Configuration	SYSTEM_CONFIG20[14,6]=00		SYSTEM_CONFIG20[14,6]=10	
PIO1[7]	Name	DVO1[15]		SC1_DETECT	
	Description	Second DVO output		Smartcard 1	
	Direction	O		I	
	Configuration	SYSTEM_CONFIG20[15,7]=00		Not required	

19.4 PIO2 alternate functions

PIO2 is on COMMS block. It provides:

- second Digital Video Output (24-bit) DVO1
- SSC0 and SSC1 interfaces with I2C half-duplex/full-duplex modes selectable by the ssc0_mux_sel and ssc1_mux_sel bits
- SSC2 and SSC3 interfaces with I2C half-duplex modes selectable

Table 101. PIO2 alternate functions

PIO2	**Config register: SYSTEM_CONFIG21[15:0]**				
	Config bus: PIO2_ALTFOP[1:0]_MUX_SEL_BUS[7:0]				
PIN	**Parameter**	**Alternate 1**	**Alternate 2**	**Alternate 3**	**Alternate 4**
		Digital video output 1	**SSC2, SSC3**	**SSC 0,1,2,3**	**SSC 0,1,2,3**
PIO2[0]	Name	DVO1[16]		SSC2_MTSR	SSC2_MRST
	Description	Second DVO output		SSC2 Data bit: master transmit/slave receive, full duplex	SSC2 Data bit: master receive/slave transmit, full duplex
	Direction	O		I/O	I/O
	Configuration	SYSTEM_CONFIG21[8,0]=00		In: SYSTEM_CONFIG16[10,9]=00 Out: SYSTEM_CONFIG21[8,0]=10	In: SYSTEM_CONFIG16[8,7]=00 Out: SYSTEM_CONFIG21[8,0]=11
PIO2[1]	Name	DVO1[17]		SSC3_MTSR	SSC3_MRST
	Description	Second DVO output		SSC3 Data bit: master transmit/slave receive, full duplex	SSC3 Data bit: master receive/slave transmit, full duplex
	Direction	O		I/O	I/O
	Configuration	SYSTEM_CONFIG21[9,1]=00		In: SYSTEM_CONFIG16[17:16]=00 Out: SYSTEM_CONFIG21[9,1]=10	In: SYSTEM_CONFIG16[15,14]=00 Out: SYSTEM_CONFIG21[9,1]=11
PIO2[2]	Name	DVO1[18]		SSC0_SCL	SSC0_SCL
	Description	Second DVO output		SSC0 serial clock in/out	SSC0 serial clock in/out
	Direction	O		I/O	I/O
	Configuration	SYSTEM_CONFIG21[10,2]=00		In: Not required Out: SYSTEM_CONFIG21[10,2]=10	In: Not required Out: SYSTEM_CONFIG21[10,2]=11

Table 101. PIO2 alternate functions (continued)

PIO2	Config register: SYSTEM_CONFIG21[15:0]				
	Config bus: PIO2_ALTFOP[1:0]_MUX_SEL_BUS[7:0]				
PIN	**Parameter**	**Alternate 1**	**Alternate 2**	**Alternate 3**	**Alternate 4**
		Digital video output 1	**SSC2, SSC3**	**SSC 0,1,2,3**	**SSC 0,1,2,3**
PIO2[3]	Name	DVO1[19]		SSC0_MTSR	SSC0_MRST
	Description	Second DVO output		SSC0 Data bit: master transmit/slave receive, full duplex	SSC0 Data bit: master receive/slave transmit, full duplex
	Direction	O		I/O	I/O
	Configuration	SYSTEM_CONFIG21[11,3]=00		In: Not required Out: SYSTEM_CONFIG21[11,3]=10	In: SYSTEM_CONFIG16[0]=0 Out: SYSTEM_CONFIG21[11,3]=11
PIO2[4]	Name	DVO1[20]		SSC0_MRST	SSC0_MRST
	Description	Second DVO output		SSC0 Data bit: master receive/slave transmit, full duplex	SSC0 Data bit: master receive/slave transmit, full duplex
	Direction	O		I/O	I/O
	Configuration	SYSTEM_CONFIG21[12,4]=00		In: SYSTEM_CONFIG16[0]=1 Out: SYSTEM_CONFIG21[12,4]=10	In: SYSTEM_CONFIG16[0]=1 Out: SYSTEM_CONFIG21[12,4]=11
PIO2[5]	Name	DVO1[21]		SSC1_SCL	SSC1_SCL
	Description	Second DVO output		SSC1 Serial Clock	SSC1 Serial Clock
	Direction	O		I/O	I/O
	Configuration	SYSTEM_CONFIG21[13,5]=00		In: Not required Out: SYSTEM_CONFIG21[13,5]=10	In: Not required Out: SYSTEM_CONFIG21[13,5]=11
PIO2[6]	Name	DVO1[22]		SSC1_MTSR	SSC1_MRST
	Description	Second DVO output		SSC1 Data bit: master transmit/slave receive, full duplex	SSC1 Data bit: master receive/slave transmit, full duplex
	Direction	O		I/O	I/O
	Configuration	SYSTEM_CONFIG21[14,6]=00		In: Not required Out: SYSTEM_CONFIG21[14,6]=10	In: SYSTEM_CONFIG16[3]=0 Out: SYSTEM_CONFIG21[14,6]=11

Table 101. PIO2 alternate functions (continued)

PIO2	Config register: SYSTEM_CONFIG21[15:0]				
	Config bus: PIO2_ALTFOP[1:0]_MUX_SEL_BUS[7:0]				
PIN	**Parameter**	**Alternate 1**	**Alternate 2**	**Alternate 3**	**Alternate 4**
		Digital video output 1	**SSC2, SSC3**	**SSC 0,1,2,3**	**SSC 0,1,2,3**
PIO2[7]	Name	DVO1[23]		SSC1_MRST	SSC1_MRST
	Description	Second DVO output		SSC1 Data bit: master receive/slave transmit, full duplex	SSC1 Data bit: master receive/slave transmit, full duplex
	Direction	O		I/O	I/O
	Configuration	SYSTEM_CONFIG21[15,7]=00		In: SYSTEM_CONFIG16[3]=1 Out: SYSTEM_CONFIG21[15,7]=10	In: SYSTEM_CONFIG16[3]=1 Out: SYSTEM_CONFIG21[15,7]=11

19.5 PIO3 alternate functions

PIO3 is on COMMS block. It provides:

- first digital video output (16-bit) DVO0
- second digital video output (24-bit) DVO1
- digital video port extension(16-bit) DVP0
- SSC2 and SSC3 interfaces with I2C half-duplex modes selectable
- infra red blaster interface IRB
- auxiliary VTG synchronizations

Table 102. PIO3 alternate functions

PIO3	Config register: SYSTEM_CONFIG25[15:0]				
	Config bus: PIO3_ALTFOP[1:0]_MUX_SEL_BUS[7:0]				
PIN	**Parameter**	**Alternate 1**	**Alternate 2**	**Alternate 3**	**Alternate 4**
		Digital video output 1	**Digital video input 0, ssc 2,3**	**Infra-red blaster, ssc 2,3**	**AUX video timing h/v refs**
PIO3[0]	Name	DVO1HS		IRB_IR_IN	VTG_AUX_HS
	Description	DVO horizontal sync		IRB IR data input	Aux video
	Direction	O		I	O
	Configuration	SYSTEM_CONFIG25[8,0]=00		Not required	SYSTEM_CONFIG25[8,0]=11
PIO3[1]	Name	DVO1_CLK		IRB_UHF_IN	
	Description	DVO clock		IRB UHF data input	
	Direction	O		I	
	Configuration	SYSTEM_CONFIG25[9,1]=00		Not required	
PIO3[2]	Name	DVO1VS	IRB_IR_DATA_OUT	IRB_IR_DATA_OUT	VTG_AUX_VS
	Description	DVO vertical sync	IRB IR data output	IRB IR data output	Aux video
	Direction	O	O	O	O
	Configuration	SYSTEM_CONFIG25[10,2]=00	SYSTEM_CONFIG25[10,2]=01	SYSTEM_CONFIG25[10,2]=10	SYSTEM_CONFIG25[10,2]=11

Table 102. PIO3 alternate functions (continued)

PIO3	Config register: SYSTEM_CONFIG25[15:0]					
	Config bus: PIO3_ALTFOP[1:0]_MUX_SEL_BUS[7:0]					
PIN	**Parameter**	**Alternate 1**	**Alternate 2**	**Alternate 3**		**Alternate 4**
		Digital video output 1	**Digital video input 0, ssc 2,3**	**Infra-red blaster, ssc 2,3**		**AUX video timing h/v refs**
PIO3[3]	Name	DVO1DE	IRB_DATA_OUT_OD	IRB_DATA_OUT_OD		VTG_AUX_BOTNOTTOP
	Description	Second DVO output	IRB data output open drain	IRB data output open drain		Aux video
	Direction	O	O	O		O
	Configuration	SYSTEM_CONFIG25[11,3]=00	SYSTEM_CONFIG25[11,3]=01	SYSTEM_CONFIG25[11,3]=10		SYSTEM_CONFIG25[11,3]=11
PIO3[4]	Name	DVO0[0]	DVP0[8]/SSC2_SCL	SSC2_SCL		
	Description	First DVO output	DVP input/SSC2 SCL out	SSC2 SCL out		
	Direction	O	I/O	I/O		
	Configuration	SYSTEM_CONFIG25[12,4]=00	In: Not required Out: SYSTEM_CONFIG25[12,4]=01	In: SYSTEM_CONFIG16[12,11]=00/01 Out: SYSTEM_CONFIG25[12,4]=10		
PIO3[5]	Name	DVO0[1]	DVP0[9]/SSC2_MTSR	SSC2_MTSR	SSC2_MRST	
	Description	First DVO output	DVP input/SSC2 Data bit: master transmit/slave receive, full duplex	SSC2 Data bit: master transmit/slave receive, full duplex	SSC2 Data bit: master receive/slave transmit, full duplex	
	Direction	O	I/O	I	I/O	
	Configuration	SYSTEM_CONFIG25[13,5]=00	In: Not required Out: SYSTEM_CONFIG25[13,5]=01	SYSTEM_CONFIG16[10,9]=01	In: SYSTEM_CONFIG16[8,7]=01 Out: SYSTEM_CONFIG25[13,5]=10	
PIO3[6]	Name	DVO0[2]	DVP0[10]/SSC3_SCL	SSC3_SCL		
	Description	First DVO output	DVP input/SSC3 SCL out	SSC3 SCL in/SSC3 SCL out		
	Direction	O	I/O	I/O		
	Configuration	SYSTEM_CONFIG25[14,6]=00	In: Not required Out: SYSTEM_CONFIG25[14,6]=01	In: SYSTEM_CONFIG16[19,18]=01 Out: SYSTEM_CONFIG25[14,6]=10		

Table 102. PIO3 alternate functions (continued)

PIO3	Config register: SYSTEM_CONFIG25[15:0]					
	Config bus: PIO3_ALTFOP[1:0]_MUX_SEL_BUS[7:0]					
PIN	**Parameter**	**Alternate 1**	**Alternate 2**	**Alternate 3**		**Alternate 4**
		Digital video output 1	**Digital video input 0, ssc 2,3**	**Infra-red blaster, ssc 2,3**		**AUX video timing h/v refs**
PIO3[7]	Name	DVO0[3]	DVP0[11]/SSC3_MTSR	SSC3_MTSR	SSC3_MRST	
	Description	First DVO output	DVP input/ SSC3 Data bit: master transmit/slave receive, full duplex	SSC3 Data bit: master transmit/slave receive, full duplex	SSC3 Data bit: master receive/slave transmit, full duplex	
	Direction	O	I/O	I	I/O	
	Configuration	SYSTEM_CONFIG25[15,7]=00	In: Not required Out: SYSTEM_CONFIG25[15,7]=01	In: SYSTEM_CONFIG16[17,16]=01	In: SYSTEM_CONFIG16[15,14]=01 Out: SYSTEM_CONFIG25[15,7]=10	

19.6 PIO4 alternate functions

PIO4 is on COMMS block. It provides:

- first digital video output (16-bit) DVO0
- digital video port extension(16-bit) DVP0
- UART2 interface
- pulse width modulator interface PWM
- USB power control

Table 103. PIO4 alternate functions

PIO4	Config register: SYSTEM_CONFIG34[15:0]				
	Config bus: PIO4_ALTFOP[1:0]_MUX_SEL_BUS[7:0]				
PIN	**Parameter**	**Alternate 1**	**Alternate 2**	**Alternate 3**	**Alternate 4**
		Digital video output 0	**Digital video input 0**	**UART 2, PWM 0,1**	**PWM 0, USB 1,2 Power ctrl**
PIO4[0]	Name	DVO0[4]	DVP0[12]	UART2_TXD	
	Description	First DVO output	DVP input	UART	
	Direction	O	I	O	
	Configuration	SYSTEM_CONFIG34[8,0]=00	Not required	SYSTEM_CONFIG34[8,0]=10	
PIO4[1]	Name	DVO0[5]	DVP0[13]	UART2_RXD	
	Description	First DVO output	DVP input	UART	
	Direction	O	I	I	
	Configuration	SYSTEM_CONFIG34[9,1]=00	Not required	Not required	
PIO4[2]	Name	DVO0[6]	DVP0[14]	UART2_CTS	
	Description	First DVO output	DVP input	UART	
	Direction	O	I	I	
	Configuration	SYSTEM_CONFIG34[10,2]=00	Not required	Not required	

Table 103. PIO4 alternate functions (continued)

PIO4	Config register: SYSTEM_CONFIG34[15:0]				
	Config bus: PIO4_ALTFOP[1:0]_MUX_SEL_BUS[7:0]				
PIN	**Parameter**	**Alternate 1**	**Alternate 2**	**Alternate 3**	**Alternate 4**
		Digital video output 0	**Digital video input 0**	**UART 2, PWM 0,1**	**PWM 0, USB 1,2 Power ctrl**
PIO4[3]	Name	DVO0[7]	DVP0[15]	PWM_CAPTURE_IN0/UART2_RTS	
	Description	First DVO output	DVP input	PWM 0 capture input/UART	
	Direction	O	I	I/O	
	Configuration	SYSTEM_CONFIG34[11,3]=00	Not required	In: Not required Out: SYSTEM_CONFIG34[11,3]=10	
PIO4[4]	Name	DVO0[8]		PWM_OUT0	USB1_PRT_OVCUR
	Description	First DVO output		PWM 0 output	USB 1 PRT overcurrent
	Direction	O		O	I
	Configuration	SYSTEM_CONFIG34[12,4]=00		SYSTEM_CONFIG34[12,4]=10	SYSTEM_CONFIG4[5]=0
PIO4[5]	Name	DVO0[9]		PWM_OUT1	USB1_PRT_PWR
	Description	First DVO output		PWM 1 output	USB 1 PRT power
	Direction	O		O	O
	Configuration	SYSTEM_CONFIG34[13,5]=00		SYSTEM_CONFIG34[13,5]=10	SYSTEM_CONFIG34[13,5]=11
PIO4[6]	Name	DVO0[10]		PWM_COMPARE_OUT1	USB2_PRT_OVCUR
	Description	First DVO output		PWM 1 compare output	USB 2 PRT overcurrent
	Direction	O		O	I
	Configuration	SYSTEM_CONFIG34[14,6]=00		SYSTEM_CONFIG34[14,6]=10	SYSTEM_CONFIG4[6]=0
PIO4[7]	Name	DVO0[11]		PWM_CAPTURE_IN1	USB2_PRT_PWR
	Description	First DVO output		PWM 1 compare output	USB 2 PRT power
	Direction	O		I	O
	Configuration	SYSTEM_CONFIG34[15,7]=00		Not required	SYSTEM_CONFIG34[15,7]=11

Caution: In case of USB signals, the usual naming convention is not used. In order to align with the STi7105 ballout names, this manual mentions two instances of USB as USB1 and USB2 rather than USB0 and USB1. Therefore, in this manual the first instance of USB is USB1 and the second instance is USB2.

19.7 PIO5 alternate functions

PIO5 is on COMMS block. It provides:

- first digital video output (16-bit) DVO0
- key scanner interface KEY SCAN
- UART3 interface
- main VTG synchronization signals

Table 104. PIO5 alternate functions

PIO5	Config register: SYSTEM_CONFIG35[15:0]				
	Config bus: PIO5_ALTFOP[1:0]_MUX_SEL_BUS[7:0]				
PIN	**Parameter**	**Alternate 1**	**Alternate 2**	**Alternate 3**	**Alternate 4**
		Digital video output 0	**Key scanning I/F, UART 3**	**UART 3, Key scanning**	**Main video timing h/v refs**
PIO5[0]	Name	DVO0[12]	UART3_TXD	KEY_SCAN_OUT[0]	
	Description	First DVO output	UART 3	Key scanning	
	Direction	O	O	O	
	Configuration	SYSTEM_CONFIG35[8,0]=00	SYSTEM_CONFIG35[8,0]=01	SYSTEM_CONFIG35[8,0]=10	
PIO5[1]	Name	DVO0[13]		UART3_RXD/KEY_SCAN_OUT[1]	
	Description	First DVO output		UART 3/Key scanning	
	Direction	O		I/O	
	Configuration	SYSTEM_CONFIG35[9,1]=00		In: Not required Out: SYSTEM_CONFIG35[9,1]=10	

Table 104. PIO5 alternate functions (continued)

PIO5	Config register: SYSTEM_CONFIG35[15:0]				
	Config bus: PIO5_ALTFOP[1:0]_MUX_SEL_BUS[7:0]				
PIN	**Parameter**	**Alternate 1**	**Alternate 2**	**Alternate 3**	**Alternate 4**
		Digital video output 0	**Key scanning I/F, UART 3**	**UART 3, Key scanning**	**Main video timing h/v refs**
PIO5[2]	Name	DVO0[14]	UART3_RTS	KEY_SCAN_OUT[2]	
	Description	First DVO output	UART 3	Key scanning	
	Direction	O	O	O	
	Configuration	SYSTEM_CONFIG35[10,2]=00	SYSTEM_CONFIG35[10,2]=01	SYSTEM_CONFIG35[10,2]=10	
PIO5[3]	Name	DVO0[15]		UART3_CTS/KEY_SCAN_OUT[3]	
	Description	First DVO output		UART 3/Key scanning	
	Direction	O		I/O	
	Configuration	SYSTEM_CONFIG35[11,3]=00		In: Not required Out: SYSTEM_CONFIG35[11,3]=10	
PIO5[4]	Name	DVO0_HSYNC	KEY_SCAN_IN[0]		VTG_MAIN_HS
	Description	First DVO output	Key scanning		VTG main
	Direction	O	I		O
	Configuration	SYSTEM_CONFIG35[12,4]=00	Not required		SYSTEM_CONFIG35[12,4]=11
PIO5[5]	Name	DVO0CLK	KEY_SCAN_IN[1]		
	Description	First DVO output	Key scanning		
	Direction	O	I		
	Configuration	SYSTEM_CONFIG35[13,5]=00	Not required		
PIO5[6]	Name	DVO0_VSYNC	KEY_SCAN_IN[2]		VTG_MAIN_VS
	Description	First DVO output	Key scanning		VTG main
	Direction	O	I		O
	Configuration	SYSTEM_CONFIG35[14,6]=00	Not required		SYSTEM_CONFIG35[14,6]=11

Table 104. PIO5 alternate functions (continued)

PIO5	Config register: SYSTEM_CONFIG35[15:0]				
	Config bus: PIO5_ALTFOP[1:0]_MUX_SEL_BUS[7:0]				
PIN	**Parameter**	**Alternate 1**	**Alternate 2**	**Alternate 3**	**Alternate 4**
		Digital video output 0	**Key scanning I/F, UART 3**	**UART 3, Key scanning**	**Main video timing h/v refs**
PIO5[7]	Name	DVO0_DATA_EN	KEY_SCAN_IN[3]		VTG_MAIN_BOTNOTTOP
	Description	First DVO output	Key scanning		VTG main
	Direction	O	I		O
	Configuration	SYSTEM_CONFIG35[15,7]=00	Not required		SYSTEM_CONFIG35[15,7]=11

19.8 PIO6 alternate functions

PIO6 is on COMMS block. It provides:

- digital video port (8-bit) DVP0
- third transport input interface TSIN2
- second PCMCIA interface
- input VTG synchronization signals
- EMI SS arbiter signals/PCI support
- EMI SS arbiter signals

Table 105. PIO6 alternate functions

PIO6	Config register: SYSTEM_CONFIG36[15:0]					
	Config bus: PIO6_ALTFOP[1:0]_MUX_SEL_BUS[7:0]					
PIN	**Parameter**	**Alternate 1**	**Alternate 2**	**Alternate 3**	**Alternate 4**	**Alternate 5**
		Digital video input 0, PCMCIA 2 I/F	**Transport stream input 2**	**PCI I/F, PCMCIA 2 i/F, Video input timing h/v refs**		**PCI I/F, EMI I/F**
PIO6[0]	Name	DVP0[0]/PCMCIA2_OE	TSIN2SER/DATA[7]	PCI_INT_TO_HOST		PCI_INT_FROM_DEVICE[0]
	Description	DVP input/ PCMCIA 2 I/F	TS2 input	PCI host		PCI device
	Direction	I/O	I	O		I
	Configuration	In: Not required Out: SYSTEM_CONFIG36[16,8,0]=000	SYSTEM_CONFIG4[10]=0	SYSTEM_CONFIG36[16,8,0]=010		SYSTEM_CONFIG5[27]=0
PIO6[1]	Name	DVP0[1]/PCMCIA2_WE	TSIN2BYTECLK			PCI_INT_FROM_DEVICE[1]
	Description	DVP input/ PCMCIA 2 I/F	TS2 input			PCI device
	Direction	I/O	I			I
	Configuration	In: Not required Out: SYSTEM_CONFIG36[17,9,1]=000	SYSTEM_CONFIG4[10]=0			Not required

Table 105. PIO6 alternate functions (continued)

PIO6	Config register: SYSTEM_CONFIG36[15:0]					
	Config bus: PIO6_ALTFOP[1:0]_MUX_SEL_BUS[7:0]					
PIN	**Parameter**	**Alternate 1**	**Alternate 2**	**Alternate 3**	**Alternate 4**	**Alternate 5**
		Digital video input 0, PCMCIA 2 I/F	**Transport stream input 2**	**PCI I/F, PCMCIA 2 i/F, Video input timing h/v refs**		**PCI I/F, EMI I/F**
PIO6[2]	Name	DVP0[2]/PCMCIA2_IORD	TSIN2BYTECLKVALID			PCI_INT_FROM_DEVICE[2]
	Description	DVP input/PCMCIA 2 i/F	TS2 input			PCI Host/device
	Direction	I/O	I			I
	Configuration	In: Not required Out: SYSTEM_CONFIG36[18,10,2]=000	SYSTEM_CONFIG4[10]=0			Not required
PIO6[3]	Name	DVP0[3]/PCMCIA2_IOWR	TSIN2ERROR			
	Description	DVP input/PCMCIA 2 I/F	TS2 input			
	Direction	I/O	I			
	Configuration	In: Not required Out: SYSTEM_CONFIG36[19,11,3]=000	SYSTEM_CONFIG4[10]=0			
PIO6[4]	Name	DVP0[4]	TSIN2PACKETCLK	PCMCIA2_WAIT		
	Description	DVP input	TS2 input	PCMCIA 2 I/F		
	Direction	I	I	I		
	Configuration	Not required	In: SYSTEM_CONFIG4[10]=0	Not required		
PIO6[5]	Name	DVP0[5]	TSIN2DATA[6]	PCMCIA_INT		PCI_BUS_REQ[1]
	Description	DVP input	TS2 input	PCMCIA 2 I/F		PCI Host/device
	Direction	I	I	I		I
	Configuration	Not required	In: SYSTEM_CONFIG4[10]=0	Not required		Not required

Table 105. PIO6 alternate functions (continued)

PIO6	Config register: SYSTEM_CONFIG36[15:0]					
	Config bus: PIO6_ALTFOP[1:0]_MUX_SEL_BUS[7:0]					
PIN	**Parameter**	**Alternate 1**	**Alternate 2**	**Alternate 3**	**Alternate 4**	**Alternate 5**
		Digital video input 0, PCMCIA 2 I/F	**Transport stream input 2**	**PCI I/F, PCMCIA 2 i/F, Video input timing h/v refs**		**PCI I/F, EMI I/F**
PIO6[6]	Name	DVP0[6]	TSIN2DATA[5]	VTG_IN_HS		PCI_BUS_REQ[2]
	Description	DVP input	TS2 input	VTG input lock		PCI Host/device
	Direction	I	I	I		I
	Configuration	Not Required	In: SYSTEM_CONFIG4[10]=0	Not required		Not required
PIO6[7]	Name	DVP0[7]	TSIN2DATA[4]	VTG_IN_VS		
	Description	DVP input	TS2 input	VTG		
	Direction	I	I	I		
	Configuration	Not required	In: SYSTEM_CONFIG4[10]=0	Not required		

19.9 PIO7 alternate functions

PIO7 is PIO0 on GPIO standalone block. It provides:

- digital video port (8-bit) DVP0
- third transport input interface TSIN2
- MII and RMII interfaces
- key scanner interface KEY SCAN
- EMI SS arbiter signals/PCI support
- EMI SS arbiter signals

Note: During reset PIO7[7:4] are in input mode for mode pin capture.

Table 106. PIO7 alternate functions

PIO7	**Config register: SYSTEM_CONFIG37[15:0]**					
	Config bus: PIO7_ALTFOP[1:0]_MUX_SEL_BUS[7:0]					
PIN	**Parameter**	**Alternate 1**	**Alternate 2**	**Alternate 3**	**Alternate 4**	**Alternate 5**
		Digital video input 0	**Transport stream input 2**	**Key scanning**	**PCI I/F**	**PCI I/F, EMI I/F**
PIO7[0]	Name	DVP0_HSYNC	TSIN2DATA[3]	KEY_SCAN_OUT[0]		PCI_LOCK_IN
	Description	DVP input	TS2 input	Key scanning		PCI Host/device
	Direction	I	I	O		I
	Configuration	Not required	SYSTEM_CONFIG4[10]=0	SYSTEM_CONFIG37[16,8,0]=010		SYSTEM_CONFIG5[25]=0
PIO7[1]	Name	DVP0_VSYNC	TSIN2DATA[2]	KEY_SCAN_OUT[1]	PCI_BUS_GNT[1]	PCI_BUS_GNT[1]
	Description	DVP input	TS2 input	Key scanning	PCI Host/device	PCI host/device
	Direction	I	I	O	O	O
	Configuration	Not required	SYSTEM_CONFIG4[10]=0	SYSTEM_CONFIG37[17,9,1]=010	Out: SYSTEM_CONFIG37[17,9,1]=011	SYSTEM_CONFIG37[17,9,1]=100

Table 106. PIO7 alternate functions (continued)

PIO7	Config register: SYSTEM_CONFIG37[15:0]					
	Config bus: PIO7_ALTFOP[1:0]_MUX_SEL_BUS[7:0]					
PIN	**Parameter**	**Alternate 1**	**Alternate 2**	**Alternate 3**	**Alternate 4**	**Alternate 5**
		Digital video input 0	**Transport stream input 2**	**Key scanning**	**PCI I/F**	**PCI I/F, EMI I/F**
PIO7[2]	Name	DVP0_CLK	TSIN2DATA[1]	KEY_SCAN_OUT[2]	PCI_BUS_GNT[2]	PCI_BUS_GNT[2]
	Description	DVP input	TS2 input	Key scanning	PCI Host/device	PCI Host/device
	Direction	I	I	O	O	O
	Configuration	Not required	SYSTEM_CONFIG4[10]=0	SYSTEM_CONFIG37[18,10,2]=010	Out: SYSTEM_CONFIG37[18,10,2]=011	SYSTEM_CONFIG37[18,10,2]=101
PIO7[3]	Name		TSIN2DATA[0]	KEY_SCAN_OUT[3]		
	Description		TS2 input	Key scanning		
	Direction		I	O		
	Configuration		SYSTEM_CONFIG4[10]=0	SYSTEM_CONFIG37[19,11,3]=010		
PIO7[4]	Name	MIIRX_DV/MII_EXCRS	RMIICRS_DV			
	Description	MII receive data valid	RMII receive data valid			
	Direction	I/O	I			
	Configuration	In: Not required Out: SYSTEM_CONFIG37[20,12,4]=000	SYSTEM_CONFIG4[10]=0			
PIO7[5]	Name	MIIRX_ER/MII_EXCOL	RMIIRX_ER			
	Description	MII receive error	RMII receive error			
	Direction	I/O	I			
	Configuration	In: Not required Out: SYSTEM_CONFIG37[21,13,5]=000	SYSTEM_CONFIG4[10]=0			

Table 106. PIO7 alternate functions (continued)

PIO7	Config register: SYSTEM_CONFIG37[15:0]					
	Config bus: PIO7_ALTFOP[1:0]_MUX_SEL_BUS[7:0]					
PIN	**Parameter**	**Alternate 1**	**Alternate 2**	**Alternate 3**	**Alternate 4**	**Alternate 5**
		Digital video input 0	**Transport stream input 2**	**Key scanning**	**PCI I/F**	**PCI I/F, EMI I/F**
PIO7[6]	Name	MIITXD[0]	RMIITXD[0]			
	Description	MII transmit data	RMII transmit data			
	Direction	O	O			
	Configuration	SYSTEM_CONFIG37[22,14,6]=000	SYSTEM_CONFIG37[22,14,6]=001			
PIO7[7]	Name	MIITXD[1]	RMIITXD[1]			
	Description	MII transmit data	RMII transmit data			
	Direction	O	O			
	Configuration	SYSTEM_CONFIG37[23,15,7]=000	SYSTEM_CONFIG37[23,15,7]=001			

19.10 PIO8 alternate functions

PIO8 is PIO1 on GPIO standalone block. It provides:

- MII and RMII interfaces
- DVO1 ALPHA coefficient output

Note: During reset PIO8[7:0] are in input mode for mode pin capture.

Table 107. PIO8 alternate functions

PIO8	Config register: SYSTEM_CONFIG46[15:0]			
	Config bus: PIO8_ALTFOP[1:0]_MUX_SEL_BUS[7:0]			
PIN	**Parameter**	**Alternate 1**	**Alternate 2**	**Alternate 3**
		MII I/F	**RMII I/F, Digital video output 1**	
PIO8[0]	Name	MIITXD[2]	DVO1_ALPHA[0]	
	Description	MII transmit data	Second DVO/Alpha output	
	Direction	O	O	
	Configuration	SYSTEM_CONFIG46[8,0]=00	SYSTEM_CONFIG46[8,0]=01	
PIO8[1]	Name	MIITXD[3]	DVO1_ALPHA[1]	
	Description	MII transmit data	Second DVO/Alpha output	
	Direction	O	O	
	Configuration	SYSTEM_CONFIG46[9,1]=00	SYSTEM_CONFIG46[9,1]=01	
PIO8[2]	Name	MIITX_EN	RMIITX_EN	
	Description	MII TX Enable	RMII TX Enable	
	Direction	O	O	
	Configuration	SYSTEM_CONFIG46[10,2]=00	SYSTEM_CONFIG46[10,2]=01	

Table 107. PIO8 alternate functions (continued)

PIO8	Config register: SYSTEM_CONFIG46[15:0]			
	Config bus: PIO8_ALTFOP[1:0]_MUX_SEL_BUS[7:0]			
PIN	**Parameter**	**Alternate 1**	**Alternate 2**	**Alternate 3**
		MII I/F	**RMII I/F, Digital video output 1**	
PIO8[3]	Name	MIIMDIO	RMIIMDIO	
	Description	MII mgmt data	RMII mgmt data	
	Direction	I/O	I/O	
	Configuration	In: Not required Out: SYSTEM_CONFIG46[11,3]=00	In: Not required Out: SYSTEM_CONFIG46[11,3]=01	
PIO8[4]	Name	MIIMDCI/MIIMDCO	RMIIMDC	
	Description	MII Mgmg Clock input/output	RMII Mgmg Clock	
	Direction	I/O	O	
	Configuration	In: Not required Out: SYSTEM_CONFIG46[12,4]=00	SYSTEM_CONFIG46[12,4]=01	
PIO8[5]	Name	MIIRXCLK	DVO1_ALPHA[2]	
	Description	MII receive clock for RXD	Second DVO/Alpha output	
	Direction	I	O	
	Configuration	Not required	SYSTEM_CONFIG46[13,5]=01	
PIO8[6]	Name	MIIRXD[0]	RMIIRXD[0]	
	Description	MII receive data	RMII receive data	
	Direction	I	I	
	Configuration	Not required	Not required	
PIO8[7]	Name	MIIRXD[1]	RMIIRXD[1]	
	Description	MII receive data	RMII receive data	
	Direction	I	I	
	Configuration	Not required	Not required	

19.11 PIO9 alternate functions

PIO9 is PIO2 on GPIO standalone block. It provides:

- MII and RMII interfaces
- DVO1 ALPHA coefficient output

Note: During reset PIO9[6, 1:0] are in input mode for mode pin capture.

Table 108. PIO9 alternate functions

PIO9	Config register: SYSTEM_CONFIG47[15:0]			
	Config bus: PIO9_ALTFOP[1:0]_MUX_SEL_BUS[7:0]			
PIN	**Parameter**	**Alternate 1**	**Alternate 2**	**Alternate 3**
		MII I/F	**RMII I/F, Digital video output 1**	
PIO9[0]	Name	MIIRXD[2]	DVO1_ALPHA[3]	
	Description	MII receive data	Second DVO/Alpha output	
	Direction	I	O	
	Configuration	Not required	SYSTEM_CONFIG47[8,0]=01	
PIO9[1]	Name	MIIRXD[3]	DVO1_ALPHA[4]	
	Description	MII receive data	Second DVO/Alpha output	
	Direction	I	O	
	Configuration	Not required	SYSTEM_CONFIG47[9,1]=01	
PIO9[2]	Name	MIITXCLK	DVO1_ALPHA[5]	
	Description	MII Transmit clock for TXD	Second DVO/Alpha output	
	Direction	I	O	
	Configuration	Not required	SYSTEM_CONFIG47[10,2]=01	
PIO9[3]	Name	MIICOL	DVO1_ALPHA[6]	
	Description	MII collision detected	Second DVO/Alpha output	
	Direction	I	O	
	Configuration	Not required	SYSTEM_CONFIG47[11,3]=01	

Table 108. PIO9 alternate functions (continued)

PIO9	Config register: SYSTEM_CONFIG47[15:0]			
	Config bus: PIO9_ALTFOP[1:0]_MUX_SEL_BUS[7:0]			
PIN	**Parameter**	**Alternate 1**	**Alternate 2**	**Alternate 3**
		MII I/F	**RMII I/F, Digital video output 1**	
PIO9[4]	Name	MIICRS	DVO1_ALPHA[7]	
	Description	MII carrier sense detected	Second DVO/Alpha output	
	Direction	I	O	
	Configuration	Not required	SYSTEM_CONFIG47[12,4]=01	
PIO9[5]	Name	MIIPHYCLK	RMIIREF_CLK	
	Description	Clock to PHY	RMII REF CLOCK	
	Direction	O	I/O	
	Configuration	SYSTEM_CONFIG47[13,5]=00	In: Not required Out: SYSTEM_CONFIG47[13,5]=01	
PIO9[6]	Name	MIIMDINT	RMIIMDINT	
	Description	Mgmt data interrupt	RMII Mgmt data interrupt	
	Direction	I	I	
	Configuration	Not required	Not required	
PIO9[7]	Name	HDMI_PLUGIN/MDO_EN		
	Description	HDMI, MDO		
	Direction	I/O		
	Configuration	In: Not required Out: SYSTEM_CONFIG47[15,7]=00		

19.12 PIO10 alternate functions

PIO10 is PIO3 on GPIO standalone block. It provides:

- multichannel digital audio PCM output AUDDIG1PCMOUT
- audio S/PDIF output S/PDIF
- stereo digital Audio PCM input AUDDIG

Table 109. PIO10 alternate functions

PIO10	Config register: Not required			
	Config bus: Not required			
PIN	**Parameter**	**Alternate 1**	**Alternate 2**	**Alternate 3**
		Digital audio output 0, SPDIF I/F, Audio digital input 0		
PIO10[0]	Name	AUDDIG0_PCM_OUT_DATA0		
	Description	PCMOUT 0 - data 0		
	Direction	O		
	Configuration	Not required		
PIO10[1]	Name	AUDDIG0_PCM_OUT_DATA1		
	Description	PCMOUT 0 - data 1		
	Direction	O		
	Configuration	Not required		
PIO10[2]	Name	PCI_IDSEL/AUDDIG0_PCM_OUT_DATA2		
	Description	PCI, PCMOUT 0 - data 2		
	Direction	I/O		
	Configuration	Not required		
PIO10[3]	Name	AUDDIG0_PCM_OUT_CLKIN/CLK		
	Description	PCMOUT 0 - clock		
	Direction	I/O		
	Configuration	Not required		

Table 109. PIO10 alternate functions (continued)

PIO10	Config register: Not required			
	Config bus: Not required			
PIN	**Parameter**	**Alternate 1**	**Alternate 2**	**Alternate 3**
		Digital audio output 0, SPDIF I/F, Audio digital input 0		
PIO10[4]	Name	AUDDIG0_PCM_OUT_LRCLK		
	Description	PCMOUT0 - LRCLK		
	Direction	O		
	Configuration	Not required		
PIO10[5]	Name	AUDDIG0_PCM_OUT_SCLK		
	Description	PCMOUT0 - SCLK		
	Direction	O		
	Configuration	Not required		
PIO10[6]	Name	AUD_SPDIF_OUT		
	Description	SPDIF out		
	Direction	O		
	Configuration	Not required		
PIO10[7]	Name	AUDDIG0_PCM_DATAIN/AUDDIG1_PCM_OUT_DATA0		
	Description	PCMIN0/PCMOUT1 - data		
	Direction	I/O		
	Configuration	Not required		

19.13 PIO11 alternate functions

PIO11 is PIO4 on GPIO standalone block. It provides:

- stereo digital audio PCM input AUD0PCMIN
- stereo digital audio PCM output AUD1PCMOUT

Note: PIO11 alternate function is controlled by SYS_CFG5[29]

Table 110. PIO11 alternate functions

PIO11	**Config register: Not required**			
	Config bus: Not required			
PIN	**Parameter**	**Alternate 1**	**Alternate 2**	**Alternate 3**
		Digital audio input 0	**Genlock**	
PIO11[0]	Name	AUDDIG0_PCM_STRBIN/AUDDIG1_PCM_OUT_LRCLK		
	Description	PCMIN0 - SCLK/PCMOUT1 - LRCLK		
	Direction	I/O		
	Configuration	Not required		
PIO11[1]	Name	AUDDIG0_PCM_LRCLKIN/AUDDIG1_PCM_OUT_SCLK		
	Description	PCMIN0 - LRCLK/PCMOUT1 - SCLK		
	Direction	I/O		
	Configuration	Not required		
PIO11[2]	Name			
	Description			
	Direction			
	Configuration			
PIO11[3]	Name			
	Description			
	Direction			
	Configuration			

Table 110. PIO11 alternate functions (continued)

PIO11	Config register: Not required			
	Config bus: Not required			
PIN	**Parameter**	**Alternate 1**	**Alternate 2**	**Alternate 3**
		Digital audio input 0	**Genlock**	
PIO11[4]	Name			
	Description			
	Direction			
	Configuration			
PIO11[5]	Name		PIXCLK_FROM_PAD	
	Description		Genlock	
	Direction		I	
	Configuration		Not required	
PIO11[6]	Name		VSYNC_FROM_PAD	
	Description		Genlock	
	Direction		I	
	Configuration		Not required	
PIO11[7]	Name		HSYNC_FROM_PAD	
	Description		Genlock	
	Direction		I	
	Configuration		Not required	

19.14 PIO12 alternate functions

PIO12 is PIO5 on GPIO standalone block. It provides:

- second transport input TSIN1
- transport output TSOUT
- SSC2 interface with I2C half-duplex modes selectable
- UART2 interface
- USB1 power control
- fourth transport input TSIN3 (serial only)

Table 111. PIO12 alternate functions

PIO12	Config register: SYSTEM_CONFIG48[23:0]						
	Config bus: PIO12_ALTFOP[2:0]_MUX_SEL_BUS[7:0]						
PIN	**Parameter**	**Alternate 1**	**Alternate 2**	**Alternate 3**		**Alternate 4**	**Alternate 5**
		Transport stream input 1	**Transport stream input**	**SSC 2, USB 1 power ctrl**		**Transport stream input 3, UART2, SSC2**	**UART2**
PIO12[0]	Name	TSIN1SER/DATA[7]	TSOUTSER/DATA[7]	SSC2_SCL		SSC2_SCL	UART2_TXD
	Description	TS1 input	TS output	SSC2 serial clock in/out		SSC2 serial clock out	UART
	Direction	I	O	I/O		O	O
	Configuration	SYSTEM_CONFIG4[9]=0	SYSTEM_CONFIG48[16,8,0]=001	In: SYSTEM_CONFIG16[12,11]=10 Out: SYSTEM_CONFIG48[16,8,0]=010		SYSTEM_CONFIG48[16,8,0]=011	SYSTEM_CONFIG48[16,8,0]=100
PIO12[1]	Name	TSIN1BYTECLK	TSOUTBYTECLK	SSC2_MTSR	SSC2_MRST	UART2_RXD	
	Description	TS1 input	TS output	SSC2 Data bit: master transmit/slave receive, full duplex	SSC2 Data bit: master receive/slave transmit, full duplex	UART	
	Direction	I	I/O	I/O	I	I	
	Configuration	SYSTEM_CONFIG4[9]=0	In: Not required Out: SYSTEM_CONFIG48[17,9,1]=001	In: SYSTEM_CONFIG16[10,9]=10 Out: SYSTEM_CONFIG48[17,9,1]=010	SYSTEM_CONFIG16[8,7]=10	Not required	

Table 111. PIO12 alternate functions (continued)

PIO12	Config register: SYSTEM_CONFIG48[23:0]					
	Config bus: PIO12_ALTFOP[2:0]_MUX_SEL_BUS[7:0]					
PIN	**Parameter**	**Alternate 1**	**Alternate 2**	**Alternate 3**	**Alternate 4**	**Alternate 5**
		Transport stream input 1	**Transport stream input**	**SSC 2, USB 1 power ctrl**	**Transport stream input 3, UART2, SSC2**	**UART2**
PIO12[2]	Name	TSIN1BYECLKVALID	TSOUTBYTECLKVALID		UART2_CTS	
	Description	TS1 input	TS output		UART	
	Direction	I	O		I	
	Configuration	SYSTEM_CONFIG4[9]=0	SYSTEM_CONFIG48[18,10,2]=001		Not required	
PIO12[3]	Name	TSIN1ERROR	TSOUTERROR			UART2_RTS
	Description	TS1 input	TS output			UART
	Direction	I	O			O
	Configuration	SYSTEM_CONFIG4[9]=0	SYSTEM_CONFIG48[19,11,3]=001			SYSTEM_CONFIG48[19,11,3]=100
PIO12[4]	Name	TSIN1PACKETCLK	TSOUTPACKETCLK			
	Description	TS1 input	TS output			
	Direction	I	O			
	Configuration	SYSTEM_CONFIG4[9]=0	SYSTEM_CONFIG48[20,12,4]=001			
PIO12[5]	Name	TSIN1DATA[6]	TSOUTDATA[6]	USB1_PRT_OVCUR	TSIN3SER/DATA[7]	
	Description	TS1 input	TS output	USB 1 PRT overcurrent	TS3 input	
	Direction	I	O	I	I	
	Configuration	SYSTEM_CONFIG4[9]=0	SYSTEM_CONFIG48[21,13,5]=001	SYSTEM_CONFIG4[5]=1	Not required	
PIO12[6]	Name	TSIN1DATA[5]	TSOUTDATA[5]	USB1_PRT_PWR	TSIN3BYTECLK	
	Description	TS1 input	TS output	USB 1 PRT power	TS3 input	
	Direction	I	O	O	I	
	Configuration	SYSTEM_CONFIG4[9]=0	SYSTEM_CONFIG48[22,14,6]=001	SYSTEM_CONFIG48[22,14,6]=010	Not required	

Table 111. PIO12 alternate functions (continued)

PIO12	Config register: SYSTEM_CONFIG48[23:0]					
	Config bus: PIO12_ALTFOP[2:0]_MUX_SEL_BUS[7:0]					
PIN	**Parameter**	**Alternate 1**	**Alternate 2**	**Alternate 3**	**Alternate 4**	**Alternate 5**
		Transport stream input 1	**Transport stream input**	**SSC 2, USB 1 power ctrl**	**Transport stream input 3, UART2, SSC2**	**UART2**
PIO12[7]	Name	TSIN1DATA[4]	TSOUTDATA[4]		TSIN3BYTECLKVALID	
	Description	TS1 input	TS output		TS3 input	
	Direction	I	O		I	
	Configuration	SYSTEM_CONFIG4[9]=0	SYSTEM_CONFIG48[23,15,7]=001		Not required	

19.15 PIO13 alternate functions

PIO13 is PIO6 on GPIO standalone block. It provides:

- second transport input TSIN1
- first transport input TSIN0
- fourth transport input TSIN3 (serial only)
- transport output TSOUT
- pulse width modulator interface PWM
- SSC2 and SSC3 interfaces with I2C half-duplex modes selectable

Table 112. PIO13 alternate functions

PIO13	Config register: SYSTEM_CONFIG49[23:0]					
	Config bus: PIO13_ALTFOP[2:0]_MUX_SEL_BUS[7:0]					
PIN	**Parameter**	**Alternate 1**	**Alternate 2**	**Alternate 3**	**Alternate 4**	**Alternate 5**
		Transport stream input 0,1	**Transport stream output, ssc 2,3**	**Transport stream output, ssc 3**	**Transport stream input 3, PWM 0,1**	**PWM 0,1, SSC3**
PIO13[0]	Name	TSIN1DATA[3]	TSOUTDATA[3]	TSOUTDATA[3]	TSIN3ERROR/PWM_OUT0	PWM_OUT0
	Description	TS1 input	TS output	TS output	TS3 input/PWM out	PWM out
	Direction	I	O	O	I/O	O
	Configuration	Not required	SYSTEM_CONFIG49[16,8,0]=001	SYSTEM_CONFIG49[16,8,0]=010	In: Not required Out: SYSTEM_CONFIG49[16,8,0]=011	SYSTEM_CONFIG49[16,8,0]=100
PIO13[1]	Name	TSIN1DATA[2]	TSOUTDATA[2]	TSOUTDATA[2]	TSIN3PACKETCLK/PWM_OUT1	PWM_OUT1
	Description	TS1 input	TS output	TS output	TS3 input	PWM out
	Direction	I	O	O	I/O	O
	Configuration	Not required	SYSTEM_CONFIG49[17,9,1]=001	SYSTEM_CONFIG49[17,9,1]=010	In: Not required Out: SYSTEM_CONFIG49[17,9,1]=011	SYSTEM_CONFIG49[17,9,1]=100

Table 112. PIO13 alternate functions (continued)

PIO13	Config register: SYSTEM_CONFIG49[23:0]					
	Config bus: PIO13_ALTFOP[2:0]_MUX_SEL_BUS[7:0]					
PIN	**Parameter**	**Alternate 1**	**Alternate 2**	**Alternate 3**	**Alternate 4**	**Alternate 5**
		Transport stream input 0,1	**Transport stream output, ssc 2,3**	**Transport stream output, ssc 3**	**Transport stream input 3, PWM 0,1**	**PWM 0,1, SSC3**
PIO13[2]	Name	TSIN1DATA[1]	TSOUTDATA[1]	SSC3_SCL/TSOUTDATA[1]	SSC3_SCL	SSC3_SCL
	Description	TS1 input	TS output	SSC3 input/TS output	SSC3 output	SSC3 output
	Direction	I	O	I/O	O	O
	Configuration	Not required	SYSTEM_CONFIG49[18,10,2]=001	In: SYSTEM_CONFIG16[19:18]=10 Out: SYSTEM_CONFIG49[18,10,2]=010	SYSTEM_CONFIG49[18,10,2]=011	SYSTEM_CONFIG49[18,10,2]=100
PIO13[3]	Name	TSIN1DATA[0]	TSOUTDATA[0]	SSC3_MTSR/SSC3_MRST/TSOUTDATA[0]	SSC3_MTSR	SSC3_MTSR
	Description	TS1 input	TS output	SSC3 Data bit: master transmit/slave receive, full duplex/TS output	SSC3 Data bit: master receive/slave transmit, full duplex	
	Direction	I	O	I/O	O	O
	Configuration	Not required	SYSTEM_CONFIG49[19,11,3]=001	In: SYSTEM_CONFIG16[17,16]=10/ SYSTEM_CONFIG16[15,14]=10 Out: SYSTEM_CONFIG49[19,11,3]=010	SYSTEM_CONFIG49[19,11,3]=011	SYSTEM_CONFIG49[19,11,3]=100
PIO13[4]	Name	TSIN0SER/DATA[7]	SSC2_SCL	SSC2_SCL		
	Description	TS0 input	SSC2 serial clock in/out	SSC2 serial clock out		
	Direction	I	I/O	O		
	Configuration	Not required	In: SYSTEM_CONFIG16[12,11]=11 Out: SYSTEM_CONFIG49[20,12,4]=001	SYSTEM_CONFIG49[20,12,4]=010		

Table 112. PIO13 alternate functions (continued)

PIO13	Config register: SYSTEM_CONFIG49[23:0]						
	Config bus: PIO13_ALTFOP[2:0]_MUX_SEL_BUS[7:0]						
PIN	**Parameter**	**Alternate 1**	**Alternate 2**		**Alternate 3**	**Alternate 4**	**Alternate 5**
		Transport stream input 0,1	**Transport stream output, ssc 2,3**		**Transport stream output, ssc 3**	**Transport stream input 3, PWM 0,1**	**PWM 0,1, SSC3**
PIO13[5]	Name	TSIN0BYTECLK	SSC2_MTSR	SSC2_MRST	SSC2_MRST		
	Description	TS input	SSC2 Data bit: master transmit/slave receive, full duplex	SSC2 Data bit: master receive/slave transmit, full duplex			
	Direction	I/O	I/O	I	O		
	Configuration	In: Not required Out: SYSTEM_CONFIG49[21,13,5]=000	In SYSTEM_CONFIG16[10,9]=11 Out: SYSTEM_CONFIG49[21,13,5]=001	SYSTEM_CONFIG16[8,7]=11	SYSTEM_CONFIG49[21,13,5]=010		
PIO13[6]	Name	TSIN0BYTECLKVALID	SSC3_SCL		SSC3_SCL		
	Description	TS0 input	SSC3 serial clock in/out		SSC3 serial clock out		
	Direction	I	I/O		O		
	Configuration	Not required	In: SYSTEM_CONFIG16[19,18]=11 Out: SYSTEM_CONFIG49[22,14,6]=001		SYSTEM_CONFIG49[22,14,6]=010		

Table 112. PIO13 alternate functions (continued)

PIO13	Config register: SYSTEM_CONFIG49[23:0]						
	Config bus: PIO13_ALTFOP[2:0]_MUX_SEL_BUS[7:0]						
PIN	**Parameter**	**Alternate 1**	**Alternate 2**		**Alternate 3**	**Alternate 4**	**Alternate 5**
		Transport stream input 0,1	**Transport stream output, ssc 2,3**		**Transport stream output, ssc 3**	**Transport stream input 3, PWM 0,1**	**PWM 0,1, SSC3**
PIO13[7]	Name	TSIN0ERROR	SSC3_MTSR	SSC3_MRST	SSC3_MRST		
	Description	TS0 input	SSC3 Data bit: master transmit/slave receive, full duplex	SSC3 Data bit: master receive/slave transmit, full duplex	SSC3 Data bit: master receive/slave transmit, full duplex		
	Direction	I	I/O	I	O		
	Configuration	Not required	In: SYSTEM_CONFIG16[17,16]=11 Out: SYSTEM_CONFIG49[23,15,7]=001	SYSTEM_CONFIG16[15,14]=11	SYSTEM_CONFIG49[23,15,7]=010		

19.16 PIO14 alternate functions

PIO14 is PIO7 on GPIO standalone block. It provides:

- first transport input TSIN0
- third transport input in serial mode only TSIN2 (serial only)
- USB2 power control

Table 113. PIO14 alternate functions

PIO14	Config register: Not required					
	Config bus: Not required					
PIN	**Parameter**	**Alternate 1**	**Alternate 2**	**Alternate 3**	**Alternate 4**	**Alternate 5**
		Transport stream input 0	**Transport stream input 2, USB 2 power ctrl**			
PIO14[0]	Name	TSIN0PACKETCLK				
	Description	TS 0 input				
	Direction	I				
	Configuration	Not required				
PIO14[1]	Name	TSIN0DATA[6]	TSIN2SER/DATA[7]			
	Description	TS 0 input	TS 2 input			
	Direction	I	I			
	Configuration	Not required	SYSTEM_CONFIG4[10]=1			
PIO14[2]	Name	TSIN0DATA[5]	TSIN2BYTECLK			
	Description	TS 0 input	TS 2 input			
	Direction	I	I			
	Configuration	Not required	In: SYSTEM_CONFIG4[10]=1			
PIO14[3]	Name	TSIN0DATA[4]	TSIN2BYTECLKVALID			
	Description	TS 0 input	TS 2 input			
	Direction	I	I			
	Configuration	Not required	SYSTEM_CONFIG4[10]=1			

Table 113. PIO14 alternate functions (continued)

PIO14	Config register: Not required					
	Config bus: Not required					
PIN	**Parameter**	**Alternate 1**	**Alternate 2**	**Alternate 3**	**Alternate 4**	**Alternate 5**
		Transport stream input 0	**Transport stream input 2, USB 2 power ctrl**			
PIO14[4]	Name	TSIN0DATA[3]	TSIN2ERROR			
	Description	TS 0 input	TS 2 input			
	Direction	I	I			
	Configuration	Not required	SYSTEM_CONFIG4[10]=1			
PIO14[5]	Name	TSIN0DATA[2]	TSIN2PACKETCLK			
	Description	TS 0 input	TS 2 input			
	Direction	I	I			
	Configuration	Not required	SYSTEM_CONFIG4[10]=1			
PIO14[6]	Name	TSIN0DATA[1]	USB2_PRT_OVCUR			
	Description	TS 0 input	USB2 PRT overcurrent			
	Direction	I	I			
	Configuration	Not required	SYSTEM_CONFIG4[10]=1			
PIO14[7]	Name	TSIN0DATA[0]	USB2_PRT_PWR			
	Description	TS 0 input	USB2 PRT power			
	Direction	I	O			
	Configuration	Not required	Not required			

19.17 PIO15 alternate functions

PIO15 is PIO8 on GPIO standalone block. It provides:

- SPI boot interface
- EMI SS arbiter signals/PCI support
- PCI interface

Table 114. PIO15 alternate functions

PIO15	Config register: SYSTEM_CONFIG50[15:0]				
	Config bus: PIO15_ALTFOP[1:0]_MUX_SEL_BUS[7:0]				
PIN	**Parameter**	**Alternate 1**	**Alternate 2**	**Alternate 3**	**Alternate 4**
		Serial peripheral I/F	**Transport stream input 1**	**PCI I/F, EMI I/F**	
PIO15[0]	Name	SPIBOOT_CLOCK	TSIN1PACKETCLK		
	Description	SPI	TS1 input		
	Direction	O	I		
	Configuration	SYSTEM_CONFIG50[8,0]=00	SYSTEM_CONFIG4[9]=1		
PIO15[1]	Name	SPIBOOT_DATA_OUT	TSIN1BYTECLK		
	Description	SPI	TS1 input		
	Direction	O	I		
	Configuration	SYSTEM_CONFIG50[9,1]=00	SYSTEM_CONFIG4[9]=1		
PIO15[2]	Name	SPIBOOT_CS	TSIN1BYTECLKVALID	EMI_SS_BUS_FREE_ACCESSPEND/EMI_SS_BUS_FREE_OUT	EMI_SS_BUS_FREE_OUT
	Description	SPI	TS1 input	EMI I/F	EMI I/F
	Direction	O	I	I/O	O
	Configuration	SYSTEM_CONFIG50[10,2]=00	SYSTEM_CONFIG4[9]=1	In: Not required Out: SYSTEM_CONFIG50[10,2]=10	SYSTEM_CONFIG50[10,2]=11

Table 114. PIO15 alternate functions (continued)

PIO15	Config register: SYSTEM_CONFIG50[15:0]				
	Config bus: PIO15_ALTFOP[1:0]_MUX_SEL_BUS[7:0]				
PIN	**Parameter**	**Alternate 1**	**Alternate 2**	**Alternate 3**	**Alternate 4**
		Serial peripheral I/F	**Transport stream input 1**	**PCI I/F, EMI I/F**	
PIO15[3]	Name	SPIBOOT_DATA_IN	TSIN1ERROR	PCI_INT_FROM_DEVICE[0]/PCI_INT_TO_HOST	PCI_INT_TO_HOST
	Description	SPI	TS1 input	PCI host/device	PCI Host
	Direction	I	I	I/O	O
	Configuration	Not required	SYSTEM_CONFIG4[9]=1	In: SYSTEM_CONFIG5[27]=1 Out: SYSTEM_CONFIG50[11,3]=10	SYSTEM_CONFIG50[11,3]=11
PIO15[4]	Name		TSIN1SER/DATA[7]	PCI_SYSTEM_ERROR	PCI_SYSTEM_ERROR
	Description		TS1 input	PCI Host/device	PCI Host/device
	Direction		I	I/O	O
	Configuration		SYSTEM_CONFIG4[9]=1	In: Not required Out: SYSTEM_CONFIG50[12,4]=10	SYSTEM_CONFIG50[12,4]=11
PIO15[5]	Name			PCI_LOCK_IN	
	Description			PCI Host/device	
	Direction			I	
	Configuration			SYSTEM_CONFIG5[25]=1	
PIO15[6]	Name			PCI_PME_IN	
	Description			PCI Host/device	
	Direction			I	
	Configuration			Not required	
PIO15[7]	Name			PCI_RESETN_FROM_HOST_TO_DEVICE	
	Description			PCI Host/device	
	Direction			I	
	Configuration			Not required	

19.18 PIO16 alternate functions

PIO16 is PIO9 on GPIO standalone block. It provides:

- MPEG recovered clock

Note: During reset PIO16[6:0] is in input mode for mode pin capture.

Table 115. PIO16 alternate functions

PIO16	Config register:Not required		
	Config bus:Not required		
		Alternate 1	Alternate 2
PIO16[0]	Name	RESERVED	RESERVED
	Description	RESERVED	RESERVED
	Direction	RESERVED	RESERVED
	Configuration	RESERVED	RESERVED
PIO16[1]	Name	RESERVED	RESERVED
	Description	RESERVED	RESERVED
	Direction	RESERVED	RESERVED
	Configuration	RESERVED	RESERVED
PIO16[2]	Name	RESERVED	RESERVED
	Description	RESERVED	RESERVED
	Direction	RESERVED	RESERVED
	Configuration	RESERVED	RESERVED
PIO16[3]	Name	RESERVED	RESERVED
	Description	RESERVED	RESERVED
	Direction	RESERVED	RESERVED
	Configuration	RESERVED	RESERVED
PIO16[4]	Name	RESERVED	RESERVED
	Description	RESERVED	RESERVED
	Direction	RESERVED	RESERVED
	Configuration	RESERVED	RESERVED

Table 115. PIO16 alternate functions (continued)

PIO16	Config register:Not required		
	Config bus:Not required		
		Alternate 1	**Alternate 2**
PIO16[5]	Name	RESERVED	RESERVED
	Description	RESERVED	RESERVED
	Direction	RESERVED	RESERVED
	Configuration	RESERVED	RESERVED
PIO16[6]	Name	RESERVED	RESERVED
	Description	RESERVED	RESERVED
	Direction	RESERVED	RESERVED
	Configuration	RESERVED	RESERVED
PIO16[7]	Name	MPEG_RECOVERED_CLOCK	
	Description	MPEG recovered clock	
	Direction	O	
	Configuration	Not required	

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21 Revision history

Table 116. Document revision history

Date	Revision	Changes
20-Feb-2009	Rev D	Changes: -- The *Figure 1* is updated. -- In *Figure 3*, STV6440AJ replaces the devices TSH94 & TSH110. -- In *Figure 33*, mux_2 is moved from TSIN2 path to TSIN3 path. -- The ClockGen B block diagram (*Figure 29*) is updated. -- The *SYSTEM_CONFIG5*(16) bit is made reserved. -- Pins and signal names with prefix USB0 and USB1 are changed to USB1 and USB2 respectively throughout in the datasheet. -- The *DEVICE_ID* register is updated for the reset value. -- The de-ringing feature is removed from the corresponding sections. -- The *SYSTEM_CONFIG16* register definition is updated. -- PIO tables for SSC2/SSc3 input configuration are updated. -- The *Figure 34*: *Oscillator recommended external circuitry* is updated. -- The *Table 32.: Pad reset conditions* is updated.
01-Dec-2008	Rev C	Changes: --PIO tables in *Chapter 19: Alternate functions on PIO* are updated. --References to TSOUT1 and TSOUT2 are removed from PIO tables. --The value of external resistors for VIDA0_REXT and VID1_REXT is changed to 7.81 kohm in *Section 6.5: Display analog output interface*. --Mention of DVO1HS/DVO1VS is swapped in *Chapter 19: Alternate functions on PIO*. Now, PIO3[0]=DVO1HS and PIO3[2]=DVO1VS --Mode pin 13 functionality to select 8/16 bits is chnaged to—0: 16 bits and 1: 8 bits—in *Chapter 13: Mode pins*. --Bit field description for Mode pin 0 is changed to —0: SYSCLKINALT (Ext) and 1: Osc (SATA)—in *Chapter 13: Mode pins*. --16 H/W perfect match MAC address filters in *Chapter 3.14.2: Ethernet controller* is changed to 32 H/W perfect match MAC address filters. --SYSCLKIN and SYSCLKOSC pins are changed to 2.5 V in *Table 5*. -- Updated electrostatic discharge voltage V_{ESD_HBM} (HBM modem) in *Section 17.1: Absolute maximum ratings on page 242*.

Table 116. Document revision history (continued)

Date	Revision	Changes
22-Aug-2008	Rev B	Major changes: --Added Interrupt network, FDMA, system config, Low power mode, and Clocking chapters. --Renamed AF22 ball to GNDSATA instead of USB_GND1V2 in *Figure 17.: Bottom-right quadrant*, *Table 3.: Pin list*, and *Table 4.: Power/ground pins*. --Mentioned Dwight Cavendish for HDTV video output in *3.10.1: Main HDTV video output* section. --Output Enable column is removed from *6.17: Pad reset conditions* section of the connection chapter. --In *Figure 34.: Oscillator recommended external circuitry* of *16.2: System* section, CL1 and CL2 are connected to GND not vdd2v5. --In *11.6.2: Reference clock*, the reset value is sysclkaltin. --SBAG I/F information is removed from the datasheet due to security constraints. --The *Chapter 16.1.2: Power-up recommendations* section is updated by deleting the power-up sequence, and specifying no specific power-up sequence in STi7105.
01-Jul-2008	Rev A	Initial release

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