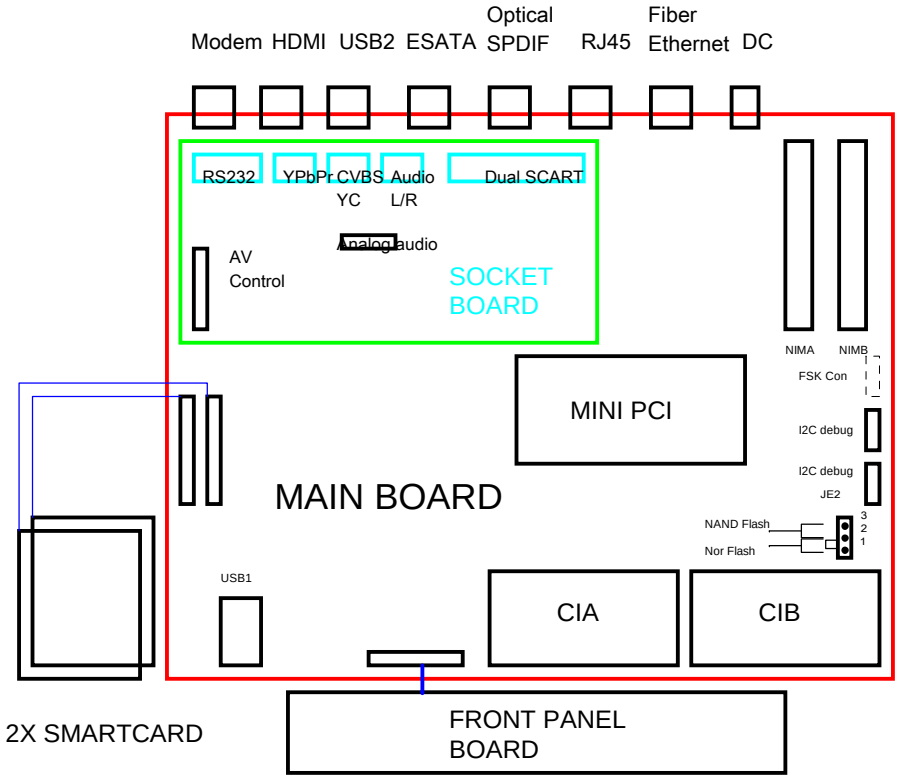
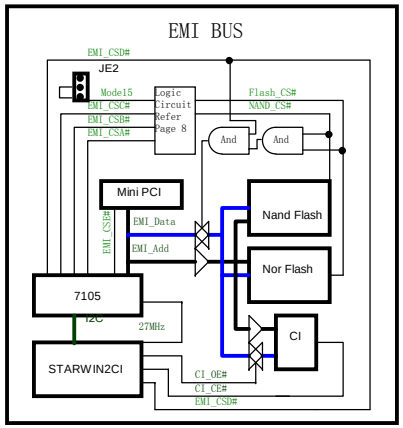
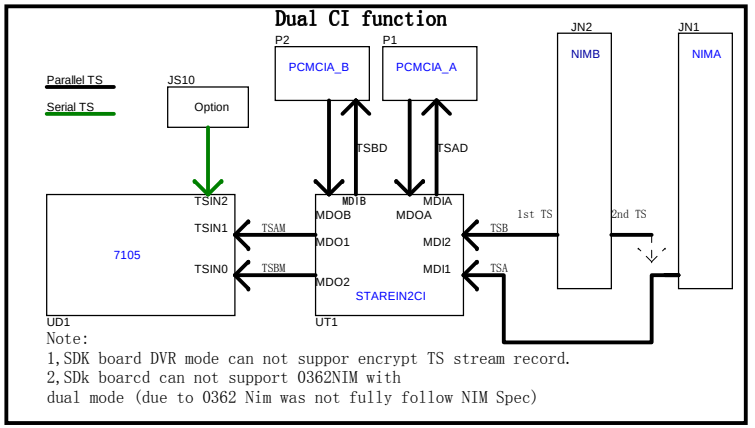
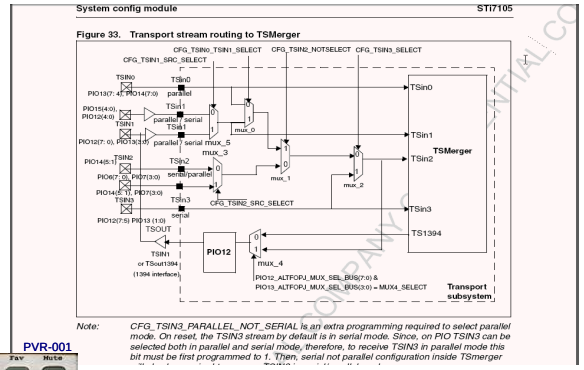
STi7105-SDK BOARD BUILDUP / OVERVIEW

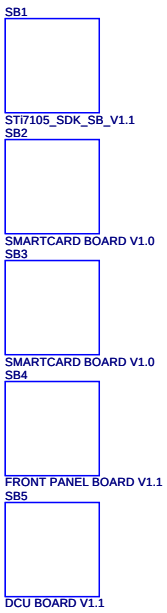


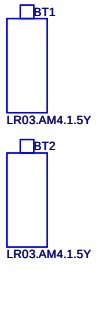


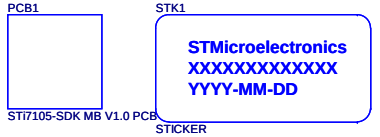


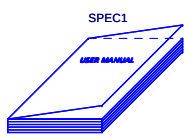


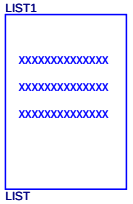
SOCKET BOARD COMPONENTS

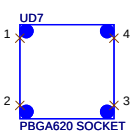


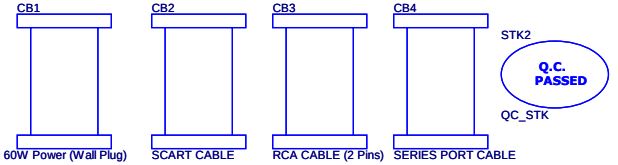


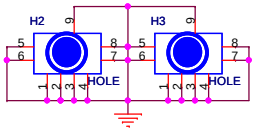


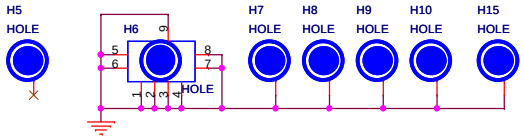


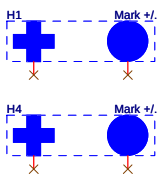


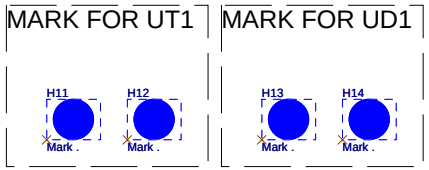












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V1.2	18/02/09	Xin.ZHANG	Improvement	
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V1.1	18/10/08	Xin.ZHANG	Updated	
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Sheet TOP

Project SDK-7105 Main Board

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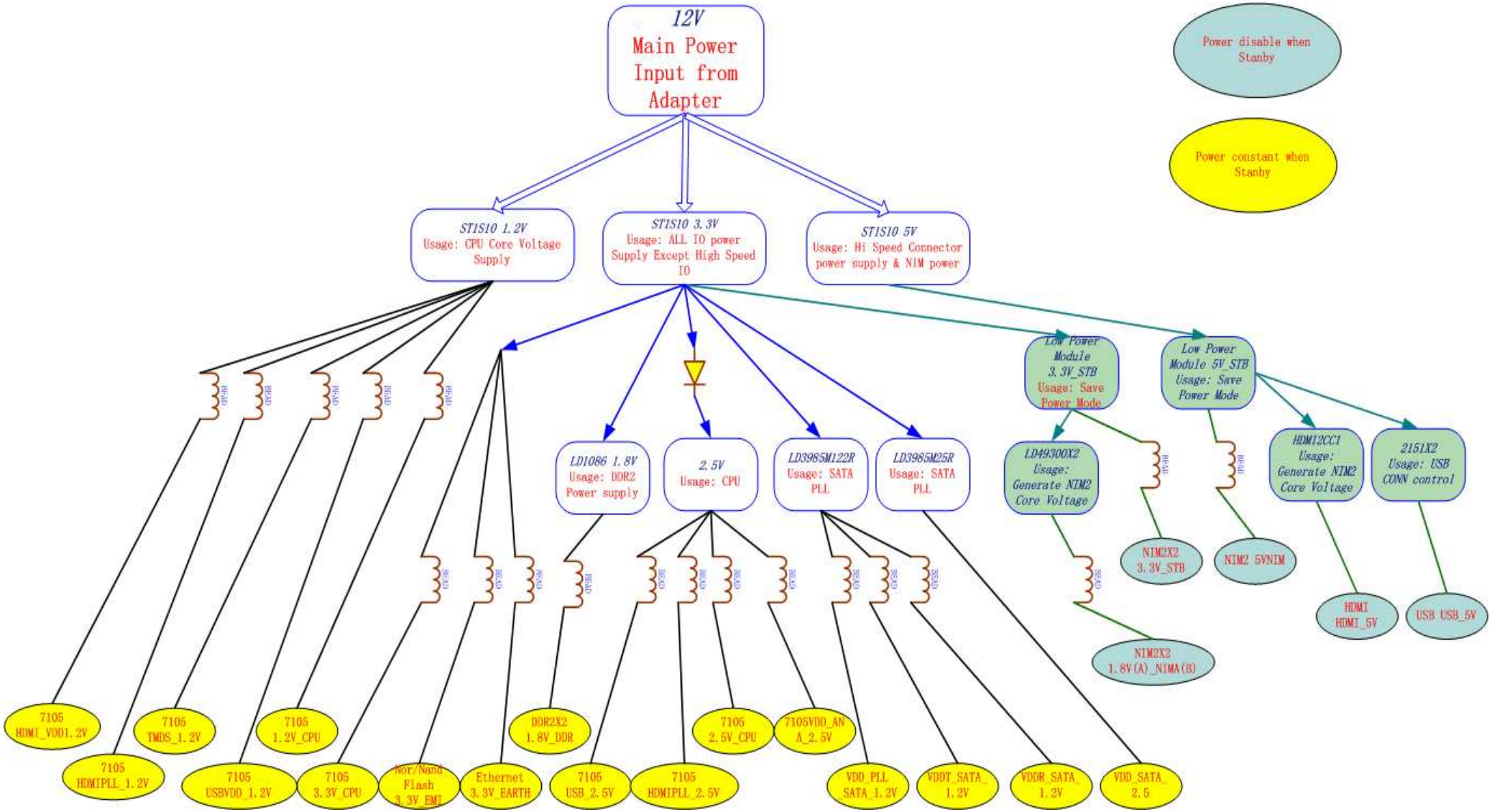
Need Updated !!!



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Sheet Power Distribution

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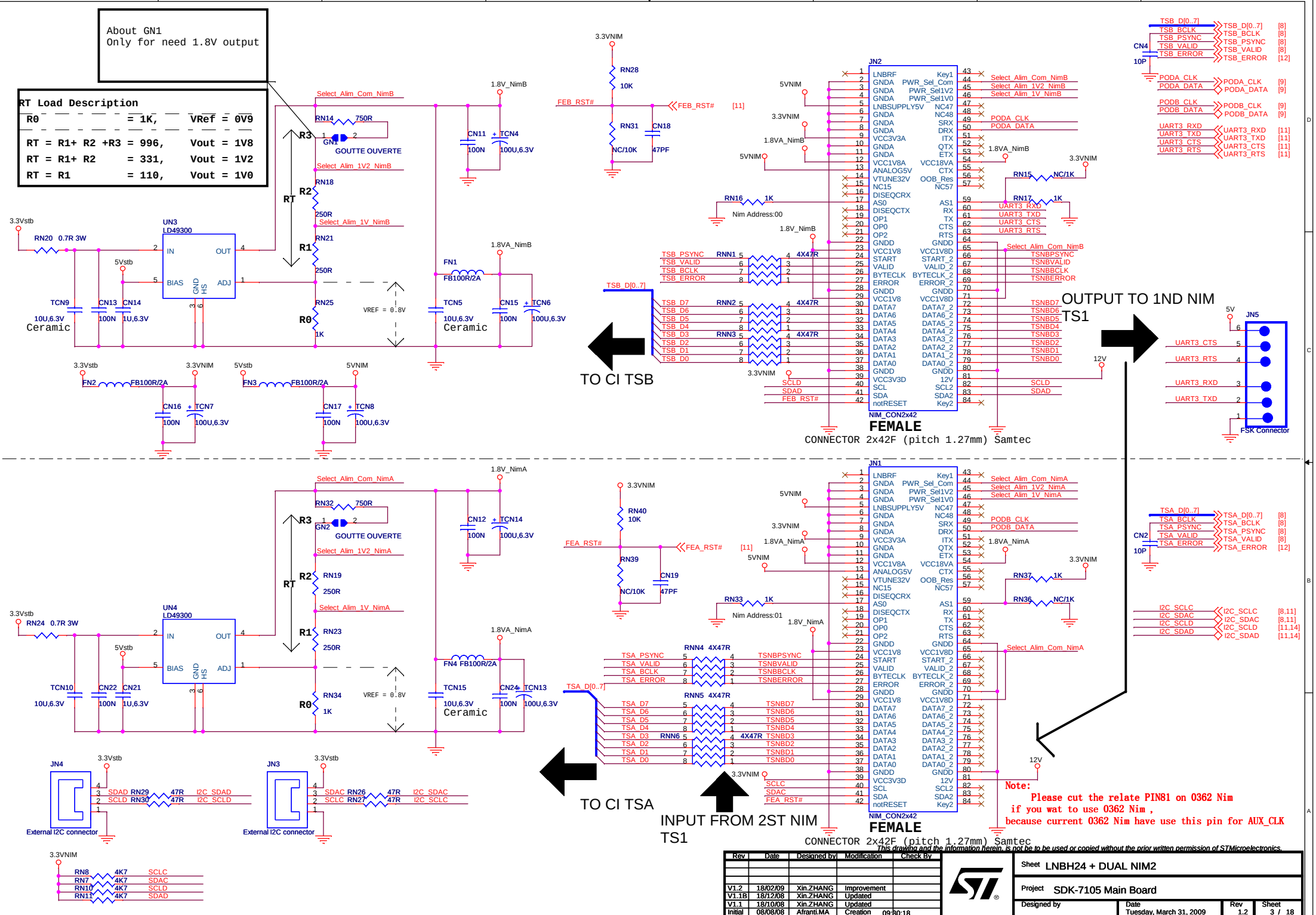
	Friday, March 27, 2009	1.2	2 / 18

About GN1
Only for need 1.8V output

RT Load Description

R0	= 1K,	VRef = 0V9
RT = R1+ R2 +R3	= 996,	Vout = 1V8
RT = R1+ R2	= 331,	Vout = 1V2
RT = R1	= 110,	Vout = 1V0



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V1.1	18/10/08	Xin.ZHANG	Updated	
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Sheet LNBH24 + DUAL NIM2
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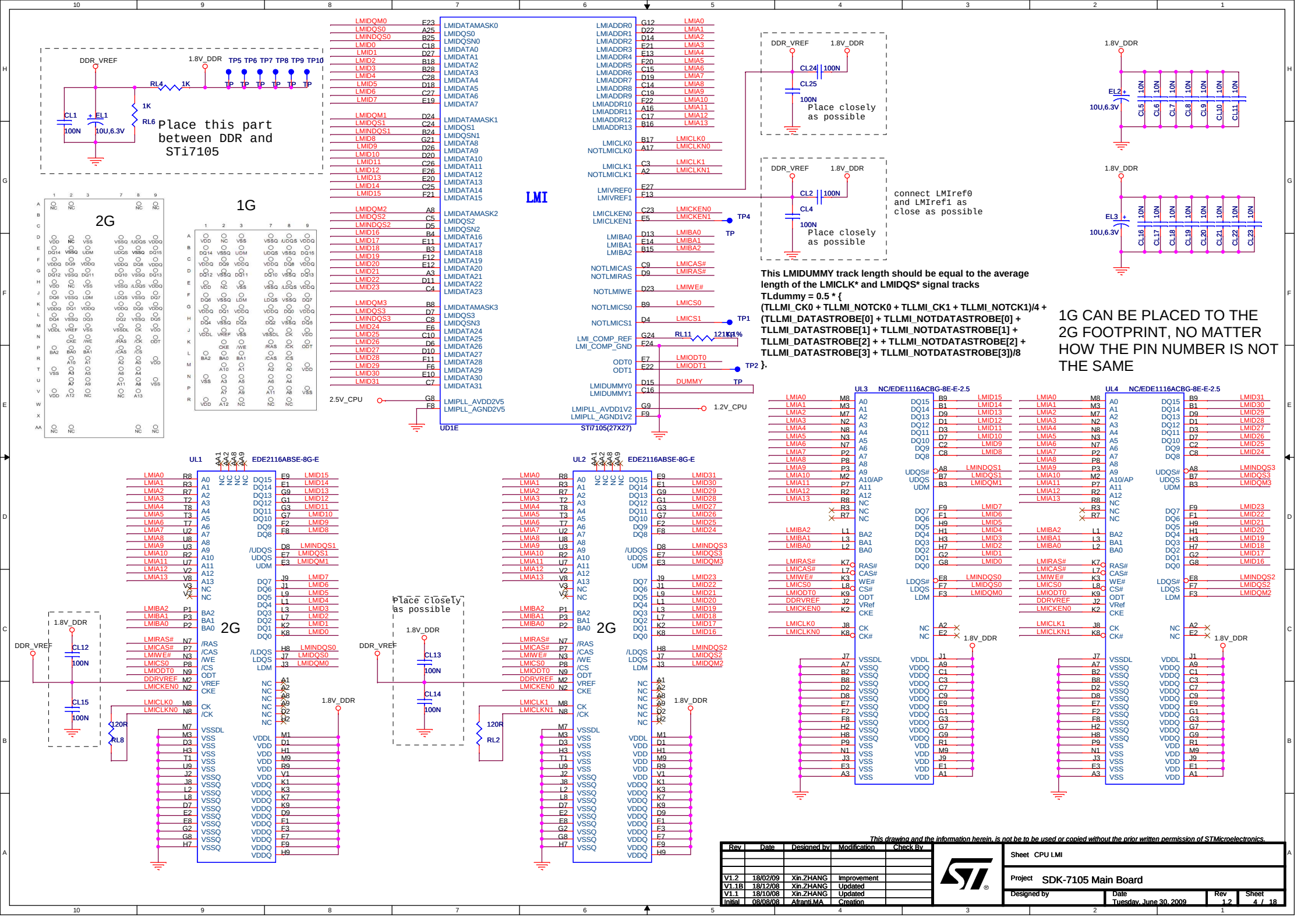

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V1.1	18/10/08	Xin.ZHANG	Updated	
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Sheet CPU LMI

Project SDK-7105 Main Board

Designed by	Date	Rev	Sheet
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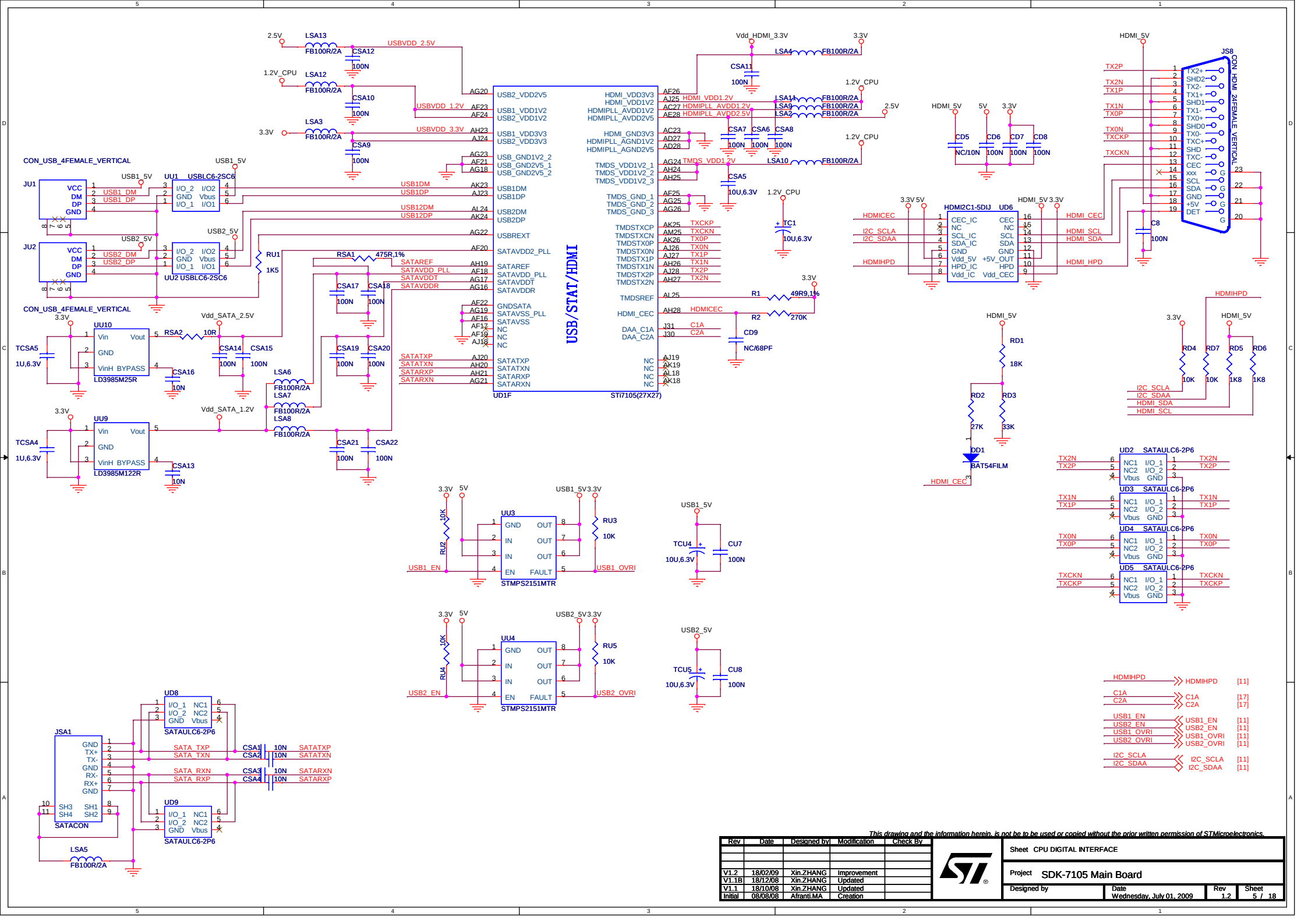

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Sheet CPU DIGITAL INTERFACE

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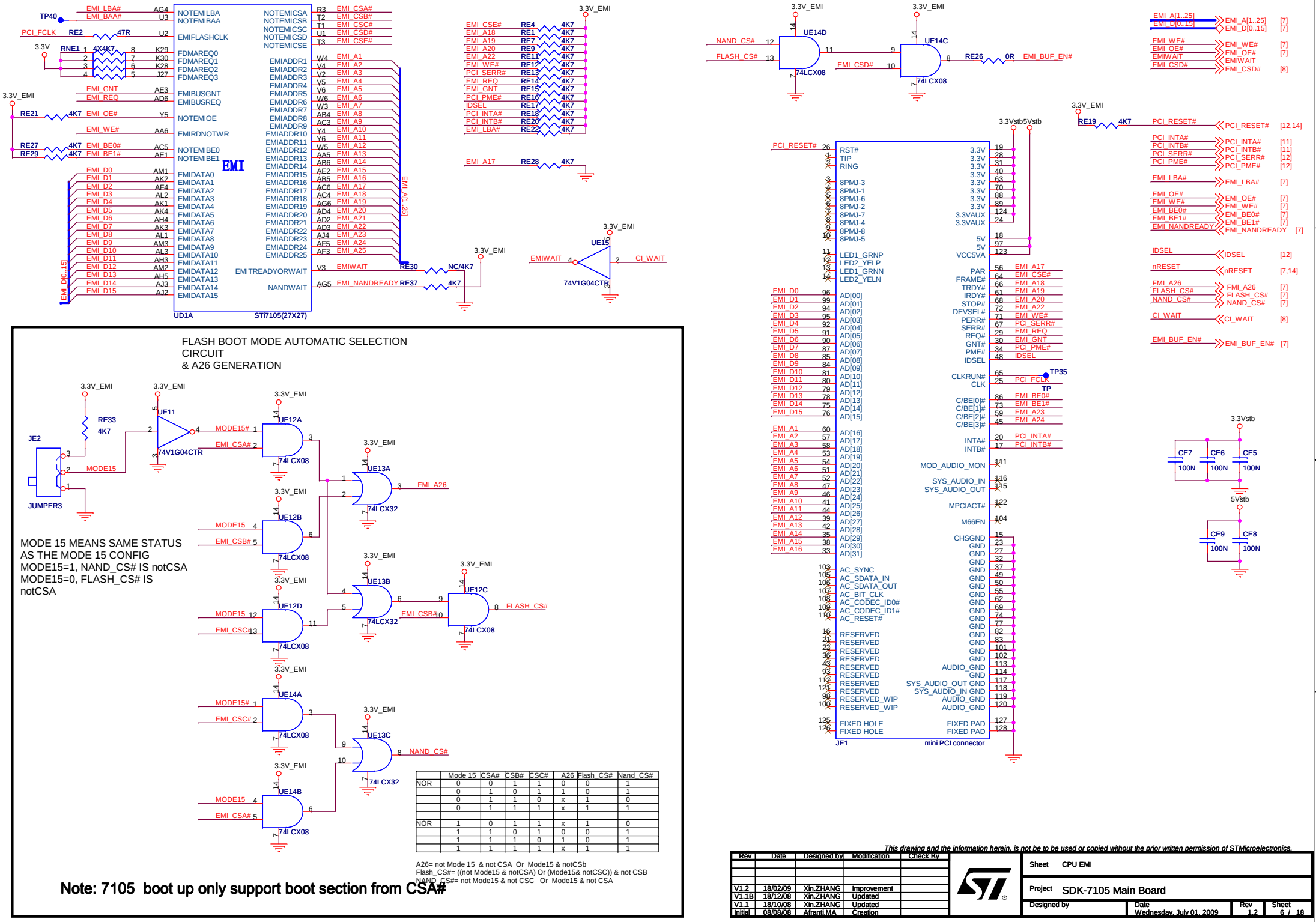

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V1.1	18/10/08	Xin.ZHANG	Updated	
Initial	08/08/08	Afranti.MA	Creation	

	Mode 15	CSA#	CSB#	CSC#	A26	Flash_CS#	Nand_CS#
NOR	0	0	1	1	0	0	1
	0	1	0	1	1	0	1
	0	1	1	0	x	1	0
	0	1	1	1	x	1	1
NOR	1	0	1	1	x	1	0
	1	1	0	1	0	0	1
	1	1	1	0	1	0	1
	1	1	1	1	x	1	1

ADDRESS

INPUT FROM MAIN CHIP

DATA

ADDRESS

OUTPUT TO NOR FLASH & NAND FLASHTHEN CI

DATA

74LCX245TTR UT12

74LCX245TTR UT13

74LCX245TTR UT14

74LCX245TTR UT19

74LCX245TTR UT20

74LCX245TTR UT21

MAIN BUFFERS TO EMI BUS

74LCX138

Table 2. Truth table

Inputs						Outputs							
Enable			Select										
G2B	G2A	G1	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	L	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
H	X	X	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

X : Do not care

3.3V_EMI

RE39 10K

FMI_WE# RE41 0R DIR

RE24&RE25 USED TO BOOT MODE FOR NAND

3.3V_EMI

NAND_CS_SEL1

NAND_CS_SEL2

RE24 4K7 RE25 4K7

NAND_CS#

C193 100N

UE4 74LCX138MTR

NAND_CS1

NAND_CS2

NAND_CS3

NAND_CS4

NAND CS EXTENSION CIRCUIT

UE3 S29GL01GP11FFCR20

FMI_A[1..25]

FMI_D[0..15]

BYTE# RE38 4K7

CE3 100N

WE#

OE#

CE#

WP#/ACC

RESET#

RY/BY#

CE4 100N

nRESET

RE36 4K7

EXCEPT Pin "D1", ALL THE OTHER NC PIN CAN BE USED FOR ROUTING

UE1 HY27UH08AG5B

UE2 HY27UH08AG5B

CE1 100N CE2 100N

CE10 100N CE11 100N

FMI_NANDREADY

2NAND FLASH COMBINED TO 16 BIT BUS WIDTH

EMI_A[1..25] EMI_D[0..15] [6]

FMI_A[1..25] FMI_D[0..15] [8,9]

EMI_BUF_EN# nRESET [6] [14]

FLASH_WP# [11]

NAND_CS_SEL1 NAND_CS_SEL2 FMI_A26 FLASH_CS# [11] [11] [6] [6]

NAND_CS# EMI_LBA# [6] [6]

EMI_OE# EMI_WE# EMI_BE0# EMI_BE1# EMI_NANDREADY [6] [6] [6] [6] [6]

FMI_OE# FMI_WE# FMI_BE1# [8] [8] [9]

FMI_BE1 IS THE LOWEST ADDRESS FOR CI

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Sheet EMI FLASH

Project SDK-7105 Main Board

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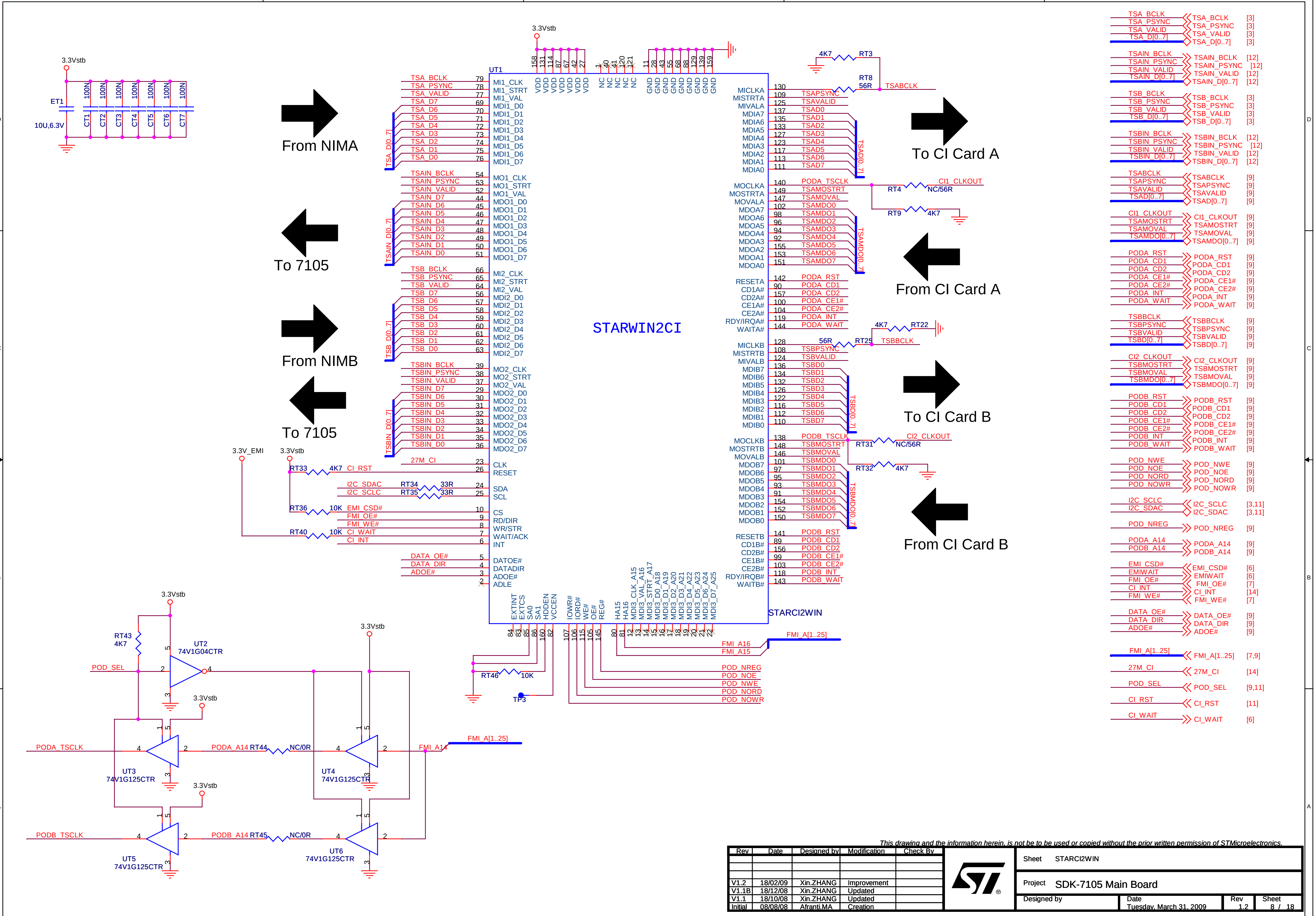

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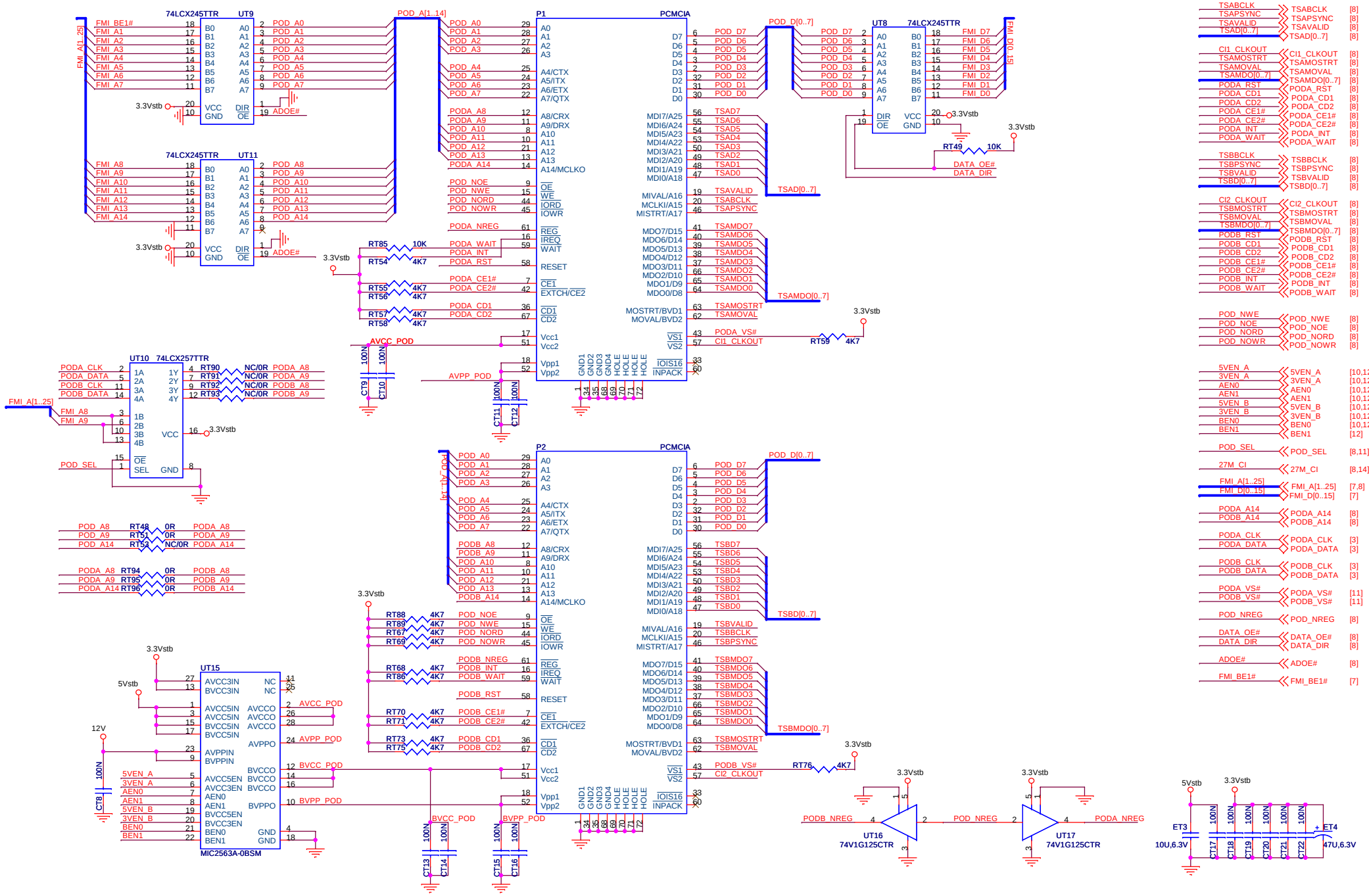
Initial	08/08/08	Afranti.MA	Creation	



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V1.1	18/10/08	Xin.ZHANG	Updated	
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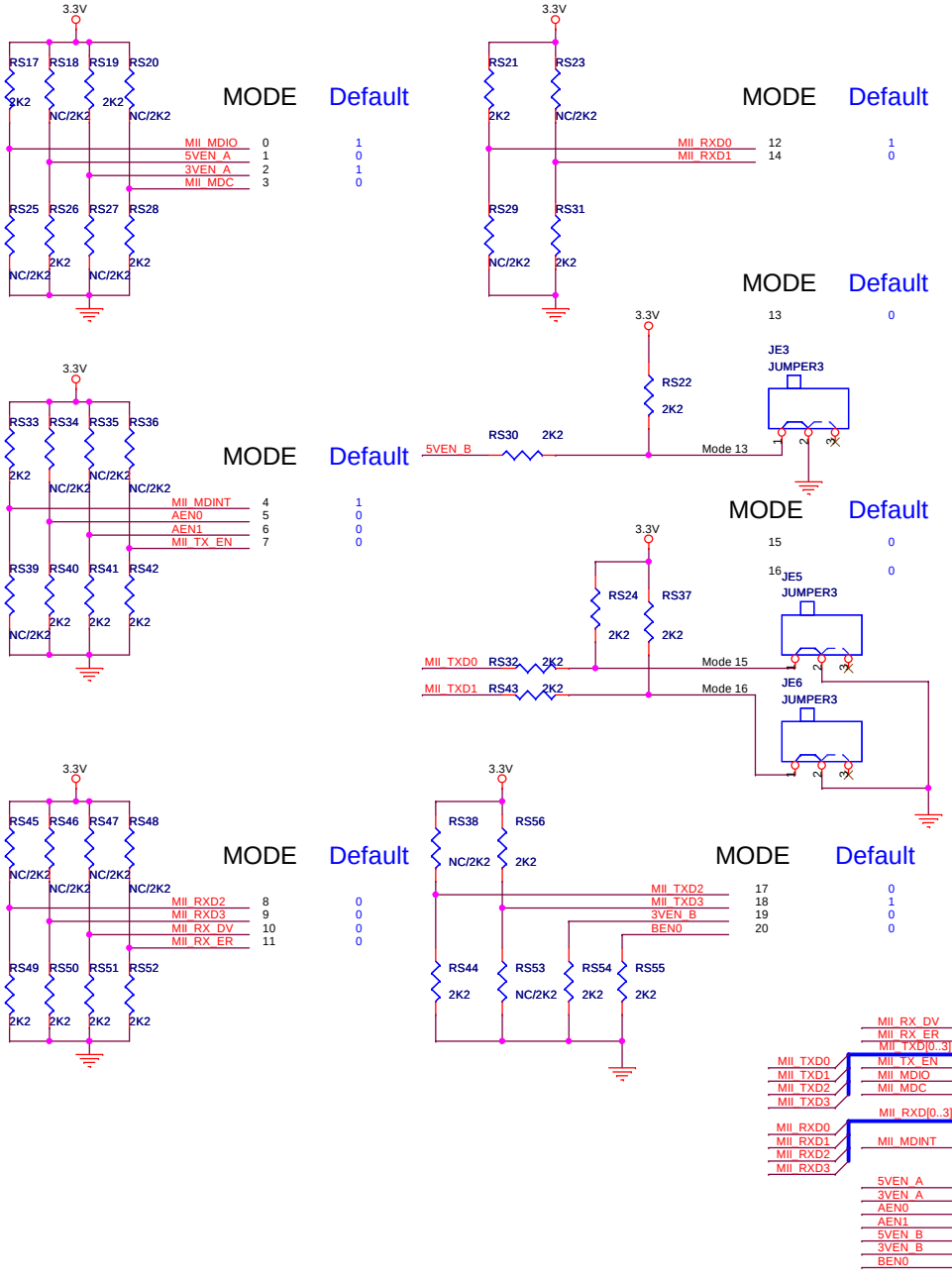
Sheet DUAL CI INTERFACE

Project SDK-7105 Main Board

Designed by | Date Tuesday, March 31, 2009 | Rev 1.2 | Sheet 9 / 18



Bit	Bit field	Controlled unit	Controlling Pad
MODE[0]	**Ref clock selection for Clockgen A** 0: SYSCLKINALT (Ext) 1: Osc (SATA)	ClockGen A	MIIMDIO [PIO8(3)]
MODE[2:1]	**PLL0 startup configuration**(1) 00: Fin/Fout–27/900 MHz 01: Fin/Fout–27/604.8 MHz 10: Fin/Fout–30/900 MHz 11: Fin/Fout–30/600 MHz	ClockGen A	[PIO16(1,0)]
MODE[4:3]	**PLL1 startup configuration**(1) 00: Fin/Fout–27/799.2 MHz 01: Fin/Fout–27/399.6 MHz 10: Fin/Fout–30/800 MHz 11: Fin/Fout–30/400 MHz	ClockGen A	MIIMDINT: MIIMDC [PIO9(6):PIO8(4)]
MODE[6:5]	**Reset bypasses**(2) CPU_RST_OUT_BYPASS[1]: bypass of (LX_Audio+LXDelphi) reset loop back CPU_RST_OUT_BYPASS[0]: bypass of (SH4+LX_Audio+LXDelphi) reset loop back	Reset generator	[PIO16(3:2)]
MODE[7]	**Resetout mode** (see SYSTEM_CONFIG9, long_reset_mode bit)(3)	Reset generator	MIITX_EN [PIO8(2)]
MODE[9:8]	**BOOT mode selection:** 00: SH4-300 boot first 01: ST231 DeltaMu boot first 10: ST231 Audio boot first	ST40, ST231 Audio, ST231 DeltaMu, request filtering	MIIRXD[3:2] [PIO9(1:0)]
MODE[10]	**Reserved** (Do not connect)	Reserved	MIIRX_DV [PIO7(4)]
MODE[11]	**nand_addr_short_not_long**(4)	Nand Controller	MIIRX_ER [PIO7(5)]
MODE[12]	**Serial Flash usage:** 0: ATMEL 1: ST Flash	EMI4	MIIRXD[0] PIO8(6)
MODE[13]	**Boot device port size at boot:** (4) 0: 16 bits 1: 8 bits	EMI4 and Nand Controller	[PIO16(4)]
MODE[14]	**emiss_slave_not_master**	EMI subsystem	MIIRXD[1] [PIO8(7)]
MODE[16:15]	**Boot Device:** 00: NOR Flash (EMI controller) 01: Nand Flash (Nand Controller) 10: Serial Flash (SPI controller) 11: MPX (EMI controller)	EMI subsystem	MIITXD[1:0] [PIO7(7:6)]
MODE[17]	**emiss_clock_slave_not_master**	EMI subsystem	MIITXD[2] [PIO8(0)]
MODE[18]	**nand_page_large_not_small**(4)	Nand Controller	MIITXD[3] [PIO8(1)]

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Sheet CPU MODE PINS

Project SDK-7105 Main Board

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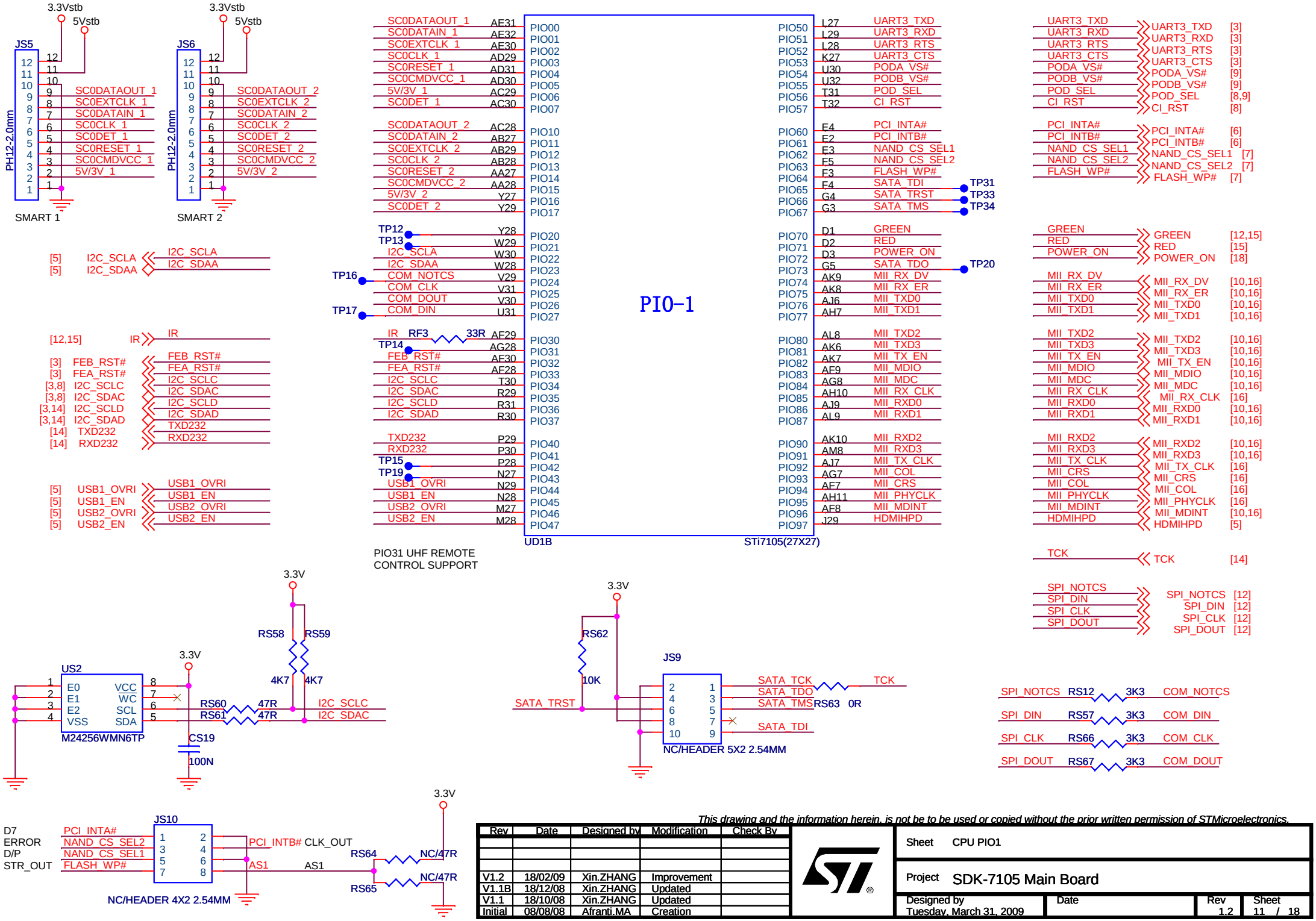

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Sheet CPU PIO1

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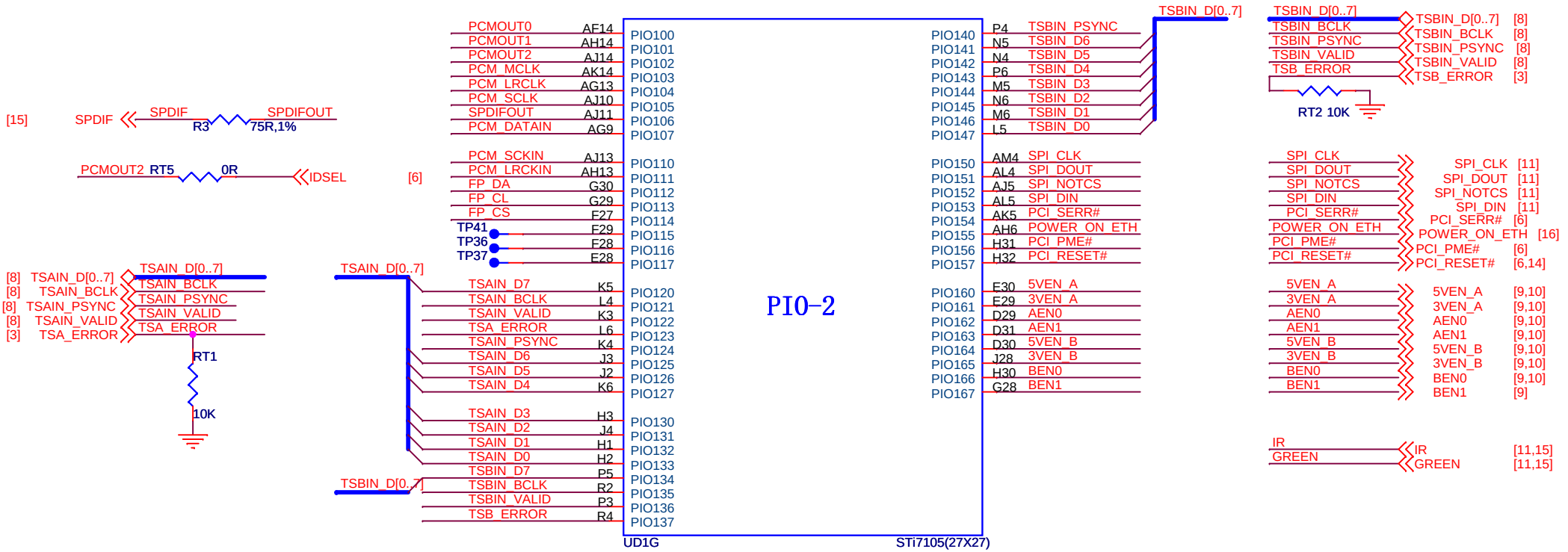

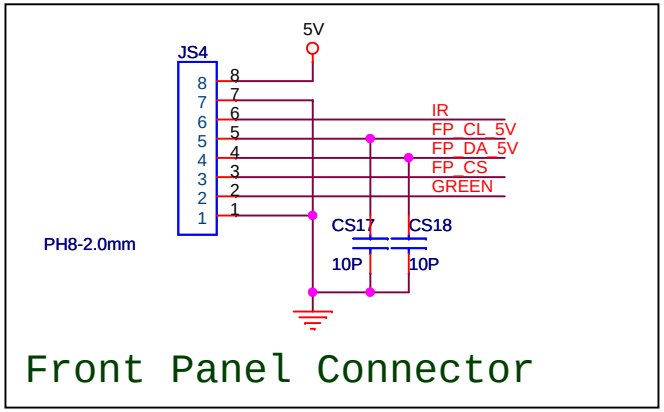

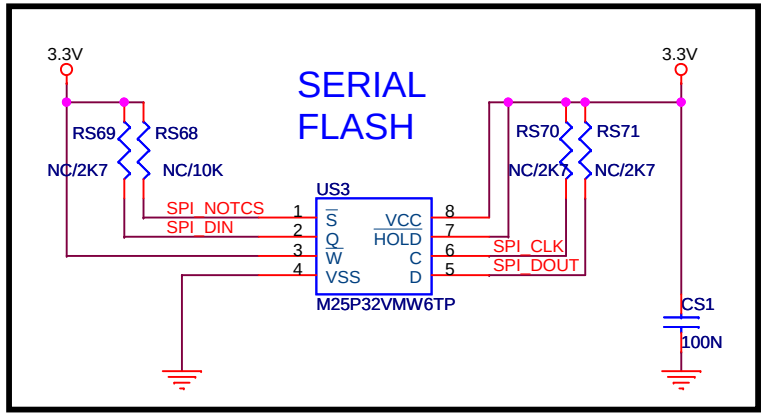

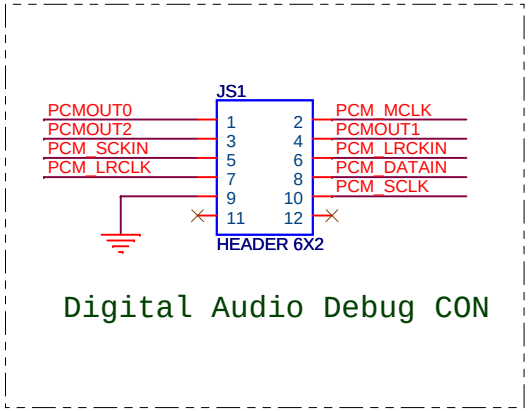

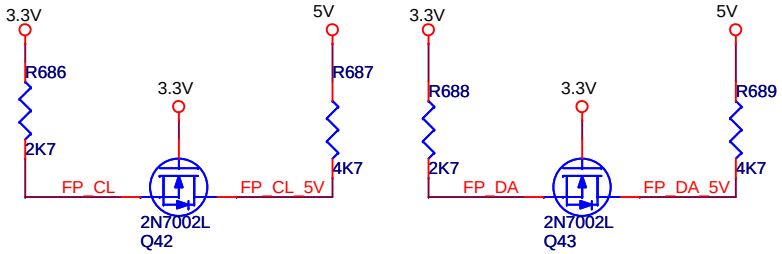

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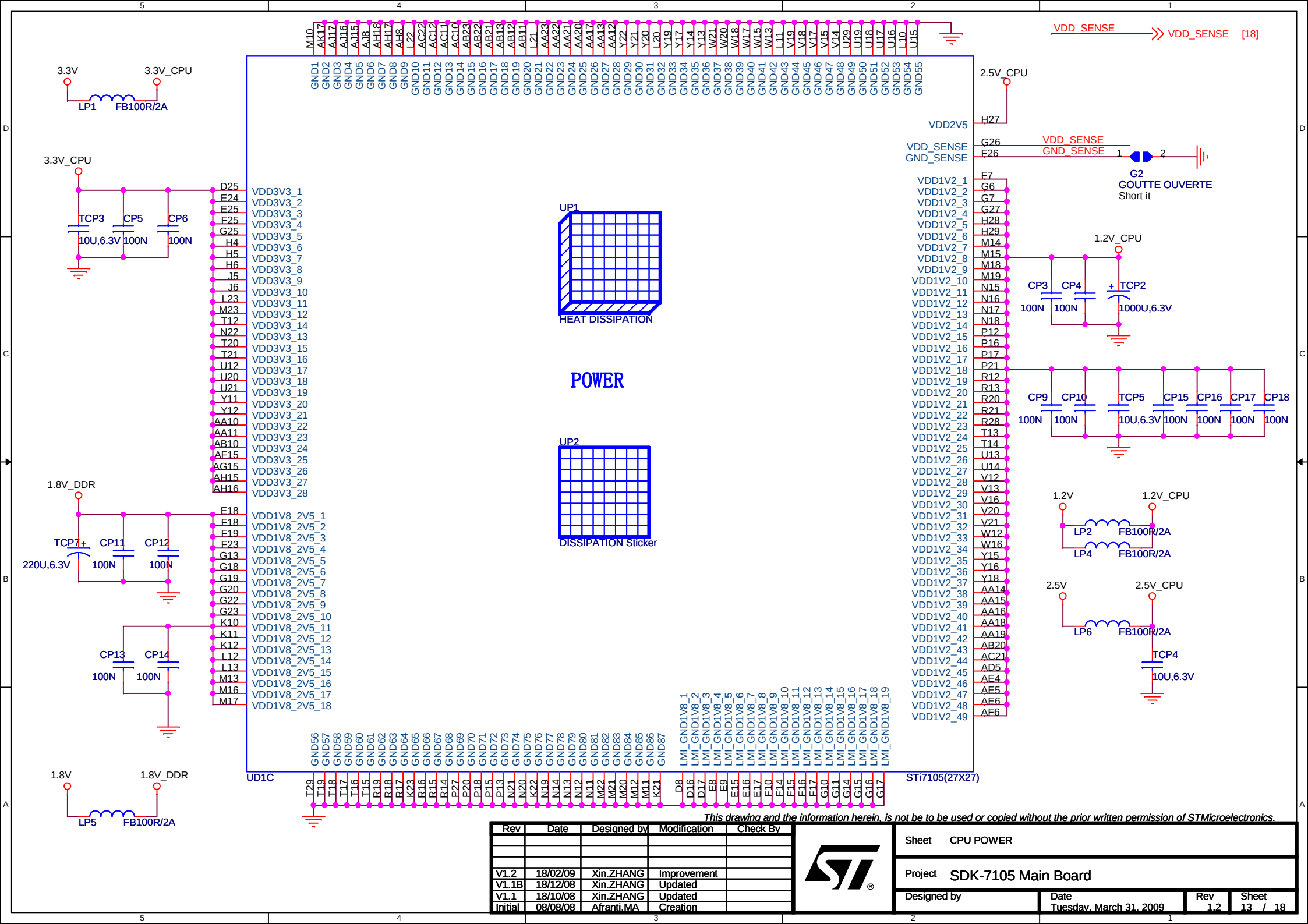
Sheet	CPU PIO2		
Project	SDK-7105 Main Board		
Designed by	Date: Wednesday, May 13, 2009	Rev: 1.2	Sheet: 12 / 18



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Sheet	CPU POWER		
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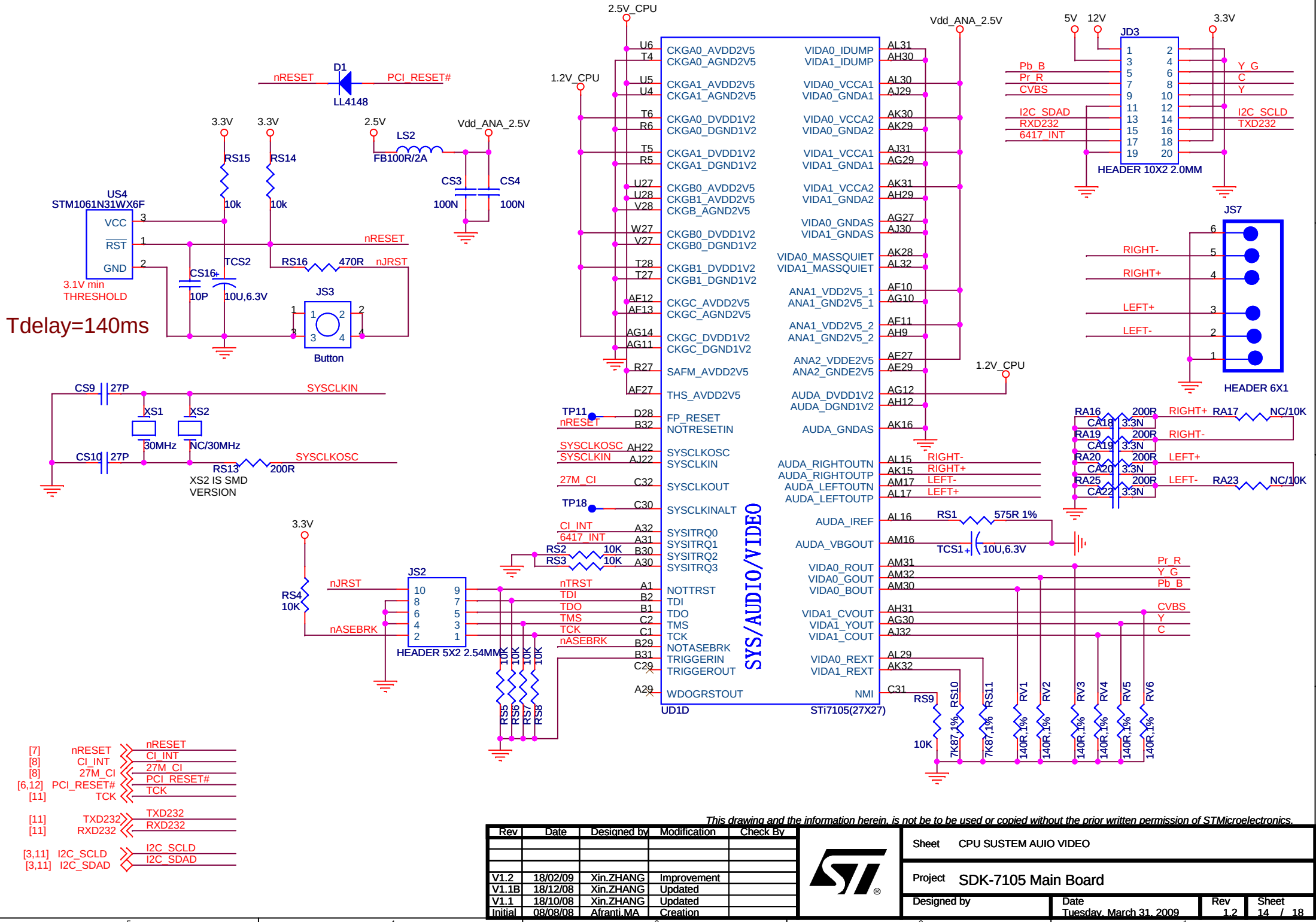

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Sheet CPU SUSTEM AUIO VIDEO

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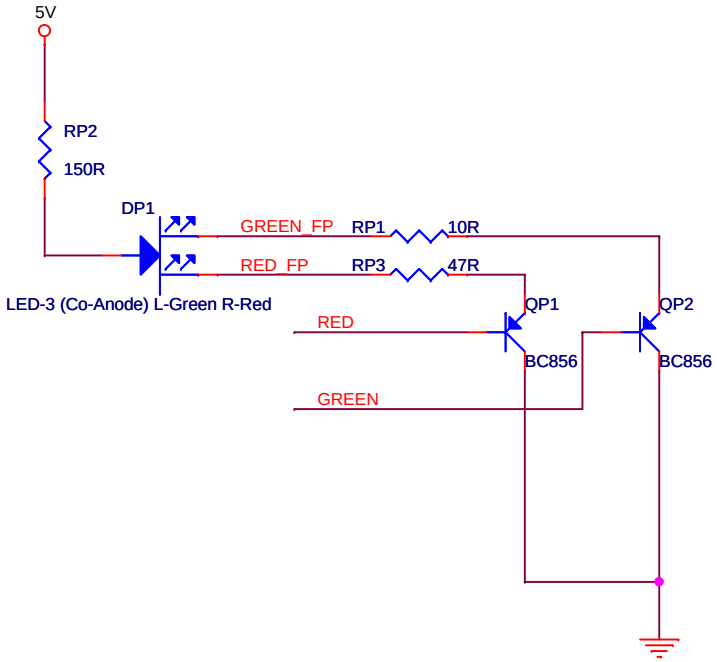
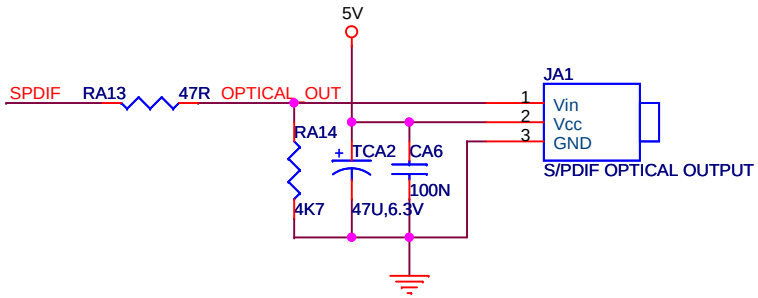
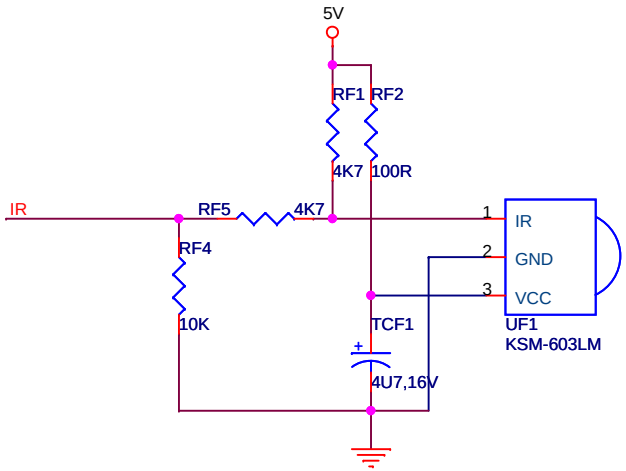
Designed by	Date	Rev	Sheet
	Tuesday, March 31, 2009	1.2	14 / 18





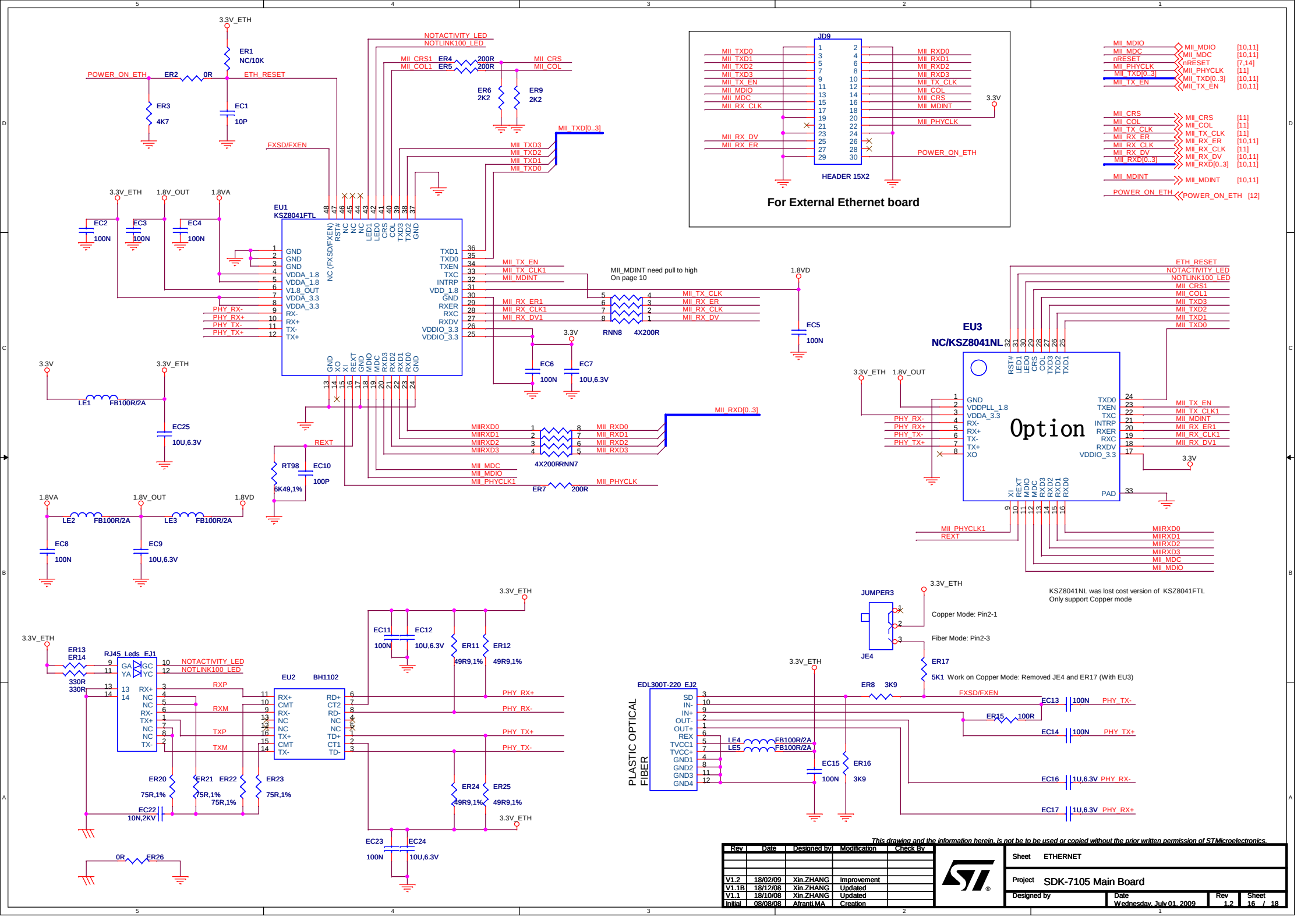


Rev	Date	Designed by	Modification	Check By
V1.2	18/02/09	Xin.ZHANG	Improvement	
V1.1B	18/12/08	Xin.ZHANG	Updated	
V1.1	18/10/08	Xin.ZHANG	Updated	
Initial	08/08/08	Afranti.MA	Creation	

Sheet AUDIO VIDEO CONNECTOR / FRONT PANEL

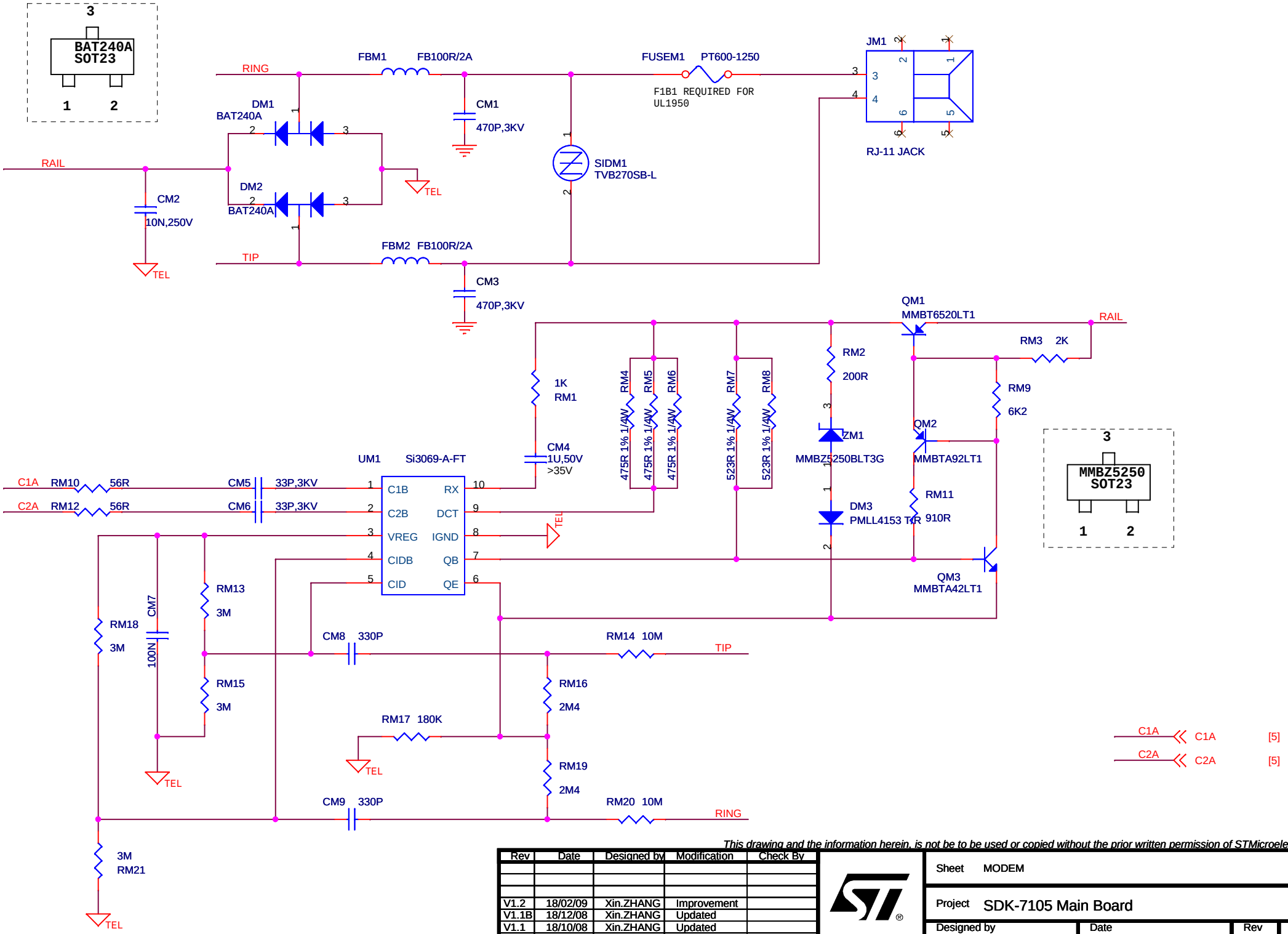
Project SDK-7105 Main Board

Designed by	Date	Rev	Sheet
	Wednesday, July 01, 2009	1.2	15 / 18



Rev	Date	Designed by	Modification	Check By
V1.2	18/02/09	Xin.ZHANG	Improvement	
V1.1B	18/12/08	Xin.ZHANG	Updated	
V1.1	18/10/08	Xin.ZHANG	Updated	
Initial	08/08/08	Afranti.MA	Creation	

Sheet	ETHERNET		
Project	SDK-7105 Main Board		
Designed by	Date: Wednesday, July 01, 2009	Rev: 1.2	Sheet: 16 / 18



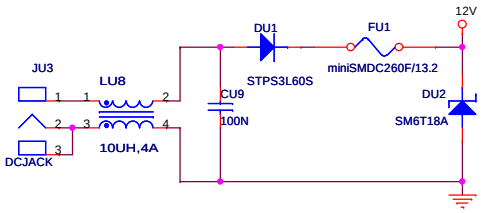
Rev	Date	Designed by	Modification	Check By
V1.2	18/02/09	Xin.ZHANG	Improvement	
V1.1B	18/12/08	Xin.ZHANG	Updated	
V1.1	18/10/08	Xin.ZHANG	Updated	
Initial	08/08/08	Afranti.MA	Creation	

Sheet MODEM

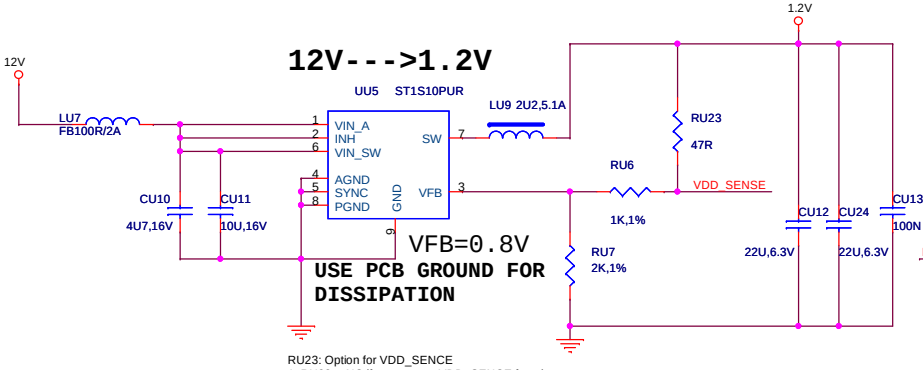
Project SDK-7105 Main Board

Designed by | Date Friday, March 27, 2009 | Rev 1.2 | Sheet 17 / 18

INPUT VOLTAGE 12V/5A



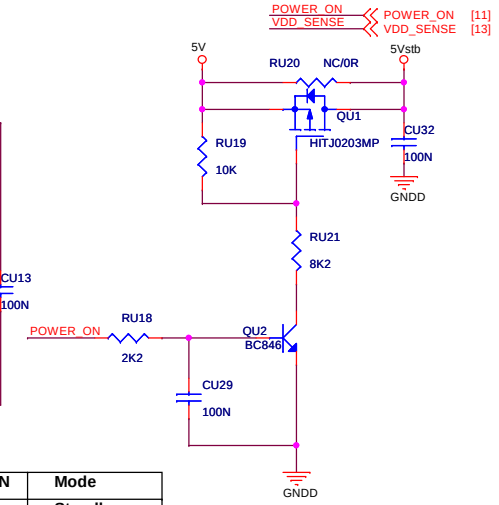
12V--->1.2V



VFB=0.8V

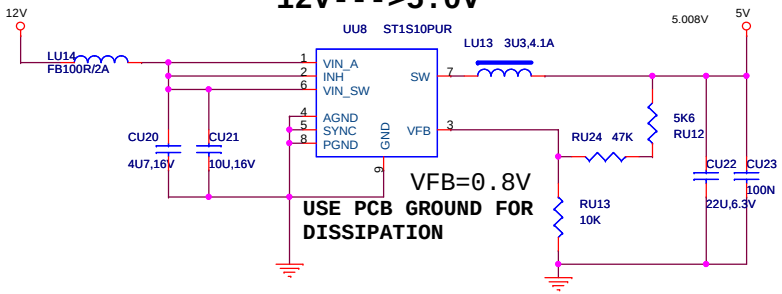
USE PCB GROUND FOR DISSIPATION

RU23: Option for VDD_SENCE
1, RU23-->NC if want to use VDD_SENCE function
2, RU23-->47R or TBD if VDD_SENCE disable
3, Keep RU23 for protection when VDD_SENCE short or open
SDK design select item 3
VDD_SENCE Function:
That's a ball/pad directly attached to the metal grid inside the chip.
Its target is to give a direct access to into the chip about Vcore



Power ON	Mode
0	Standby
1	Normal

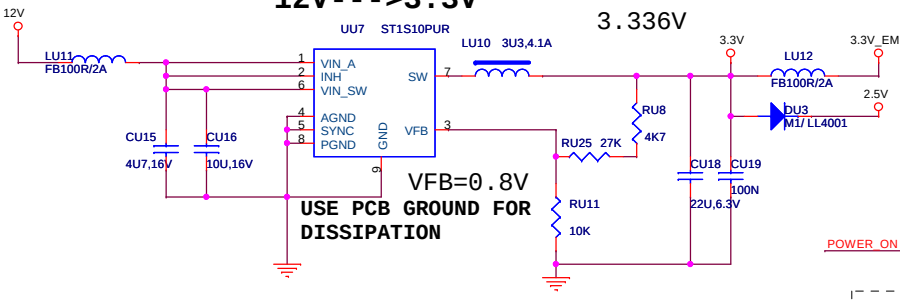
12V--->5.0V



VFB=0.8V

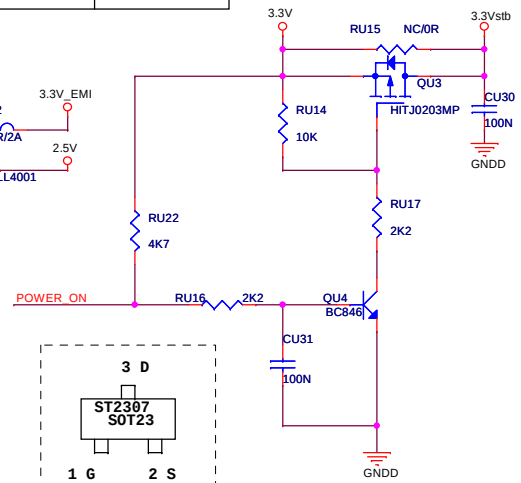
USE PCB GROUND FOR DISSIPATION

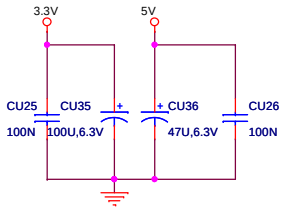
12V--->3.3V



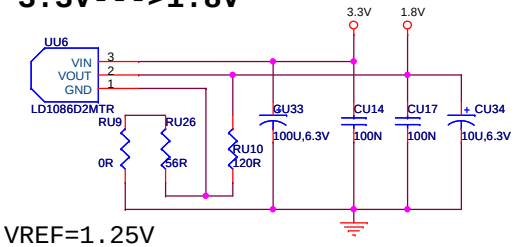
VFB=0.8V

USE PCB GROUND FOR DISSIPATION





3.3V--->1.8V



VREF=1.25V

Rev	Date	Designed by	Modification	Check By
V1.2	18/02/09	Xin.ZHANG	Improvement	
V1.1B	18/12/08	Xin.ZHANG	Updated	
V1.1	18/10/08	Xin.ZHANG	Updated	
Initial	08/08/08	Afranti.MA	Creation	

Sheet ON BOARD POWER

Project SDK-7105 Main Board

Designed by | Date Wednesday, April 15, 2009 | Rev 1.2 | Sheet 18 / 18