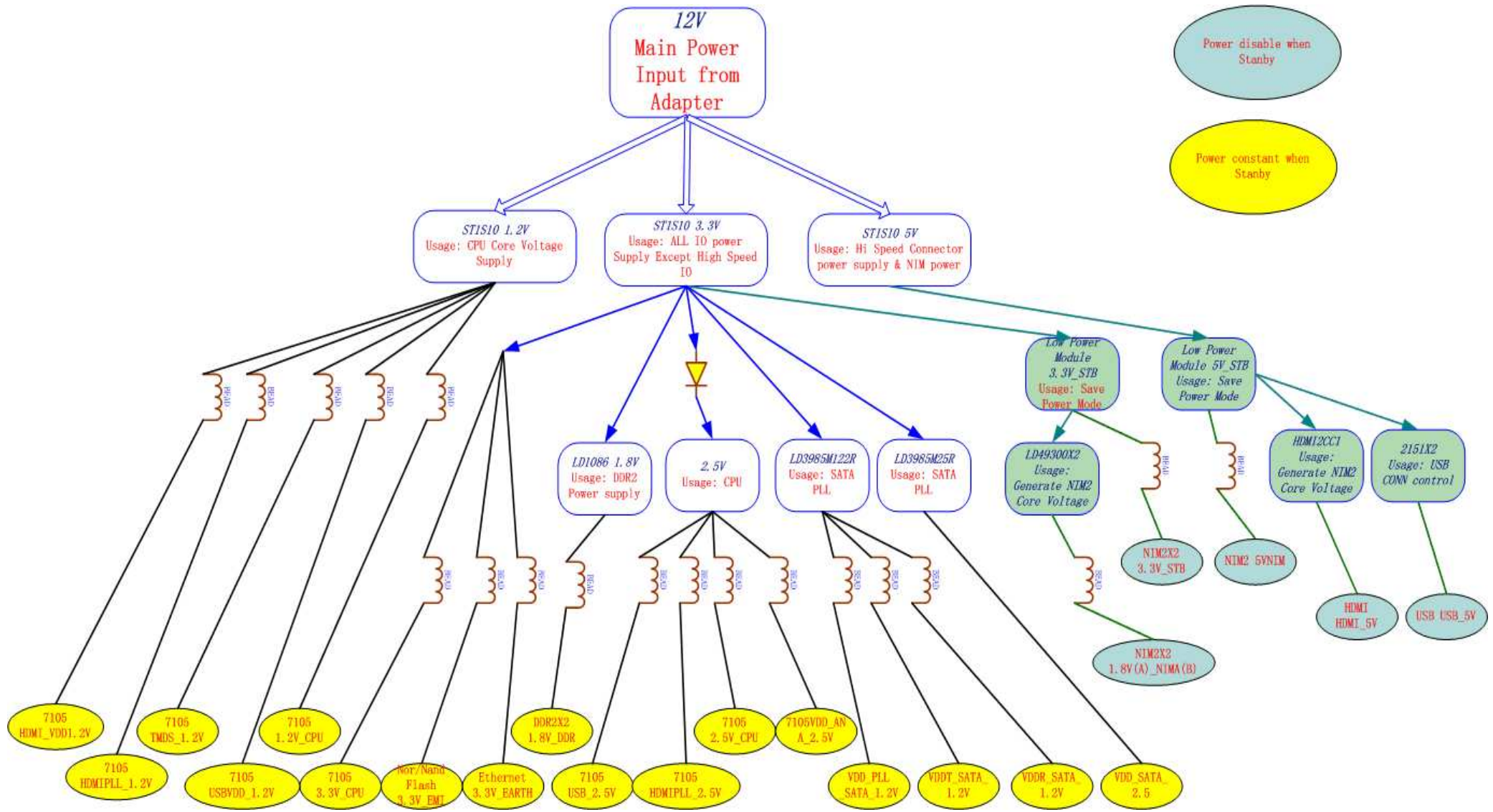




# Need Updated !!!



Power disable when Standby

Power constant when Standby

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Rev	Date	Designed by	Modification	Check By
V1.2	18/02/09	Xin.ZHANG	Improvement	
V1.1B	18/12/08	Xin.ZHANG	Updated	
V1.1	18/10/08	Xin.ZHANG	Updated	
Initial	08/08/08	Afrant.MA	Creation	

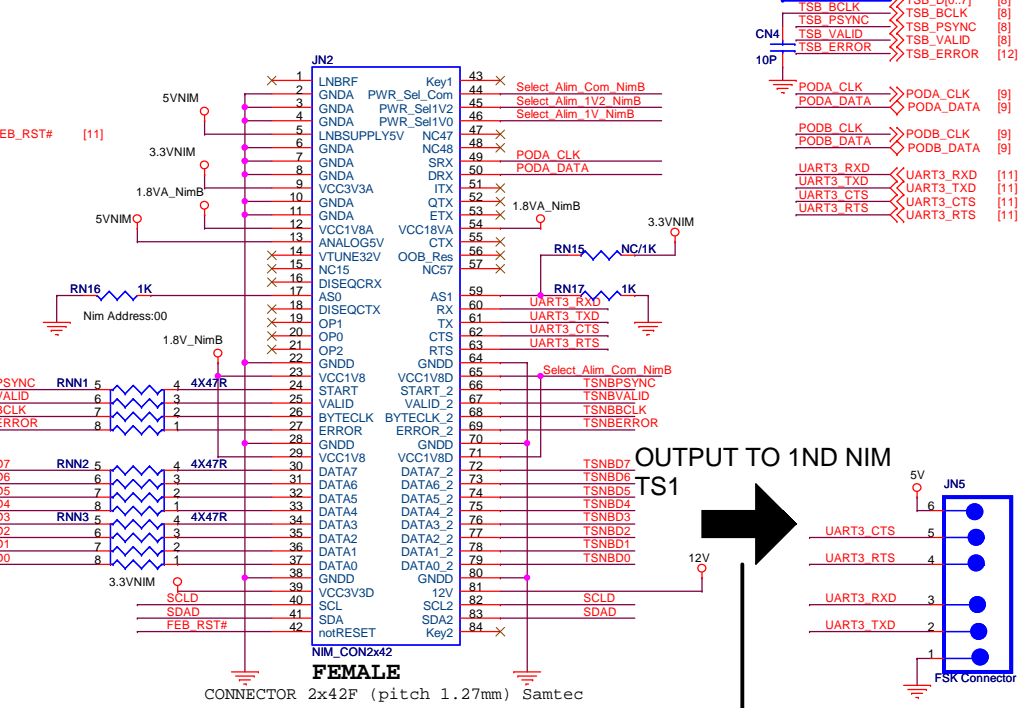
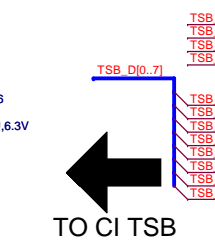
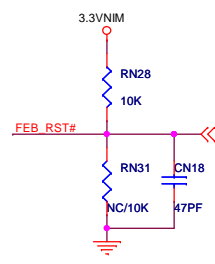
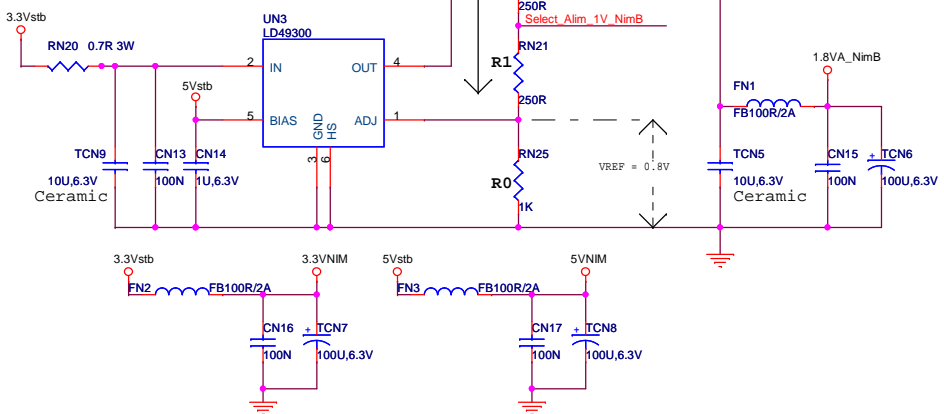


Sheet Power Distribution				
Project SDK-7105 Main Board				
Designed by	Date	Rev	Sheet	
	Friday, March 27, 2009	1.2	2 / 18	

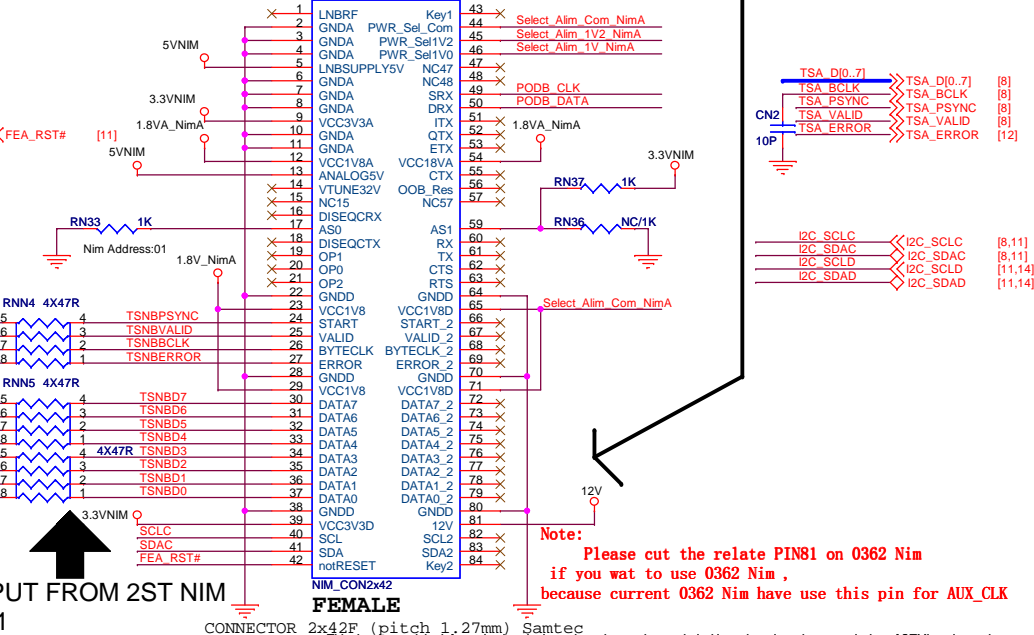
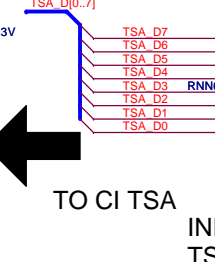
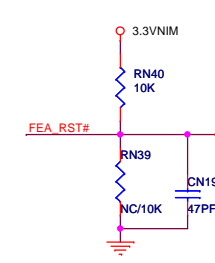
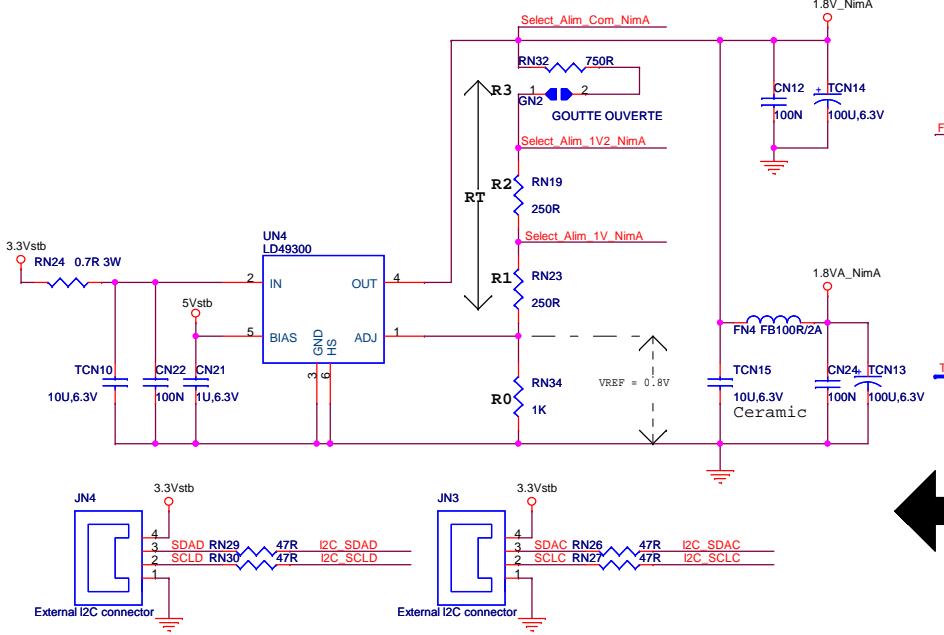
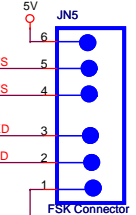
About GN1  
Only for need 1.8V output

**RT Load Description**

R0	=	1K,	VRef =	0V9
RT = R1+ R2 +R3	=	996,	Vout =	1V8
RT = R1+ R2	=	331,	Vout =	1V2
RT = R1	=	110,	Vout =	1V0



OUTPUT TO 1ND NIM  
TS1



**Note:**  
Please cut the relate PIN81 on 0362 Nim  
if you want to use 0362 Nim,  
because current 0362 Nim have use this pin for AUX\_CLK



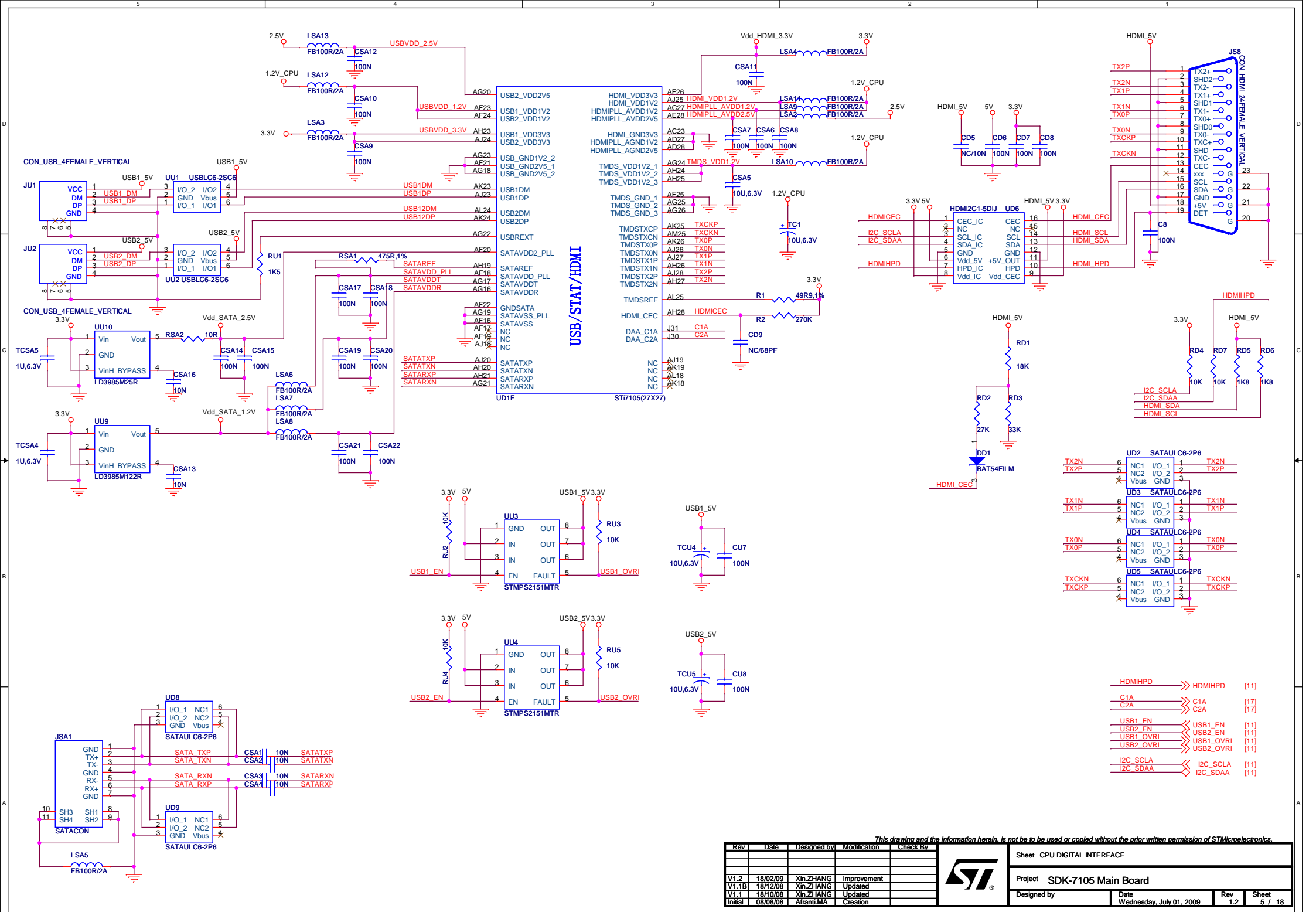
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V1.1B	18/12/08	Xin_ZHANG	Updated	
V1.1	18/10/08	Xin_ZHANG	Updated	
Initial	08/08/08	Afranti.MA	Creation	09-10-18



Sheet LNBH24 + DUAL NIM2	
Project SDK-7105 Main Board	Rev 1.2
Designed by	Date Tuesday, March 31, 2009
	Rev 1.2
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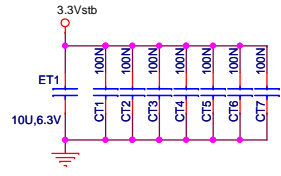
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V1.1	18/10/08	Xin_ZHANG	Updated	
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Sheet CPU DIGITAL INTERFACE				
Project SDK-7105 Main Board				
Designed by	Date	Rev	Sheet	
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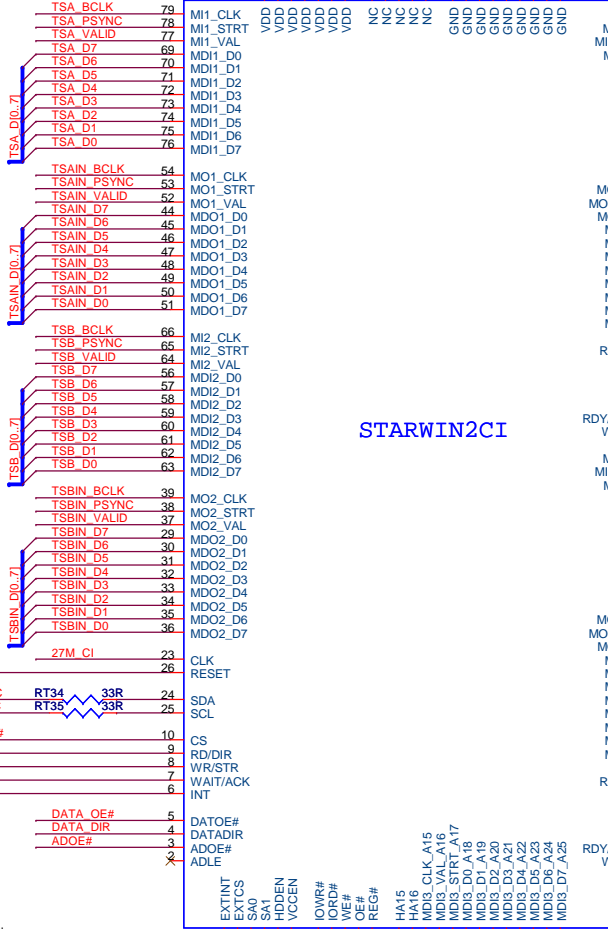
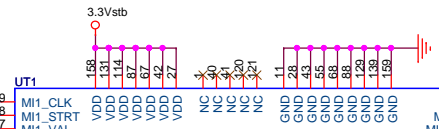
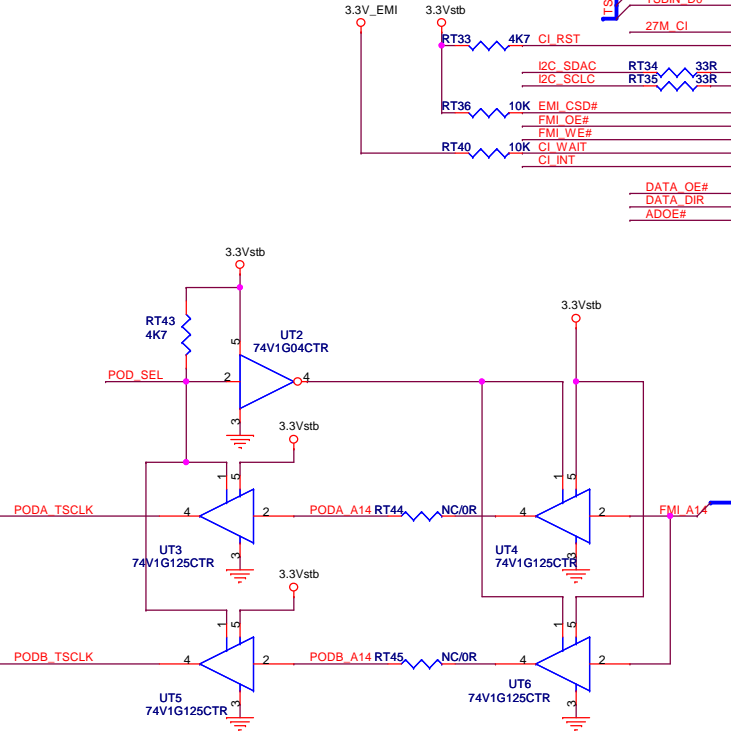


From NIMA

To 7105

From NIMB

To 7105



STARWIN2CI

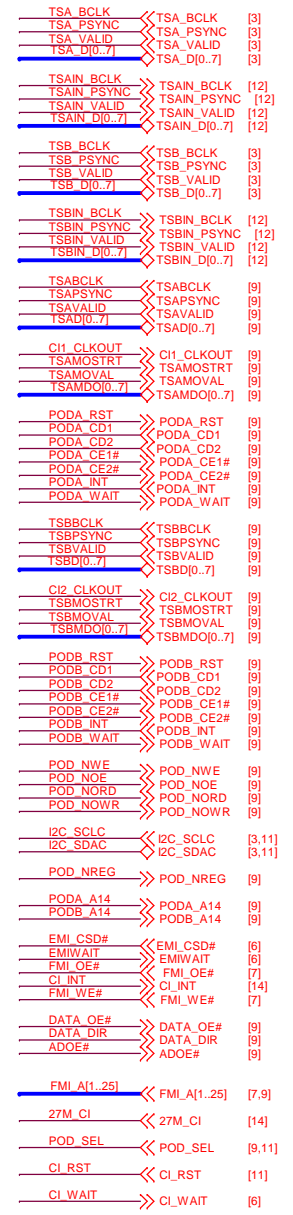
STARCI2WIN

Rev	Date	Designed by	Modification	Check by
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V1.1B	18/12/08	Xin ZHANG	Updated	
V1.1	18/10/08	Xin ZHANG	Updated	
Initial	05/09/08	Afranti.MA	Creation	



Sheet	STARCI2WIN			
Project	SDK-7105 Main Board			
Designed by	Date	Rev	Sheet	
	Tuesday, March 31, 2009	1.2	8 / 18	

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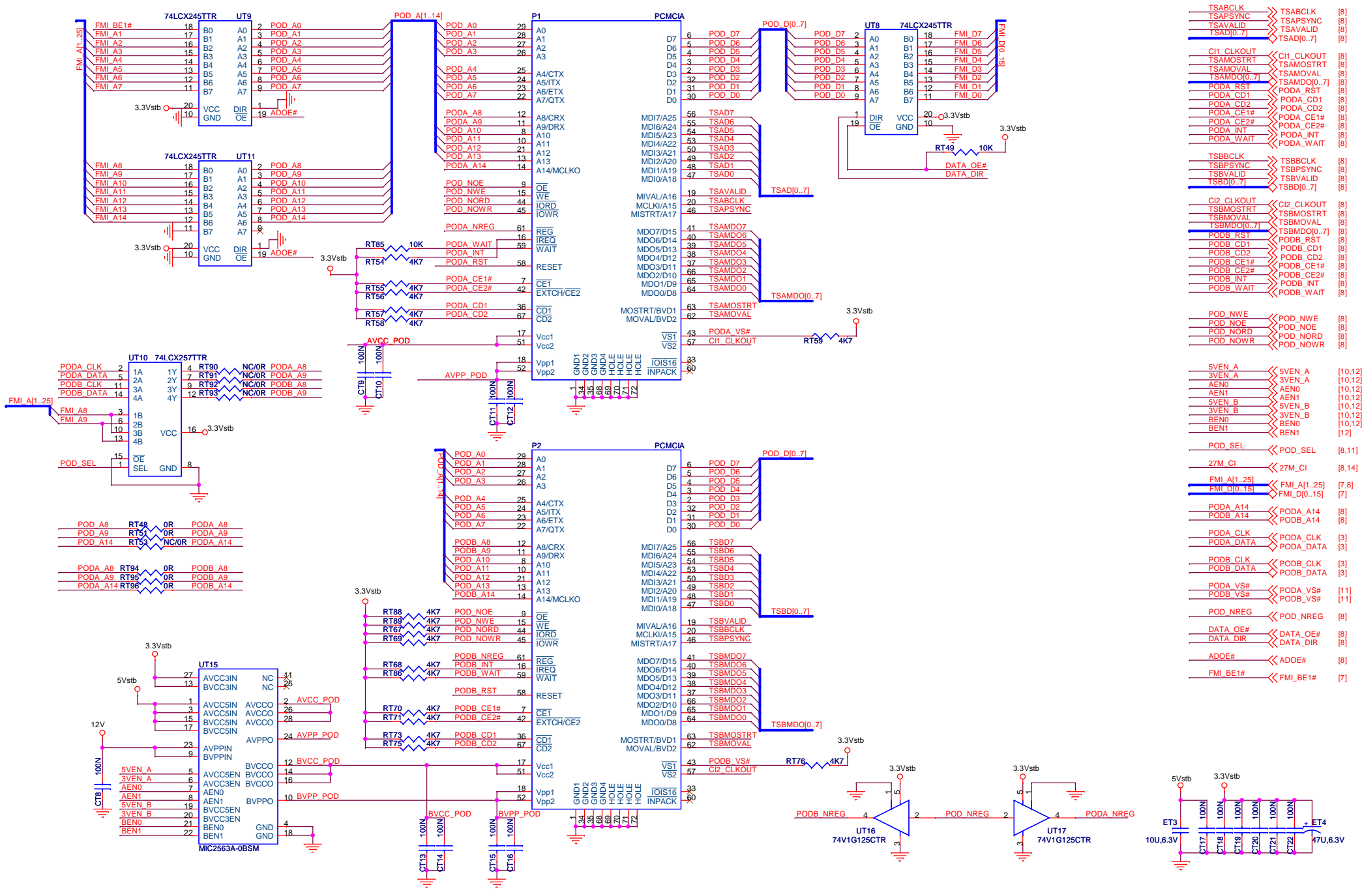
To CI Card A

From CI Card A

To CI Card B

From CI Card B





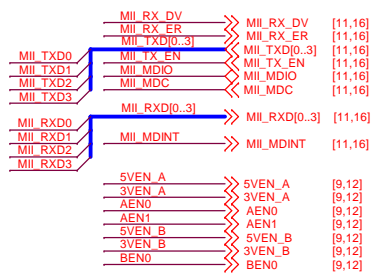
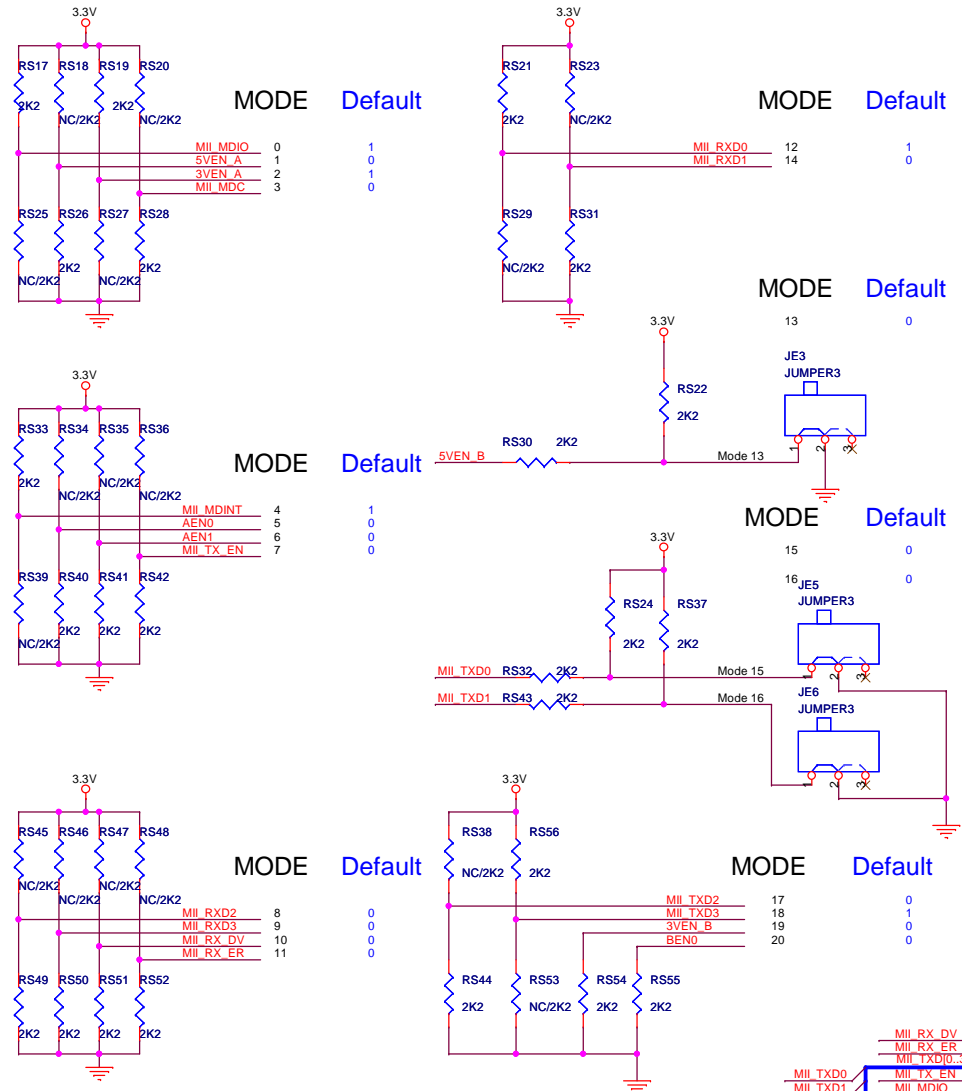
- TSABCLK << TSABCLK [8]
- TSAPSYNC << TSAPSYNC [8]
- TSVALID << TSVALID [8]
- TSAD[0..7] << TSAD[0..7] [8]
- C11\_CLKOUT << C11\_CLKOUT [8]
- TSAMOSTRT << TSAMOSTRT [8]
- TSAMOVAL << TSAMOVAL [8]
- TSAMDO[0..7] << TSAMDO[0..7] [8]
- PODA\_RST << PODA\_RST [8]
- PODA\_CD1 << PODA\_CD1 [8]
- PODA\_CD2 << PODA\_CD2 [8]
- PODA\_CE1# << PODA\_CE1# [8]
- PODA\_CE2# << PODA\_CE2# [8]
- PODA\_INT << PODA\_INT [8]
- PODA\_WAIT << PODA\_WAIT [8]
- TSBCLK << TSBCLK [8]
- TSBPSYNC << TSBPSYNC [8]
- TSBVALID << TSBVALID [8]
- TSBD[0..7] << TSBD[0..7] [8]
- C12\_CLKOUT << C12\_CLKOUT [8]
- TSBMOSTRT << TSBMOSTRT [8]
- TSBMOVAL << TSBMOVAL [8]
- TSBMD[0..7] << TSBMD[0..7] [8]
- PODB\_RST << PODB\_RST [8]
- PODB\_CD1 << PODB\_CD1 [8]
- PODB\_CD2 << PODB\_CD2 [8]
- PODB\_CE1# << PODB\_CE1# [8]
- PODB\_CE2# << PODB\_CE2# [8]
- PODB\_INT << PODB\_INT [8]
- PODB\_WAIT << PODB\_WAIT [8]
- POD\_NWE << POD\_NWE [8]
- POD\_NOE << POD\_NOE [8]
- POD\_NORD << POD\_NORD [8]
- POD\_NOWR << POD\_NOWR [8]
- SVEN\_A << SVEN\_A [10,12]
- SVEN\_A << SVEN\_A [10,12]
- AEN0 << AEN0 [10,12]
- AEN1 << AEN1 [10,12]
- SVEN\_B << SVEN\_B [10,12]
- SVEN\_B << SVEN\_B [10,12]
- BEN0 << BEN0 [10,12]
- BEN1 << BEN1 [10,12]
- POD\_SEL << POD\_SEL [8,11]
- 27M\_Ci << 27M\_Ci [8,14]
- FMI\_A[1..25] << FMI\_A[1..25] [7,8]
- FMI\_D[0..15] << FMI\_D[0..15] [7]
- PODA\_A14 << PODA\_A14 [8]
- PODB\_A14 << PODB\_A14 [8]
- PODA\_CLK << PODA\_CLK [3]
- PODA\_DATA << PODA\_DATA [3]
- PODB\_CLK << PODB\_CLK [3]
- PODB\_DATA << PODB\_DATA [3]
- PODA\_VS# << PODA\_VS# [11]
- PODB\_VS# << PODB\_VS# [11]
- POD\_NREG << POD\_NREG [8]
- DATA\_OE# << DATA\_OE# [8]
- DATA\_DIR << DATA\_DIR [8]
- ADOE# << ADOE# [8]
- FMI\_BE1# << FMI\_BE1# [7]

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V1.2	18/02/09	Xin ZHANG	Improvement	
V1.1B	18/12/08	Xin ZHANG	Updated	
V1.1	18/10/08	Xin ZHANG	Updated	
Initial	08/08/08	Afranti.MA	Creation	



Sheet	DUAL CI INTERFACE			
Project	SDK-7105 Main Board			
Designed by	Date	Rev	Sheet	
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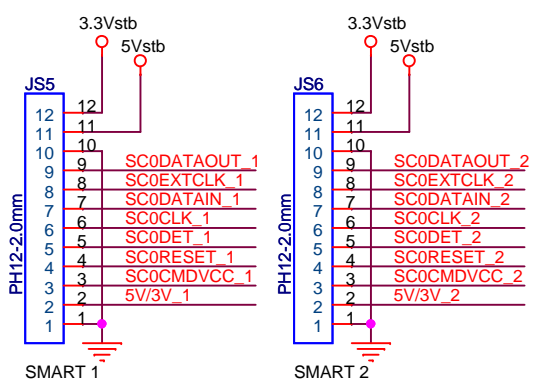
Bit	Bit field	Controlled unit	Controlling Pad
MODE[0]	<b>Ref clock selection for Clockgen A</b> 0: SYSCLOCKAL (Ext) 1: Osc (SATA)	ClockGen A	MIIMDIO [PIO8(3)]
MODE[2:1]	<b>PLL0 startup configuration<sup>(1)</sup></b> 00: Fin/Fout=27/900 MHz 01: Fin/Fout=27/604.8 MHz 10: Fin/Fout=30/900 MHz 11: Fin/Fout=30/600 MHz	ClockGen A	[PIO16(1,0)]
MODE[4:3]	<b>PLL1 startup configuration<sup>(1)</sup></b> 00: Fin/Fout=27/799.2 MHz 01: Fin/Fout=27/399.6 MHz 10: Fin/Fout=30/800 MHz 11: Fin/Fout=30/400 MHz	ClockGen A	MIIMDINT: MIIMDC [PIO9(6):PIO8(4)]
MODE[6:5]	<b>Reset bypasses<sup>(2)</sup></b> CPU_RST_OUT_BYPASS[1]: bypass of (LX_Audio+LXDelphi) reset loop back CPU_RST_OUT_BYPASS[0]: bypass of (SH4+LX_Audio+LXDelphi) reset loop back	Reset generator	[PIO16(3:2)]
MODE[7]	<b>Resetout mode</b> (see SYSTEM_CONFIG, long_reset_mode bit) <sup>(3)</sup>	Reset generator	MIITX_EN [PIO8(2)]
MODE[9:8]	<b>BOOT mode selection:</b> 00: SH4-300 boot first 01: ST231 DeltaMu boot first 10: ST231 Audio boot first	ST40, ST231 Audio, ST231 DeltaMu, request filtering	MIIRXD[3:2] [PIO9(1:0)]
MODE[10]	Reserved (Do not connect)	Reserved	MIIRX_DV [PIO7(4)]
MODE[11]	nand_addr_short_not_long <sup>(4)</sup>	Nand Controller	MIIRX_ER [PIO7(5)]
MODE[12]	<b>Serial Flash usage:</b> 0: ATME1 1: ST Flash	EMI4	MIIRXD[0] [PIO8(6)]
MODE[13]	<b>Boot device port size at boot: <sup>(4)</sup></b> 0: 16 bits 1: 8 bits	EMI4 and Nand Controller	[PIO16(4)]
MODE[14]	emiss_slave_not_master	EMI subsystem	MIIRXD[1] [PIO8(7)]
MODE[16:15]	<b>Boot Device:</b> 00: NOR Flash (EMI controller) 01: Nand Flash (Nand Controller) 10: Serial Flash (SPI controller) 11: MPX (EMI controller)	EMI subsystem	MIITXD[1:0] [PIO7(7:6)]
MODE[17]	emiss_clock_slave_not_master	EMI subsystem	MIITXD[2] [PIO8(0)]
MODE[18]	nand_page_large_not_small <sup>(4)</sup>	Nand Controller	MIITXD[3] [PIO8(1)]

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V1.1B	18/12/08	Xin.ZHANG	Updated	
V1.1	18/10/08	Xin.ZHANG	Updated	
Initial	05/02/08	Afranti.MA	Creation	



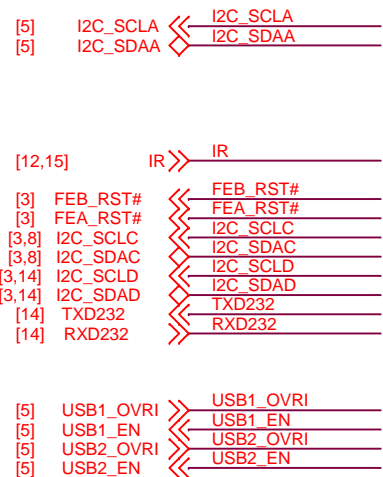
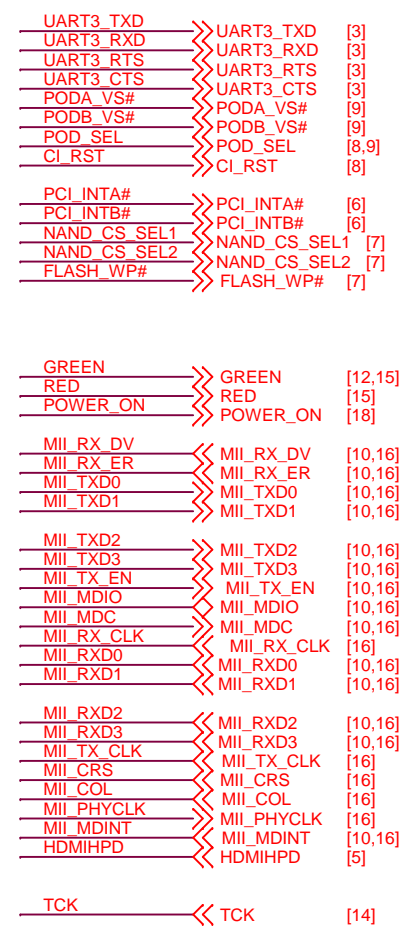
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Project SDK-7105 Main Board	
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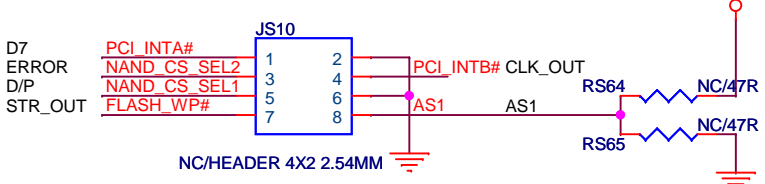
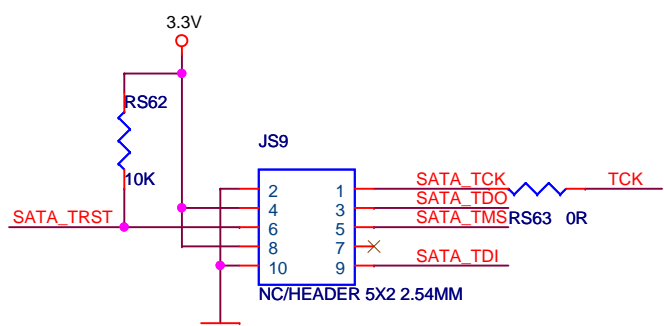
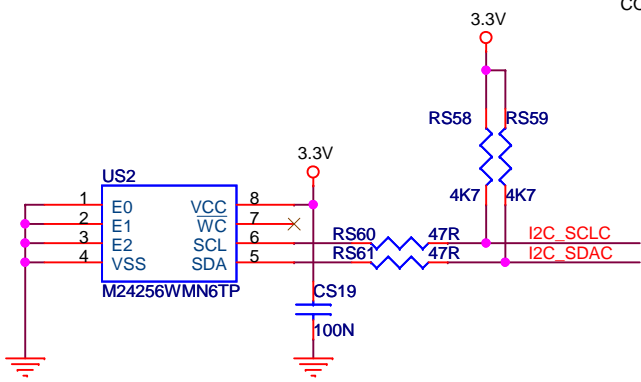
SC0DATAOUT_1	AE31	PIO00
SC0DATAIN_1	AE32	PIO01
SC0EXTCLK_1	AE30	PIO02
SC0CLK_1	AD29	PIO03
SC0RESET_1	AD31	PIO04
SC0CMDVCC_1	AD30	PIO05
5V/3V_1	AC29	PIO06
SC0DET_1	AC30	PIO07
SC0DATAOUT_2	AC28	PIO10
SC0DATAIN_2	AB27	PIO11
SC0EXTCLK_2	AB29	PIO12
SC0CLK_2	AB28	PIO13
SC0RESET_2	AA27	PIO14
SC0CMDVCC_2	AA28	PIO15
5V/3V_2	Y27	PIO16
SC0DET_2	Y29	PIO17
TP12	Y28	PIO20
TP13	W29	PIO21
I2C_SCL	W30	PIO22
I2C_SDA	W28	PIO23
COM_NOTCS	V29	PIO24
COM_CLK	V31	PIO25
COM_DOUT	V30	PIO26
COM_DIN	U31	PIO27
IR RF3	AF29	PIO30
TP14	AG28	PIO31
FEB_RST#	AF30	PIO32
FEA_RST#	AF28	PIO33
I2C_SCL	T30	PIO34
I2C_SDAC	R29	PIO35
I2C_SCLD	R31	PIO36
I2C_SDAD	R30	PIO37
TXD232	P29	PIO40
RXD232	P30	PIO41
TP15	P28	PIO42
TP19	N27	PIO43
USB1_OVRI	N29	PIO44
USB1_EN	N28	PIO45
USB2_OVRI	M27	PIO46
USB2_EN	M28	PIO47

### PIO-1

L27	UART3_TXD	PIO50
L29	UART3_RXD	PIO51
L28	UART3_RTS	PIO52
K27	UART3_CTS	PIO53
U30	PODA_VS#	PIO54
U32	PODB_VS#	PIO55
T31	POD_SEL	PIO56
T32	CI_RST	PIO57
E4	PCI_INTA#	PIO60
E2	PCI_INTB#	PIO61
E3	NAND_CS_SEL1	PIO62
E5	NAND_CS_SEL2	PIO63
F3	FLASH_WP#	PIO64
F4	SATA_TDI	PIO65
G4	SATA_TRST	PIO66
G3	SATA_TMS	PIO67
D1	GREEN	PIO70
D2	RED	PIO71
D3	POWER_ON	PIO72
G5	SATA_TDO	PIO73
AK9	MII_RX_DV	PIO74
AK8	MII_RX_ER	PIO75
AJ6	MII_TXD0	PIO76
AH7	MII_TXD1	PIO77
AL8	MII_TXD2	PIO80
AK6	MII_TXD3	PIO81
AK7	MII_TX_EN	PIO82
AF9	MII_MDIO	PIO83
AG8	MII_MDC	PIO84
AH10	MII_RX_CLK	PIO85
AJ9	MII_RXD0	PIO86
AL9	MII_RXD1	PIO87
AK10	MII_RXD2	PIO90
AM8	MII_RXD3	PIO91
AJ7	MII_TX_CLK	PIO92
AG7	MII_COL	PIO93
AF7	MII_CRS	PIO94
AH11	MII_PHYCLK	PIO95
AF8	MII_MDINT	PIO96
I29	HDMIHPD	PIO97



PIO31 UHF REMOTE CONTROL SUPPORT

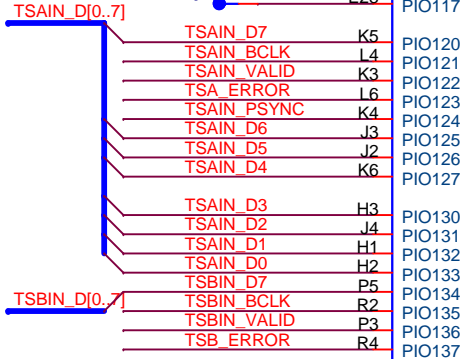
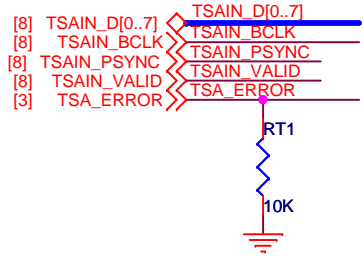
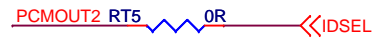


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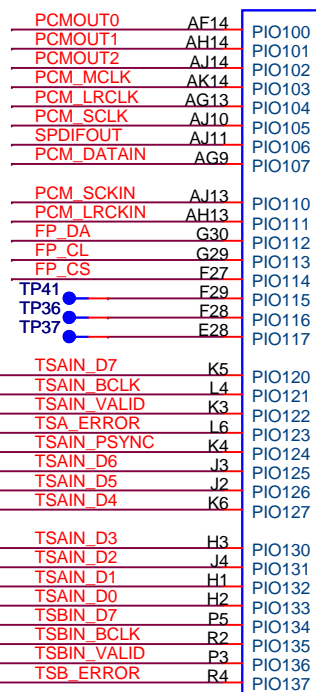
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V1.2	18/02/09	Xin.ZHANG	Improvement	
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V1.1	18/10/08	Xin.ZHANG	Updated	
Initial	08/08/08	Afranti.MA	Creation	



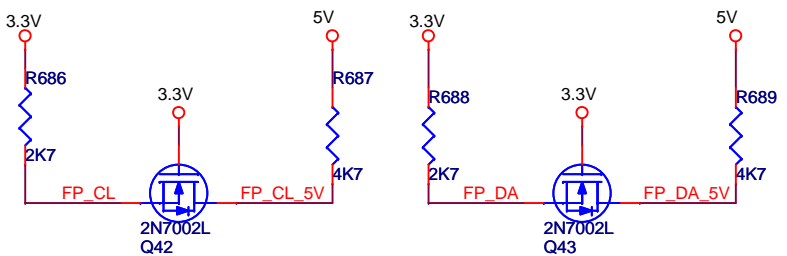
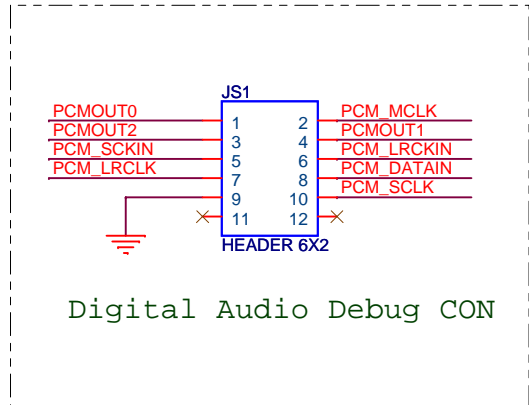
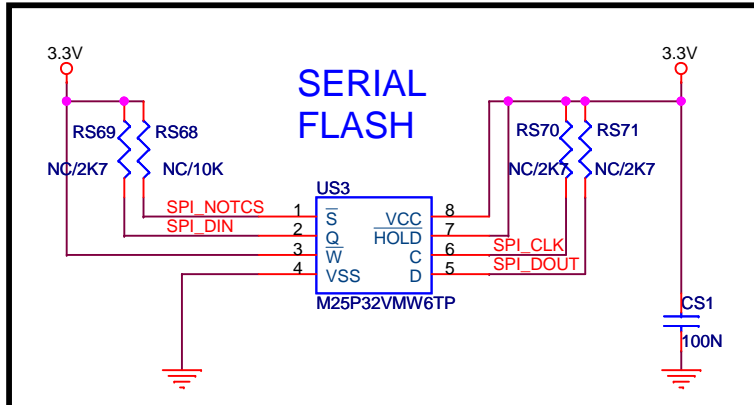
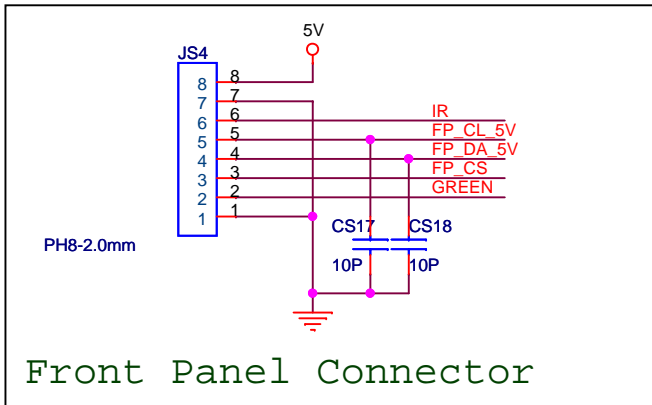
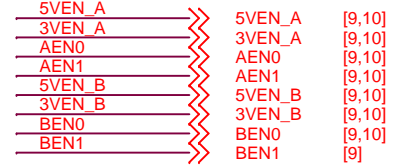
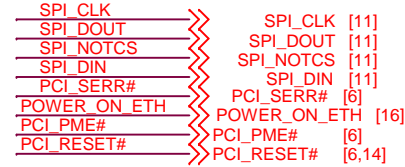
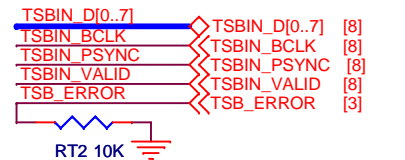
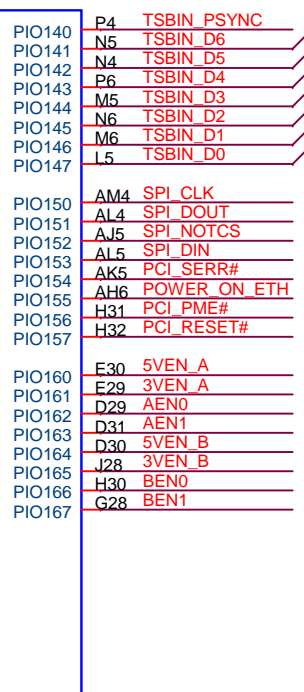
Sheet	CPU PIO1
Project	SDK-7105 Main Board
Designed by	Tuesday, March 31, 2009
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### PIO-2



UD1G STi7105(27X27)



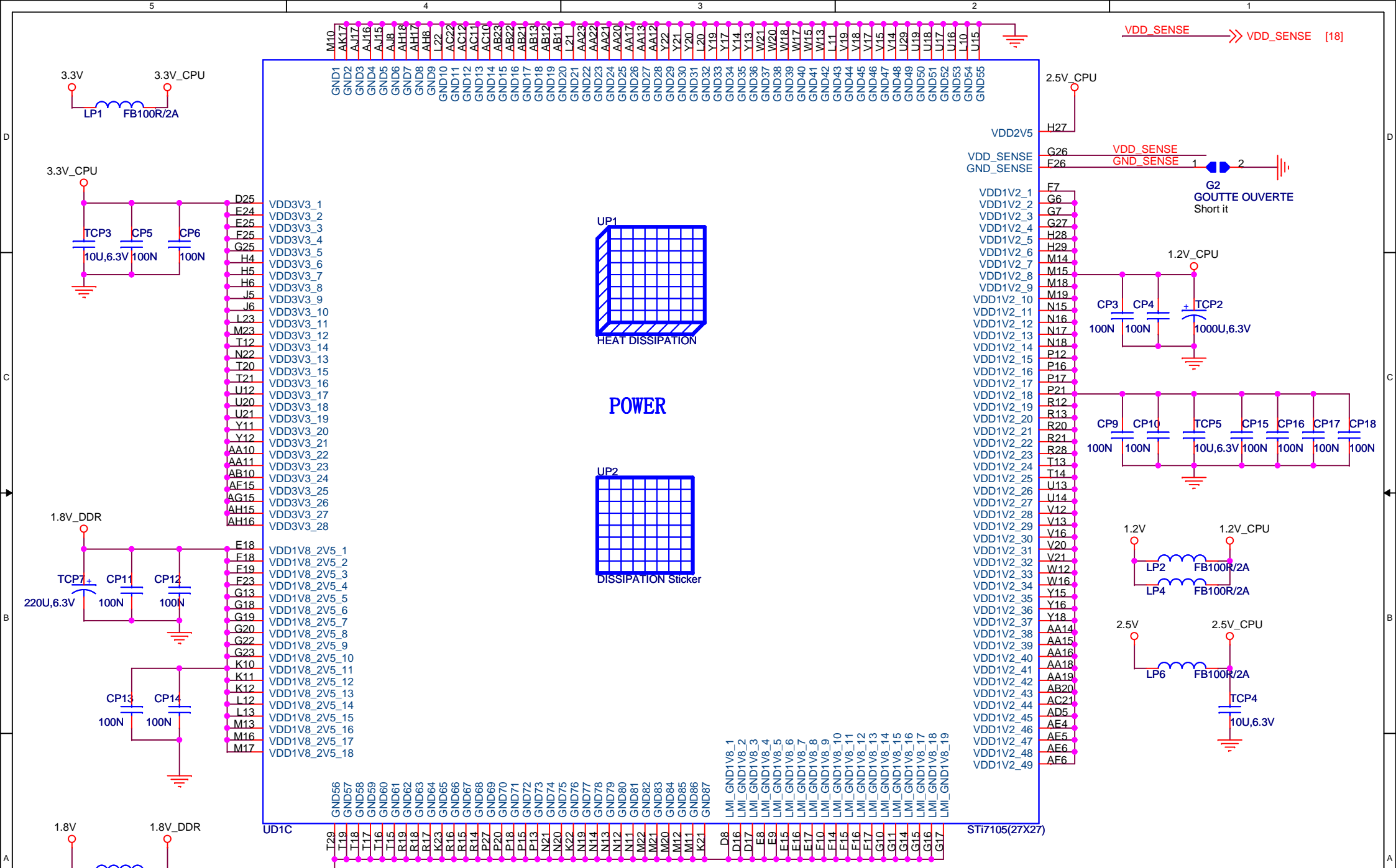
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V1.1	18/10/08	Xin.ZHANG	Updated	
Initial	08/08/08	Afrant.MA	Creation	



Sheet	CPU PIO2		
Project	SDK-7105 Main Board		
Designed by	Date	Rev	Sheet
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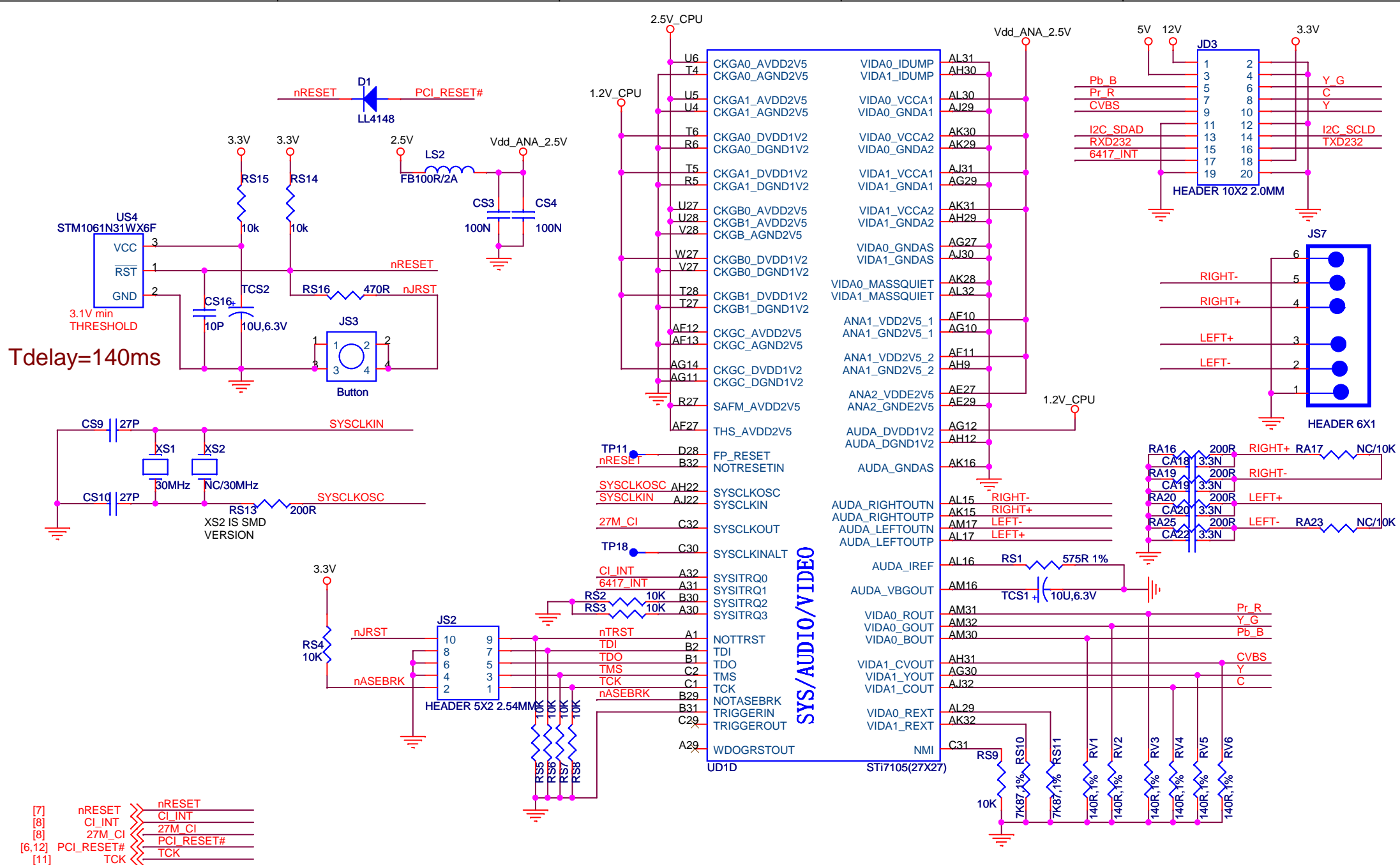


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V1.1	18/10/08	Xin.ZHANG	Updated	
Initial	08/08/08	Afrant.MA	Creation	



Sheet CPU POWER		Project SDK-7105 Main Board	
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Tdelay=140ms

SYS/AUDIO/VIDEO

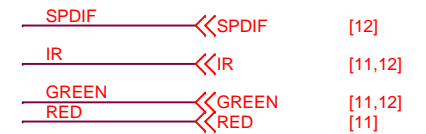
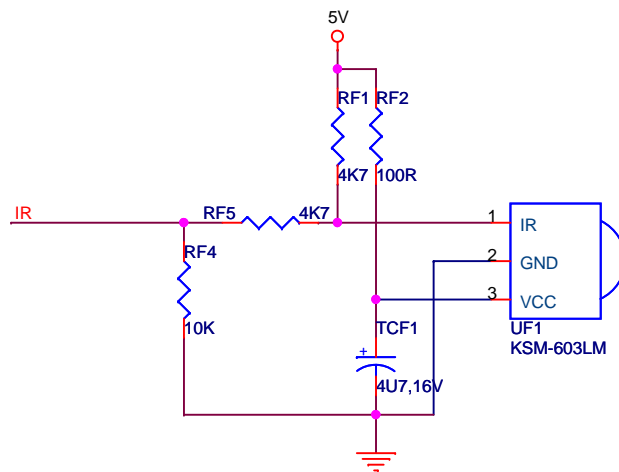
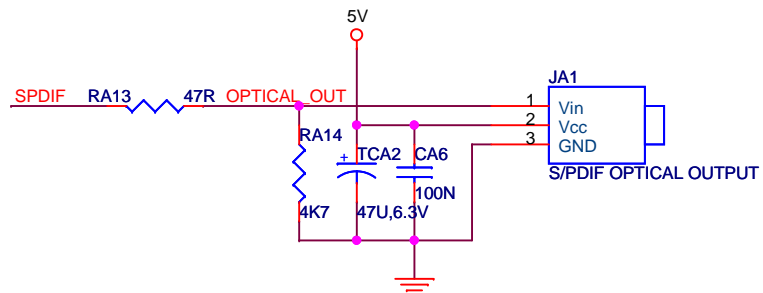
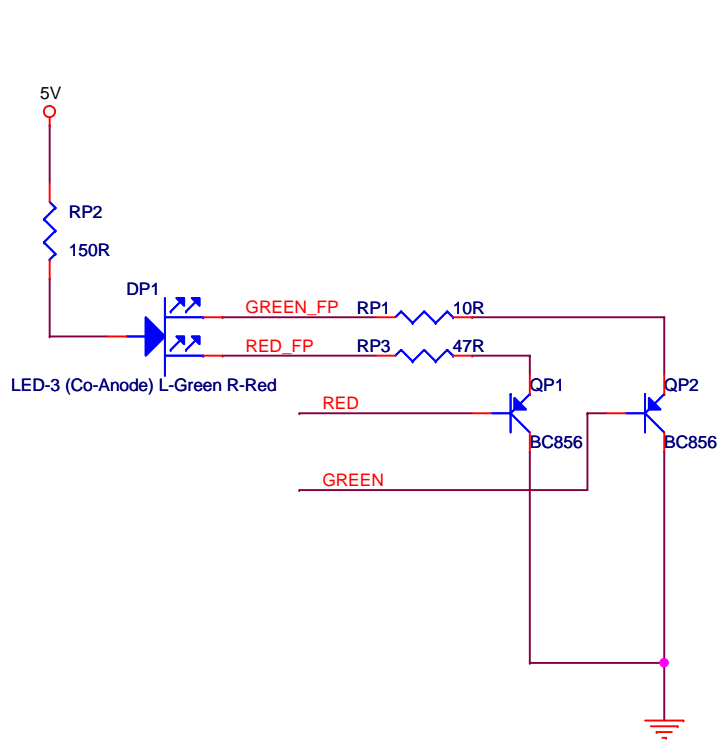
- [7] nRESET <-> nRESET
- [8] CI\_INT <-> CI\_INT
- [8] 27M\_CI <-> 27M\_CI
- [6,12] PCL\_RESET# <-> PCI\_RESET#
- [11] TCK <-> TCK
  
- [11] TXD232 <-> TXD232
- [11] RXD232 <-> RXD232
  
- [3,11] I2C\_SCLD <-> I2C\_SCLD
- [3,11] I2C\_SDAD <-> I2C\_SDAD

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Rev	Date	Designed by	Modification	Check By
V1.2	18/02/09	Xin.ZHANG	Improvement	
V1.1B	18/12/08	Xin.ZHANG	Updated	
V1.1	18/10/08	Xin.ZHANG	Updated	
Initial	08/08/08	Afrant.MA	Creation	



Sheet CPU SUSTEM AUIO VIDEO	
Project SDK-7105 Main Board	
Designed by	Date Tuesday, March 31, 2009
Rev 1.2	Sheet 14 / 18



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V1.1B	18/12/08	Xin_ZHANG	Updated	
V1.1	18/10/08	Xin_ZHANG	Updated	
Initial	08/08/08	Afranti.MA	Creation	



Sheet AUDIO VIDEO CONNECTOR / FRONT PANEL

Project SDK-7105 Main Board

Designed by

Date

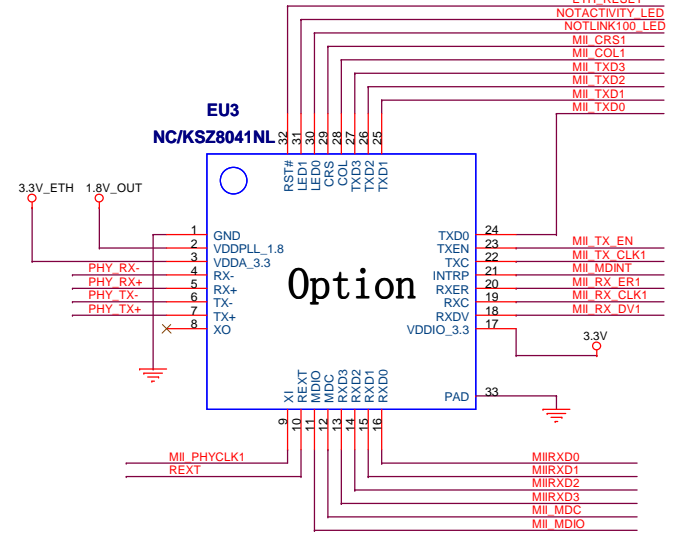
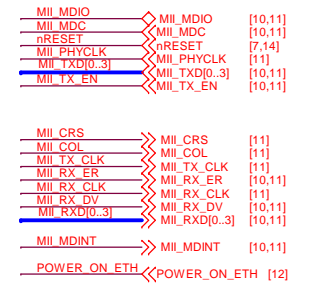
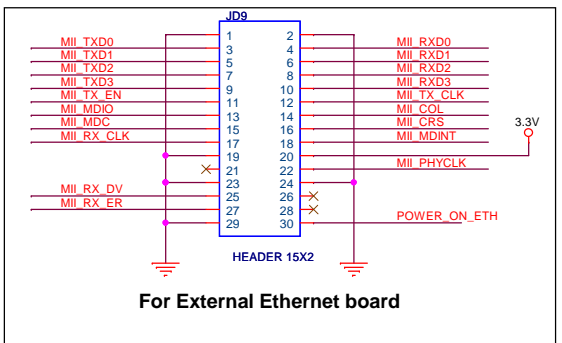
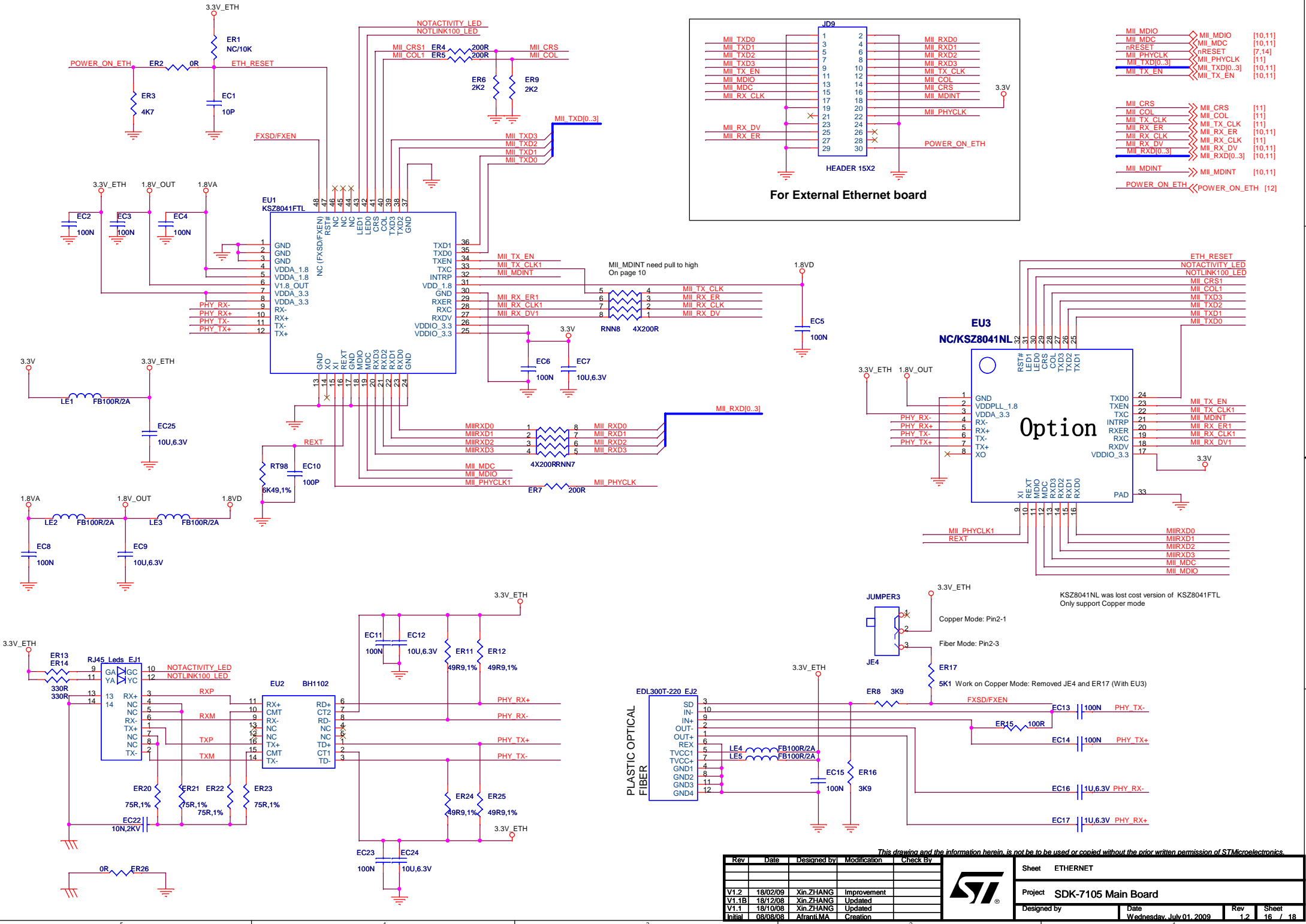
Wednesday, July 01, 2009

Rev

1.2

Sheet

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KSZ8041NL is lost cost version of KSZ8041FTL  
Only support Copper mode

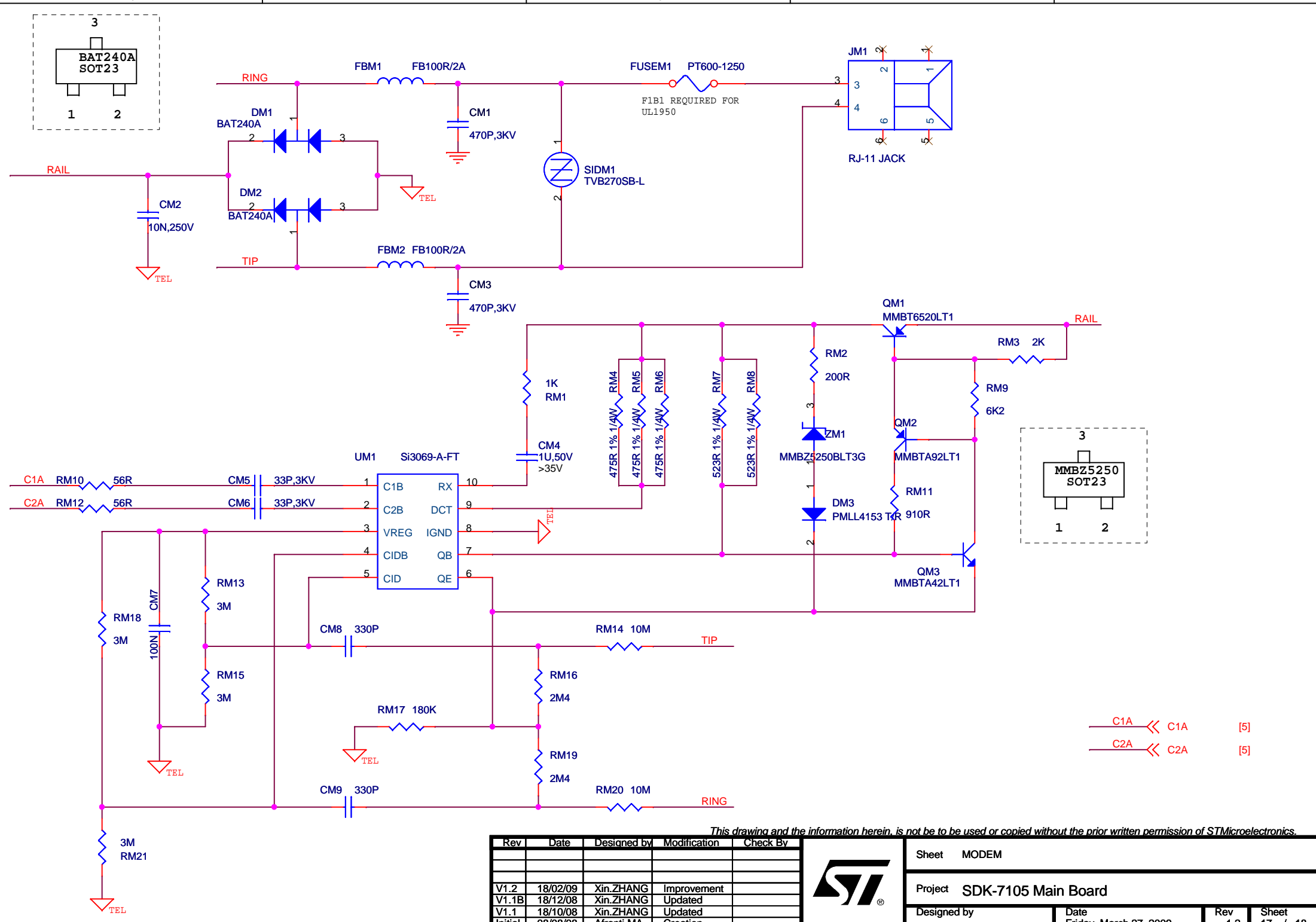
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V1.1B	18/12/08	Xin-ZHANG	Updated	
V1.1	18/10/08	Xin-ZHANG	Updated	
Initial	08/08/08	AfranilMA	Creation	



Sheet	ETHERNET		
Project	SDK-7105 Main Board		
Designed by	Date	Rev	Sheet
	Wednesday, July 01, 2009	1.2	16 / 18





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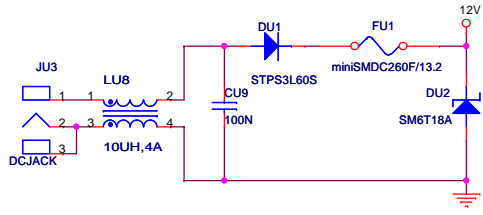
Rev	Date	Designed by	Modification	Check By
V1.2	18/02/09	Xin.ZHANG	Improvement	
V1.1B	18/12/08	Xin.ZHANG	Updated	
V1.1	18/10/08	Xin.ZHANG	Updated	
Initial	08/08/08	Afrant.MA	Creation	



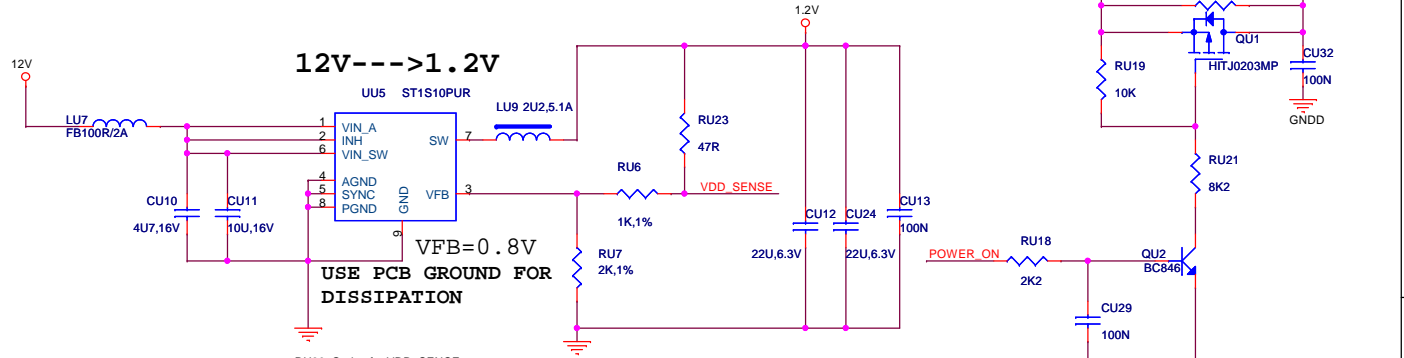
Sheet MODEM	
Project SDK-7105 Main Board	
Designed by	Date
	Friday, March 27, 2009
Rev	Sheet
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C1A << C1A [5]  
 C2A << C2A [5]

### INPUT VOLTAGE 12V/5A



### 12V--->1.2V

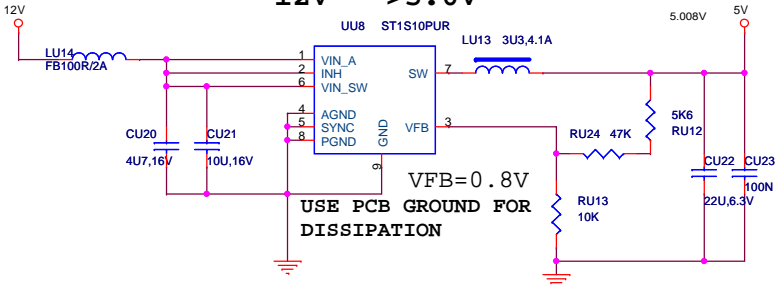


VFB=0.8V  
USE PCB GROUND FOR DISSIPATION

UU5: Option for VDD\_SENSE  
1. RU23-->NC if want to use VDD\_SENSE function  
2. RU23-->47R or 10K if VDD\_SENSE disable  
3. Keep RU23 for protection when VDD\_SENSE short or open  
SDK design select item 3  
VDD\_SENSE Function:  
That's a ball/pad directly attached to the metal grid inside the chip.  
Its target is to give a direct access to into the chip about Vcore

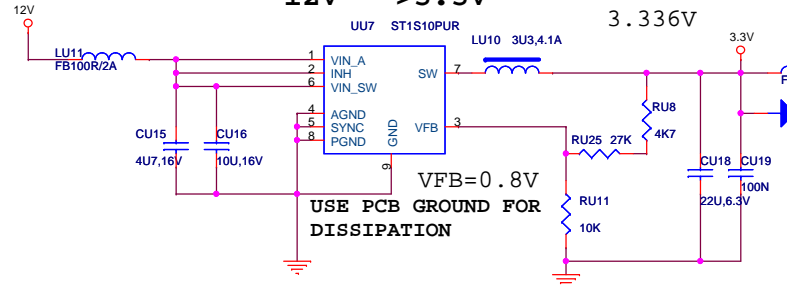
Power ON	Mode
0	Standby
1	Normal

### 12V--->5.0V



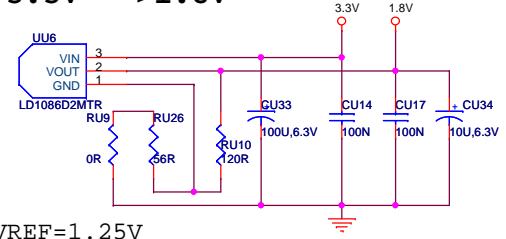
VFB=0.8V  
USE PCB GROUND FOR DISSIPATION

### 12V--->3.3V

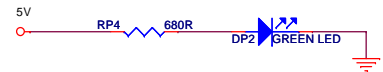
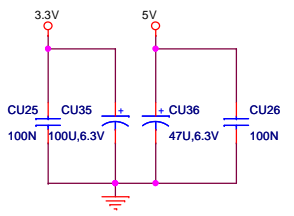
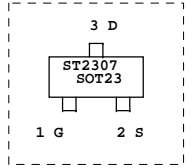
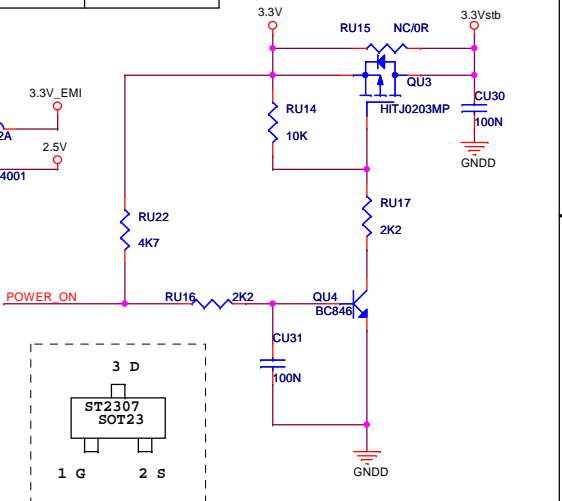


VFB=0.8V  
USE PCB GROUND FOR DISSIPATION

### 3.3V--->1.8V



VREF=1.25V



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V1.1	18/10/08	Xin_ZHANG	Updated	
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Sheet	ON BOARD POWER		
Project	SDK-7105 Main Board		
Designed by	Date	Rev	Sheet
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