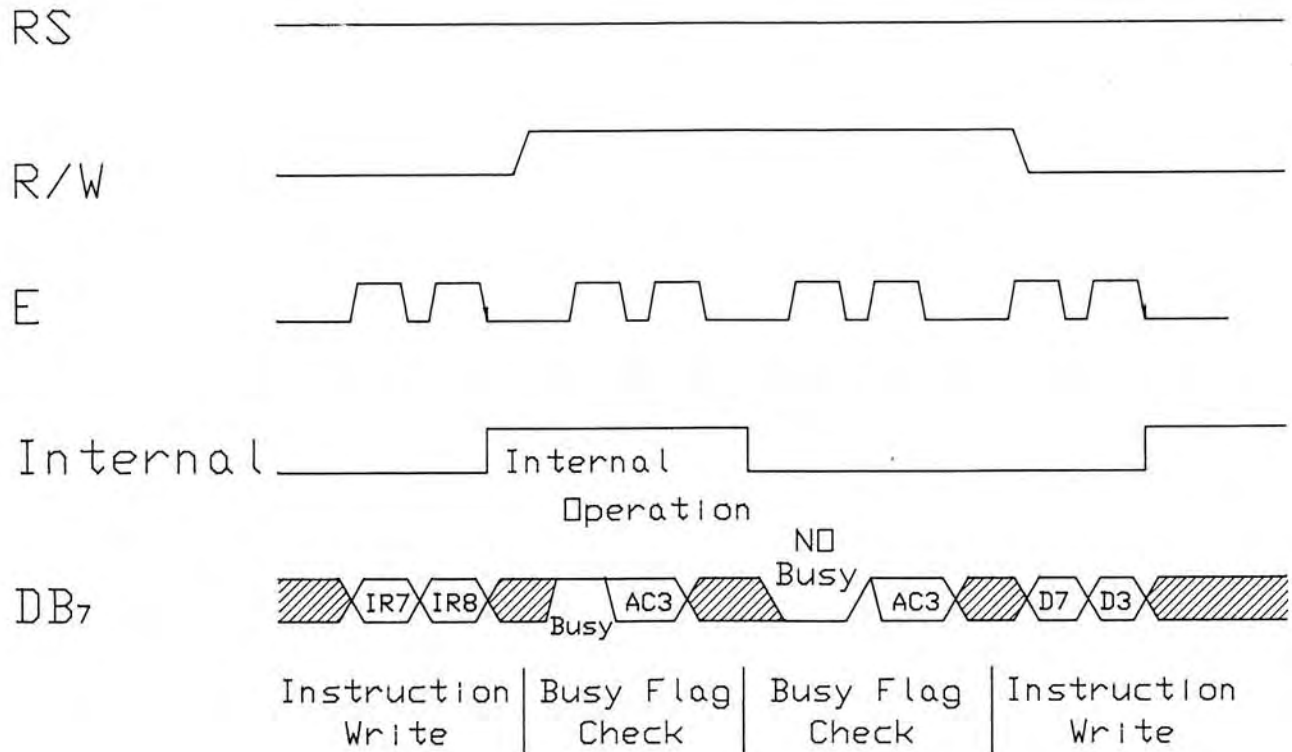


Interface To Mpu

Interface to 4-BIT Mpu:



(Note) IR7, IR3: Instruction 7th bit, 3rd bit

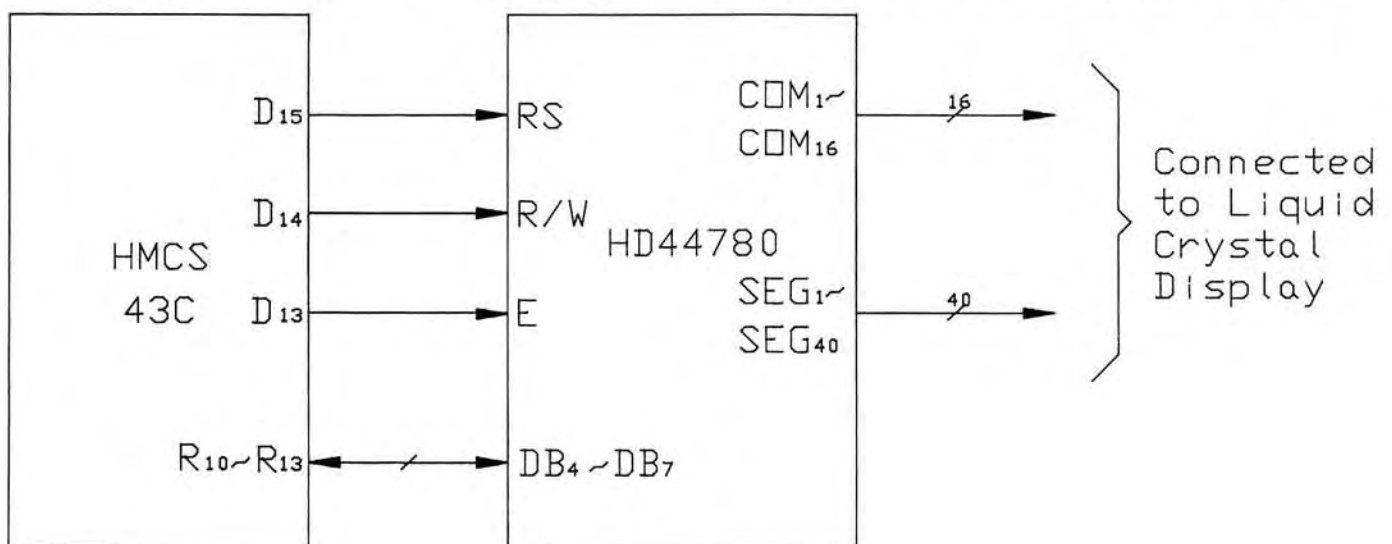
AC3: Address Counter 3rd bit

Example of 4-bit Data Transfer timing sequence

The HD44780 can be connected to a 4-bit MPU through the 4-bit MPU I/O port. If the I/O port has enough bits, data can be transferred in 8-bit lengths, but if the bits are insufficient, the transfer is made in two operations of 4 bits each (with designation of interface data length for 4 bits). In the latter case, the timing sequence becomes somewhat complex.

Fig-13-4 shows an example of interface to the HMCS43C.

Note that 2 cycles are needed for the busy flag check as well as the data transfer. 4-bit operation is selected by program.



HMCS43C: Hitach: 4-bit Single-chip microcomputer Example of Interface to the HMCS43C

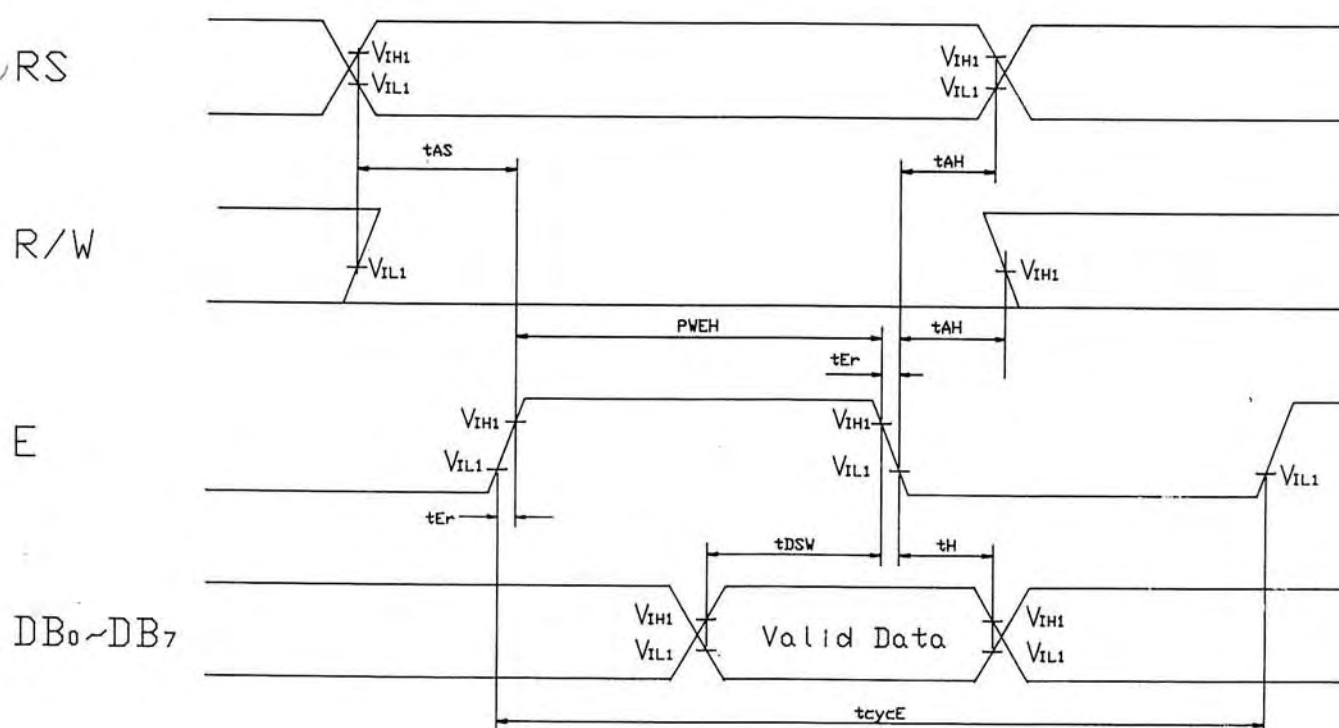
Interface To Mpu

Item	Symbol	Measuring Condition	Standard Value			Unit.
			min.	typ.	max.	
Enable Cycle Time	T_{CYCE}	Figs. 1.2	1000	—	—	ns
Enable Pulse Width, High Level	P_{WEH}	Figs. 1.2	450	—	—	ns
Enable Rise and Decay Time	t_{Er}, t_{Ed}	Figs. 1.2	—	—	25	ns
Address Setup Time, RS, R/W-E	t_{AS}	Figs. 1.2	140	—	—	ns
Data Delay Time	t_{DDR}	Fig. 2	—	—	320	ns
Data Setup Time	t_{DSW}	Fig. 1	195	—	—	ns
Data Hold Time (Write Operation)	t_H	Fig. 1	10	—	—	ns
Data Hold Time (Read Operation)	t_{DHR}	Fig. 2	20	—	—	ns
Address Hold Time	t_{AH}	Figs. 1.2	10	—	—	ns

* $V_{CC} = 5.0V \pm 10\%$, $GND = 0V$, $T_a = -20 \sim +75^\circ C$

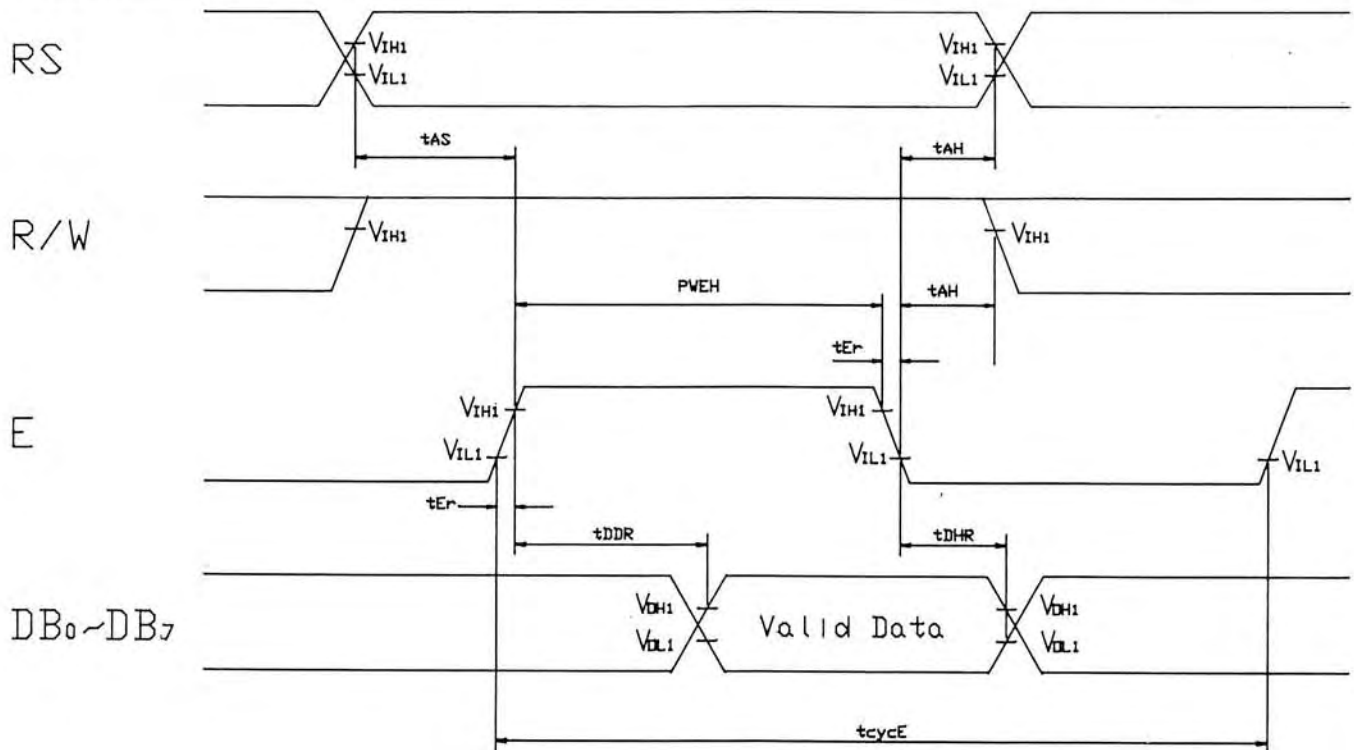
(In case control LSI is HD44780)

FIG.1 Write operation

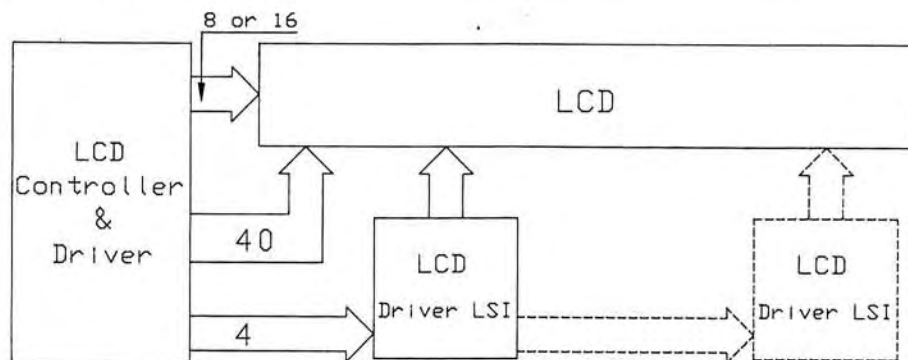


Interface To Mpu

FIG.2 Read operation



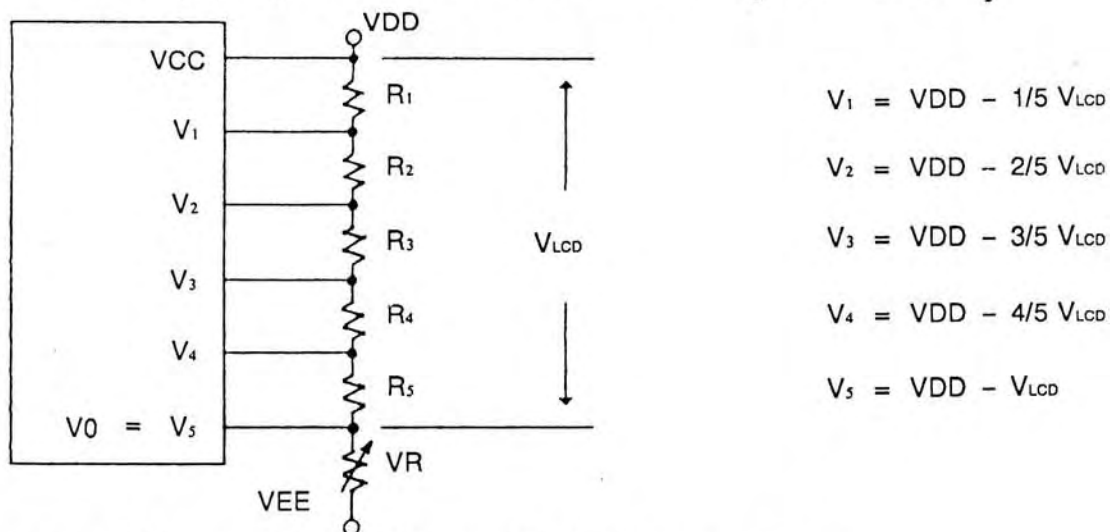
Block diagram:



Interface pin connections

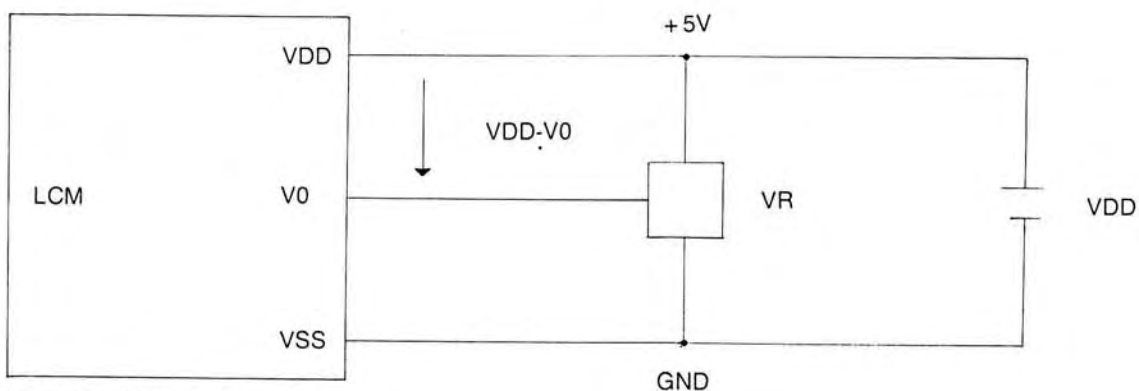
Pin No	Symbol	Level	Pin Description	Functions
1	V _{SS}	—	Ground	0V
2	V _{DD}	—	Supply voltage for logic	5V ± 5%
3	V ₀	—	Contrast adjustment	Decision by user system
4	RS	H/L	Register selection	H: Data input L: Instruction code input
5	R/W	H/L	Read/Write	H: Read L: Write
6	E	H, H → L	Enable signal	—
7	DB0	H/L	Data bit 0	$\updownarrow$ 4 BITS $\updownarrow$ 8 BITS
8	DB1	H/L	Data bit 1	
9	DB2	H/L	Data bit 2	
10	DB3	H/L	Data bit 3	
11	DB4	H/L	Data bit 4	
12	DB5	H/L	Data bit 5	
13	DB6	H/L	Data bit 6	
14	DB7	H/L	Data bit 7	

Power Supply For Lcd Driver (1/5 Bias)

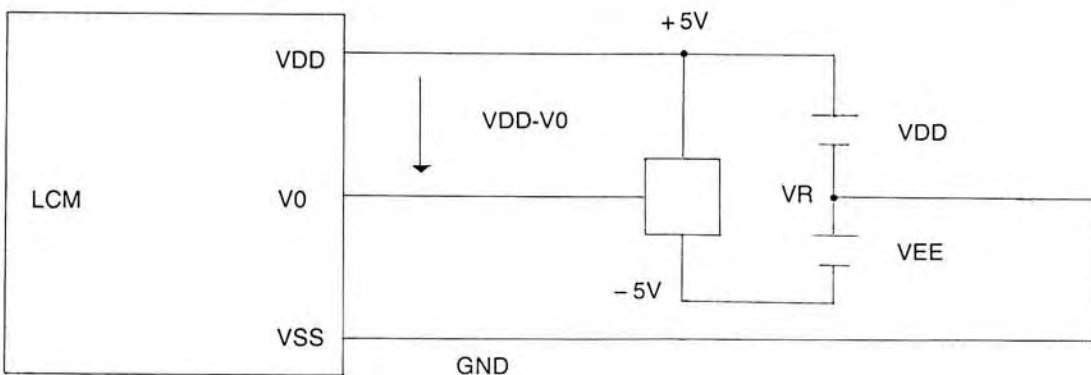


Power Supply Circuit Diagram:

Single supply voltage types



Dual supply voltage types



Character Generator Rom (CG Rom)

This character generator ROM (CG ROM) generates a character pattern of 5×7 dots from 8-bit character code and provides 192 character patterns.

Correspondence between Character Codes and Character Pattern

High Lower 4bit 4bit		0000	0010	0011	0100	0101	0110	0111	1010	1011	1100	1101	1110	1111
xxxx0000	CG RAM (1)		0	a	P	`	P		-	9	E		α	p
xxxx0001	(2)	!	1	A	Q	a	9	u	7	7	4		ä	q
xxxx0010	(3)	"	2	B	R	b	r	Γ	イ	ウ	×		β	θ
xxxx0011	(4)	#	3	C	S	c	s	┘	ウ	テ	E		ε	ω
xxxx0100	(5)	\$	4	D	T	d	t	、	エ	ト	ト		μ	Ω
xxxx0101	(6)	%	5	E	U	e	u	・	オ	ナ	コ		ε	0
xxxx0110	(7)	&	6	F	V	f	v	ヲ	カ	ニ	ヨ		ρ	Σ
xxxx0111	(8)	'	7	G	W	g	w	7	キ	ズ	ウ		g	π
xxxx1000	(1)	(	8	H	X	h	x	ィ	ウ	ホ	リ		γ	×
xxxx1001	(2)	)	9	I	Y	i	y	ウ	ウ	7	ル		γ	γ
xxxx1010	(3)	*	:	J	Z	j	z	エ	コ	ン	レ		j	7
xxxx1011	(4)	+	;	K	[	k	[	オ	サ	ヒ	ロ		*	π
xxxx1100	(5)	,	<	L	*	1	1	7	シ	フ	ワ		φ	π
xxxx1101	(6)	-	=	M	]	m	]	ユ	ズ	ハ	コ		ε	÷
xxxx1110	(7)	.	>	N	^	n	+	ヨ	セ	ホ	ハ		h	
xxxx1111	(8)	/	?	O	_	o	+	ッ	リ	7	7		ö	■

* The user can specify any pattern for character-generator ROM.

Character Generator Rom (CG Rom)

Instruction Table

instruction	Code										Description	Execution time (when fosc is 250 kHz) Note.1	Execution time (when fosc is 160 kHz) Note 2
	RS	R/W	DB ₇	DB ₆	DB ₅	DB ₄	DB ₃	DB ₂	DB ₁	DB ₀			
Clear display	0	0	0	0	0	0	0	0	0	1	Clears all display and returns the cursor to the home position (Address 0).	82μs ~ 1.64ms	120μs ~ 4.9ms
Return home	0	0	0	0	0	0	0	0	1	•	Returns the cursor to the home position (Address0). Also returns the display being shifted to the original position. DD RAM contents remain unchanged.	40μs ~ 1.6ms	120μs ~ 4.8ms
Entry mode set	0	0	0	0	0	0	0	1	I/D	S	Sets the cursor move direction and specifies or not to shift the display. These operations are performed during data write and read.	40 μs	120 μs
Display ON/OFF control	0	0	0	0	0	0	1	D	C	B	Sets ON/OFF of all display (D), cursor ON/OFF (C), and blink of cursor position character (B).	40 μs	120 μs
Cursor and display shift	0	0	0	0	0	1	S/C	R/L	•	•	Moves the cursor and shifts the display without changing DD RAM contents	40 μs	120 μs
Function set	0	0	0	0	1	DL	N	F	•	•	Sets interface data length (DL) number of display lines (L) and character font (F).	40 μs	120 μs
Set CG RAM address	0	0	0	1	A _{CG}						Sets the CG RAM address. CG RAM data is sent and received after this setting.	40 μs	120 μs
Set DD RAM address	0	0	1	A _{DD}						Sets the DD RAM address. DD RAM data is sent and received after this setting.	40 μs	120 μs	
Read busy flag & address	0	1	BF	AC						Reads Busy flag (BF) indicating internal operation is being performed and reads address counter contents.	1 μs	1 μs	
Write data to CG or DD RAM	1	0	Write Data								Writes data into DD RAM or CG RAM.	40 μs	102 μs
Read data to CG or DD RAM	1	1	Read Data								Reads data from DD RAM or CG RAM.	40 μs	120 μs
	I/D = 1: Increment(+1) I/D = 0: Decrement (-1) S = 1: Accompanies display shift. S/C = 1: Display shift S/C = 0: Cursor move R/L = 1: Shift to the right. R/L = 0: Shift to the left. DL = 1: 8 bits DL = 0: 4 bits N = 1: 2 lines N = 0: 1 line F = 1: 5×10 dots F = 0: 5 × 7 dots BF = 1: Internally operating BF = 0: Can accept instruction										DD RAM: Display data RAM CG RAM: Character generator RAM A _{CG} : CG RAM address A _{DD} : DD RAM address Corresponds to cursor address. AC: Address counter used for both of DD and CG RAM address.	Execution time changes when frequency changes. (Example) When fosc is 270 kHz: 40 μs × _____ = 37 μs	

No effect

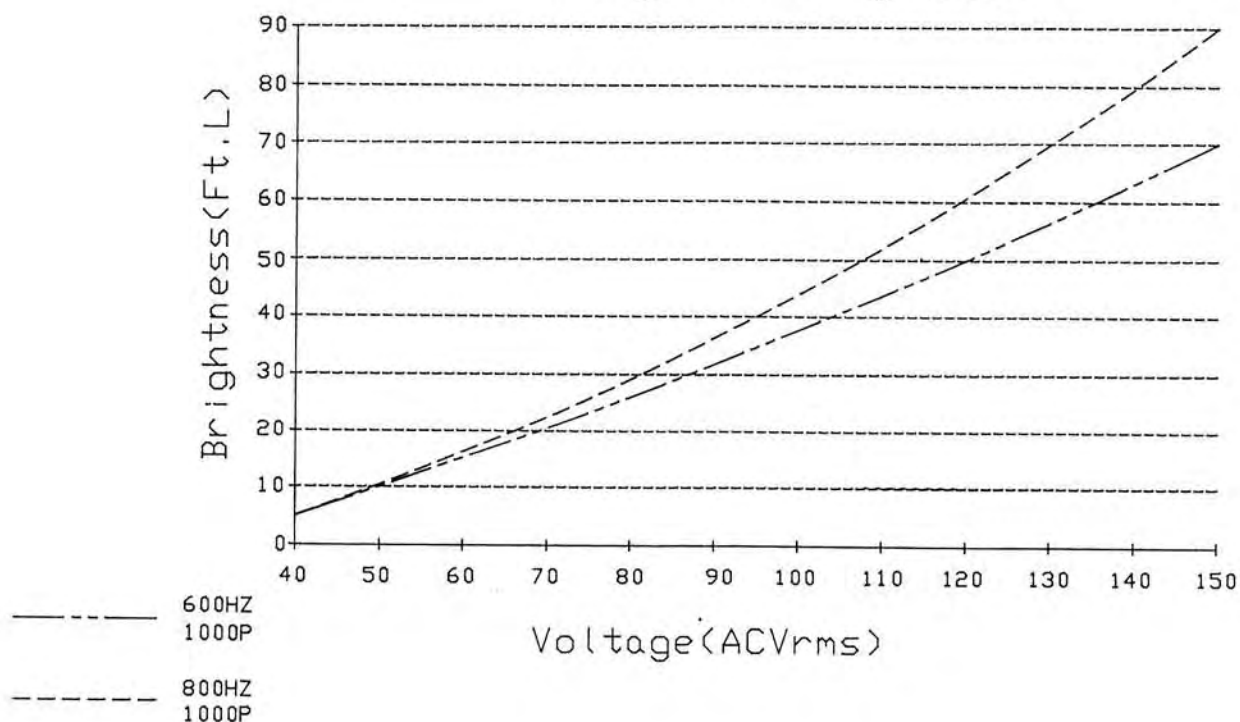
250 270

Dot Matrix Module With Backlight

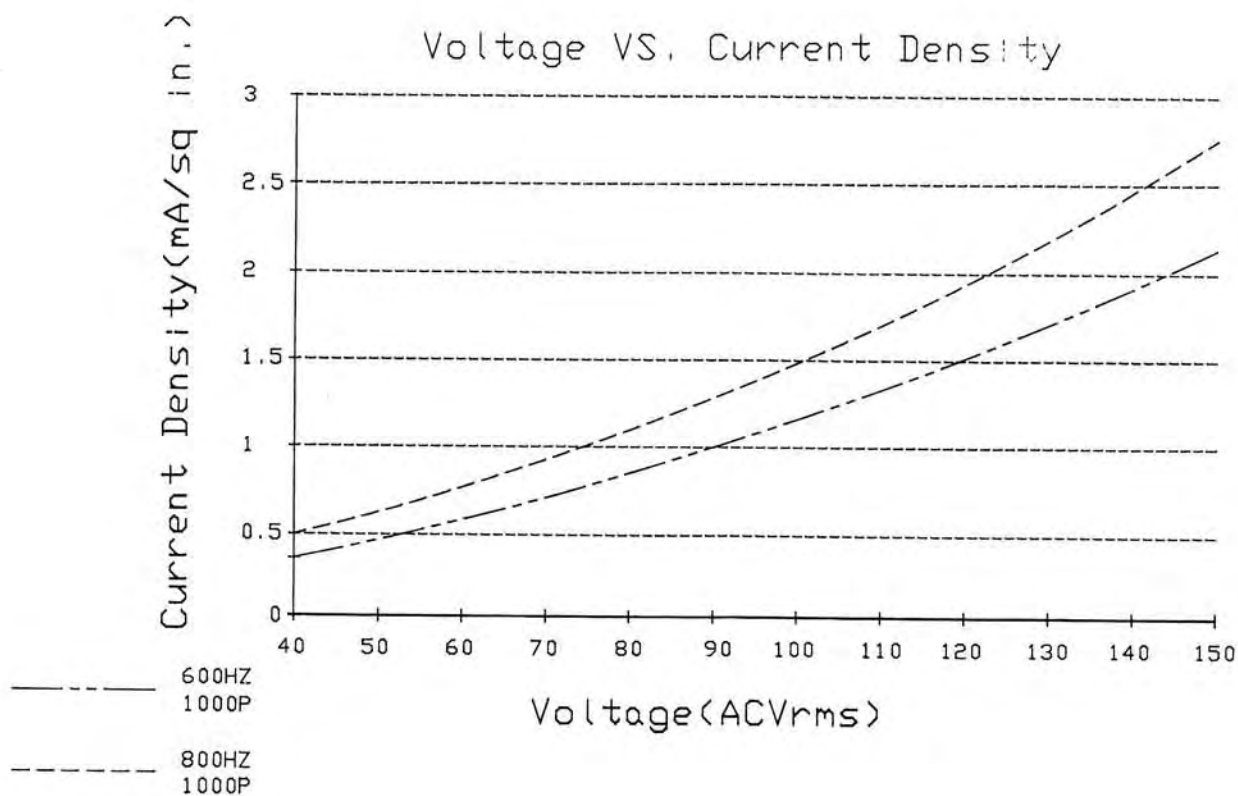
Electroluminescent backlighting

- THICKNESS: (AVG) 1.0mm
- Wide driving condition of 40-2000 Hz & 30V-250V (Typ: 120V, 400Hz)
- Standard Colors: Aviation Green, Blue Green, Yellow Green, Green, Warm White, Cool White, Auto White.
- Temp. range: Operating: $-40^{\circ}\text{C} \sim +55^{\circ}\text{C}$
Storage: $-65^{\circ}\text{C} \sim +65^{\circ}\text{C}$

Voltage VS. Brightness



Voltage VS. Current Density



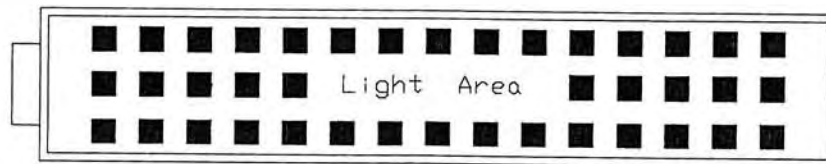
Light Emitting Diode Backlighting

- Lifetime: more than 100,000hrs.
- Low voltage DC: +5V
- Various color: Yellow Green (Standard), Red, Orange, Amber, Green (Option)
- 2 backlight methods are available: Bottom Backlight, Edge Backlight.

Example of Bottom Backlight (PVC160205 AYL)

Standard lamp styles:

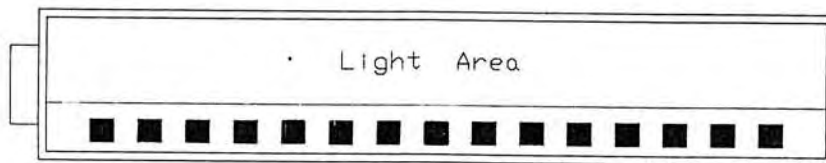
The LED chips are distributed over the whole light area of the illumination unit, which gives the most uniform light. As below:



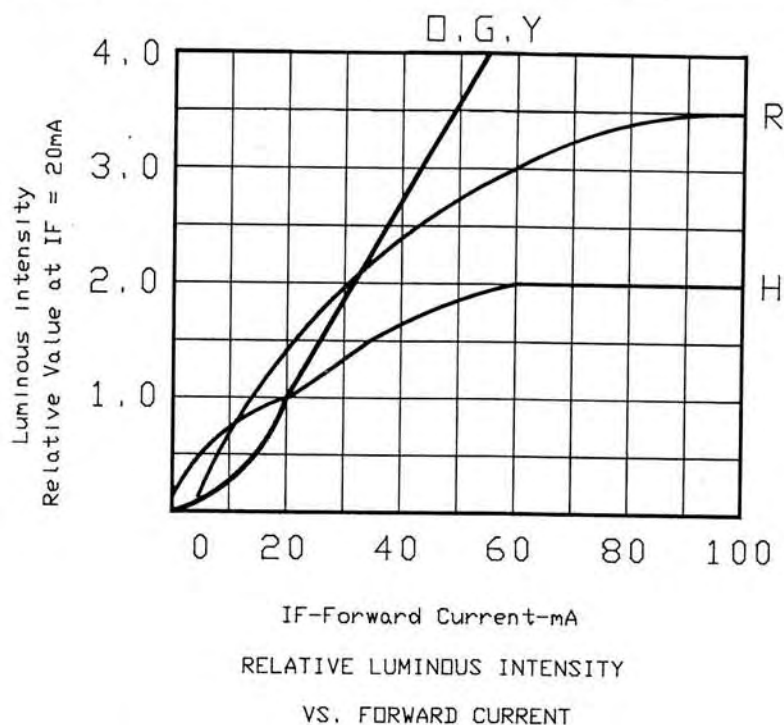
Example of edge backlight (PVC400201 AYL)

Standard lamp styles:

The LED chips are distributed over the edge of the illumination unit, which gives the most uniform light. As below:

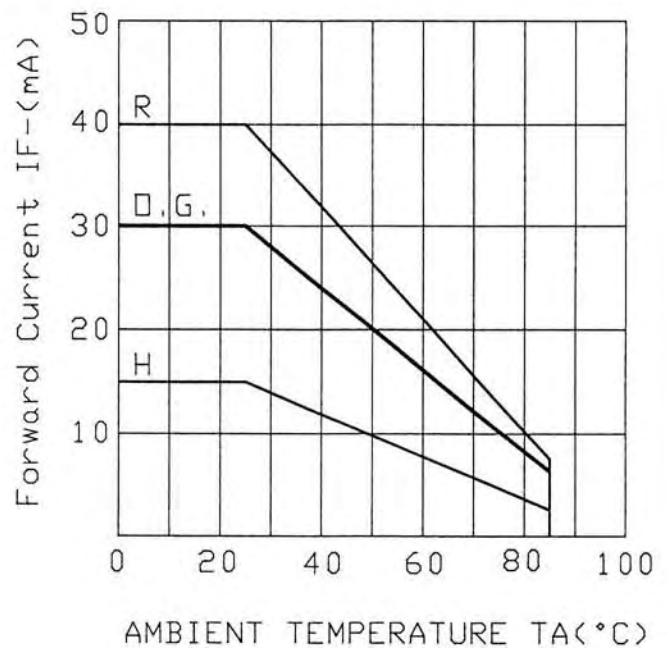
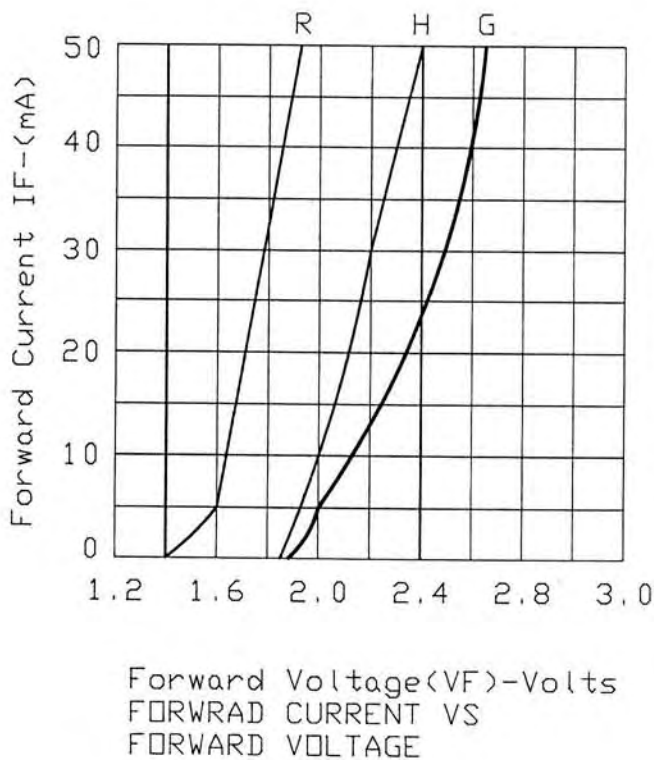
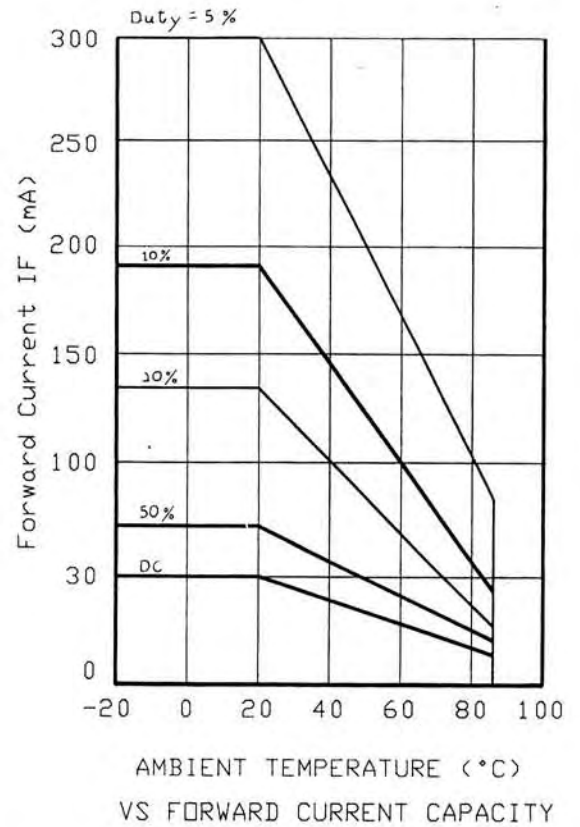
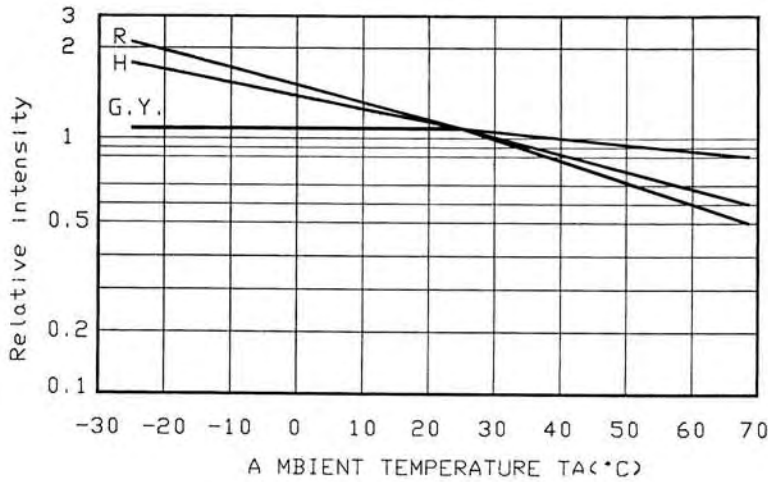


Characteristic curves



Light Emitting Diode Backlighting

Characteristic curves



NOTICE: 25 $^{\circ}\text{C}$ free air temperature unless otherwise specified

G: GREEN
Y: YELLOW
O: ORANGE

Optical Specifications Of 1/16 Duty TN Dot Matrix Module

Optical specifications ($T_a = 25^\circ\text{C}$, $V_{DD} = 5.0\text{V} \pm 0.25\text{V}$)

Item		Symbol	Min.	Typ.	Max.	Unit
View angle (Vertically)	$C_r \geq 4$	θ_v	25	—	—	Degree
View angle (Horizontally)	$C_r \geq 4$	ϕ	- 30	—	30	Degree
Contrast ratio		C_R	4	—	—	
Response time 25°C	(Rise)	T_{ON}	—	100	150	mS
Response time 25°C	(Decay)	T_{OFF}	—	120	150	mS

Optical specification of 1/16 duty stn dot matrix module

Item		Symbol	Min.	Typ.	Max.	Unit
View angle (Vertically)	$C_r \geq 2$	θ_x	- 35	—	35	Degree
View angle (Horizontally)	$C_r \geq 2$	θ_y	- 40	—	40	Degree
Contrast ratio		C_R	—	6	—	
Response time 25°C	(Rise)	T_{ON}	—	180	250	mS
Response time 25°C	(Decay)	T_{OFF}	—	190	250	mS

Mas rating absolute

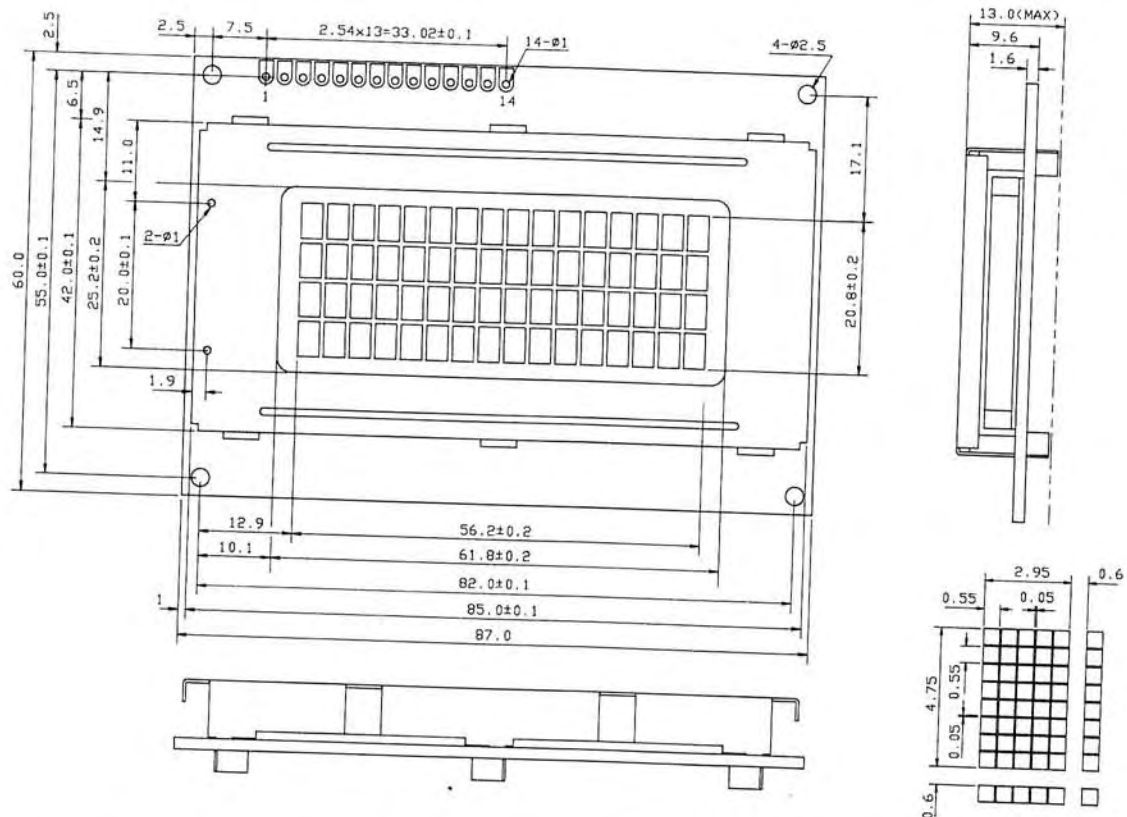
Item	Symbol	Min.	Typ.	Max.	Unit
Operating temperature	T_{op}	0	23	50	$^\circ\text{C}$
Storage temperature	T_{st}	- 20	25	70	$^\circ\text{C}$
Input voltage	V_i	V_{ss}	—	V_{DD}	V
Supply voltage for logic	$V_{DD}-V_{ss}$	0	5.0	6.5	V
Supply voltage for LCD	$V_{DD}-V_0$	0	—	6.5	V

Electrical characteristics ($T_a = 25^\circ\text{C}$, $V_{DD} = 5.0\text{V} \pm 0.25\text{V}$)

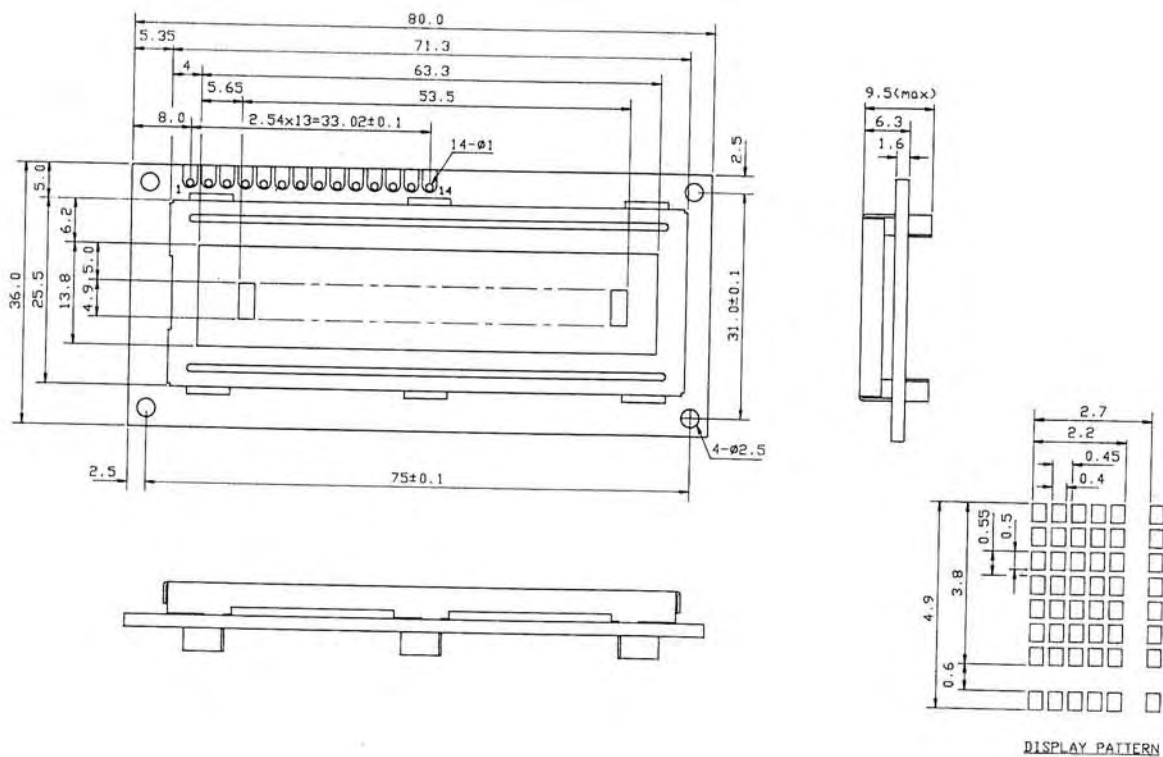
Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Supply voltage for LCD	$V_{DD}-V_0$	$T_a = 0^\circ\text{C}$	—	4.8	—	V
		$T_a = 25^\circ\text{C}$	—	4.5	—	V
		$T_a = 50^\circ\text{C}$	—	4.2	—	V
Input voltage	V_i	—	4.7	5.0	5.3	V
Input high voltage	V_{IH}	—	2.2	—	V_{DD}	V
Input low voltage	V_{IL}	—	0	—	0.6	V
Output high voltage	V_{OH}	$I_{OH} = 0.2\text{mA}$	2.4	—	—	V
Output low voltage	V_{OL}	$I_{OL} = 1.2\text{mA}$	—	—	0.4	V
Supply current	I_{DD}	$V_{DD} = 5.0\text{V}$	—	1.6	2.5	mA
Input leakage current	I_{LKG}	—	—	—	1.0	μA

Character Series

PVC160401ATL

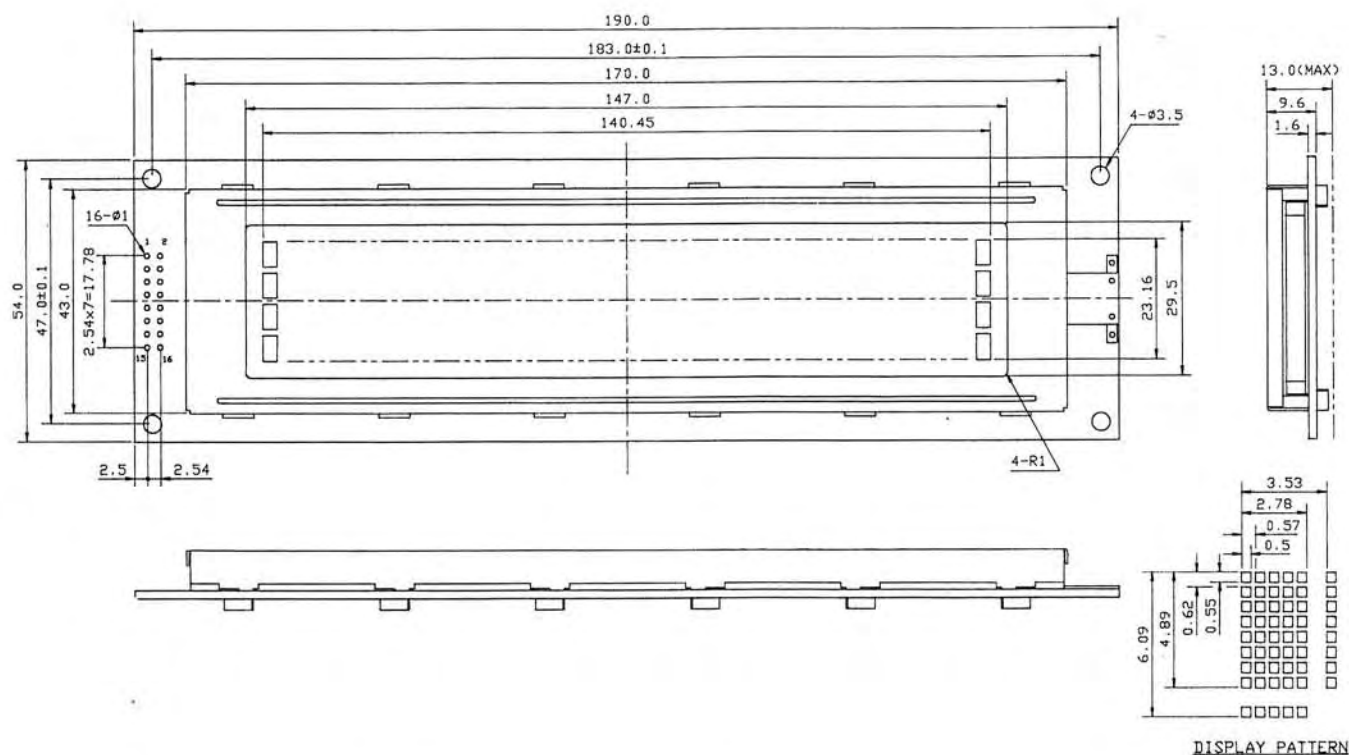


PVC200101ATN

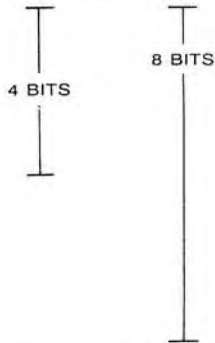


Character Series

PVC400401ATL



Interface pin connections

Pin NO.	Symbol	Level	Pin Description	Functions
1	DB7	H/L	Data bit 7	
2	DB6	H/L	Data bit 6	
3	DB5	H/L	Data bit 5	
4	DB4	H/L	Data bit 4	
5	DB3	H/L	Data bit 3	
6	DB2	H/L	Data bit 2	
7	DB1	H/L	Data bit 1	
8	DB0	H/L	Data bit 0	
9	E1	H, H/L	Enable signal for vpper panel	-
10	R/W	H/L	Read/Write	H: Read L: Write
11	RS	H/L	Register selection	H: Data Input L: Instruction code Input
12	V0	--	Contrast adjustment	Decision by user system
13	GND	-	Ground	0V
14	VDD	-	Supply voltage for logic	5V $\pm$ 5%
15	E2	H, H-L	Enable signal for lower panel	-
16	NC	-	No connection	

Initializing By Instruction:

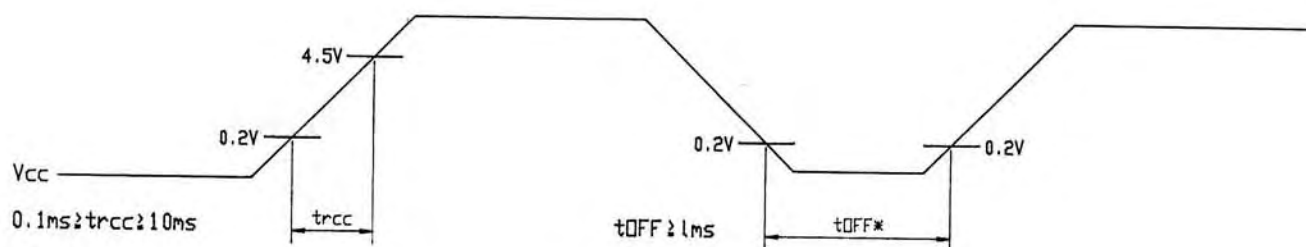
• Power Supply Conditions Using Internal Reset Circuit

If the power supply conditions for correct operation of the internal reset circuit are not met, initialization by instruction is required.

Item	Symbol	Test condition	Limit		Unit
			min	max	
Power Supply Rise Time	t_{rcc}	—	0.1	10	ms
Power Supply OFF Time	t_{OFF}	—	1	—	ms

• Power Supply Conditions Using Internal Reset Circuit

Since the internal reset circuit will not operate normally unless the preceding conditions are met, initialize by instruction. (Refer to "Initializing by Instruction")

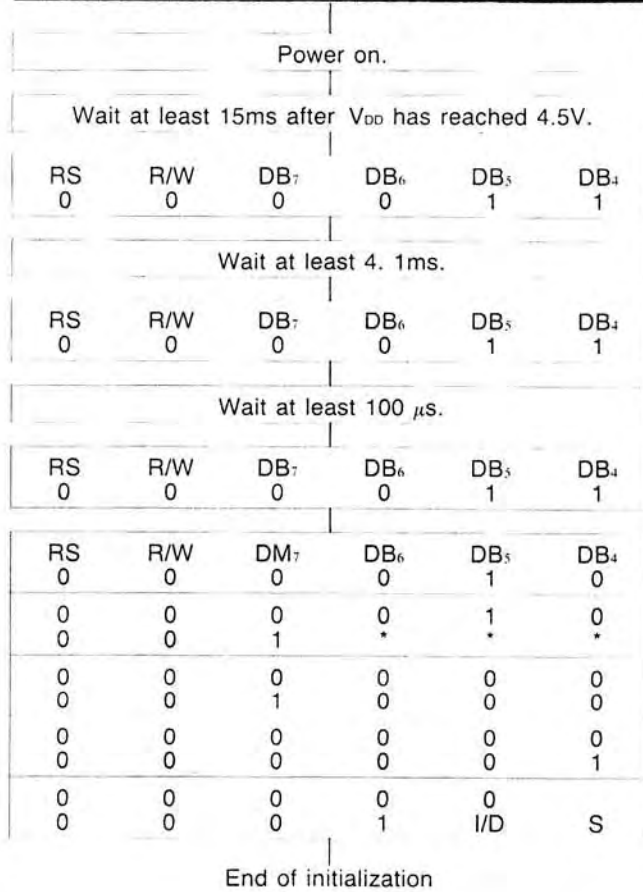


VCC 0.2V 4.5V t_{rcc} 0.2V $t_{OFF} \geq 1ms$ t_{OFF}^* 0.2V 0.2V $0.1ms \leq t_{rcc} \leq 10ms$

(Note) t_{OFF} stipulates the time of power OFF for momentary power supply instantaneous dip or when power supply cycles ON and OFF.

Initializing By Instruction:

How to initialize for which interface data length is 4 BITs



Busy flag cannot be checked before this instruction is executed.

Function set (interface data length of 8 bits)

Busy flag cannot be checked before this instruction is executed.

Function set (interface data length of 8 bits)

Busy flag cannot be checked before this instruction is executed.

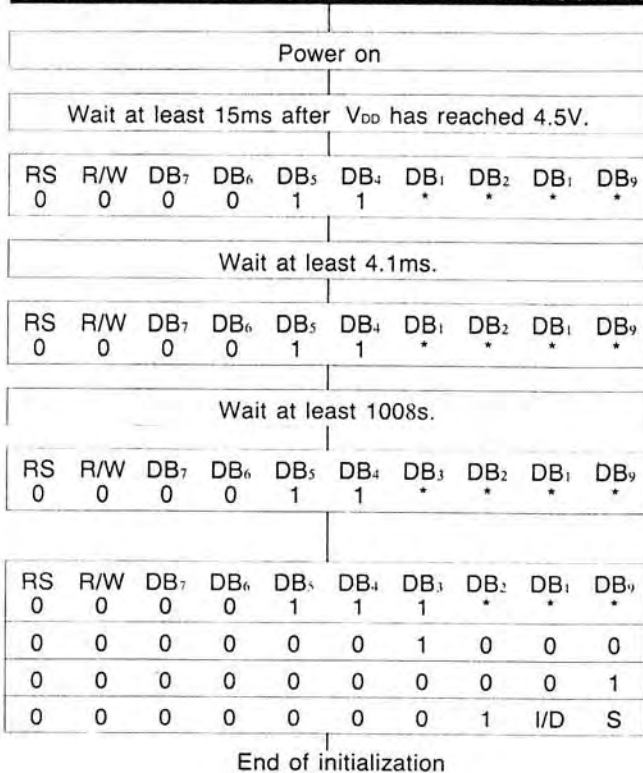
Function set (interface data length of a bits)

Busy flag can be checked from the following instructions on. When busy flag is not checked, the waiting time taken till the next instruction is given is required more than the executing time of instructions.

→ Function Set (set to interface data length of 4 bits) (instruction of 8 bits length).

→ Function Set
→ Display OFF
→ Display clear
→ Entry Mode Set

How to initialize for which interface data length is 8 BITs



Function set (interface data length of 8 bits)

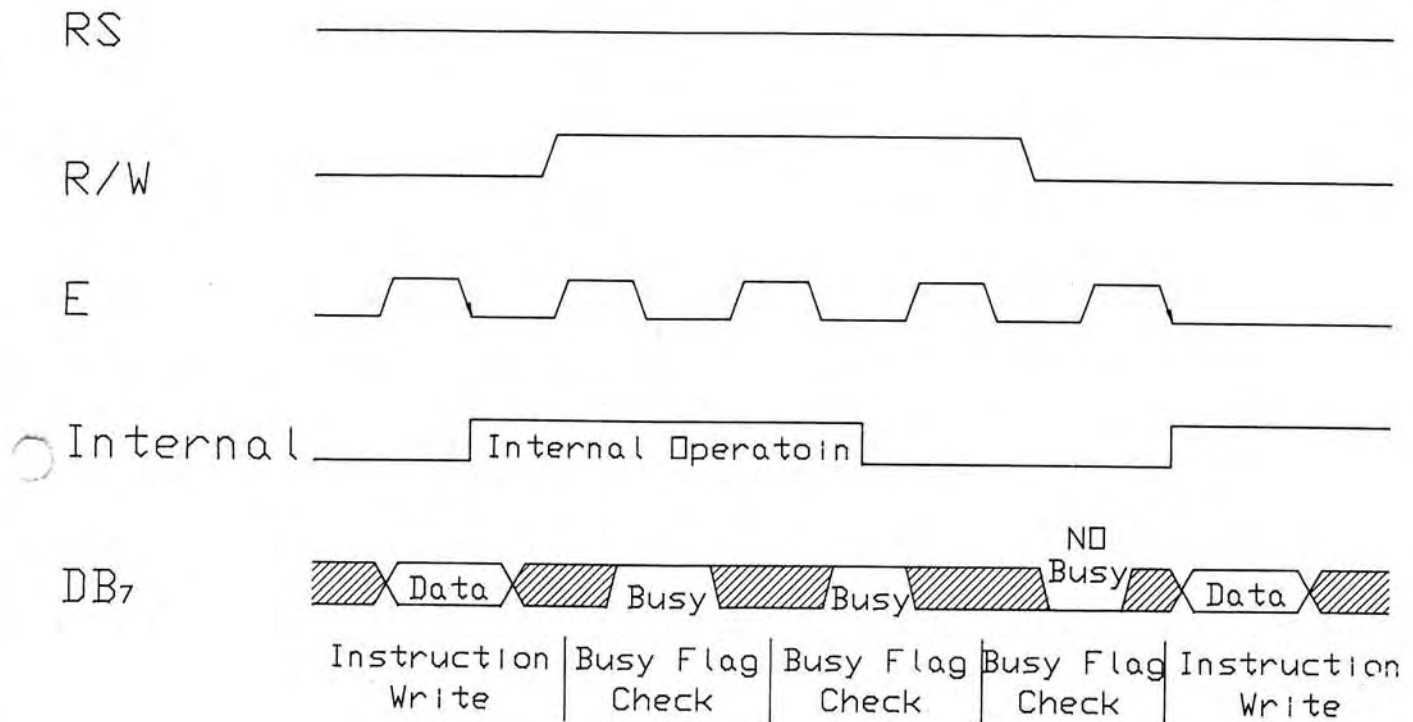
Function set (interface data length of 8 bits)

Busy flag can be checked from the following instructions on. When busy flag is not checked, the waiting time taken till the next instruction is given is required more than the executing time of instructions.

→ Function Set
→ Display OFF
→ Display clear
→ Entry Mode Set

Interface To Mpu

Interface to 8-BIT Mpu:

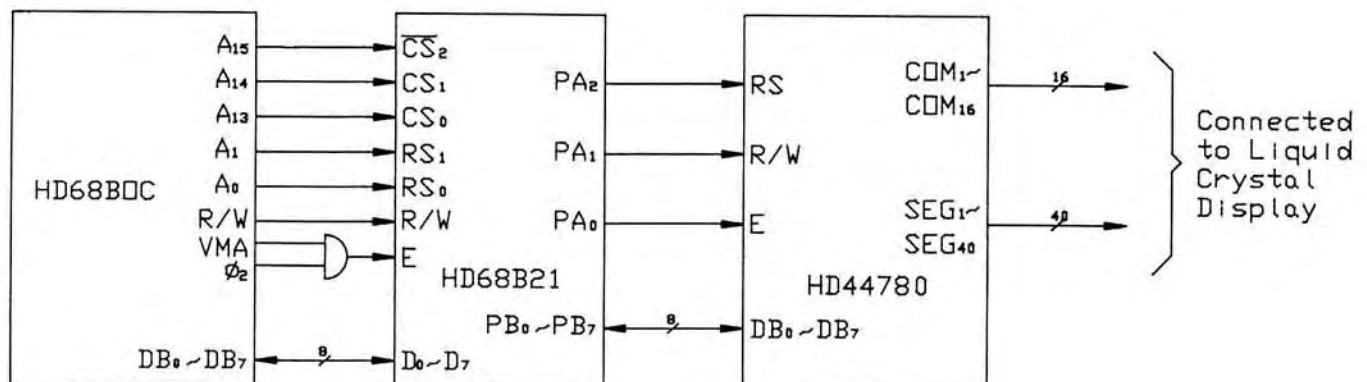


Example of Busy Flag Check timing sequence

- (1) When connecting to 8-bit MPU through PIA

Fig.13-2 is an example of using a PIA or I/O port (for single chip microcomputer) as an interface device. Input and output of the device is TTL compatible.

In the example, PB₀ to PB₇ are connected to the data buses DB₀ to DB₇ and PA₀ to PA₂ are connected to E, R/W and RS respectively. Pay attention to the timing relation between E and other signals when reading or writing data and using PIA as an interface.



HD68B00: 8 bit CPU

Example of Interface to HD68B00 Using PIA (HDG8B21)