AN1048
APPLICATION NOTE

ST7 SOFTWARE LCD DRIVER

by Microcontroller Division Applications

INTRODUCTION

This note describes a technique for driving Liquid Crystal Displays (LCD) with any standard ST7 Microcontroller (MCU) i.e without any specific on-chip LCD driver hardware. This technique offers a solution for applications which require a display at low cost together with the versatile capabilities of the standard ST72 MCU. This note also provides a technique to control the LCD contrast through software.

After an introduction on LCDs in Section 1, Section 2 & 3 of this note describes the typical waveforms required to drive an LCD with a multiplexing rate of 1 or 2 (duplex) and 4 (quadruplex). Section 3 presents a solution based on a standard ST7 MCU directly driving a quadruplex LCD. This solution can be implemented with any ST7 MCU as it only requires the standard
I/O ports and one timer, both of which are standard features on all ST7 MCUs. Section 4 describes how to control the contrast through software.

The program size (~300 bytes), the CPU load required for controlling the LCD (0.2%), and the number of external components is kept to the minimum (two external resistors per COM line). The number of I/O's is the same as a solution using an on-chip LCD hardware driver or an external hardware LCD driver. With software contrast control, it is a very flexible solution that can be adapted easily to a range of applications.

Rev. 1.1

1 LCD REQUIREMENTS

With a low Root Mean Square (RMS i.e.: $\sqrt{Mean(Signal^2)}$) voltage applied to it, an LCD is practically transparent. The LCD segment is inactive(OFF) if the RMS voltage is below the LCD threshold voltage and is active(ON) if the LCD RMS voltage is above the threshold voltage. The LCD threshold voltage depends on the quality of the liquid used in the LCD and the temperature. The optical contrast is defined by the difference in transparency of a LCD segment ON (dark) and a LCD segment OFF(transparent). The optical contrast depends on the difference between the RMS voltage on an ON segment (Von) and the RMS voltage on an OFF segment (Voff). The higher the difference between Von(rms) and Voff(rms), the higher the optical contrast. The optical contrast also depends on the level of Von versus the LCD threshold voltage. If Von is below or close to the threshold voltage, the LCD is completely or almost transparent. If Voff is close or above the threshold voltage, the LCD is completely dark.

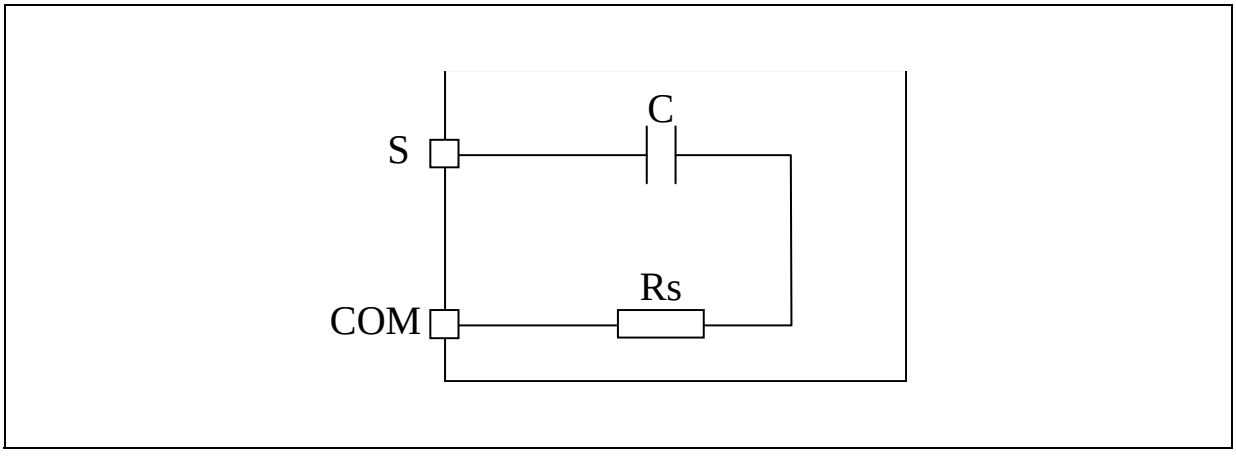
In this document, contrast is defined as D = Von(rms) / Voff(rms).

The applied LCD voltage must alternate to give a zero DC value in order to ensure a long LCD life time.

The higher the multiplexing rates, the lower the contrast. The signal period has also to be short enough to avoid visible flickering on the display.

The LCD voltage for each segment is equal to the difference between the S and COM voltages (see figure 1).

Figure 1. Equivalent Electrical Schematic of an LCD Segment



Notes: The DC Value should never be more than 100mV (refer to the LCD manufacturer's datasheet). Otherwise the life time can be shortened. The frequency range is 30 - 200Hz typically. If it is less, it flickers; if it is more, the power consumption increases.

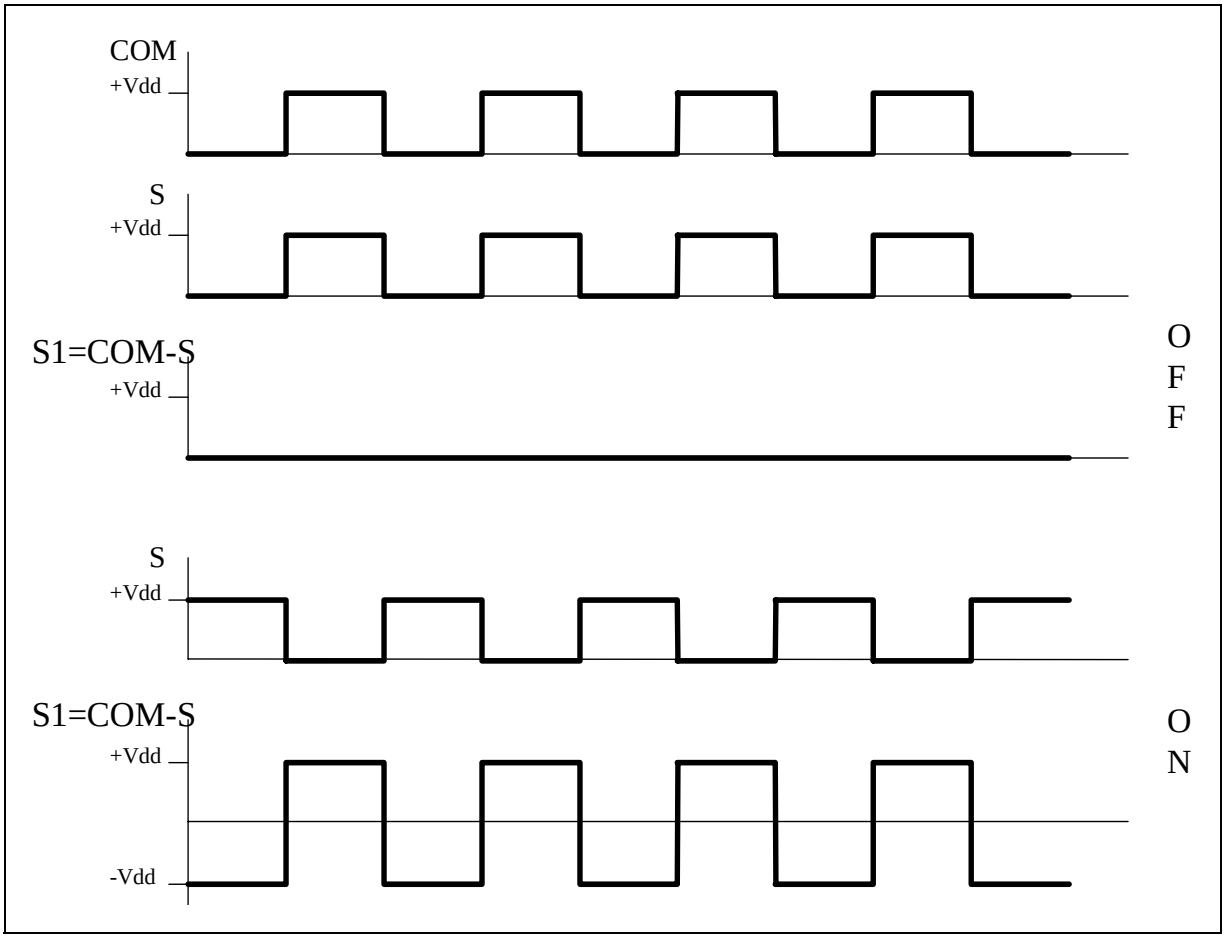
2 LCD DRIVE SIGNALS

2.1 SINGLE BACKPLANE LCD DRIVE

In a single backplane drive, each LCD segment is connected to a segment line(Sx) and to one backplane(common line) common to all the segments. A display using S segments is driven with S+1 MCU output lines. The backplane is driven with a "COM" signal controlled between 0 and Vdd with a duty cycle of 50%.

When switching a segment "ON", a signal with opposite polarity to "COM" is sent to the corresponding "Segment" pin. When the non-inverted signal "COM" is sent to the "Segment" pin, the segment is "OFF". Using an MCU, the I/O operates in output mode either at logic 0 or 1.

Figure 2. LCD Signals for Direct drive



2.2 DUPLEXED LCD DRIVE

In a duplexed drive, two backplanes are used instead of one. Each LCD segment line(Sx) is connected to two LCD segments, each one connected on the other side to one of the two backplanes or common lines(refer to figure 3). Thus, only (S/2)+2 MCU pins are necessary to drive an LCD with S segments.

Three different voltage levels have to be generated on the backplanes : 0, $V_{DD}/2$ and V_{DD}. The “Segment” voltage levels are 0 and Vdd only. Figure 4 shows typical Backplane, Segment and LCD waveforms. The intermediate voltage $V_{DD}/2$ is only required for the Backplane voltages. The ST7 I/O pins selected as “Backplanes” are set by software to output mode for 0 or Vdd levels and to high impedance input mode for $V_{DD}/2$. When one backplane is active, the other one is neutralised by applying Vdd/2 to it. This Vdd/2 voltage is defined by two resistors of equal value, externally connected to the I/O pin. By using an MCU with flexible I/O pin configuration, a duplexed LCD drive can be implemented with only 2 external resistors bridge (each on two com lines).

Figure 3. Basic LCD Segment Connection in duplexed mode

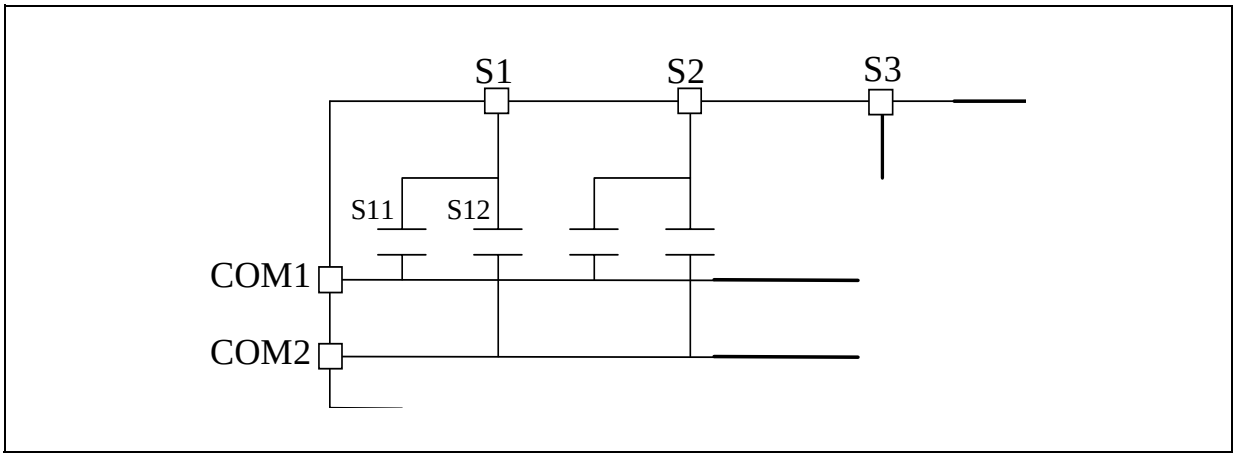
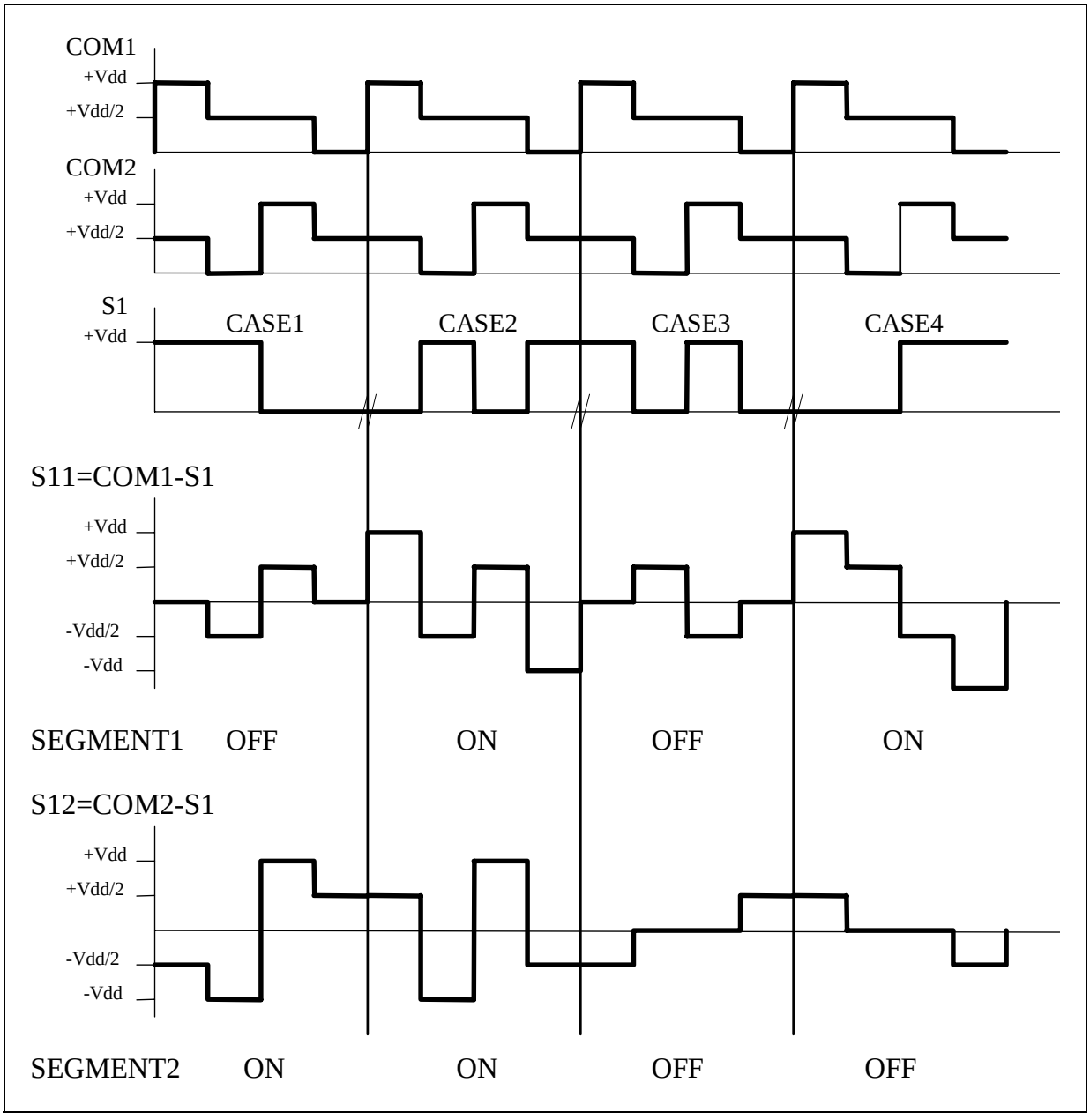


Figure 4. LCD signals for duplexed mode (used in the ST7 example)



2.3 QUADRUPLEX LCD DRIVE

In a quadruplex LCD drive, four backplanes are used. Each LCD pin is connected to four LCD segments, with each segment connected on the other side to one of the four backplanes. Thus, only (S/4)+4 MCU pins are necessary to drive an LCD with S segments. For example: to drive an LCD with 128 segments (32 x4), only 36 I/O ports are required (32 I/O ports to drive the segments, 4 I/O ports to drive the backplanes).

Three different voltage levels have to be generated on the common lines: 0, Vdd/2, Vdd. The Segment line voltage levels are 0 and Vdd only. The LCD segment is inactive if the RMS voltage is below the LCD threshold voltage and is active if the LCD RMS voltage is above the threshold. Figure 6 shows typical Backplane, Segment and LCD waveforms. The intermediate voltage Vdd/2 is only required for Backplane voltages. The MCU I/O pins selected as “Backplanes” are set by software to output mode for 0 or Vdd levels and to the high impedence input mode for Vdd/2. The Vdd/2 voltage is defined by two resistors of equal value, externally connected to the I/O pins. When one backplane or COM is active, the other ones are neutralized by applying Vdd/2 to them.

Figure 5. Basic LCD Segment Connection in Quadruplexed Mode

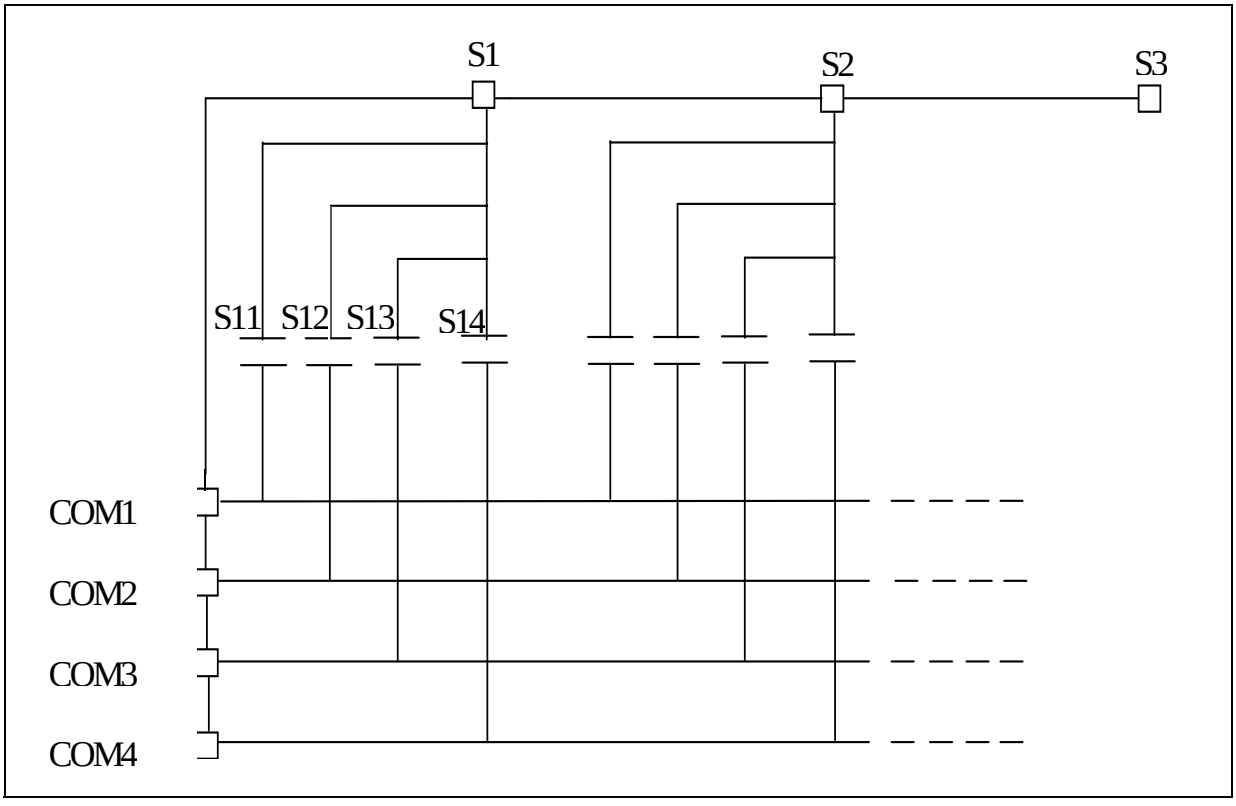


Figure 6. LCD timing diagram for Quadruplex Mode

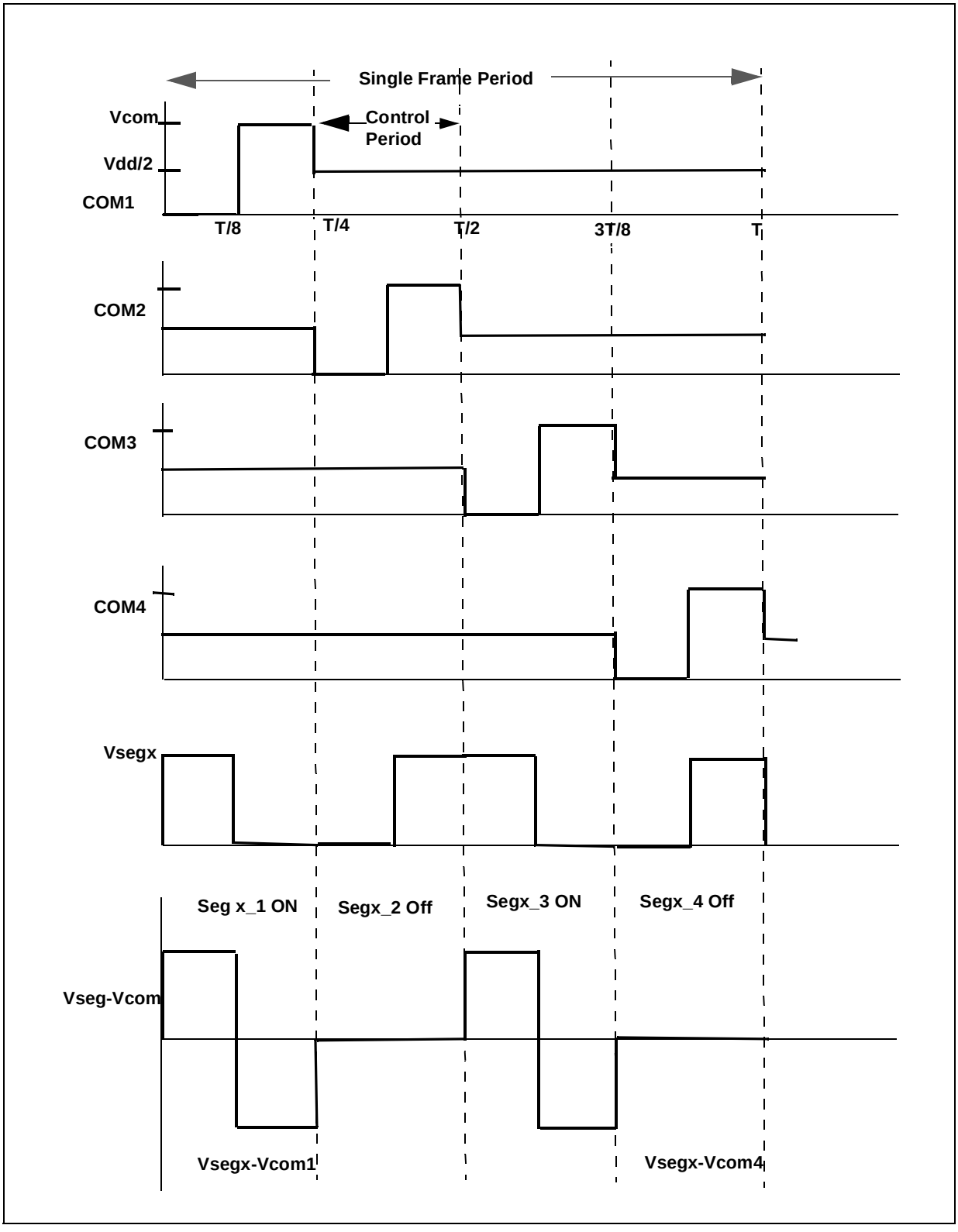
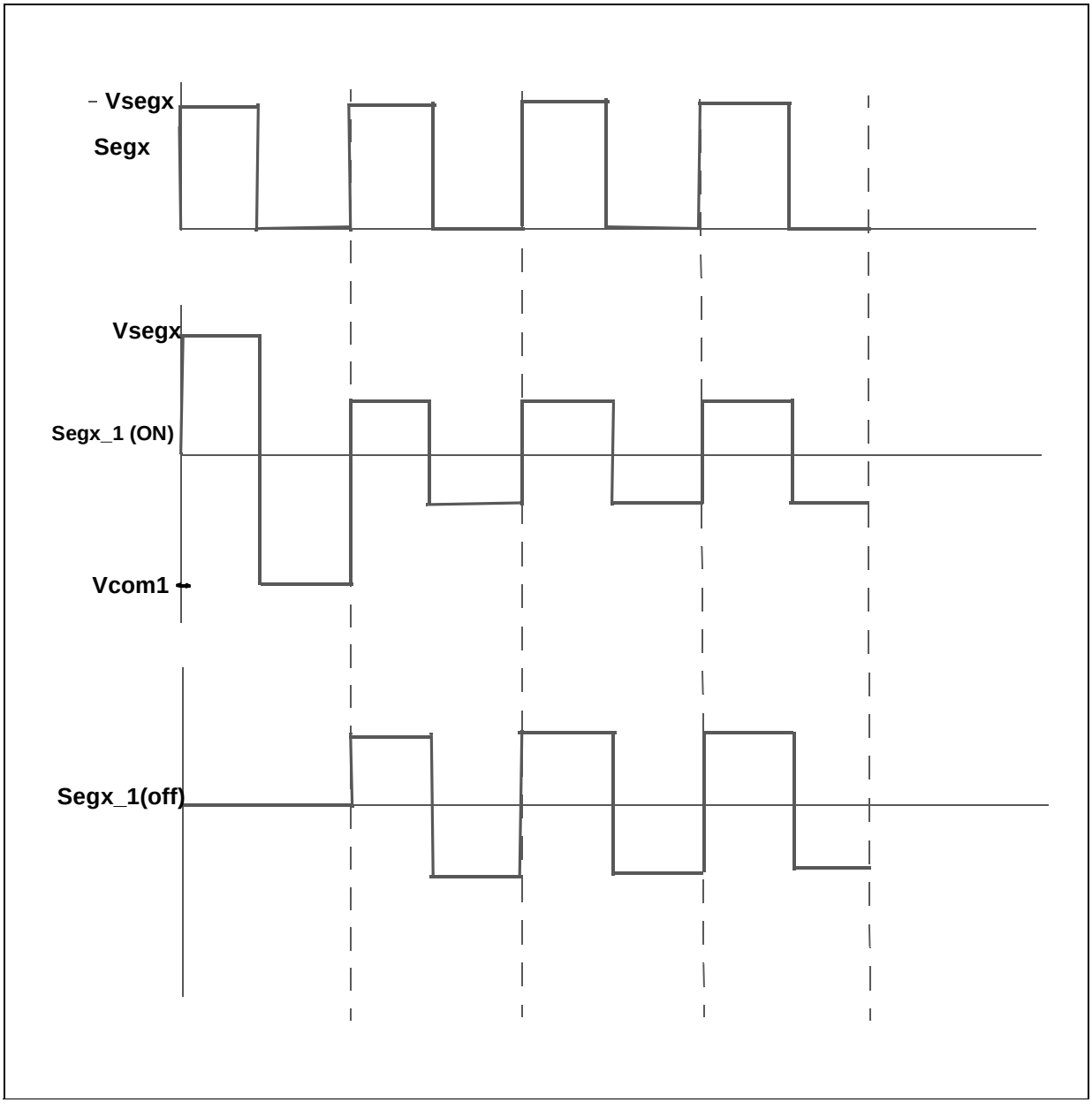


Figure 7. LCD Timing Diagram for a single segment



2.3.1 LCD Mean Voltage Calculation

The LCD mean voltage must be very close to zero to guarantee long life to the LCD. The LCD mean voltage for ON and OFF periods can be calculated as-

Vmean(ON) = 1/8 Vseg + 1/8 (-Vcom) + 3(Vseg - Vr/2) + 3(-Vr/2) ----(1)

Vmean(Off) = 3(Vseg/2) + 3(-Vr/2) -----(2)

Vmean(ON) and Vmean(Off) assume identical periods for each phase.

From eqn (1) & (2), to get Vmean(ON) and Vmean(Off) = zero

Vseg = Vcom = Vr = Vcc

Where:

Vcom = Max voltage on COM line

Vr/2 = Voltage in the middle of the resistor bridge applied on the COM line

Vseg = Max voltage on Segx line

Vcc = Microcontroller power supply

2.3.2 CONTRAST CALCULATION

The performance of an LCD driving system is defined by the contrast-

Contrast(D) = Vrms(ON) / Vrms(Off)

For the quadruplex signal as described on the previous page:

$$Vrms(ON) = \sqrt{1/T \int_0^T (f(t))^2 dt}$$

$$Vrms(ON) = \sqrt{1/T \left(\int_0^{T/8} (Vcc)^2 dt + \int_{T/8}^{2T/8} (-Vcc)^2 dt + \int_{2T/8}^{T} (Vcc/2)^2 dt \right)}$$

$$Vrms(ON) = \sqrt{1/T \left((Vcc^2 \times T/8) + (Vcc^2 \times T/8) + (Vcc^2/2)(6T/8) \right)}$$

$$Vrms(ON) = \sqrt{14\, Vcc / 32}$$

$$Vrms(ON) = 0.661Vcc$$

$$Vrms(Off) = \sqrt{1/T \left(\int_{0}^{T/8} (0)\, dt + \int_{T/8}^{2T/8} (0)\, dt + \int_{2T/8}^{T} (Vcc/2)^2\, dt \right)}$$

$$Vrms(Off) = \sqrt{3/16\, Vcc^2}$$

$$Vrms(Off) = 0.43\ Vcc$$

Contrast(D) = Vrms (On) / Vrms (Off) = 0.661 / 0.43 = 1.52

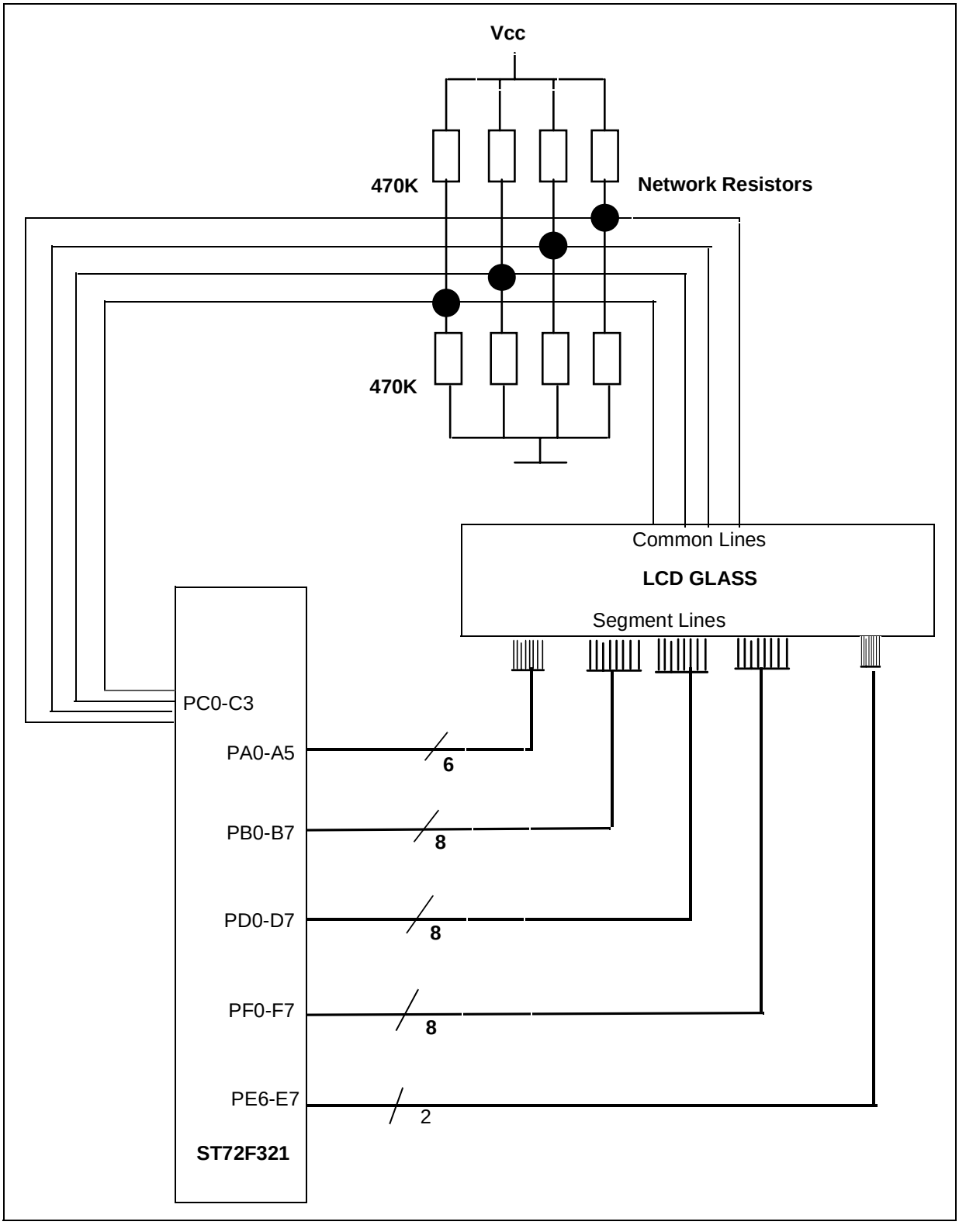
For comparison, a hardware LCD drive uses 1/3 bias voltage. With 1/3 bias control, the contrast value (D) is **1.73** . Therefore, 1/3 bias gives only a small advantage of contrast versus temperature. This advantage is reduced to zero when using software contrast control.

3 EXAMPLE OF A QUADRUPLEX LCD WITH ST72F321

The following example describes a drive for a quadruplex mode (4COM) LCD using the ST72F321 (TQFP64 pin package 10 x 10). Refer to Figure 8. The only external components needed for driving the LCD are eight resistors. One I/O port per segment and one I/O port for each COM line are needed to drive the LCD. For example: To drive a quadruplex LCD that has 128 segments (with 32 segment lines and 4 COM lines) requires only a total of 36 I/O ports.

In the example program, the Port PA0-A5 , PB0-B7, PD0-D7, PF7-F0, PE7-E6 pins are connected to the 32 segment lines and are used to generate the segment signals. Ports PC3...PC0 are connected to the 4 COM lines and used to generate the COM signals. The LCD driver consists of two initialization routines (port init, timer init) and a TimerA interrupt routine “timer_rt”. To activate the LCD, these two initialization routines have to be called. After these routines are called, the ST7 gets the timer Output Compare 1 & Output Compare 2 interrupts.

Figure 8. Hardware Connection Diagram



The LCD Timing is generated by the TimerA ouput compare interrupt. Each cycle consists of four phases, one for each backplane. Each COM line generates its waveform during the corresponding phase e.g. COM1 line during phase1. During other phases it remains at level Vdd/2. Each phase consists of two parts:

1. Active time

2. Dead time

During the Active time, the segment lines and COM lines are used to drive the LCD. During dead time Segment and COM lines are used to tune the contrast.

Active time starts after the Output Compare 1 interrupt and dead time starts after the Output Compare 2 interrupt. A total of 16 interrupts are generated in each frame period with four interrupts per control period. There are 2 Output Compare 1 events (OC1_1 and OC1_2) and 2 Output Compare 2 events in each phase.These are explained as follows:

During OC1_1, Vdd is applied to the segments which have to be turned ON and 0 for the segments which have to be turned OFF. The COM line which corresponds to this phase is set to low level. Other COM lines are set to level Vdd/2.

During OC2, all segments and COM lines are inactive (set to low level) if we want to decrease the Vrms (see Figure 9) and COM lines are set low, segments are set high if we want to increase the Vrms (see Figure 10).

During OC1_2, Segment Lines are supplied with voltage levels which are inverted to the one applied during OC1_1.COM line which corresponds to this phase is set to high level.Other COM lines are set to level Vdd/2.

Again during OC2, all segments and COM lines are inactive(set to low level) if we want to decrease the Vrms and COM lines are set high, segments are set low if we want to increase the Vrms (see Figure 10).

Figure 9. LCD timing diagram with Dead & Active Time (to decrease Vrms)

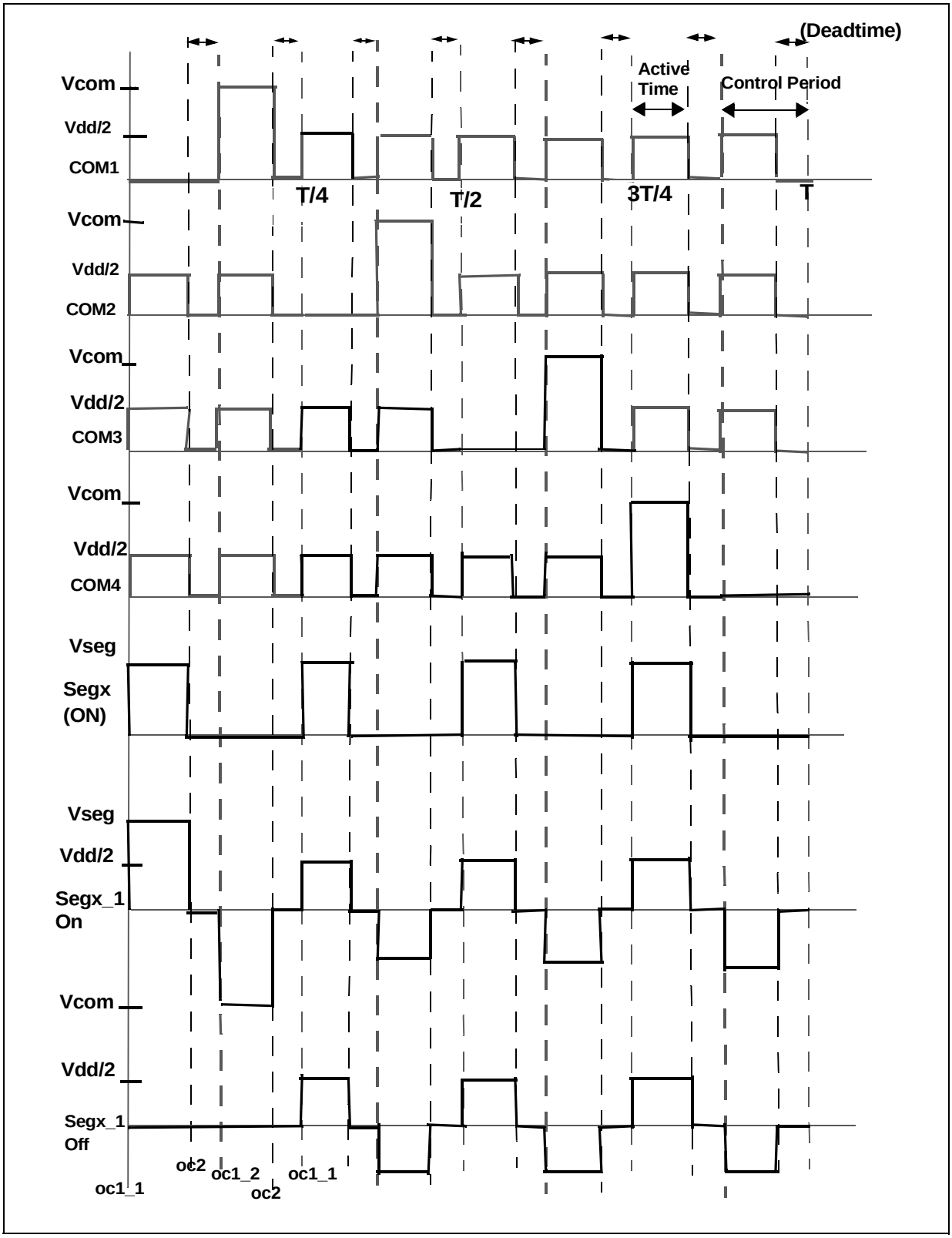
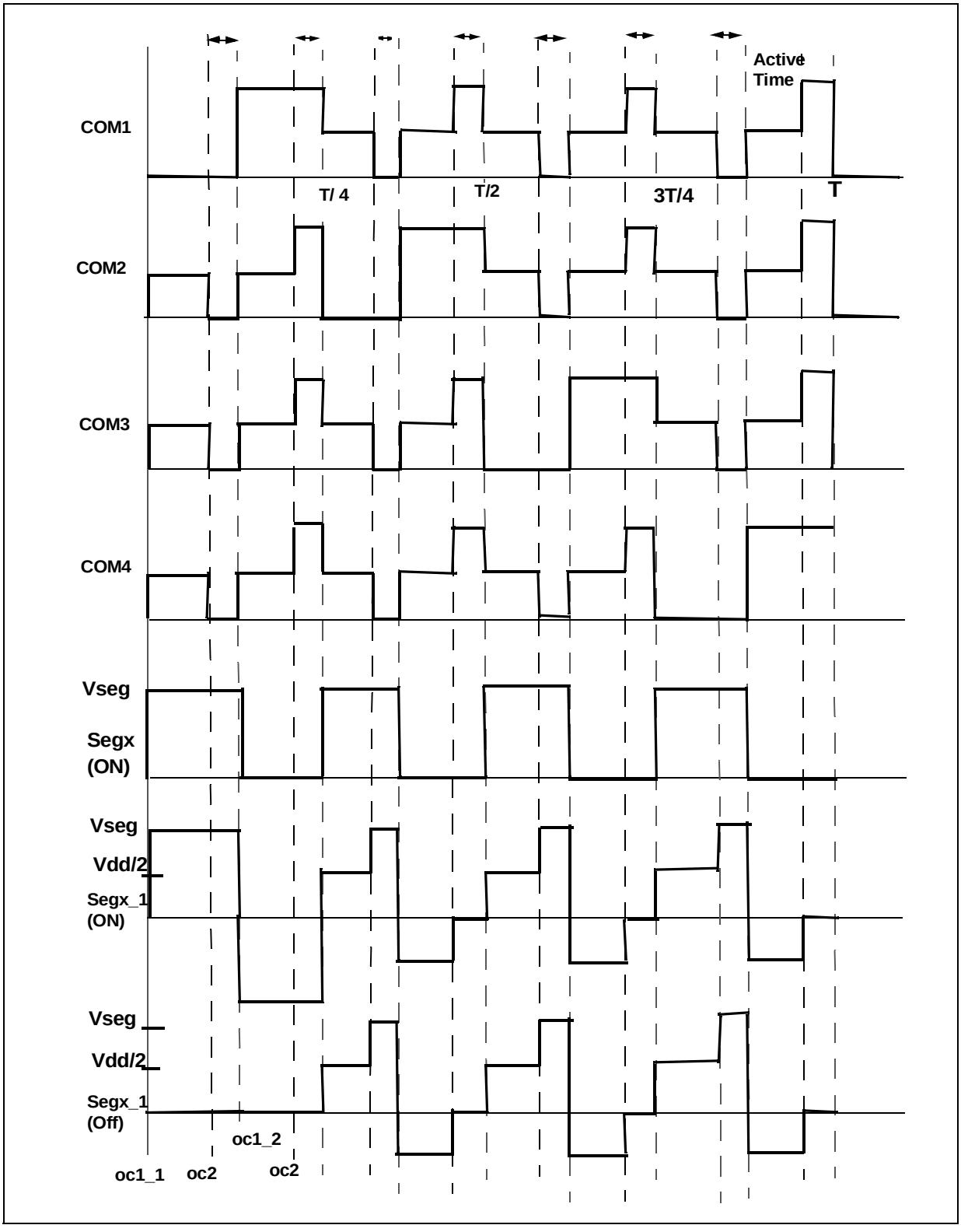


Figure 10. LCD timing diagram with Active and dead time (to increase Vrms)



4 SOFTWARE CONTRAST CONTROL

The software contrast control is under pending patent from STMicroelectonics. The use of this techniques with none STMicroelectonics' Microcontroller has to be agreed by STMicroelectronics.

The LCD contrast is controlled entirely by software without the use of any external components. LCD contrast can be adjusted by the user to the optimal value depending on the operating voltage of the LCD used. The LCD contrast is controlled by varying the timing of dead phase as shown in the LCD timing diagram.

Deadtime can be used to decrease as well as to increase the Vrms of the LCD. Deadtime is the voltage compensation time to regulate rms voltage up and down. Dead time can be implemented either after each control period or at the end of the frame. To avoid flickering, the duration of the dead time must be adjusted depending on the quality of LCD and the frequency of the frame.

In the example in Figure 9, the Rms value of the LCD decreases if the duration of dead time is increased and Rms value increases if the duration of dead time decreases. In Figure 10, this works the opposite way.

4.1 CONTRAST CALCULATIONS

Let the frame period = T + xT

where T - Active Time

xT - Dead Time

$$Vrms\ (ON) = \sqrt{\frac{1}{T+xT}\int_{0}^{T+xT} (f(t))^2\ dt}$$

$$Vrms\ (ON) = \sqrt{\frac{1}{T+xT}\left(\int_{0}^{T/8} (Vcc)^2\ dt + \int_{0}^{2T/8} (-Vcc)^2\ dt + \int_{0}^{2T/8} (Vcc/2)^2\ dt + \int_{0}^{xT/8} (Vx\ dt)^2 . 8\right)}$$

x- Proportion of dead time

$$Vrms\ (ON) = \sqrt{\frac{1}{T+xT}\left((Vcc)^2 . T/8 + (Vcc)^2 .T/8 + (Vcc)^2 / 4 + (Vx . T/8)^2 . 8\right)}$$

Since Vx = 0 (in case of a decrease in Vrms)

$$Vrms(ON) = \sqrt{\frac{1}{1+x}\left(14Vcc/32\right)^2 + \left(Vx\right)^2 . x}$$

$$Vrms(ON) = \sqrt{\frac{1}{1+x}\left(14Vcc/32\right)^2}$$

$$Vrms(ON) = \sqrt{\frac{1}{1+x}} \quad 0.661\ Vcc$$

$$Vrms(Off) = \sqrt{\frac{1}{T+xT}\left(\int_0^{T/8} 0\ dt + \int_0^{2T/8} 0\ dt + \int_0^{2T/8} (Vcc/2)^2\ dt + \int_0^{xT/8} (Vx\ dt)^2 . 8\right)}$$

$$Vrms(Off) = \sqrt{\frac{1}{1+x}\left(6Vcc/32\right)^2 + Vx^2 . x}$$

Since Vx = 0 (in case of a decrease in Vrms)

$$Vrms\ (Off) = \sqrt{\frac{1}{1+x}}\ 0.18\ Vcc$$

Dx = Vrms(ON) / Vrms(Off) =

$$\frac{\sqrt{\frac{1}{1+x}}\ 0.661\ Vcc}{\sqrt{\frac{1}{1+x}}\ 0.18\ Vcc} = \mathbf{D}$$

Where Dx = Contrast with contrast control

The contrast D, between Von and Voff is constant (quality of contrast). We only change the optical contrast by tuning Von close to the threshold value of the LCD.

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