ispXP Technology Power-up and Hot Socketing

December 2002 Technical Note TN1041

Introduction

The ispXP™ (eXpanded in-system Programmable) device families from Lattice offer the non-volatility of E^2 cells together with the infinite reconfigurability of SRAM. This is achieved by the one-to-one relationship between SRAM memory and E^2 cells, where SRAM is used to control the functionality of the device during normal operation, and E^2 cells are used to store information for SRAM configuration. By combining the strengths of E^2 cells and SRAM, the ispXP device families are able to provide instant-on logic at power-up, high security during reconfiguration, and simplified system design with a single-chip solution. This special feature represents a breakthrough in programmable logic technology. In order to utilize the ispXP feature to its full potential, users need to understand the behavior of the ispXP devices under various board conditions. This technical note addresses two important topics related to device behavior. The first is the power-up characteristic of the ispXP devices. The second is the I/O characteristics of the latest Lattice products including the ispXPGA™, ispXPLD™, ispMACH® 4000, and the ispGDX2™ device families. Detailed analysis of power-up/power-down sequences will also be discussed.

ispXP Power-up Characteristics

The SRAM is a volatile technology and requires refresh/initialization at power-up before beginning the normal operation. The ispXP devices accomplish this by automatically downloading the contents of on-chip E^2 cells into SRAM memory at every power up. This automatic process is triggered by the V_{CC} threshold with proper settings of the CFG0 and PROGRAM pins. The whole process typically takes less than 200μs to complete. The download trip point at 1.4V is tightly controlled in the hardware and is independent of the V_{CCO} level and settings. With CFG0 and PROGRAM pins both set to logic high (the default value), any V_{CC} value below the trip point will guarantee an automatic SRAM refresh. Thus V_{CC} does not need to go to zero for this automatic refresh to occur. Although monotonic V_{CC} at power up is recommended, the contents of SRAM will remain intact as long as the V_{CC} is above the recommended minimum value.

I/O Hot Socketing Characteristics

For a device to function well in a hot socketing environment, it is critical that there are no abnormal current surges on the pins, and that no V_{CC}/V_{CCO} sequencing is required during the power-up or power-down process. The ispXPGA, ispXPLD, ispMACH 4000 and ispGDX2 families are well suited for applications that require the hot socketing capability. There is no V_{CC}/ V_{CCO} power-up or power-down sequence requirement for these families and the typical input or I/O leakage current at room temperature is in low μA per pin. Refer to individual data sheets for the specification of each device family. The following input/output (I/O) characteristic plots illustrate the typical behaviors of the ispXPGA, ispXPLD, ispMACH 4000 and ispGDX2 devices in a hot socketing environment.

V_{CC} and V_{CCO} of the Latest Lattice Products

There are two types of power supply pins in the ispXPGA, ispXPLD, ispMACH 4000 and ispGDX2 families. The V_{CC} pin supplies the power for the core of the device, while V_{CCO} supplies power for the I/O pins of the device. The V_{CCO} pin is used to set the output voltage for the entire I/O bank. Therefore I/O standards that do not have the same V_{CCO} value cannot be used in the same I/O bank. The number of I/O banks of a device determines the number of available V_{CCO} pins. For example, in the ispGDX2, there are eight V_{CCO} pins or one per I/O bank as shown in the ispGDX2 data sheet, sysIO banks figure.

V_{CC} and V_{CCO} Sequencing

In order to ensure proper operation, the ispXPGA, ispXPLD, ispMACH 4000 and ispGDX2 devices are designed in such way that all the pins of an I/O bank will remain tri-stated when one of the power pins, either V_{CC} or its corresponding $V_{CCO,}$ is not powered up. In other words, only when both V_{CC} and V_{CCO} are supplied with power, will a device and its corresponding I/O pins start to respond. However, in a hot socketing environment there is no guarantee as to which power supply will become available to the device first. To thoroughly understand the behavior of the

Lattice device under these random situations, it is necessary to know when the device outputs turn on and off during a power-up or power-down cycle so that proper load/behavior on the board can be expected. Two combinations of V_{CC}/V_{CCO} sequencing are considered and examined in this technical note for both lower voltage (1.8V) and upper voltage (2.5/3.3V) devices. Figures 1a through 3b show a sample of the typical V_{CC} and V_{CCO} ramp sequencing plots taken at room temperature. The Lattice internal characterization test covers not only the sequencing but also the various ramp rates from microseconds to tens of milliseconds for V_{CC} and V_{CCO}.

Test Condition for the Following Data Plots: V_{CC} Ramps with V_{CCO} Applied

Under this condition, the V_{CCO} pin is always connected to a stable power supply while the V_{CC} pin is being powered up or down. A simple non-inverting buffer pattern is used in the analysis. It is observed that the internal pull-up on the output pin will be activated at about 0.8V $V_{CC,}$ then the output will follow the user-defined state at about 1.5V V_{CC} as indicated by Figures 1a and 1b. The I/O behaviors are taken with a 10Kohm pull-down resistor connected to the output pin. Figure 1c shows the power-down sequence under the same setups as Figures 1a and 1b. Figures 2a, 2b and 2c show the I/O behavior with a 1Kohm pull-down resistor connected to the output pin. As shown in these plots, the internal pull-up can be overridden with an external 1Kohm pull-down resistor.

Figure 1a. V_{CC} power-up from 0V to 1.8V, V_{CCO} = 2.5V (pull-down on input, output with external 10Kohm pull-down resistor)

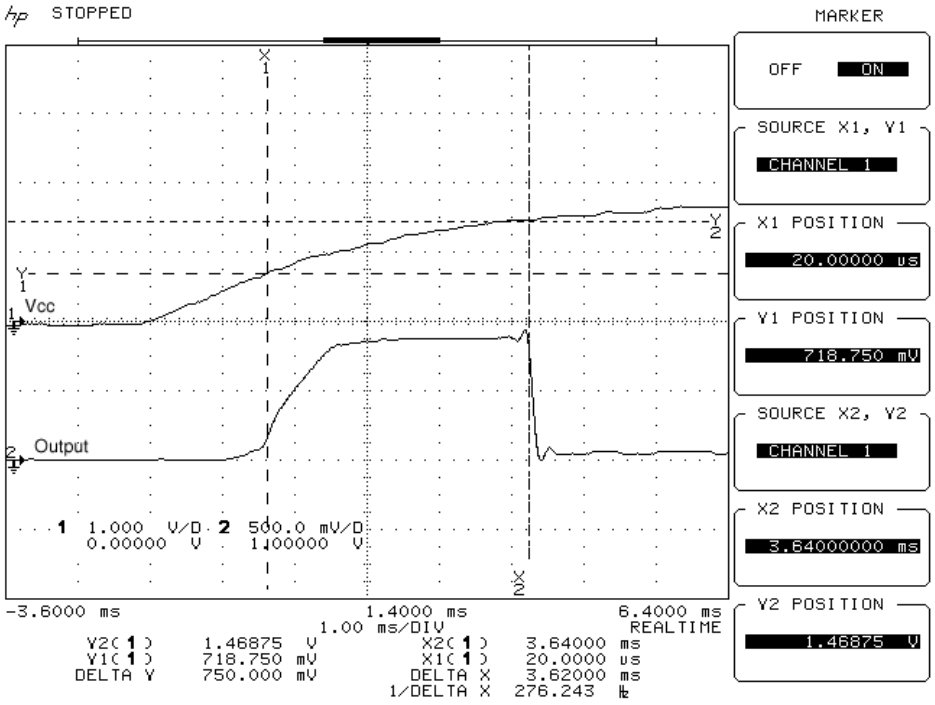


Figure 1b. V_{CC} power-up from 0V to 1.8V, V_{CCO} = 2.5V (pull-up on input, output with external 10Kohm pull-down resistor)

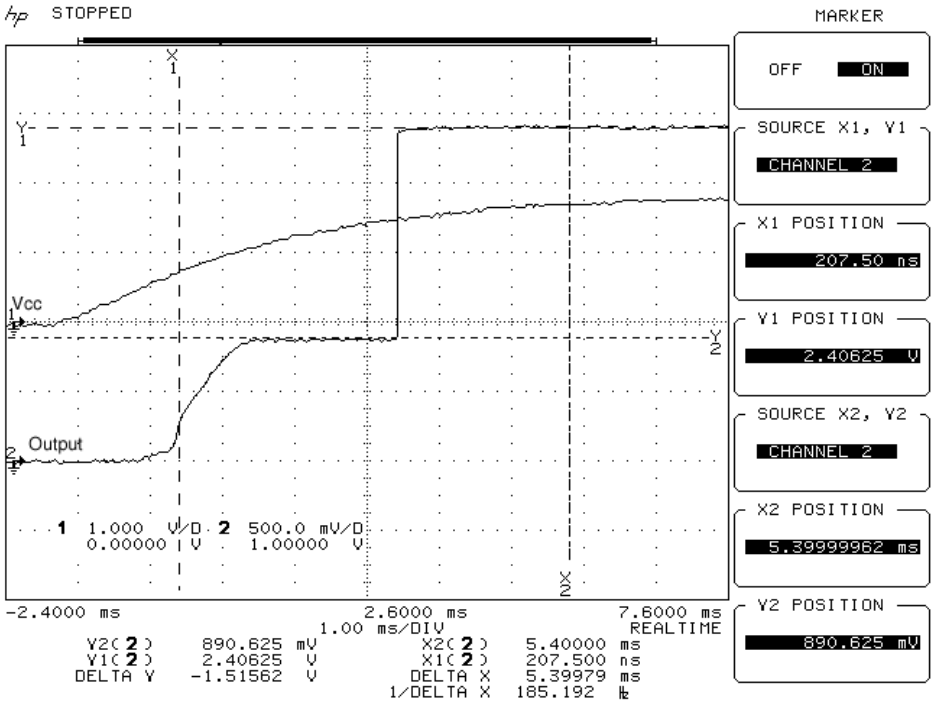


Figure 1c. V_{CC} power down from 1.8V to 0V, V_{CCO} = 2.5V (pull-down on input, output with external 10Kohm pull-down resistor)

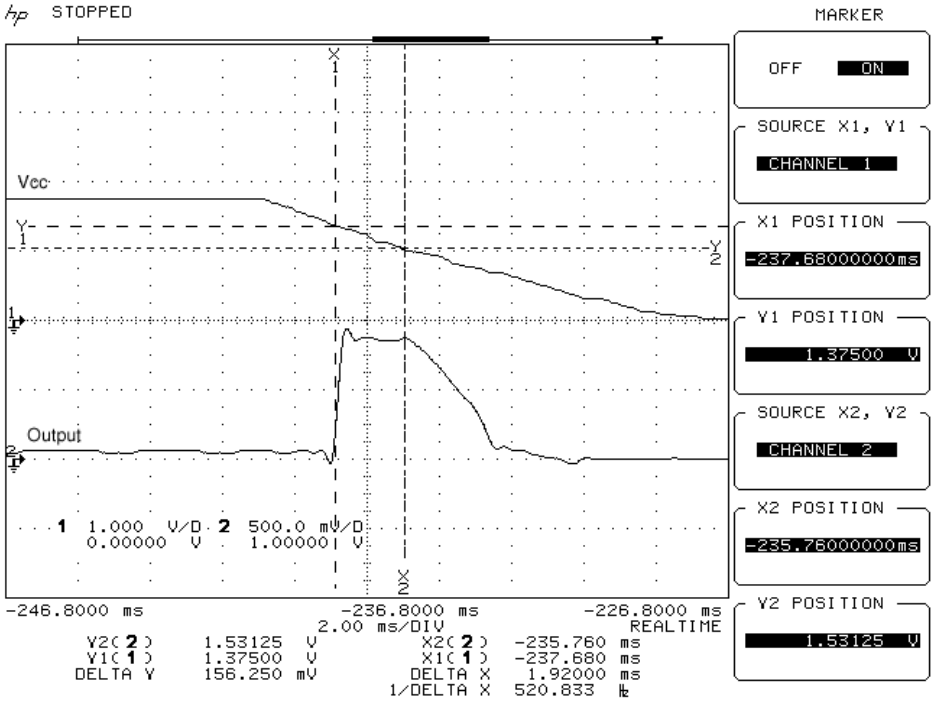


Figure 2a. V_{CC} power up from 0V to 1.8V, V_{CCO} = 2.5V (pull-down on input, output with external 1Kohm pull-down resistor)

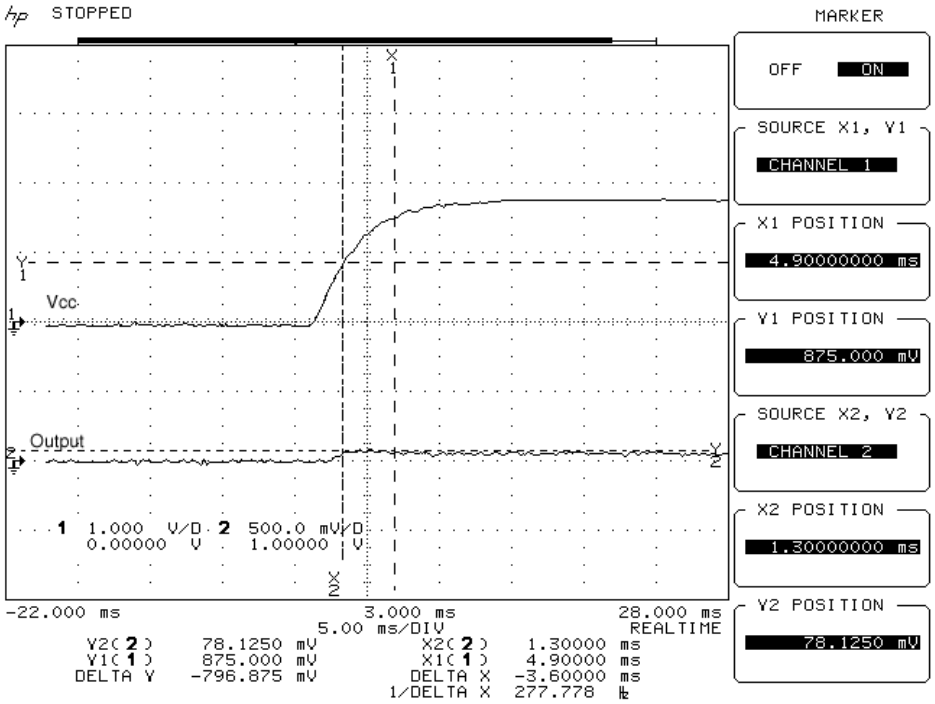


Figure 2b. V_{CC} power up from 0V to 1.8V, V_{CCO} = 2.5V (pull-up on input, output with external pull-down resistor = 1Kohm)

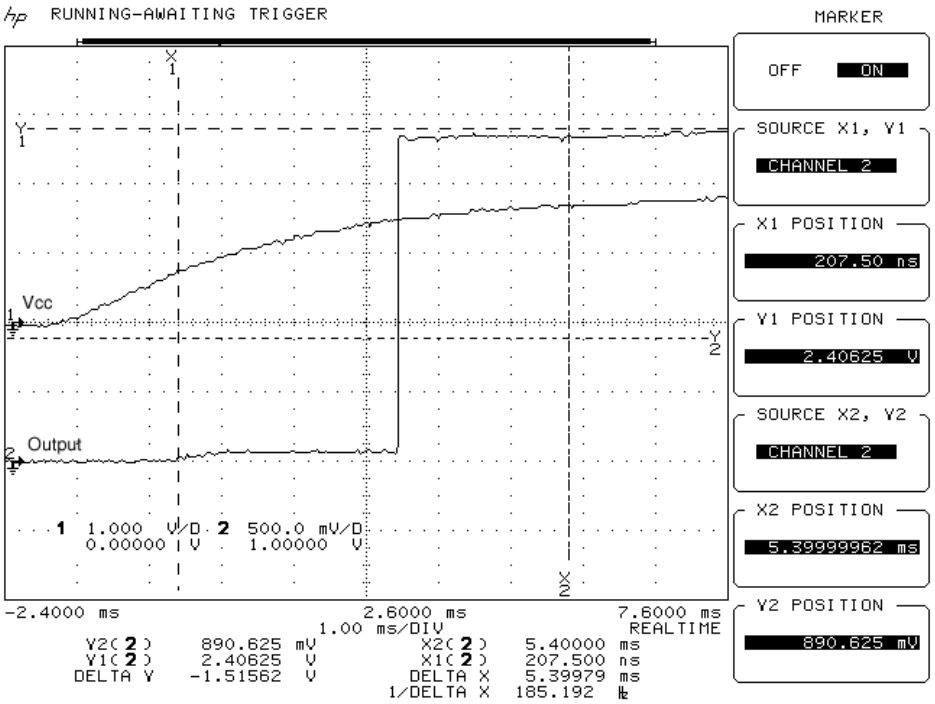
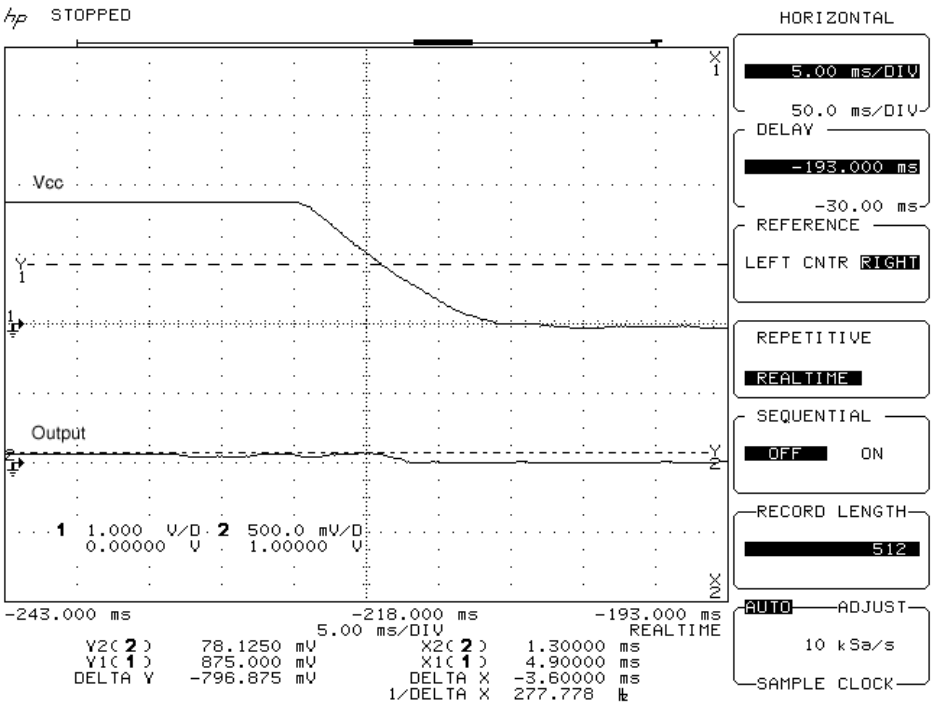


Figure 2c. V_{CC} power down from 1.8V to 0V, V_{CCO} = 2.5V (pull-down on input, output with external pull-down resistor = 1Kohm)



Test Condition for the Following Data Plots: V_{CCO} Ramps with V_{CC} Applied

This is the opposite situation as described in the previous condition: the V_{CC} pin is always connected to a stable power supply while the V_{CCO} pin is being powered up or down. The output will follow the input once the power supply is available at V_{CCO} pin. Figures 3a and 3b show the conditions with output pin being driven high.

Figure 3a. V_{CCO} power-up from 0V to 2.5V, V_{CC} = 2.5V (pull-up on input pin, output open)

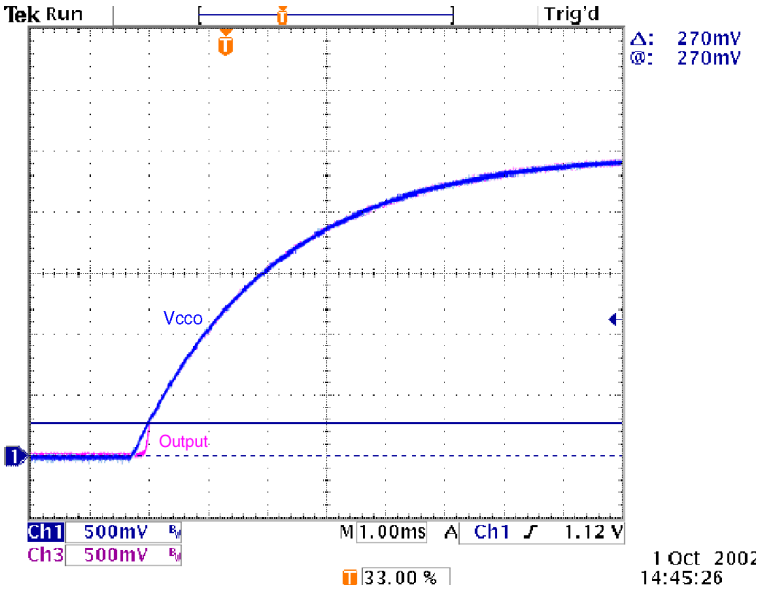
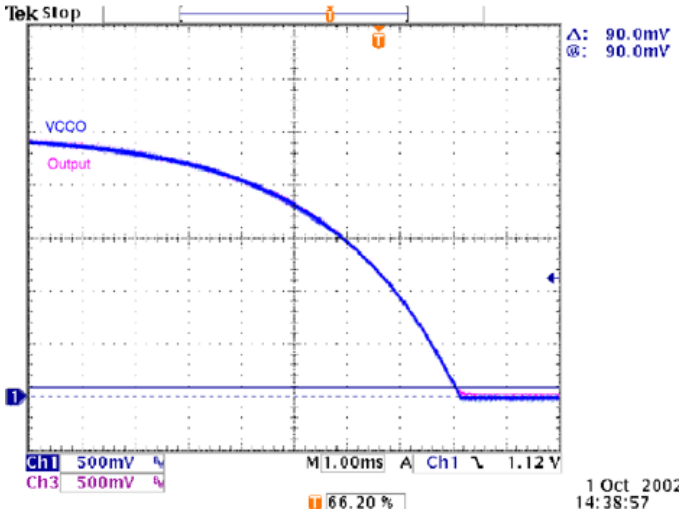


Figure 3b. V_{CCO} power-down from 2.5V to 0V, V_{CC} = 2.5V (pull-up on input pin, output open)



V/I Curves for an I/O Pin

The following I/O leakage current data is taken at room temperature with an I/O being configured as input or tri-stated output, and without internal pull-up/pull-down. Four combinations of the power supply sequencing are considered. The input voltage is swept from -0.5V to +3.0V. Under typical conditions, the I/O leakage current will not exceed 50µA as specified in the data sheet.

Figure 4a. V_{CC} = Off and V_{CCO} = Off

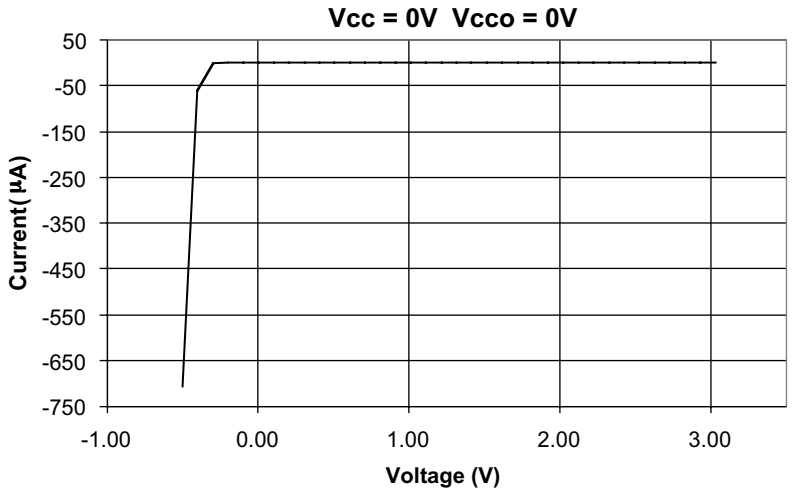


Figure 4b. V_{CC} = Off and V_{CCO} = On

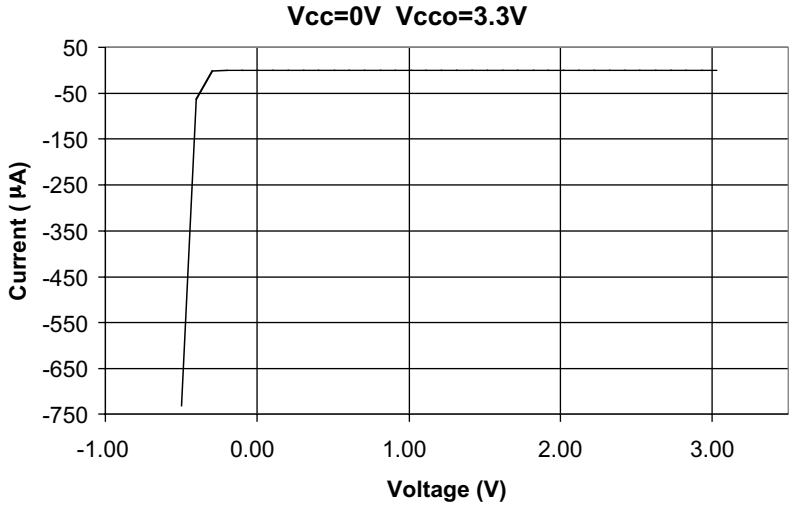


Figure 4c. V_{CC} = On and V_{CCO} = Off

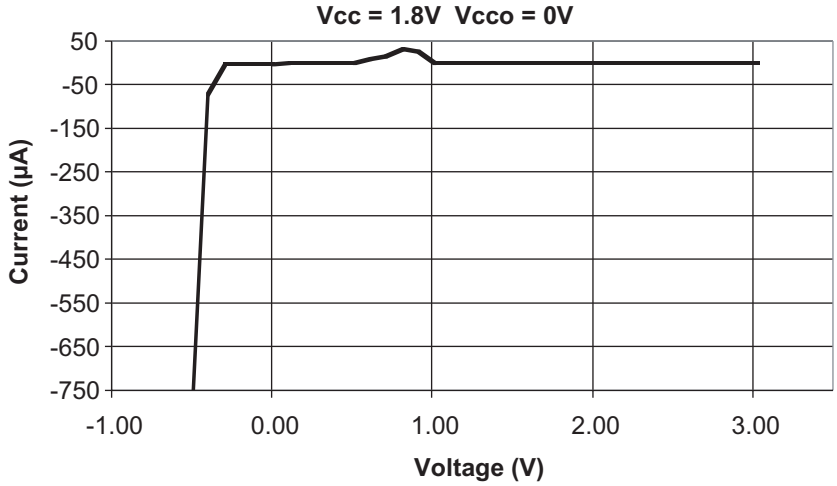
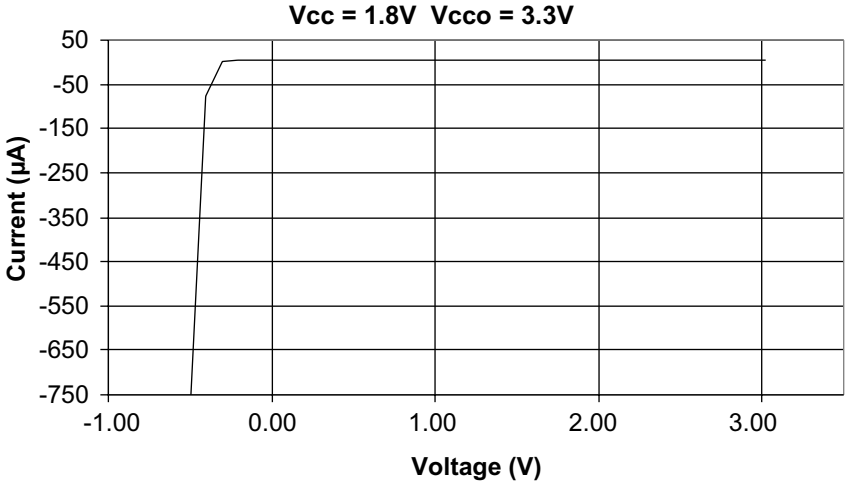


Figure 4d. V_{CC} = On and V_{CCO} = On



Summary

The V_{CC}/V_{CCO} sequencing tests do not show any current discontinuity during the power-up and power-down of the Lattice devices. There is no I/O current surge in the positive voltage range when the input voltage stays within the specification of the data sheet. This demonstrates that the ispXPGA, ispXPLD, ispMACH 4000 and the ispGDX2 families can tolerate active signals on I/O and input pins while in the power-up or power-down state. In addition, the small leakage current allows the Lattice devices to have minimal effect on active signals in the system when Lattice devices have no power. Altogether these characteristics make the latest Lattice products ideal candidates for hot socketing applications. Devices will not be damaged with random power-up sequences, nor will they go into undesirable states so long as all the external I/O signal sources meet the specifications outlined in the data sheet.

Technical Support Assistance

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