# NAND Flash and LP-DRAM 168-Ball Package-on-a-Package (PoP) Combination Memory (TI OMAP™)

## Features

- Micron® NAND Flash and LP-DRAM components
- RoHS-compliant, "green" package
- Separate NAND Flash and LP-DRAM interfaces
- Space-saving package-on-a-package combination
- Low-voltage operation (1.70–1.95V)
- Industrial temperature range: –40C° to +85C°

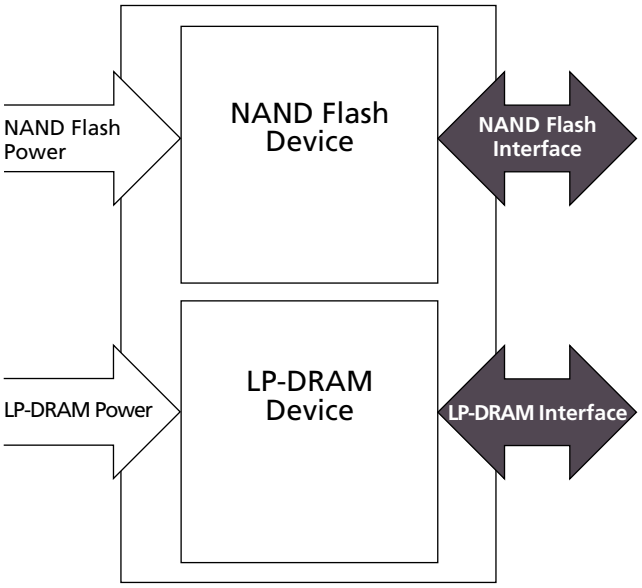
### NAND Flash-Specific Features

- Organization
  - Page size
    x8: 2112 bytes (2048 + 64 bytes)
    x16: 1056 words (1024 + 32 words)
  - Block size: 64 pages (128K + 4K bytes)
  - Device size
    1Gb: 1024 blocks
    2Gb: 2048 blocks
    4Gb: 4096 blocks

### LP-DRAM-Specific Features

- No external voltage reference required
- No minimum clock rate requirement
- 1.8V LVCMOS-compatible inputs
- Programmable burst lengths
- Partial-array self refresh (PASR)
- Deep power-down (DPD) mode
- Selectable output drive strength
- STATUS REGISTER READ (SRR) supported[1]

**Figure 1: PoP Block Diagram**



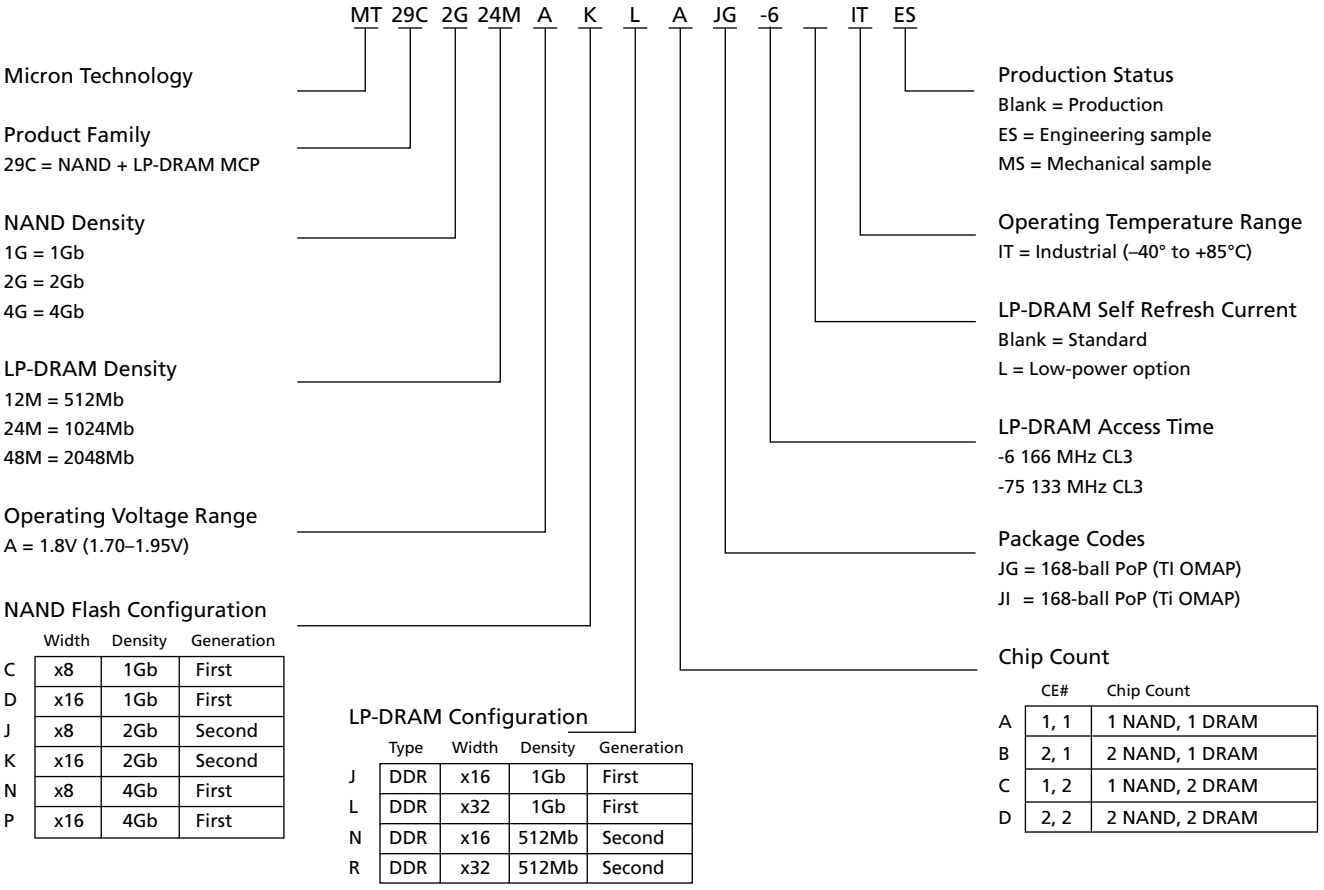

| Options | Marking |
|---|---|
| • LP-DRAM | |
| 166 MHz CL3[2] | -6 |
| 133 MHz CL3 | -75 |

Notes: 1. Contact factory for remapped SRR output.
2. CL = CAS (READ) latency.

# Part Numbering Information – 168-Ball PoP

Micron NAND Flash and LP-DRAM devices are available in different configurations and densities.

**Figure 2: 168-Ball Part Number Chart**




Note: Not all possible combinations are available. Contact factory for availability.

**Table 1: 168-Ball Production Part Numbers**

| Part Numbers | NAND Product | LPDDR Product | Physical Part Marking |
|---|---|---|---|
| MT29C2G24MAKLAJG-6 IT | MT29F2G16ABDHC-ET | MT46H32M32LFJG-6 IT | JW192 |
| MT29C2G24MAKLAJG-75 IT | MT29F2G16ABDHC-ET | MT46H32M32LFJG-6 IT | JW193 |
| MT29C2G48MAKLCJI-6 IT | MT29F2G16ABDHC-ET | MT46H32M32LFJG-6 IT | JW256 |
| MT29C2G48MAKLCJI-75 IT | MT29F2G16ABDHC-ET | MT46H32M32LFJG-6 IT | JW255 |
| MT29C4G48MAPLCJI-6 IT | MT29F4G16ABCWC-ET | MT46H32M32LFJG-6 IT | JW295 |
| MT29C4G48MAPLCJI-75 IT | MT29F4G16ABCWC-ET | MT46H32M32LFJG-6 IT | JW294 |

## Device Marking

Due to the size of the package, the Micron-standard part number is not printed on the top of the device. Instead, an abbreviated device mark consisting of a 5-digit alphanumeric code is used. The abbreviated device marks are cross-referenced to the Micron part numbers at the FBGA Part Marking Decoder site: www.micron.com/decoder. To view the location of the abbreviated mark on the device, refer to customer service note CSN-11, "Product Mark/Label," at www.micron.com/csn.

## General Description

Micron package-on-a-package (PoP) products combine NAND Flash and LP-DRAM devices in a single multichip package (MCP). These products target mobile applications with low-power, high-performance, and minimal package-footprint design requirements. The NAND Flash and LP-DRAM devices are also members of the Micron discrete memory products portfolio.

The NAND Flash and LP-DRAM devices are packaged with separate interfaces (no shared address, control, data, or power balls). This bus architecture supports an optimized interface to processors with separate NAND Flash and LP-DRAM buses. The NAND Flash and LP-DRAM devices have separate core power connections and share a common ground (i.e., Vss is tied together on the two devices).

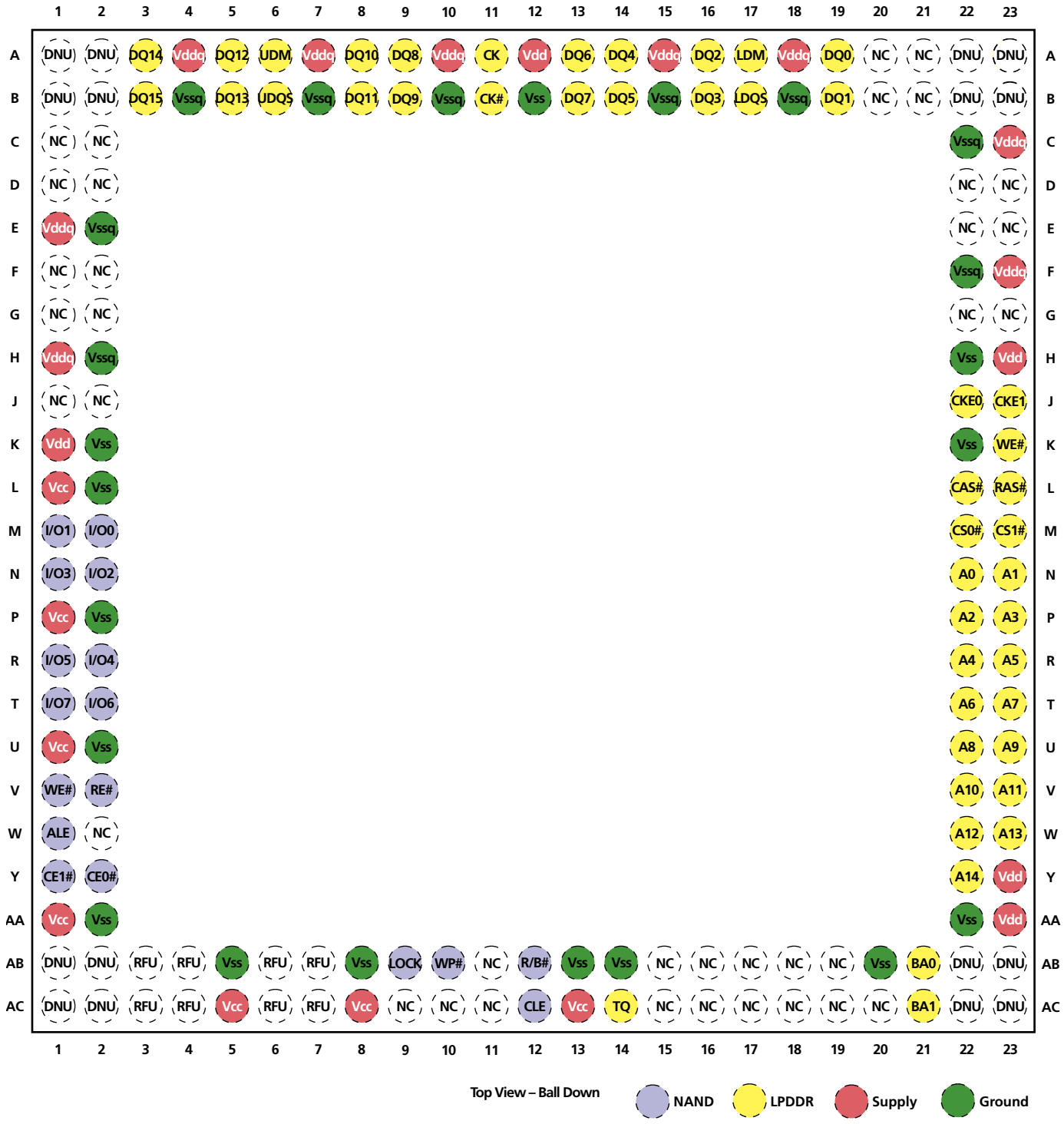
The bus architecture of this device also supports separate NAND Flash and LP-DRAM functionality without concern for device interaction. Operational characteristics for the NAND Flash and LP-DRAM devices are found in the standard Micron data sheets for each of the discrete devices.

For device specifications and complete Micron NAND Flash features documentation, please refer to the component data sheet at www.micron.com/products/nand, or contact your local Micron sales office.

For device specifications and complete LP-DRAM features documentation, please refer to the component data sheet at www.micron.com/products/mobiledram, or contact your local Micron sales office.

# Ball Assignments and Descriptions

**Figure 3: 168-Ball VFBGA (NAND x8; LPDDR x16) Ball Assignments**




Note: Contact factory for availability of x16 LPDDR configuration.

**Figure 4: 168-Ball VFBGA (NAND x16; LPDDR x32) Ball Assignments**

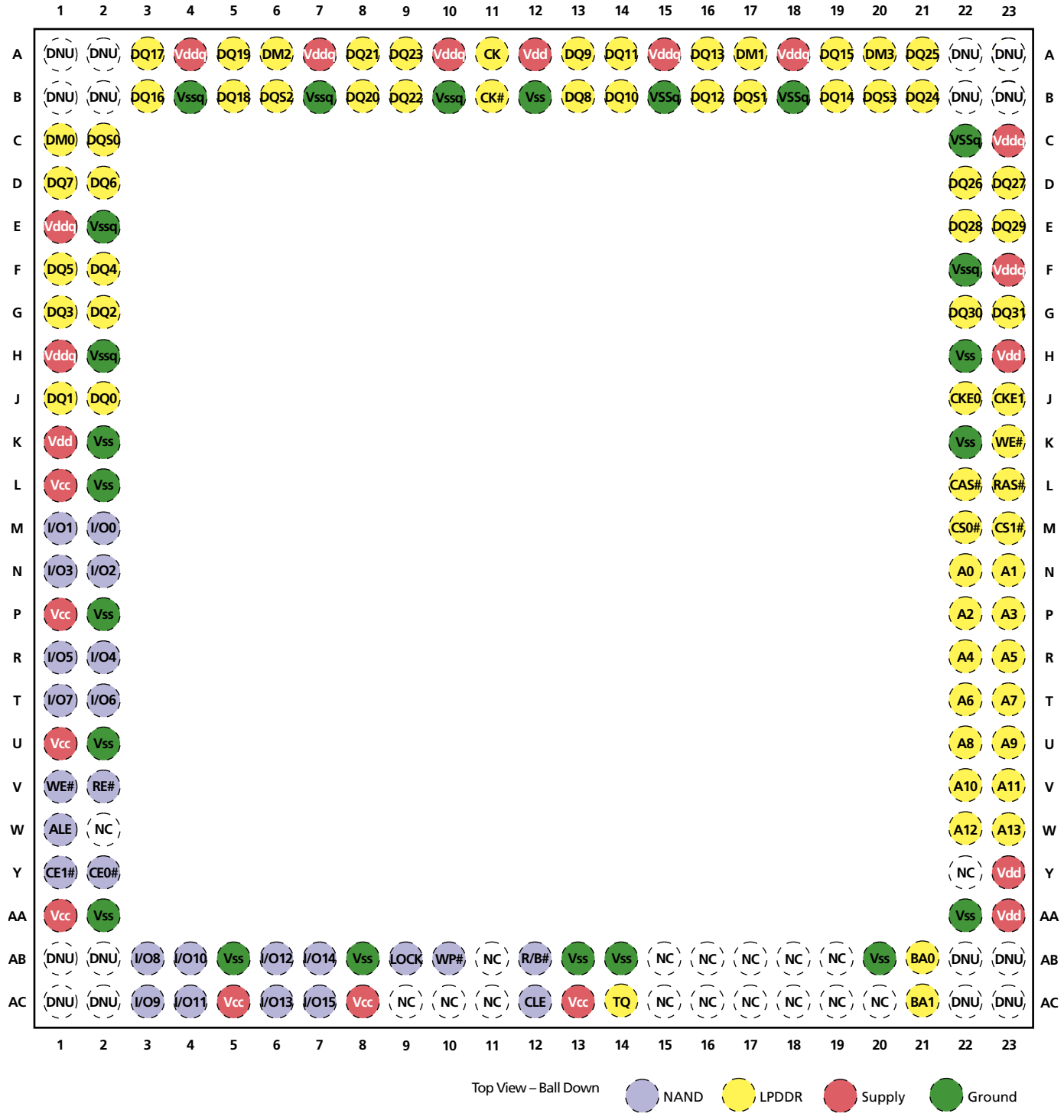


**Table 2: NAND Flash Ball Descriptions**

| NAND Flash x8 Ball Number | NAND Flash x16 Ball Number | Symbol | Type | Description |
|---|---|---|---|---|
| W1 | W1 | ALE | Input | Address latch enable: When ALE is HIGH, addresses can be transferred to the on-chip address register. |
| Y1, Y2 | Y1, Y2 | CE1#, CE0# | Input | Chip enable: Gates transfers between the host system and the NAND Flash device. CE1# is used for the second NAND Flash device in a multiple NAND implementation requiring separate CE# control. |
| AC12 | AC12 | CLE | Input | Command latch enable: When CLE is HIGH, commands can be transferred to the on-chip command register. |
| AB9 | AB9 | LOCK | Input | When LOCK is HIGH during power-up, the BLOCK LOCK function is enabled. To disable BLOCK LOCK, connect LOCK to Vss during power-up, or leave it unconnected (internal pull-down). |
| V2 | V2 | RE# | Input | Read enable: Gates information from the NAND Flash device to the host system. |
| V1 | V1 | WE# | Input | Write enable: Gates information from the host system to the NAND Flash device. |
| AB10 | AB10 | WP# | Input | Write protect: Driving WP# LOW blocks ERASE and PROGRAM operations. |
| T1, T2, R1, R2, N1, N2, M1, M2 | AC7, AB7, AC6, AB6, AC4, AB4, AC3, AB3, T1, T2, R1, R2, N1, N2, M1, M2 | I/O[7:0] (x8)<br><br>I/O[15:0] (x16) | Input/ output | Data inputs/outputs: The bidirectional I/Os transfer address, data, and instruction information. Data is output only during READ operations; at other times the I/Os are inputs.<br>I/O[15:8] are RFU[1] for NAND x8 devices. |
| AB12 | AB12 | R/B# | Output | Ready/busy: Open-drain, active-LOW output that indicates when an internal operation is in progress. |
| L1, P1, U1, AA1, AC5, AC8, AC13 | L1, P1, U1, AA1, AC5, AC8, AC13 | Vcc | Supply | Vcc: NAND Flash power supply. |

Notes: 1. Balls marked RFU may or may not be connected internally. These balls should not be used. Contact the factory for details.

**Table 3: LPDDR Ball Descriptions**

| LPDDR x16 Ball Number | LPDDR x32 Ball Number | Symbol | Type | Description |
|---|---|---|---|---|
| Y22, W23, W22, V23, V22, U23, U22, T23, T22, R23, R22, P23, P22, N23, N22 | W23, W22, V23, V22, U23, U22, T23, T22, R23, R22, P23, P22, N23, N22 | A[14:0] (x16)<br><br>A[13:0] (x32) | Input | Address inputs: Specifies the row or column address. Also used to load the mode registers. The maximum LPDDR address is determined by density and configuration. Consult the LPDDR product data sheet for the maximum address for a given density and configuration. Unused address pins become RFU.[1] |
| AC21, AB21 | AC21, AB21 | BA1, BA0 | Input | Bank address inputs: Specifies one of the 4 banks. |
| L22 | L22 | CAS# | Input | Column select: Specifies the command to execute. |
| A11, B11 | A11, B11 | CK, CK# | Input | CK is the system clock. CK and CK# are differential clock inputs. All address and control signals are sampled and referenced on the crossing of the rising edge of CK with the falling edge of CK#. |
| J23, J22 | J23, J22 | CKE1, CKE0 | Input | Clock enable:<br>CKE0 is used for a single LPDDR product.<br>CKE1 is used for dual LPDDR products. |
| M23, M22 | M23, M22 | CS1#, CS0# | Input | Chip select:<br>CS0# is used for a single LPDDR product.<br>CS1# is used for dual LPDDR products. |
| A17, A6 | A20, A6, A17, C1 | DM[1:0] (x16)<br><br>DM[3:0] (x32) | Input | Data mask: Determines which bytes are written during WRITE operations.<br>For x16 LPDDR, unused DM balls become NC. |
| L23 | L23 | RAS# | Input | Row select: Specifies the command to execute. |
| K23 | K23 | WE# | Input | Write enable: Specifies the command to execute. |
| B3, A3, B5, A5, B8, A8, B9, A9, B13, A13, B14, A14, B16, A16, B19, A19 | G23, G22, E23, E22, D23, D22, A21, B21, A9, B9, A8, B8, A5, B5, A3, B3, A19, B19, A16, B16, A14, B14, A13, B13, D1, D2, F1, F2, G1, G2, J1, J2 | DQ[15:0] (x16)<br><br>DQ[31:0] (x32) | Input/ output | Data bus: Data inputs/outputs.<br>DQ[31:16] are NC for x16 LPDDR devices. |
| B17, B6 | B20, B6, B17, C2 | DQS[1:0] (x16)<br><br>DQS[3:0] x(32) | Input/ output | Data strobe: Coordinates READ/WRITE transfers of data; one DQS per DQ byte. |
| AC14 | AC14 | TQ | Output | Temperature sensor output: TQ HIGH when LPDDR $T_J$ exceeds 85°C. |
| A12, H23, K1, Y23, AA23 | A12, H23, K1, Y23, AA23 | Vdd | Supply | Vdd: LPDDR power supply. |
| A4, A7, A10, A15, A18, C23, E1, F23, H1 | A4, A7, A10, A15, A18, C23, E1, F23, H1 | Vddq | Supply | Vddq: LPDDR I/O power supply. |
| B4, B7, B10, B15, B18, C22, E2, F22, H2 | B4, B7, B10, B15, B18, C22, E2, F22, H2 | Vssq | Supply | Vssq: LPDDR ground. |

Notes: 1. Balls marked RFU may or may not be connected internally. These balls should not be used. Contact the factory for details.

**Table 4: Non-Device-Specific Ball Descriptions**

| Miscellaneous Ball Numbers | | Symbol | Type | Description |
|---|---|---|---|---|
| **Shared (NAND Flash and LP-DRAM)** | | | | |
| B12, H22, K2, K22, L2, P2, U2, AA2, AA22, AB5, AB8, AB13, AB14, AB20 | B12, H22, K2, K22, L2, P2, U2, AA2, AA22, AB5, AB8, AB13, AB14, AB20 | $V_{SS}$ | Supply | $V_{SS}$: Shared ground. |
| **LP-DRAM x16** | **LP-DRAM x32** | | | |
| A20, A21, B20, B21, C1, C2, D1, D2, D22, D23, E22, E23, F1, F2, G1, G2, G22, G23, J1, J2, W2, AB11, AB15, AB16, AB17, AB18, AB19, AC9, AC10, AC11, AC15, AC16, AC17, AC18, AC19, AC20 | W2, Y22, AB11, AB15, AB16, AB17, AB18, AB19, AC9, AC10, AC11, AC15, AC16, AC17, AC18, AC19, AC20 | NC | – | No connect: Not internally connected. |
| A1, A2, A22, A23, B1, B2, B22, B23, AB1, AB2, AB22, AB23, AC1, AC2, AC22, AC23 | A1, A2, A22, A23, B1, B2, B22, B23, AB1, AB2, AB22, AB23, AC1, AC2, AC22, AC23 | DNU | – | Do not use: Must be grounded or left floating. |
| AB3, AB4, AB6, AB7, AC3, AC4, AC6, AC7 | | RFU[1] | – | Reserved for future use. |

Notes: 1. Balls marked RFU may or may not be connected internally. These balls should not be used. Contact the factory for details.

# Electrical Specifications

**Table 5: Absolute Maximum Ratings**

| Parameters/Conditions | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Vcc, Vdd, Vddq supply voltage relative to Vss | Vcc, Vdd, Vddq | –1.0 | 2.4 | V |
| Voltage on any pin relative to Vss | Vin | –0.5 | 2.4 or (supply voltage + 0.3V), whichever is less | V |
| Storage temperature range | – | –55 | +150 | °C |

Note: Supply voltage references either Vddq or Vcc.

Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Table 6: Recommended Operating Conditions**

| Parameters | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply voltage | Vcc, Vdd | 1.70 | 1.80 | 1.95 | V |
| I/O supply voltage | Vddq | 1.70 | 1.80 | 1.95 | V |
| Operating temperature range | – | –40 | – | +85 | °C |

# Device Diagrams

**Figure 5: 168-Ball Functional Block Diagram**

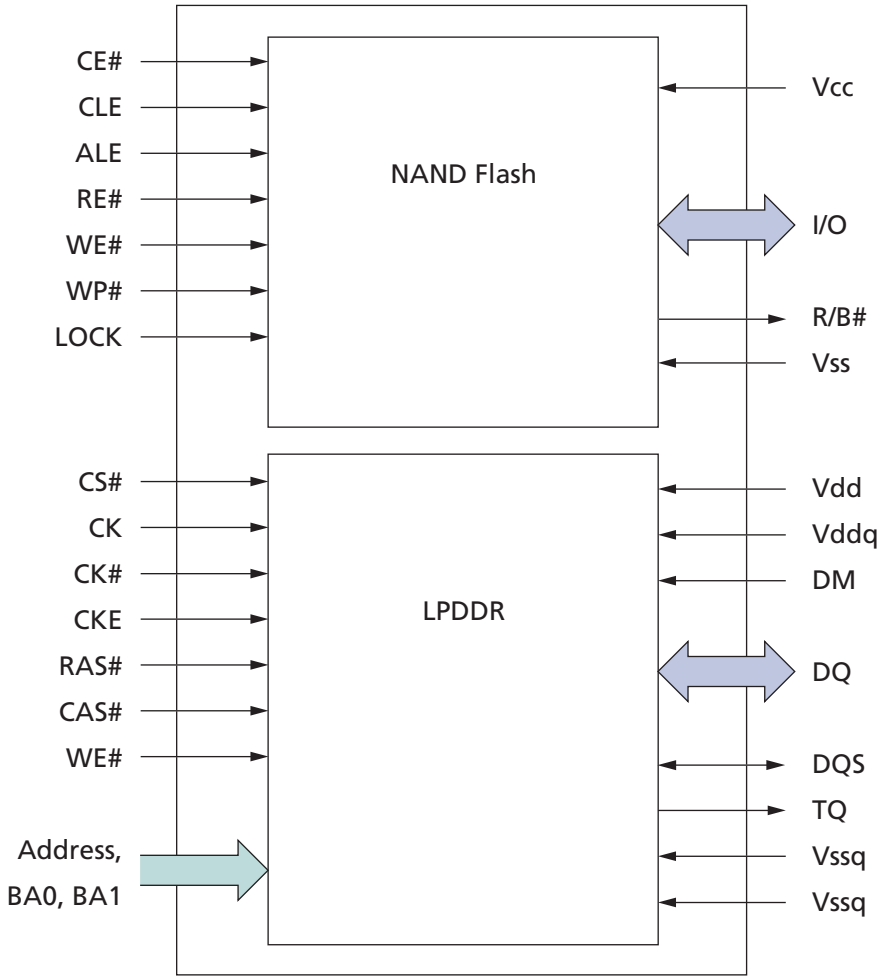
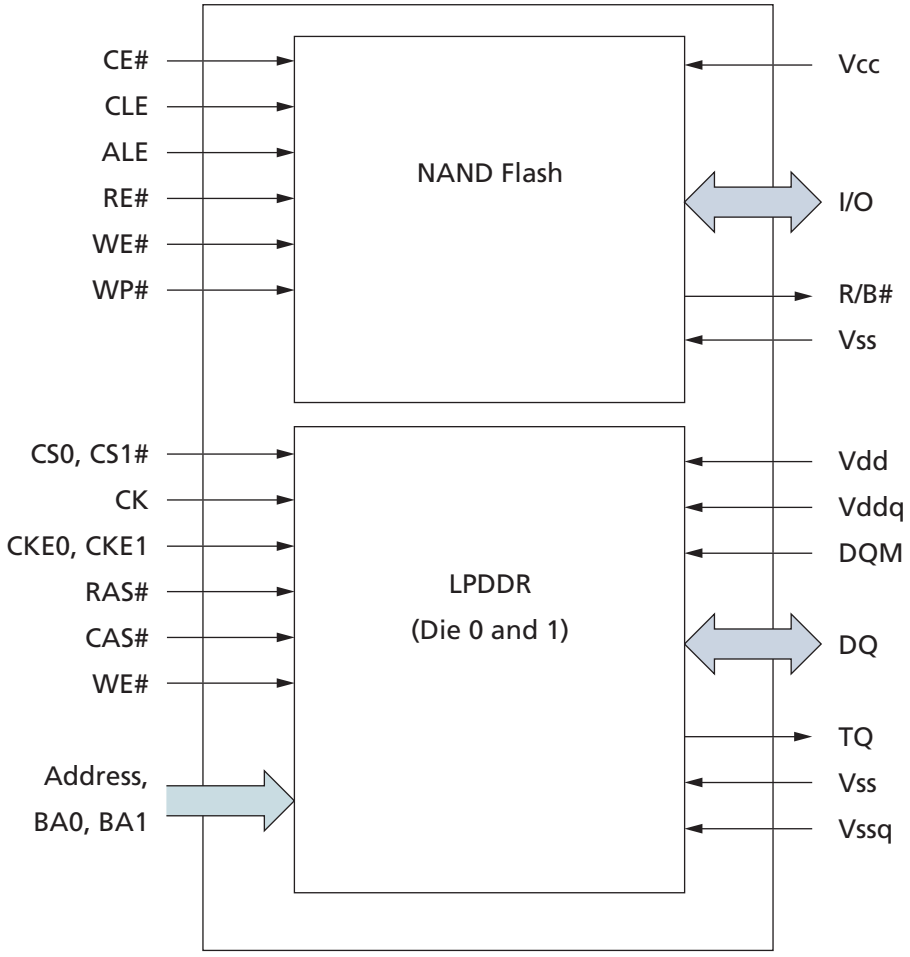
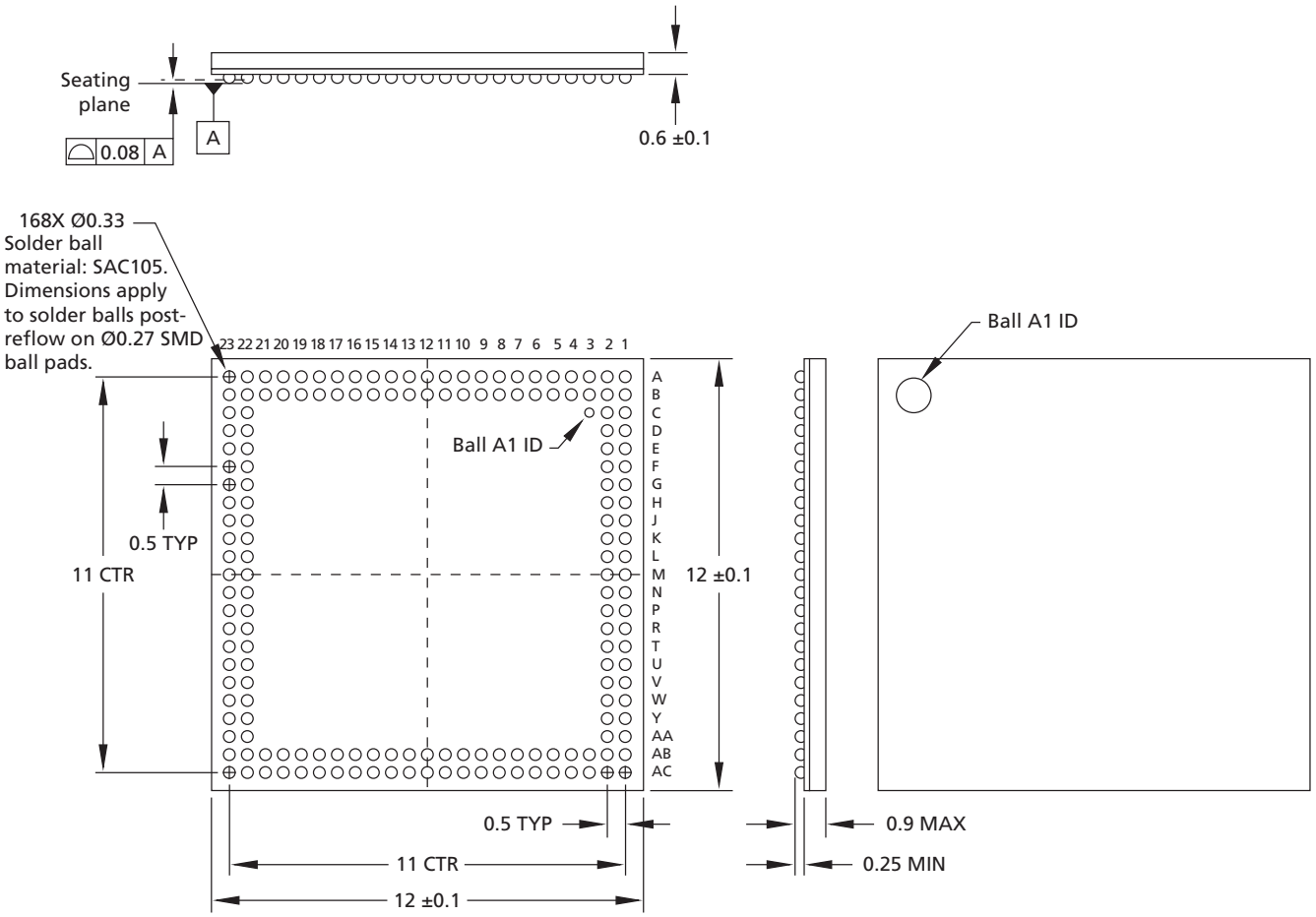


**Figure 6: 168-Ball Dual LPDDR Functional Block Diagram**



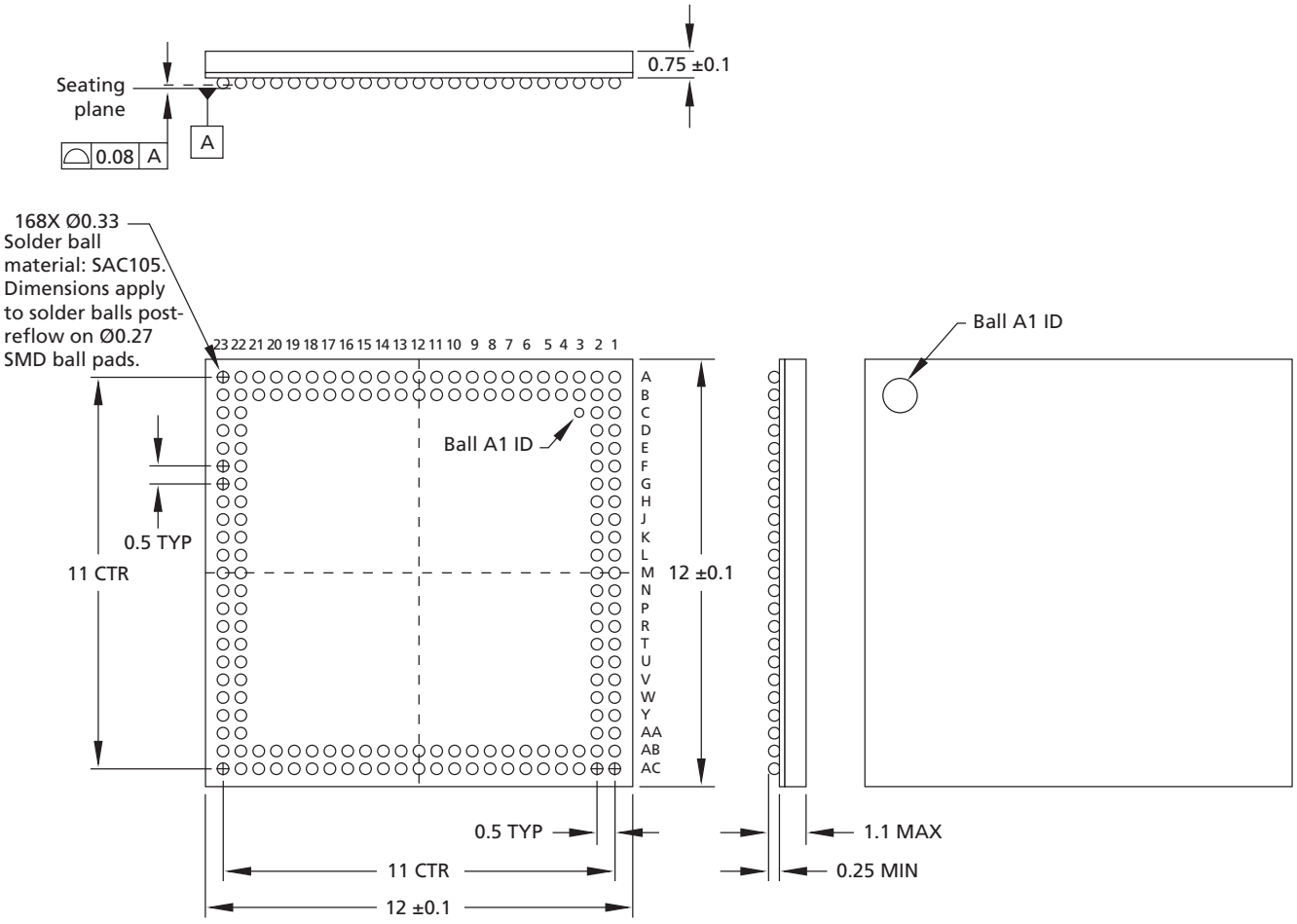
# Package Dimensions

**Figure 7: 168-Ball VFBGA (Package Code: JG)**




Note: All dimensions are in millimeters.

**Figure 8: 168-Ball VFBGA (Package Code: JI)**




Note: All dimensions are in millimeters.

# Revision History

**Rev. F, Preliminary . . . . . 11/08**

- Updated template for external publication

**Rev. E, Preliminary . . . . . 9/08**

- "MT29CxGxxMAxxxJG, MT29CxGxxMAxxxJI" on page 1: As the third-from-the-last character in the part number, replaced "A" with an "x."
- Figure 3, Ball Assignment: 168-Ball VFBGA (x8 NAND Flash and x16 LP-DRAM), on page 4: Updated figure by replacing "NC"s in lower-left corner with "RFU"s.
- Table 2, "NAND Flash Ball Descriptions," on page 6: In CE1#/CE0# row, reversed order of ball numbers to reflect correct highest-to-lowest order; changed "NC" to "RFU1" in the I/O row; added note 1.
- Table 3, "LPDDR Ball Descriptions," on page 7: In BA1/BA0, CKE1/CKE0, and CS1#/CS0# rows, reversed order of ball numbers to reflect correct highest-to-lowest order; in NC row, removed AE-indicated ball assignments and created a new RFU row.
- Figure 6, 168-Ball Dual LPDDR Functional Block Diagram, on page 11: Added figure adapted from 152-ball.
- Figure 7, 168-Ball VFBGA (Package Code: JG), on page 12: Updated figure with current version from MDM.
- Figure 8, 168-Ball VFBGA (Package Code: JI), on page 13: Updated figure with current version from MDM.

**Rev. D, Preliminary . . . . . 4/08**

- Changed status to preliminary.
- On page 1 and Figure 2: 168-Ball Part Number Chart on page 2: Added JI part number and package code.
- Figure 3: Ball Assignment: 168-Ball VFBGA (x8 NAND Flash and x16 LP-DRAM) on page 4; Figure 4: 168-Ball VFBGA (NAND x16; LPDDR x32) Ball Assignments on page 5; Table 2, "NAND Flash Ball Descriptions," on page 6; Table 3, "LPDDR Ball Descriptions," on page 7; and Table 4, "Non-Device-Specific Ball Descriptions," on page 8: Updated ball assignments.
- Removed former capacitance tables. See component data sheets for capacitance.
- Figure 8: 168-Ball VFBGA (Package Code: JI) on page 13: Added figure.

**Rev. C, Advance . . . . . 2/08**

- Figure 2: 168-Ball Part Number Chart on page 2: Updated self-refresh current definition.
- Figure 7: 168-Ball VFBGA (Package Code: JG) on page 12: Updated package diagram with 0.15 tolerance.

**Rev. B, Preliminary . . . . . 12/07**

- "LP-DRAM-Specific Features" on page 1: Added SRR feature.
- Separated original single ball-assignment table into separate tables: Table 2, "NAND Flash Ball Descriptions," on page 6, Table 3, "LPDDR Ball Descriptions," on page 7, and Table 4, "Non-Device-Specific Ball Descriptions," on page 8.
- Removed "Mobile" from LP-DRAM references.

**Rev. A, Preliminary . . . . . 12/07**

- Initial release.