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Hybrid MOSFET/Driver for Ultra-Fast Switching

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ABSTRACT

The ultra-fast switching of power MOSFETs, in about 1ns, is very challenging. This is largely due to the parasitic inductance that is intrinsic to commercial packages used for both MOSFETs and drivers. Parasitic gate and source inductance not only limit the voltage rise time on the MOSFET internal gate structure but can also cause the gate voltage to oscillate. This paper describes a hybrid approach that substantially reduces the parasitic inductance between the driver and MOSFET gate, as well as between the MOSFET source and its external connection. A flip chip assembly is used to directly attach a die-form power MOSFET and driver on a PCB. The parasitic inductances are significantly reduced by eliminating bond wires and minimizing lead length. The experimental results demonstrate ultra-fast switching of the power MOSFET with excellent control of the gate-source voltage.

Index Terms — **MOSFET switches, power MOSFETs, high-speed electronics, pulse power system switches, Hybrid integrated circuits, flip-chip devices.**

1 INTRODUCTION

Power MOSFETs have great potential as switches for high speed high voltage applications like pulsed power. The theoretical carrier transit time from drain to source is on the order of 200ps in any cell of the silicon die [1]. Although the power MOSFET is intrinsically capable of switching in about 1ns, this is not achieved in commercial devices, largely due to the package inductances. The major contributors are the parasitic gate inductance (Lg) and parasitic source inductance (Ls), each typically several nH. At high frequency, the inductive impedance of Lg will isolate the driver from the gate electrode of the MOSFET die. Further, during fast switching the large dI/dt through the MOSFET source produces a large voltage drop across Ls. This negative feedback can drive the MOSFET into an oscillatory state. A damping resistor is normally inserted in series with the gate electrode to prevent such oscillations. However, this further impedes the transfer of charge to the gate and increases the switching time (defined herein as the time for the drain to source voltage to decrease from 90% to 10% of the applied voltage).

Two methods are currently used to improve the switching speed of commercial power MOSFETs. One method is to use a specially designed package and die to minimize the parasitic inductances, the other is to integrate the driver and die into the same package. IXYS RF uses the first method in their DEI-series MOSFET, which has a low stated parasitic inductance (~1nH). The second method is used in the Microsemi DRF100/DRF1200 MOSFET. However, the minimum switching time for these devices is still ~3 ns. One possible reason is the aluminum bonding wires, used in both devices to make the connection between the die and terminal, introduce a significant amount of parasitic inductance.

DCA (direct chip attachment) is now available as a common PCB assembly method. Among all the DCA methods [3], flip-chip assembly is the most promising for this application since it completely eliminates the use of bonding wires. Using this method, several hybrid boards have been developed for ultra-fast MOSFET switching.

2 DESIGN

Three generations of hybrid (PCB#1, PCB#2 and PCB#3) were made to accommodate different package and circuit configurations. All three use the totem pole driver topology shown in Figure 1. PCB#1 connects a single totem pole driver to either a DE275 or TO247-packaged power MOSFET. PCB#2 and PCB#3 connect two identical drivers, in parallel, to a die form power MOSFET. The difference is that the totem pole driver of PCB#2 is in a SO8 package and in PCB#3 it is assembled from a complementary pair of bare P-channel/N-channel MOSFET dies using the flip-chip method. Because of the limited availability of complementary P/N-channel dies, the totem pole driver and input buffer of PCB#3 is slightly different from those used for PCB#2. Figure 2 is a photo of PCB#3, the power MOSFET is mounted on the back side of the board. The major specifications of the critical components for all three versions are listed in Table 1.

The circuits are composed of 4 function blocks; load, power MOSFET, totem pole driver and input buffer. The design and assembly of these blocks will be discussed separately in the following sections.

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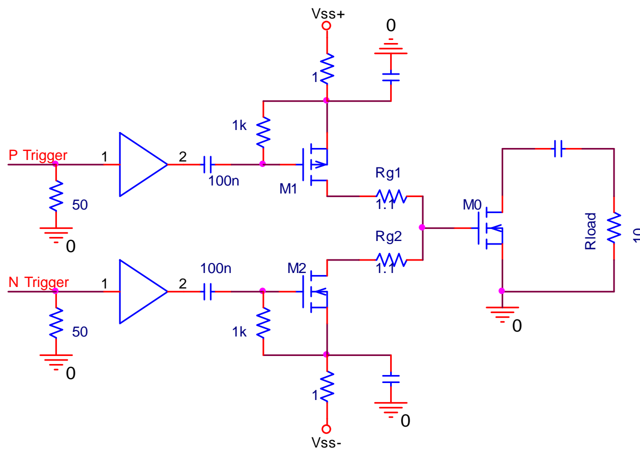

Figure 1. Schematic diagram of the hybrid circuit

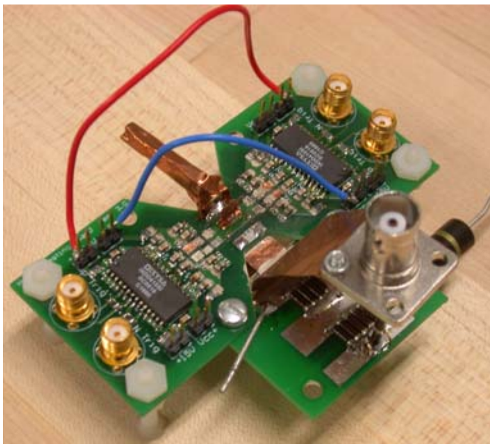

Figure 2. A photo of the PCB#3 hybrid circuit.

TABLE 1. Specifications of the critical hybrid circuit elements

		PCB #1		PCB#2	PCB#3
Input Buffer	PN	EL7158			IXDD415SI
	Min PW	~8ns			6ns
	Iout	12A			15A
	Vcc	12V			30V
Totem Pole	PN	FDS4559			IRFC120/9120
	Vdss	60/-60 V			100/-100V
	Rds(on)	0.055/0.105 Ω			0.21/0.48 Ω
	Id	4.5/-3.5 A			9.4/-6.6A
	Qg	12.5/15 nC			25/27 nC
	Ciss	650/759 pF			330/350 pF
Power MOS FET	PN	DE275-102N06A	APT30M 75BLL	APT30 M75	APT1201R2
	Package	DE275	TO-247	Die	Die
	Vdss	1000V	300 V		1200V
	Rds(on)	1.6 Ω	0.075 Ω		1.2 Ω
	Id	8A	44A		12A
	Id(peak)	48A	176A		48A
	Qg	50 nC	57 nC		100 nC
	Ciss	1800pF	3018 pF		2540 pF

2.1 LOAD

The load is a separate PCB that is used with all three variations of hybrid boards. Five 1nF, 1000V, C0G capacitors and two, 47nF, 1000V, X7R capacitors (all 1812 SMD) were connected in parallel as energy storage elements. Ten HSF-1 cylindrical thick film SMD resistors (27 or 68 Ω) were connected in a 2-series by 5-parallel array to form a resistive load of 10.6 or 27 Ω. These resistors have no trim cut, which minimizes the inductance and potential voltage enhancement on the trim edge. The load was connected to the power MOSFET drain using a 1cm wide copper foil.

Standard commercial high voltage probes (~1000V) have ~0.25GHz bandwidth (BW), which is not sufficient for the measurement of signals with ~1ns rise/fall time. An attenuator was built into the load board for this measurement. The attenuator consists of 3 series HSF-1 resistors (270 Ω) connecting the HV side of the load resistor to a BNC adapter with a ground plane, which is then terminated into 50 Ω at the scope. The attenuator was calibrated with a 500MHz bandwidth probe (Tektronix P6039A) using a 300V signal.

2.2 POWER MOSFET

The circuit performance is critically dependent on the layout of the power MOSFET section. It was designed to connect the die form MOSFET to the driver and load with a minimum of parasitic inductance.

The die form power MOSFET has interleaved gate and source terminals on the front side and the back side is the drain terminal, all coated with aluminum metallization. The flip-chip assembly technique facilitates low inductance connections to all MOSFET terminals. "Solder bumpers" are deposited on the source and gate pads. In order to minimize inductance, as many bumpers as possible are used. Then the die is "flipped," front down, and the source and gate terminals are connected to corresponding pads on the PCB using conductive epoxy. Then silver epoxy is applied on the back side of the die (now facing up), and a copper foil is attached to the drain terminal to make the external connection to the load board. This technique connects the full surface of all the terminals to the external circuit, a significant improvement over bonding wires.

2.3 TOTEM POLE DRIVER

The driver is based on a current source, rather than the traditional voltage source, design. This drive topology was selected based on an analysis of MOSFET switching processes [4]. It was concluded that the switching speed of the MOSFET does not depend on the final gate voltage but rather, the gate current at the start of conduction. Using a voltage source driving scheme, the maximum voltage is limited by the M0 gate breakdown voltage. Because a series resistor is needed to damp out the oscillation caused by parasitic inductance and gate capacitance, any voltage source is effectively a current source. Therefore, optimum switching is achieved by designing to maximize driver current and adjusting the on time of the current source/sink to control the gate voltage.

The drive current is set by the source voltage and total impedance between the source and power MOSFET gate. This includes the driver MOSFET "on" state resistance, the external gate resistance (Rg1 or Rg2 in Fig. 1) and the power MOSFET gate resistance plus any parasitic inductance. The totem pole driver employs a complimentary P/N-channel MOSFET pair. The P-channel is connected to the positive

voltage source (Vss+ in Figure 1) and controls the turn-on of the power MOSFET and the N-channel attaches to the negative source (Vss- in Figure 1) and controls the turn-off of the power MOSFET. The two output resistors, Rg1 and Rg2, provide independent control of on/off switching and limit shoot through current. The final voltage on the M0 gate is controlled by the relative timing of totem pole P/N-channel triggers.

The totem pole driver in PCB #1 and PCB #2 were SO-8 packaged P/N MOSFET pairs. The SO-8 package inductance, a few nH [2] may be the dominant gate circuit inductance when the power MOSFET is attached using the flip chip assembly method. Therefore, the SO-8 P/N MOSFET pair was replace by die form MOSFETs attached using the flip chip method to further reduce the parasitic inductance in PCB #3.

2.4 INPUT BUFFER

A commercial integrated circuit MOSFET driver was used as the input buffer, which converts the TTL level trigger from the function generator to a higher voltage level suitable for totem pole MOSFET switching. An EL7158 driver was used for PCB#1 and PCB#2. An IXDD415SI was used in PCB#3 because it has a shorter minimum output pulse length. With the shorter pulse length the driver current can be increased without risk of excessive voltage on the power MOSFET gate.

The input buffer was capacitively coupled to the totem pole gates. This isolation provides level shifting to the Vss+ and Vss- referenced gates of the P/N MOSFET totem pole.

3 RESULTS

The hybrid boards PCB#1 and PCB#2 were designed to compare the performance of a MOSFET die (APT30M75) in the standard TO247 package to the flip chip assembly. Figure 3 shows the typical gate and output waveforms for the TO247 package and the hybrid assembly under similar conditions. The waveform was measured using a Tektronix TDS684C scope (1GHz BW) with P6139A probe (500MHz BW). The merits of the hybrid circuit are clearly shown in these waveforms:

1. The turn on time of the hybrid circuit is more than a factor of 2 less than the TO247 packaged device, 1.40±0.03 ns versus 3.25±0.09 ns.

2. The gate waveform of the hybrid circuit has much less oscillatory behavior.

3. The switching delay, especially the turn off delay, is much smaller for the hybrid circuit.

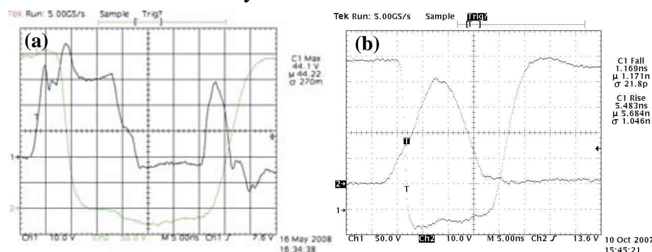

Figure 3. APT30M75 MOSFET gate and drain voltage waveforms in (a) PCB#1-TO247 package (gate: CH1, drain: CH2) and (b) PCB#2-hybrid circuit (gate: CH2, drain: CH1). Charge voltage: 300V, R_{load}: 10.6 Ω.

A patented "low inductance" commercial power MOSFET, DE275-102N06A, was also tested using the PCB#1 platform. However, because this MOSFET was not available in die form, it is compared to an APT1201R2DLL installed in PCB#3 with a single driver. Results are presented in Figure 4. Although the DE275 is a low inductance package, this device still exhibits greater oscillatory behavior on the gate waveform than the hybrid circuit, which suggests the hybrid has significantly less parasitic inductance. This is also indicated by the relative turn on speed of the MOSFETs. The turn on time of the hybrid circuit is 30% less than the DE275 MOSFET with the same gate drive and load condition, 1.66±0.04ns versus 2.41±0.04ns.

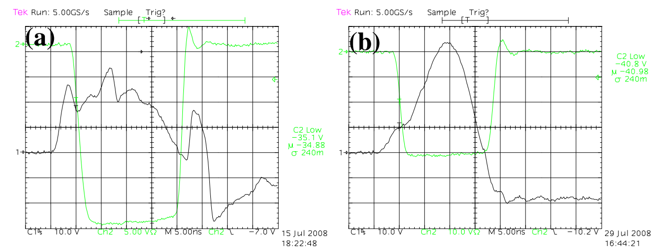

Figure 4. Comparison of the gate and output voltage waveforms of (a) DE275-102N06A MOSFET on PCB#1 and (b) APT1201R2DLL MOSFET on PCB#3 hybrid circuit. Gate voltage: CH2, Output (load) voltage: CH1 (attenuation ratio: 1:17.1). Charge voltage: 1000V, R_{Load}: 10.6Ω.

A series of experiments were performed using PCB#3 with two parallel gate drivers, measuring of the turn on time while varying the power MOSFET charge voltage (i.e. drain current) and totem pole charge voltage, Vss+ (i.e. driver current). The results are shown in Figure 5. As the charge voltage increases, so does the amount of Miller charge that must be injected into the gate to turn the power MOSFET on. At a fixed gate driver current, this translates to a longer switching time. Conversely, as Vss+ increases, the driver current increases, resulting in faster switching. However, the turn on time asymptotically approaches a minimum at Vss+ ~50 V, which is near the current limit of the P-channel MOSFET in the driver. Also, the measured switching time, ~1 ns, is near the switching limit of the power MOSFET itself.

The fastest switching was achieved using two parallel drivers on PCB#3. At near full device power; 1000 V charge and 27 Ω load (33 A), the 90% to 10% voltage fall time was 1.19±0.03ns as shown in the voltage waveform in Figure 6.

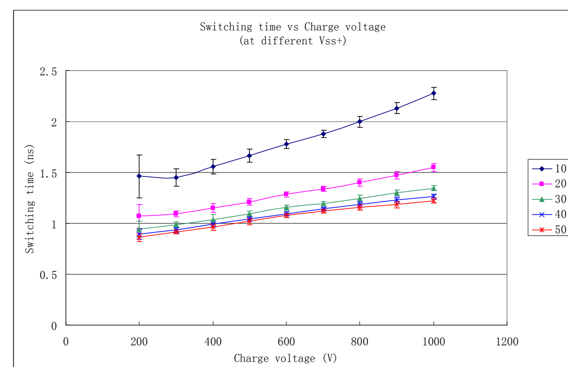

Figure 5. Switching time verses charge voltage as a function of driver Vss+. R_{Load}: 27 Ω

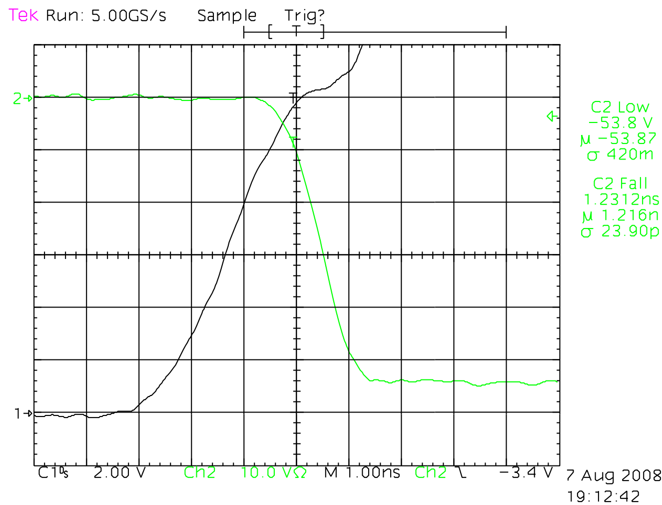

Figure 6. Ultra-fast switching achieved with the PCB#3 hybrid circuit, CH1: gate voltage, CH2: drain voltage (with 16.6:1 attenuator). Switching time: 1.19±0.03ns. Charge voltage: 1000V, R_{Load}: 27 Ω, I_{Drain}: 33A.

4 CONCLUSION

A hybrid MOSFET/driver configuration has been developed to achieve ultra-fast switching. The flip-chip assembly method was used to attach the power and driver MOSFETs on the PCB. This direct chip attachment method significantly reduces the package inductance, resulting in very good control of the power MOSFET gate and reducing the switching time to ~40% of the limit for standard packaged devices. The hybrid has demonstrated a turn on time of 1.2 ns with 1000V applied voltage and 33A drain current (27 Ω load), dI/dt ~ 3×10^{10} A/s.

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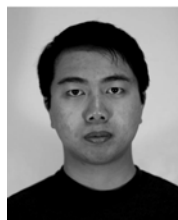

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