

Interactive and Differential Pair Routing

Summary

Application Note AP0135 (v1.2) Jun 19, 2006 After component placement, the most important stage of the PCB design process is routing the connections. Altium Designer includes a number of interactive routing features to help you efficiently and accurately route your board.

Printed circuit board design was, and by some still is, referred to as artwork. It was called artwork because the design was created by placing black objects onto clear film, and these film layers were then used to fabricate the board, in a way that is analogous to how the printing industry transfers magazine 'artwork' to print.

Artwork is still a good name, not only because of how the design is transferred to fabrication, but also because there are artistic qualities to a well designed PCB. A well routed board will have the connections between the component pins flowing in neat patterns, moving around obstacles and between layers in an ordered, yet often creative way. Good routing requires the designer to have good 3 dimensional spatial skills, a thorough and methodical approach, backed up by a sense of what gives routing style and quality.

Getting ready to route

Once the components are positioned on the board, you are ready to start routing. Before launching into Altium Designer's routing features, let's first cover the features that will help you manage the routing process.

Is it ready to route?

There is a saying that PCB design is 90% placement and 10% routing. While you could argue about the percentage of each, it is generally accepted that good component placement is the most important aspect to good board design. Keep in mind that you may need to tune the placement as your route too, perhaps running a test autoroute on a dense area first, tweaking the placement to improve routability.

Prioritizing the routing

Where to being, you ask? An autorouter typically routes connections one by one, whereas a human can consider the impact of many connections simultaneously. For the autorouter to have any hope it must do a good job of ordering the connections for routing. It will use factors such as connection length, density of connections, assignment of direction to routing layers, alignment of the connection direction to routing directions, and so on. And if it is any good, it will review the order constantly as it routes. A human will consider these factors as well, but will also use higher-order skills, such as will this set of 16

routes pass between those two components, should these noisy nets be routed on a separate pair of layers from these sensitive nets, and so on.

Using the PCB Panel

An unrouted board can appear intimidating – a mass of connection lines criss-crossing all over the board. Controlling the display of the connection lines and setting their color will help you manage the routing process.

Finding that net

A valuable feature is the PCB editor's ability to mask, or filter objects in the workspace. This feature will fade out everything except the object(s) of interest. To explore this set the mode of the **PCB** panel to **Nets**, this will display a list of nets on the board. As you click on a net name in the panel the workspace display will change, zooming to show the nodes in the net, and fading out everything except the pads and connection lines in the net – effectively *pulling out* that net from the rest of the board. Note that even when you click in the workspace the mask remains, the chosen net remains clearly visible, making it easy to examine or route. Click the <u>Clear</u> button at the bottom right of the workspace to clear the mask and restore the entire workspace to normal brightness.

Note that as well as an individual net, you can mask a Class of nets (if any classes are defined), and also multiple nets (by holding the Ctrl key as you click in the panel to select a net name).

Changing the Connection Line Color

When the design is transferred from the schematic into the PCB workspace, a default color is assigned to each connection line, as defined in the *Board Layers and Colors* dialog. An easy way to make the important nets stand out is to change the color of their connection lines. To do this, double click on the net name in the PCB panel to open the *Edit Net* dialog, where you can edit the connection line color.

Hiding/displaying connection lines

As an alternate to masking, you can completely hide one, many, or all of the connection lines. There are a number of commands to control the display of connection lines in the **View** » **Connections** submenu. You can also access these commands while you are working by pressing the **N** shortcut key.

Are the Design Rules defined?

Before you start routing you need to configure the applicable routing design rules. Select **Design Rules** from the menus to display the *PCB Rules and Constraint Editor*. The tree on the left of the dialog shows the 10 *rule categories* (Electrical, down to Signal Integrity). In each category there are a number of *rule types*, for example there are 8 different types of routing rules you can define.

Right-click on a rule type, for example **Width**, to add a new rule of that type.

Selecting a rule type will display all the rules of that type that are currently defined. Figure 1 shows the 4 routing width rules defined for a board. Note the rule priority, this defines the precedence of the rules, with 1 being the highest priority.

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Name 🖉 🖉	Priority	En	Туре	Category	Scope	Attributes	
💑 DiffPair_Width 👘	2	V	Width	Routing	InAnyDifferentialPair	Pref Width = 0.2mm	Min Width = 0.15mm
🖧 Net_GND	1	✓	Width	Routing	InNet('GND')	Pref Width = 0.3mm	Min Width = 0.2mm
🖧 Rocket IO Width	3	✓	Width	Routing	InNetClass('ROCKET_IO_LINES')	Pref Width = 0.2mm	Min Width = 0.15mm
🖧 Width	4	✓	Width	Routing	All	Pref Width = 0.2mm	Min Width = 0.127mn

Figure 1. Routing width rules defined for a board.

Click on an individual rule name in the tree on the left of the dialog to display the settings for that rule. There are 2 distinct parts to every design rule, the constraint – *what are my requirements*, and the scope – *what do I want this rule to target.* Using the routing width design rule as an example, let's look at this in more detail.

The rule constraints

The constraints of the rule specify the settings or limits you want applied to the objects targeted by this rule.



Figure 2. The rule constraint defines the requirements of that rule, this rule specifies that the routing width must be between 0.2mm and 0.6mm.

For the width rule the constraints are the minimum, preferred, and maximum widths of the track segments that make up the routing. Note that the min / preferred / max settings can also be defined for each of the layers on the board, giving you complete control over how the board is routed. A handy feature to know is that you can increase and decrease the routing width as you route, between the minimum and maximum settings, read about this in the *Changing the width during interactive routing* section.

The rule scope

Altium Designer has a powerful and flexible rule definition system, making it possible to exactly specify the design requirements, however complex they might be. Rather than defining routing requirements as attributes of the objects, design rules are defined separately, and then target the objects they apply to via the rule's *scope* – I want *this* rule to apply to *those* objects, sort of thing.

It is this ability to exactly scope each rule, in combination with the ability to assign each rule's priority that gives you complete control over the PCB design requirements.

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 Where the First object 	matches	r Full Query
	GND 🗸	InNet('GND')
💽 Net		
🔘 Net Class	~	
C Layer	Queru Helper	
Net and Layer	gdely Helpel	
Advanced (Query)	Query Builder	

Figure 3. The scope of the rule is specified by entering a query that defines what objects this rule will target.

Figure 3 shows the scope of a routing width design rule that is targeting the GND net. If the scope (Full Query) of the rule had been set to All, then it would apply to All nets on the board.

Rules are scoped by writing a query. The query is written automatically if you select from the options on the left of the dialog, like AII, Net, Net Class, and so on. If you are new to writing queries then why not try the Query Builder, it will walk you through the process and write the query for you.



For an overview of the guery system read the Introduction to the Query Language article, or for more detail read An Insiders Guide to the Query Language.

The Width rule

The most basic routing rule is the Routing Width rule, which determines the width that the nets will be routed at. As a minimum your design will have one width rule, targeting All nets on the board.

It is not good design practice to simply have only one width rule for a board, with the minimum width set to the smallest routing width you need on the board, and the maximum set to the widest route you need.

A better approach is to have one rule that targets the largest number of nets, with a scope of All. You then add extra rules that target individual nets or classes of nets, such the GND net, or the PowerNets net class (if such a class has been created). These rules will have a higher priority, so whenever you start to route one of these nets the higher priority rule will override the All nets rule, giving you the correct routing width. Suitable Width rules need to be defined before you start routing.

The Clearance Constraint

The partner to the width rule is the clearance constraint, which defines how close the net you are routing is allowed to get to other objects on that layer of the board. Again you can define multiple clearance constraints, to keep higher voltage nets or differential pair nets away from other routing, to keep polygon pours a specific distance from routing, and so on. Suitable Clearance Constraints need to be defined before you start routing.



For more information on understanding design rules, refer to the article Specifying the PCB Design Rules and Resolving Violations.

For detailed information about each rule, refer to the *Design Rules Reference*.

Setting up the routing layers

Routing layers, also referred to as signal layers, are set up in the Layer Stack Manager (Design » Layer Stack Manager). Use the controls in the dialog to add layers and set their location in the layer stack.



Figure 4. Electrical layers are added in the Layer Stack Manager.

The display of all layers, and the addition of mechanical layers, is controlled in the Board Layers and Colors dialog (press L to display it).

Board Layers and C	Colors											? 🗙
Signal Layers (S) Top Layer (T)	Color	Show	Internal Planes (P) InternalPlane1 (P)	Color	Show	Mechanical Layers(M)	Color	Show	Enable	Single Layer Mode	Linked To Sheet	^
MidLayer1 (1) MidLayer2 (2) MidLayer3 (3)		~	Internalmane2 (G)	-		PCB Boundary Gerber ID		>	>			
MidLayer4 (4) Bottom Layer (B)		>				Printout ID Dimensions		>	>			
						Mechanical 5 Mechanical 7 Design Information			> >			>
🗹 Only show layers in	layer sta	ack	🗹 Only show planes in la	iyer stack		🗹 Only show enable	d mecha	anical La	yers		<u>L</u> ayer Pairs	
Mask Layers (A)	Color	Show	Other Layers (O)	Color	Show	System Colors (Y)				Co	lor Show	
Top Paste	0		Drill Guide			Connections and Fro	om Tos					
Bottom Paste			Keep-Out Layer		~	DRC Error Markers]
Top Solder			Drill Drawing		~	Selections						
Bottom Solder			Multi-Layer	1 million	~	Visible Grid 1						
						Visible Grid 2						
						Pad Holes						
	1 - 1	1.00				Via Holes						12
Silkscreen Layers (K)	Color	Show				Highlight Color						
Top Uverlay (E)						Board Line Color						
Bottom Uverlay (R)						Board Area Color				5		
						Sheet Line Color						
						Sheet Area Color						
						Workspace Start Co	lor					
						Workspace End Col	or					
										- 20		-
<u>A</u> ll On All <u>O</u>	ff	<u>J</u> sed On	Selected On Selecte	ed Off	Cļear			De	fault Color	Set	lassi <u>c</u> Color	Set
										ОК	Can	cel

Figure 5. The display of all layers is controlled in the Board Layers and Colors dialog.

Interactive routing

Time to start routing. Interactive Routing is more than simply placing down track objects to join the dots (pads).

Altium Designer supports three interactive routing modes, all are available in the **Place** menu, and the right-click menu.

- Using the standard **Interactive Routing** mode you place down track segments to define the routing path.
- In the **Smart Interactive Routing** mode the software works with you, seeking out a path for the connection, walking around existing objects. The Smart Interactive routing mode also includes an auto complete feature, allowing you to route an entire connection with a single click.
- An extension to the Smart Interactive mode is the **Differential Pair Routing** mode, where you are routing a pair of connections simultaneously.

Standard Interactive Routing

When you select **Place** » **Interactive Routing** from the menus the PCB editor will not only let you start to place track objects, it will monitor where you click and apply all applicable design rules, it will monitor the connectivity and update the connection lines as soon as you finish a route, and it will support you with route-type shortcuts, like pressing the * key to push to the next signal layer, inserting a via in accordance with the routing via style design rule.

Interactive routing – looking ahead

The most important concept to grasp when you start routing in Altium Designer is the look-ahead feature. When you select **Place** » **Interactive Routing** and click to start routing the look-ahead feature will give you two track segments attached to the cursor, one drawn in solid color, the other as an outline. The next click you make will place the solid segment. The outline segment is so you can look-ahead to see where the next segment will go, while exactly positioning the last segment. Figure 6 shows this in detail. You can disable the look-ahead feature if you wish (press the **1** shortcut to toggle), in this mode both segments will place with each click.



Figure 6. the look-ahead feature allows you to predict the correct location of the current segment, using the next segment.

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Handling conflicts – Slam'n'jam, Push'n'shove, Walkaround, or Ignore

Routing is a juggling process, placing the new route amongst the existing component pads, tracks and vias. Altium Designer has different ways of dealing with potential conflicts created between your new route and the existing objects that you encounter during interactive routing.

Between them, the interactive routing tools have the following methods of dealing with potential conflicts created during routing.

- Stop at First Conflicting Object (obstacle) this is the default mode, and is often referred to as *slam'n'jam*, meaning that as you route you can slam up against existing objects without any fear of creating a conflict, your routing will automatically be clipped, maintaining the clearance in accordance with the design rules.
- Push Conflicting Objects (obstacles) also known as the *push'n'shove* mode, this mode will attempt to move existing track work to make way for the new routing. If the conflicting objects cannot be pushed the routing mode will drop back to the **Ignore** Objects mode. This mode is currently available in the standard Interactive router only.
- Walkaround Objects (obstacles) this mode will attempt to find a route path around obstacles. If a path cannot be found the route mode will drop back to the Stop at First Conflicting Object mode. This mode is only available in the Smart Interactive router.
- Ignore Objects (obstacles) this mode makes no attempt to avoid routing conflicts, rule violations are highlighted as you route, but you are free to route wherever you choose.

The Interactive Routing Conflict Resolution settings are configured in the PCB Editor – Routing Options page of the *Preferences* dialog. You can also cycle through the available modes while you are routing by pressing **Shift+R**, the Status bar will report the current mode.



Avoiding obstacles, note the routing is clipped to prevent a violation.



Pushing obstacles, existing routing is moved.



Walkaround obstacles, the path is found automatically.



Figure 7. Ignoring obstacles

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 System Schematic FPGA 	PCB Editor – Interactive Routing					
 Version Control Embedded System PCB Editor Board Insight Display Board Insight Modes Board Insight Modes Board Insight Nodes Board Insight Nodes Board Insight Control Board Insight Nodes The Type Fonts Mouse Wheel Configuration Defaults CB 3D Reports CAM Editor Wave 	Interactive Routing Conflict Resolution None Stop at First Conflicting Object Push Conflicting Objects Plow Through Polygons Interactive Routing Options Restrict To 30/45 Auto Complete Automatically Terminate Routing Automatically Remove Loops Smart Connection Pad Exits Allow Diagonal Interactive Routing Width / Via Size Sources Pickup Track Width From Existing Routes Track Width Mode Rule Preferred Via Size Mode Eavorite Interactive Routing Widths	Smart Connection Routing Conflict Resolution ○ None ○ Stop at First Conflicting Object ⓒ Walkaround Conflicting Object Plow Through Polygons Dragging ♥ Preserve Angle When Dragging ○ Ignore Obstacles ④ Avoid Obstacles (Snap Grid) ▲void Obstacles				
Set To Defaults 🔻 Save	Load Import From 💌	OK Cancel Apply				

Figure 8. Configure the interactive routing options in the Preferences dialog, or use the Shift+R shortcut and monitor the current mode on the Status bar.

Via on layer change

Press the * key on the numeric keypad to change to another signal layer while routing. A via will automatically be inserted, the properties of the via are determined by the applicable **Routing Via Style** design rule.

Interactive Routing Shortcuts

Press the tilda key (~) during Interactive Routing to display the available shortcuts, or refer to Table 1 at the end of this document.

Modifying existing routing

Routing is probably the most iterative process you perform designing your board, constantly defining and re-defining connection paths as the board layout evolves. This iterative nature requires routing modification tools that compliment the interactive routing tools. Altium Designer includes features that allow you to approach the task of modifying the existing routing with either your *re-router's* hat on – let me redefine that routing path, or your *drafter's* hat on – let me move that set of tracks over to free another routing channel.

The *re-router* is supported by a feature called Loop Removal. The *drafter* is supported by sophisticated dragging capabilities, which are actually useful for both modifying existing routing, and creating new routing – but more on that later.

Rerouting an existing route - loop removal

As you route there will be many instances where you need to change some of the existing routing. Rather than attempting to change the existing routing using a drafting type approach of clicking and dragging track segments, you simply re-route. To do this you select one of the **Interactive Routing** commands from the **Place** menu, click on the existing routing to start and then route the new path, coming back to meet the existing routing. This will create a loop with the old path and the new path, no need to worry though, as soon as you press **Esc** to terminate the route the old redundant segments are automatically removed, including any redundant vias. This feature is known as **Loop Removal**.



Figure 9. Re-routing an existing route, using push and shove. The old loop is automatically removed.

Protecting an existing route

There are times when this loop removal behavior works against you though, for example when you are routing a power net. You can disable Loop Removal selectively for any net, simply double click on the net name in the panel and clear the **Remove Loops** checkbox in the *Edit Net* dialog.

Smart multi-track dragging with angle preservation

Re-routing is not always the best approach to modifying the routing, for example the situation where you want to slide a track segment slightly, keeping the neat 45° and 90° corners at either end. Altium Designer supports this, with smart multi-track dragging with angle preservation.

To drag, click once on the segment to select it – the cursor will change to a quad-arrow – then click and drag to slide it to a new location. You will notice that the angles to adjacent track segments are preserved, maintaining the routing quality.

By selecting it first you have indicated that you want segments connected at either end to remain connected. Alternatively, use the **Ctrl+Click+Drag** shortcuts to drag without having to select first.

Multiple selected track segments can also be dragged, as long as they share the same orientation and are not part of the same connected copper.

Dragging behavior is controlled by the **Preserve Angle When Dragging** option in the **PCB Interactive Routing** page of the *Preferences* dialog.

Like the interactive routing modes, you can use the **Shift+R** shortcuts to cycle through options that control how obstacles should be handled during dragging (Ignore Obstacle, Avoid Obstacle or Avoid Obstacle (snap grid)). If one of the Avoid Obstacle modes is enabled the rules will be obeyed during dragging, preventing you from dragging a segment into violation. It also supports pad/via hopping, allowing you to drag a walk-around from one side of a pad or via to the other side.

Dragging on a track end will add a segment to preserve the routing quality, hold the **Alt** key before dragging to simply move the end of the segment.

To use the smart drag feature you need to select first. To support this new selection techniques have been added, press the **S** shortcut to pop up the **Selection** submenu, where you will find **Select Touching Line** and **Select Touching Rectangle**.



Note the special drag cursor.



All selected segments are dragged.



Figure 10. Selected segments have been dragged to a new location.

Using smart drag for multi-trace routing

The ability to drag multiple track segments can be used for more than just modifying existing routes, it can also be used to form new routing.

It utilizes a simple yet elegant feature for extending unconnected track ends. Clicking and dragging on the end vertex of a dangling track segment does more than extend that segment.

As well as extending the current segment, new segments are automatically added, connected at 45 degrees to the current track segments. This, in effect, gives the ability to extend existing routing.

This system also supports selecting a group of tracks and extending them, as a single entity.

To extend the routing on a set of track segments, select the segments and then click and drag on the end vertex of one of the selected segments. New segments will automatically be added as you move the mouse, when you release these segments will be selected. You can then continue to click and drag to add new segments to the end of all selected segments, as shown in Figure 11.

As well as clicking on the end vertex of a selected segment and dragging, you can also use the **Place** » **Multiple Traces** command to extend selected routing.



Figure 11. Smart dragging multiple traces – use it to quickly build up a bus of any width, using successive drags of selected track ends.

Place and gather multiple traces

Complimenting the smart drag's multi-track placement capabilities is the **Place** » **Multiple Traces** command. Using this command you can start with an unrouted component and effectively *pull* the routing out of the selected component pads. The multiple traces are then automatically gathered together, as shown in Figure 12.

The command is launched from the **Place** menu, press the **P** shortcut key to pop it up.

Keep the following tips in mind when working with the Place » Multiple Traces command:

- Rather than selecting component pads one by one, hold the **Ctrl** key as you click and drag a rectangle to select. Holding Ctrl limits the selection to the pad objects only, rather than selecting the parent component. This also works with the **Select Touching Line** and **Select Touching Rectangle** commands.
- Press the **Tab** key to open the *Bus Routing* dialog, where you set the **Bus Spacing** (track center to track center separation).
- Alternatively, use the , (comma) and . (full stop) shortcuts to interactively decrement and increment the bus spacing, in steps of the current snap grid.
- Press the **Spacebar** to change the end alignment (once the first set of segments have been placed).



• Press the ~ (Tilda) key for a list of interactive shortcuts.

Figure 12. Use the Gather and Route Bus command to start from an unrouted component.

Smart Interactive Routing

Smart Interactive Routing is the name of Altium Designer's new intelligent interactive routing mode. Smart Interactive Routing works with you in an intuitive way, attempting to completely route the chosen connection along the shortest path, using horizontal, vertical and diagonal segments, while automatically *walking around* any obstacle along the path. Smart Interactive Routing can automatically complete the entire connection if both the start and end nodes are on the same layer, while maintaining any applicable design rules.

Select **Place** » **Smart Interactive Routing** from the menus to start smart routing, or select the command from the right-click menu.



Figure 13. A set of connections being Smart Routed, each requiring just a single click to completely route that connection. Press the tilda key to display the Smart Interactive Routing shortcuts menu during routing.

Since Smart Routing is an interactive routing tool you control the behavior using the cursor and the built-in shortcuts. It has 2 basic modes of operation, an auto complete mode where it will attempt to find a path for the entire connection, and auto-complete off, where it will attempt to route up to the current cursor location.

With auto complete on the segments up to the cursor are shown as solid and will place when you click, while the segments beyond the cursor are proposed, and are shown as dashed outlines. If you like the proposed path then simply hold **Ctrl** as you click, and the entire connection is routed!

If you prefer to use it in a route-to-cursor type mode, simply press **5** to toggle auto complete off and the Smart Interactive Router will seek out a path from the connection start point up to the cursor, walking around obstacles along the way.

As well as walking around obstacles to avoid conflicting with them, you can instruct it to stop at the first conflict, or ignore conflicts – press **Shift+R** to cycle through the modes. To

select another connection leaving the pad you are routing from press the **7** shortcut. Press the **Spacebar** to change the corner mode.

Press the tilda key (~) while Smart Interactive Routing to display the available shortcuts, or refer to Table 2 at the end of this document.

Help	F1	
Commit autocomplete segments (if applicable)	Ctrl+Click	
Remove Last Segment or Shift+Backspace to remove last placed d	luster BkSp	
Terminate Current Trace	Esc	
Toggle Routing Mode	Shift+R	
Choose Favorite Width	Shift+₩	
Place Segment	Enter	
Next Layer	Num +	
Previous Layer	Num -	
Next Signal Layer	Num *	
Cycle Placement Mode	Space	
Edit Trace Properties	Tab	
Cycle Track-Width Source	3	
Cycle Via-Size Source	4	
Toggle Auto Complete	5	
Change Via mode	6	
Switch Leader trace or switch routing target in single trace mode	7	

Changing the width during interactive routing

So far you have learnt the basics of interactive routing – standard and Smart interactive routing, how to slam'n'jam or push'n'shove, how to change layers, and how to reroute or adjust existing routing.

You have also learnt that interactive routing obeys the design rules, automatically applying the defined track width, using the defined via, and maintaining the specified clearances.

There is another level to Altium Designer's interactive routing capabilities, a set of features that will make you far more productive during the crucial phase of routing the board.

Setting the constraints

The rules define the limits that are acceptable in your design. Typically there is a range to these limits, for example you might want signal tracks to be 0.2mm wide (\approx 8mils), but your board fabricator will handle a small amount of tracks down to 0.13mm (\approx 5mils), at no extra cost. Or your power fanout tracks are typically routed at 0.4mm, but you can accept them down to 0.2mm if necessary, and will always make them wider wherever it is possible!

The Routing Width design rule includes a preferred setting, use this if you want a preferred starting width that is somewhere between the minimum and maximum widths.

You configure which width should be used when you start interactive routing in the **PCB Editor – Interactive Routing** page of the *Preferences* dialog, as shown in Figure 14.



Figure 14. Specify which width should be used when you start routing a net.

Freedom, within the defined constraints

Sure you say, the minimum and maximum settings define the boundaries, and the preferred setting is handy, but I need greater choice over what width I use in a given situation.

Altium Designer can give you this – the safety of the rule boundaries, with complete flexibility to choose a width between them.

Read on to learn about the three ways you can select a different routing width while you are routing.

Imperia	al	Metric				
Width 🗠	Units	Width	Units			
5	mil	0.127	mm			
6	mil	0.152	mm			
8	mil	0.203	mm			
10	mil	0.254	mm			
12	mil	0.305	mm			
20	mil	0.508	mm			
25	mil	0.635	mm			
50	mil	1.27	mm			
100	mil	2.54	mm			
3.937	mil	0.1	mm			
7.874	mil	0.2	mm			
11.811	mil	0.3	mm			
19.685	mil	0.5	mm			
29.528	mil	0.75	mm			
39.37	mil	1	mm			
452.756	mil	11.5	mm			
Apply To All Layers						

Pick the width from pre-defined favorites

Press the **Shift+W** shortcut while you are routing to pop up a palette of pre-defined widths, and click to select the width you want, either metric or imperial.

You still have the full protection of the rules system, if the number you click on is outside the min-max rule setting the width you will be clipped back to the minimum or maximum, whichever is appropriate.

Figure 15 shows the **Choose Routing Width** list that appears when you press **Shift+W** as you route. Right-click in the dialog to hide/display the different columns.

Use the *Apply To All Layer* check box to set the current routing width in all of your signal layers.

Figure 15. Select from the pre-defined
outing widths by pressing Shift+W during
outing.

Favorite routing widths can be configured using the dialog available from the Favorite Interactive Routing Widths button in the Interactive Routing page of the *Preferences* dialog, or use the Favorite Routing Widths menu item in the Options popup menu (press O).

Note the shading in the dialog. Entries without shading indicates the preferred units of this entry, the board units will be switched automatically when the entry is chosen.

To enter a new preferred width click the Add button. If you include the units (either or mm or mil) then you can control the units you want used for that entry.

Favorite Interactive Routing Widths								
Imperia	1	Metric						
Width 🛆	Units	Width	Units					
5	mil	0.127	mm					
6	mil	0.152	mm					
8	mil	0.203	mm					
10	mil	0.254	mm					
12	mil	0.305	mm					
20	mil	0.508	mm					
25	mil	0.635	mm					
50	mil	1.27	mm					
100	mil	2.54	mm					
3.937	mil	0.1	mm					
7.874	mil	0.2	mm					
11.811	mil	0.3	mm					
19.685	mil	0.5	mm					
29.528	mil	0.75	mm					
39.37	mil	1	mm					
452.756	mil	11.5	mm					
Add Delete	e <u>E</u> dit	ОК	Cancel					

Figure 16. Use the Favorite Interactive Routing Widths dialog to add and remove your favorites.. These are saved with system preferences.

Using your own pre-defined width as you route

Figure 14 on the previous page shows the **Track Width Mode**, note that as well as being able to specify that you are given the minimum, preferred or maximum rule width when you start to route, there is also a **User Choice** option.

When you use the **Shift+W** shortcut to change the width Altium Designer will switch the **Track Width Mode** to **User Choice**, and save the setting you choose as a property of that net. The width you choose is saved as the **Current Interactive Routing Setting** property of the net, which you can see in the *Edit Net* dialog.

it Net										?
Properties	1.4			Pi	ns in Other	Nets	~		Pins in	This Net
Net Name VFILT			Pin /	Net (Befor	e Change)			Pin / Net	(Before Change)	
			U1-F19	104	e enange,		_	C64-1 VEILT	(contro onlingo)	
Connection Cold	or			U1-F20	100				C65-2 VFILT	
Hide Connection	ns 🔲			U1-F21	SRAM0 A1	5		(B21-1 VFILT	
				U1-F22	SRAM0 A1-	4			U6-5 VFILT	
Remove Loops				U1-G1	SRAM1_D1			>	U6-12 VFILT	
				U1-G2	SRAM1_D2					
				U1-G3	SP11					
				U1-G4	SP5			<		
				U1-G5	SP4					
				U1-G6	VCC			11		
				U1-G7	VCCINT		-			
Current Interactive F Current Routing	Routing Settings Layer Stack	Referen	ce		Absolute Laye	r	ſ			
Track Width	Name	1	Index	Name		Index		Via H	lole Size	
0.2mm	Bottom Layer		5	BottomL	.ayer	32		0.3r	nm	Via Diameter
0.12mm	MidLayer1		1	MidLaye	er1	2			<u> </u>	0.6mm
0.12mm	MidLayer2		2	MidLaye	er2	3		35	< \	
0.12mm	MidLayer3		3	MidLaye	er3	4		1		1 contraction of the second se
0.12mm	MidLayer4		4	MidLaye	er4	5				
0.2mm	Top Layer		0	TopLay	er	1		Ť		
							A 0	ll Wid	ths	
								Layer	s in Layer-Stack only	y
									ОК	Cancel

Figure 17. The Edit Net dialog can store user-preferred interactive routing track width settings, for this net.

Right-click on a net object and select Properties from the Net Actions sub-menu to open the Edit Net

dialog. Alternatively, double click on the net name in the **PCB** panel to open the dialog. You can define these settings in advance, and changes you make during routing are saved here.

Again you still have the full protection of the rules system, if the value you have defined in the *Edit Net* dialog is outside the min-max rule setting the width you get will be clipped back to the minimum or maximum defined in the applicable rule, whichever is appropriate.

You can cycle through the Track Width Modes (press 3) while you are routing. You can also cycle through the Via Width Modes, press 4 to do this.

Enter a width that is not pre-defined

For the ultimate level of control, you can enter a specific width while you are routing. Using Altium Designer's generic edit on-the-fly feature that is available during schematic or PCB object placement, pressing **Tab** will open the *Interactive Routing for Net* dialog, as shown in Figure 18.

Interactive Routing For Net [VFILT]	<u>?</u> 🛛
Properties Via Hole Size 0.3mm Apply to all layers (Impedance 144.7ohms) Routing Width Constraints Edit Width Rule (148.1ohms) and a maximum of 5mm (85.14ohms).	Interactive Routing Conflict Resolution None Stop at First Conflicting Object Dubh Conflicting Objects Plow Through Polygons Interactive Routing Options V Restrict To 30/45 Auto Complete Automatically Terminate Routing V Automatically Remove Loops Smart Connection Pad Exits V Allow Diagonal
Via Style Constraints Via Style is currently constrained by the rule 'RoutingVias'. The minimum and maximum hole sizes are 0.3mm and 0.5mm. The minimum and maximum diameters Set From Rule are 0.5mm and 1mm.	Interactive Bouting Width / Via Size Sources Pickup Track Width From Existing Routes Track Width Mode User Choice Via Size Mode User Choice Eavoite Interactive Routing Widths
Menu	OK Cancel

Figure 18. Press Tab while routing to open the Interactive Routing dialog, where you can enter the routing width.

Here you can type in an exact track width or via size. You can also check the current Interactive Routing settings, rather than having to drop out of routing and open the *Preferences* dialog.

The value you enter in the *Interactive Routing for Net* dialog is saved as your user choice for that net, opening the *Edit Net* dialog for that net will confirm this.

Picking up the existing track width

Figure 14 shows the routing width you will be given when you start to route. Note the **Pickup Track Width from Existing Routes** option – this feature is invaluable if you do use a variety of widths, with it on you will automatically be given the width of the existing routing that you are starting from.

To temporarily inhibit the pickup behavior hold the **Shift** key as you click to start routing. To pickup a width from an existing track on the board, start routing, then move the cursor over the track, and press the **Insert** key. Current layer objects have higher priority. Using any of these options will set the user choice value (in the *Edit Net* dialog) and switch the **Track Width Mode** to **User Choice**.

Keeping track of your Status

During interactive routing keep an eye on the status bar, it will let you know what Interactive Routing Width mode you are currently in as well as providing detailed feedback on the net, including the current routed net length.

Line 45 End:Avoid Obstacle [Width From:User Choice] [Via-Size From:User Choice] Net Length(VFILT) = 28.352mm Track[0.23mm x 0.3mm][Z0: 144.65]

Figure 19. The Status bar gives detailed information on the routing mode and the net being routed.

Differential pair routing

Background

A differential signaling system is one where a signal is transmitted down a pair of tightly coupled carriers, one of these carrying the signal, the other carrying an equal but opposite image of the signal. Differential signaling was developed to cater for situations where the logic reference ground of the signal source could not be well connected to the logic reference ground of the load. Differential signaling is inherently immune to common mode electrical noise, the most common interference artifact present in an electronic product. Another major advantage of differential signaling is that it minimizes electromagnetic interference (EMI) generated from the signal pair.

Differential pair routing is a design technique employed to create a balanced transmission system able to carry differential (equal and opposite) signals across a printed circuit board. Typically this differential routing will interface to an external differential transmission system, such as a connector and cable.

It is important to note that while the coupling ratio achieved in a twisted pair differential cable may be better than 99%, the coupling achieved in differential pair routing will typically be less than 50%. Current expert opinion is that the PCB routing task is not to try ensure a specific *differential impedance* is achieved, rather the objective is to maintain the properties required to ensure the differential signal arrives in good condition at the target component as it travels from the external cabling.

According to Lee Ritchey, a noted industry high-speed PCB design expert, successful differential signaling does not require working to a specific differential impedance. What it does require is:

- To set each of the routing signal impedances to half the incoming differential cable impedance.
- That each of the two signal lines is properly terminated in its own characteristic impedance at the receiver end.
- That the two lines should be of equal length, to within tolerances of the logic family. Typically a length difference of up to 500mils is acceptable.
- Use the benefit of routing the two signals side-by-side to help achieve good quality routing of matched lengths, where required it is acceptable to separate to route around obstacles.
- Layer changes are acceptable, as long as the signal impedances are maintained.

For more information, refer to the article *Differential Signaling Doesn't Require Differential Impedance*, by Lee W. Ritchey, available from *http://www.speedingedge.com/RelatedArticles.htm*.

Defining the differential pairs on the schematic

Pairs can be defined on the schematic by placing a Differential Pair directive (**Place** » **Directive**) on each of the nets in the pair. The net pair must be named with net label suffixes of _N and _P. Placing a Differential Pair directive on each pair net applies a parameter to the net, which has a parameter Name of **DifferentialPair** and a Value of **True**.

Differential pair definitions are then transferred to the PCB during design synchronization.

E		AA10			
S		AA9			
ž		_AB10	V_RX1_N	<i>*</i>	
Y	RANPAD 19	∑AB9	V_RX1_P	\sim	
R	RXPPAD19	~ Y9			
—	GNDA19	AB8	GND V TX1 P	,≈∓	
	TXPPAD19	AB7	V TX1 N	≂≂=	
	TXNPAD19	AA7			
	VITXPAD19	AA8			
	AVCCAUXTX19			T	

Figure 20. Place Directives on the schematic to define differential pairs.

Defining the differential pairs on the PCB

For those special circumstances where pairs cannot be defined on the schematic, differential Pair objects can also be defined in the PCB editor. To create a **Differential Pair object** and assign two nets to it, you can either select the two nets in the graphical space using the Place » **Differential Pair** command, or click the Create From Nets button in the PCB editor panel, when the panel is set to the new Differential Pair Editor mode.

Differential Pair	? 🗙
Positive Net: V_RX0_P	
Negative Net: V_RX0_N	~
Gather Control	
Properties Name: V_RX0	
OK Car	ncel

Figure 21. Create a Pair on the PCB using the Differential Pair dialog.

Placing a Differential Pair object by clicking to nominate the member nets in the graphical space will present the *Differential Pair* dialog, with the two chosen net names selected. Simply define the pair **Name** to complete the definition, as shown in Figure 21.

Clicking the **Create From Nets** button in the **PCB** editor panel will open the *Create Differential Pairs From Nets* dialog. This dialog makes it very easy to create pairs if the net names use a naming convention with a common prefix, followed by a consistent positive/negative suffix, for example TX0_P and TX0_N. Use the filters at the top of the dialog to present net pairs, based on existing net names. Figure 22 shows the set of differential pair nets on the board that end with the letters _P and _N.

Interactive and Differential Pair Routing

Create Differential Pairs From Nets							
	Use nets from class All Nets differing by P or N to create differential pair with prefix . Create differential pairs in class All Differential Pairs						
	Differential Pair Name	Positive Net	Negative Net	Create			
	D_TX0	TX0_P	TX0_N				
	D_RX0	RX0_P	RX0_N	✓			
	D_DX	DX_P	DX_N	✓			
			V_TXU_N	✓			
			V_RXU_N V_PV1_N	v 			
		BX1 P	BX1 N	 ✓ 			
		V TX1 P	V TX1 N	 Image: A start of the start of			
	TX1	TX1_P	TX1_N	✓			
_							
				Execute C	lose		

Figure 22. Quickly create pairs for the entire board, based on logical net naming.

Viewing and Managing the Pairs

Differential pair definitions are viewed and managed in the **PCB** editor panel, set to **Differential Pairs Editor**. Figure 23 shows the pairs that belong to the All Differential Pairs class. Pair D_V_TX1 is highlighted, the nets in this pair are V_TX1N and V_TX1P. The (-) and (+) displayed next to each member net name is a system flag, indicating if it is the positive or negative member of the pair.

Applicable design rules

There are 3 design rules you will need to configure to route a differential pair. These are:

- Routing Width defines the routing width required for both nets in the pair. Set the scope of this rule to target objects that are members of a differential pair, eg. *InDifferentialPair*.
- Differential Pairs Routing defines the separation between the nets in the pair, the gap allowed, and the overall uncoupled length (the pair is uncoupled when the gap is wider than the Max Gap setting). Set the scope of this rule to target objects that are a differential pair, eg. *IsDifferentialPair*.
- Matched Net Length defines how much the overall routing lengths can differ for the two nets in the pair. Note that the rule is also used to configure the routing shape to be used if you run the Equalize Net Length command. Set the scope of this rule to target objects that are a differential pair, eg. *IsDifferentialPair*.

Setting the Scope of the Design Rules

PCB 🔻 🗙					
Differential Pairs Editor					
Apply X Clear					
Mask Select Zoom Clear Existing					
1 Differential Pair Class (1 Highlighted)					
All Differential Pairs					
7 Differential Pairs (1 Highlighted)					
Designator A					
RX0					
RX1					
TX1					
V_RX0					
V_RX1					
V_TX0					
V_1X1					
Add 🔀 Delete 🛛 🎠 Edit					
2 Nets (0 Highlighted)					
Name 🛆					
V_RX0_N (·)					
V_RX0_P (+)					
Create From Nets 🗦 Rule Wizard					

Figure 23. Differential pairs can be viewed and managed in the Differential Pair Editor.

The scope of the design rule defines the set of objects that you want the rule to applied to. Since a differential pair is an object, you can use queries like the following examples to scope the rule to target differential pairs:

- InDifferentialPairClass('All Differential Pairs') targets all nets in all pairs belonging to the differential pair class called All Differential Pairs.
- InDifferentialPair('D_V_TX1') targets both nets in the differential pair named D_V_TX1.
- (IsDifferentialPair And (Name = 'D_V_TX1')) targets the differential pair object that has a name
 of D_V_TX1.
- (IsDifferentialPair And (Name Like 'D*')) targets all differential pair objects whose name starts with the letter D.

Using the Differential Pair Wizard to define the rules

Clicking the **Rule Wizard** button in the Differential Pairs Editor (**PCB** panel) will walk you through the process of setting the required design rules. Note that the scope used for the created rules will depend on what was selected when the Rule Wizard button was clicked – if one pair was selected the rules will target the nets in and that pair, but if a differential pair class was selected then the rules will target the nets in and all pairs in that class.

Routing a differential pair

Differential pairs are routed as a pair – that is you route two nets simultaneously. To route a differential pair select **Place** » **Smart Diff Pair Routing** from the menus. You will be prompted to select one of the nets in the pair, click on either to start routing. Figure 24 shows a differential pair being routed. To make the connection lines for the pair easier to see, click on the pair in the Differential Pair Editor. This will mask all other nets in the design.



Figure 24. Both nets in the differential pair are routed simultaneously.

Differential pairs are routed using Altium Designer's new Smart Interactive Routing mode, which is described earlier in this document. Standard routing shortcuts remain, such as pressing the * key on the numeric keypad to switch to the next routing layer. During differential pair routing the Smart Route shortcuts are also available, as shown in Table 2.

Full differential pair support for FPGA designs, including pin swapping

Modern FPGAs, even those with very low cost, can have a large number of I/O pins that can be configured as differential pairs. To make it easy to harness the power of these Altium Designer includes full support for integration of FPGA-based differential pairs, in both the FPGA design and the PCB design.

In your FPGA design you can assign a single net to a differential I/O standard, such as LVDS, and this will be mapped to a pair of physical nets at the PCB design level. This process is under your control using the **FPGA Signal Manager**.

The design compiler can also determine if the pins used as differential pairs at the PCB design level map correctly to the allowable pairs on an FPGA device.

Signal Integrity support for differential pairs

Altium Designer's Signal Integrity analyzer provides full support for the simulation of differential pairs. This uses the correct signal integrity model for pins when using the LVDS standard with FPGAs.

Fanout and Escape routing

Altium Designer has excellent surface mount component fanout tools. These have been enhanced by the addition of support for BGA Escape routing. The escape routing engine will attempt to route each pad out to just beyond the edge of the device – making the remaining routing challenge much easier.



Figure 25. Note how the escape route feature presents each connected pad as an accessible route outside the edge of the BGA.

Figure 25 shows the escape routing from a 1mm pad pitch BGA. Used inner pads are first fanned out using the traditional dog-bone (a short route with a via on the end) to access another layer, and then from the via they are escape routed out just beyond the edge of the device, working through the available routing layers until all pads have been escape routed.

Right-click on a BGA and select **Component Actions** » **Fanout Component** from the context menu. The routing will be done in accordance with the applicable design rules. A report of all pads that could not be escape routed will be generated and opened, click on an entry in the report to cross probe to the PCB and examine that object.

Interactive routing shortcuts

Standard Interactive Routing Shortcut Keys				
~	Tilda, display list of shortcuts			
Backspace	Remove Last Segment			
Escape	Terminate Current Trace			
Shift+R	Toggle Routing Mode			
Shift+W	Open Choose Favorite Width dialog. Widths are defined via the Interactive Routing page of the Preferences dialog.			
,	Decrease Arc Setback			
	Increase Arc Setback			
1	Connect To Internal Plane			
Enter	Place Segment			
Plus (+)	Next Layer			
Minus (-)	Previous Layer			
Multiply (*)	Next Signal Layer			
Space	Cycle Placement Mode			
Shift+Space	Cycle corner styles (if restrict to 90/45 is not enabled)			
Tab	Edit Trace Properties			
1	Toggle Look-ahead Mode – Switches between 1 and 2 segment placement mode.			
2	Add via, no layer change			
3	Cycle Track Width source			
4	Cycle Via Size source			

Table 1. Standard Interactive Routing shortcut keys.

Smart Interactive and Differential Pair routing shortcuts

Smart Interactive and Differential Routing Shortcut Keys					
~	Tilda, display list of shortcuts				
Ctrl+Click	Commit auto complete segments (if applicable)				
Backspace	Remove last segment				
Shift+Backspace	Remove last cluster of segments				
Escape	Terminate current trace				
Shift+R	Toggle Routing Mode				
Shift+W	Open Choose Favorite Width dialog. Widths are defined via the Interactive Routing page of the Preferences dialog.				
Enter	Place Segment				
Plus (+)	Next Layer				
Minus (-)	Previous Layer				
Multiply (*)	Next Signal Layer				
Space	Cycle Placement Mode				
Shift+Space	Cycle corner styles (if restrict to 90/45 is not enabled)				
Tab	Edit Trace Properties				
3	Cycle Track Width source				
4	Cycle Via Size source				
5	Toggle Auto Complete				
6	Change via mode				
7	Switch leader trace (diff pair) or switch routing target (smart interactive)				

Table 2. Smart Interactive and Differential Routing shortcut keys.

Revision History

Date	Version No.	Revision
1-Dec-2005	1.0	New release
16-Dec-2005	1.1	New interactive routing detail added
19-Jun-2006	1.2	New multi-track smart dragging detail added

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