intel®

I8212
8-BIT INPUT/OUTPUT PORT
INDUSTRIAL

- **Fully Parallel 8-Bit Data Register and Buffer**
- **Service Request Flip-Flop for Interrupt Generation**
- **Low Input Load Current — .25mA Max**
- **Three State Outputs**
- **Outputs Sink 15mA**

- **3.65V Output High Voltage for Direct Interface to ID8085A CPU**
- **Asynchronous Register Clear**
- **Replaces Buffers, Latches and Multiplexers in Microcomputer Systems**
- **Industrial Temperature Range: −40°C to +85°C**

The I8212 input/output port consists of an 8-bit latch with 3-state output buffers along with control and device selection logic. Also included is a service request flip-flop for the generation and control of interrupts to the microprocessor.

The device is multimode in nature. It can be used to implement latches, gated buffers or multiplexers. Thus, all of the principal peripheral and input/output functions of a microcomputer system can be implemented with this device.

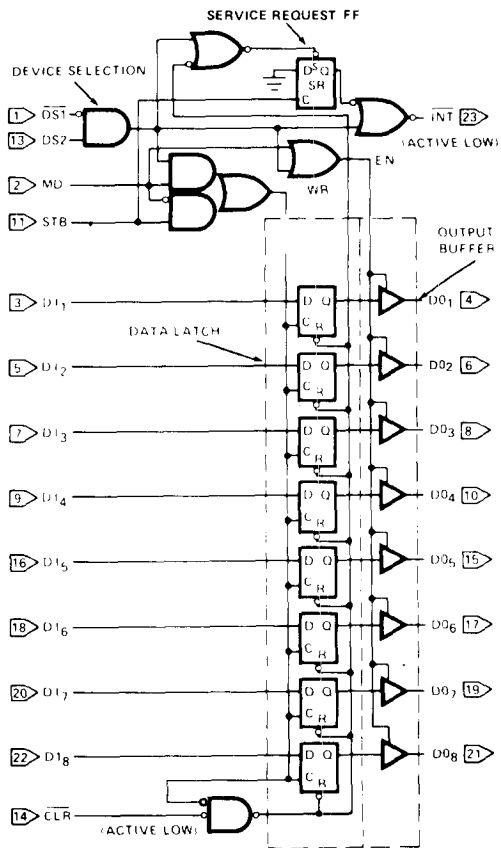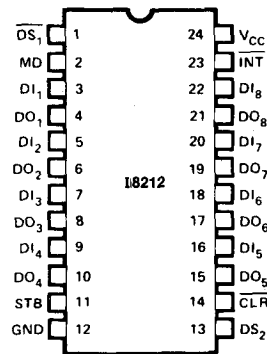Note: The specifications for the 3212 are identical with those for the 8212.

Figure 1. Logic Diagram

Figure 2. Pin Configuration

DI_1-DI_8	DATA IN
DO_1-DO_8	DATA OUT
$\overline{DS}_1$-DS_2	DEVICE SELECT
MD	MODE
STB	STROBE
$\overline{INT}$	INTERRUPT (ACTIVE LOW)
$\overline{CLR}$	CLEAR (ACTIVE LOW)

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias Plastic ...... $-40°C$ to $85°C$
Storage Temperature .... $-65°C$ to $+160°C$
All Output or Supply Voltages .... -0.5 to $+7$ Volts
All Input Voltages .... -1.0 to 5.5 Volts
Output Currents .... $100mA$

NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS ($T_A = -40°C$ to $85°C$, $V_{CC} = +5V \pm 5\%$)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
I_F	Input Load Current, ACK, DS_2, CR, DI_1-DI_8 Inputs			-.25	mA	$V_F = .45V$
I_F	Input Load Current MD Input			-.75	mA	$V_F = .45V$
I_F	Input Load Current DS_1 Input			-1.0	mA	$V_F = .45V$
I_R	Input Leakage Current, ACK, DS, CR, DI_1-DI_8 Inputs			10	μA	$V_R \leq V_{CC}$
I_R	Input Leakage Current MO Input			30	μA	$V_R \leq V_{CC}$
I_R	Input Leakage Current DS_1 Input			40	μA	$V_R \leq V_{CC}$
V_C	Input Forward Voltage Clamp			-1	V	$I_C = -5mA$
V_{IL}	Input "Low" Voltage			0.85	V	
V_{IH}	Input "High" Voltage	2.0			V	
V_{OL}	Output "Low" Voltage			0.45	V	$I_{OL} = 15mA$
V_{OH}	Output "High" Voltage	3.65	4.0		V	$I_{OH} = -1mA$
I_{SC}	Short Circuit Output Current	-15		-75	mA	$V_O = 0V$, $V_{CC} = 5V$
$|I_O|$	Output Leakage Current High Impedance State			-20 / 20	μA	$V_O = .45V$ / $V_O = 5.25V$
I_{CC}	Power Supply Current		90	130	mA	

CAPACITANCE* ($F = 1$ MHz, $V_{BIAS} = 2.5V$, $V_{CC} = +5V$, $T_A = 25°C$)

Symbol	Test	Limits	
		Typ.	Max.
C_{IN}	DS_1 MD Input Capacitance	9pF	15 pF
C_{IN}	DS_2, CK, ACK, DI_1-DI_8 Input Capacitance	5pF	10 pF
C_{OUT}	DO_1-DO_8 Output Capacitance	8pF	15 pF

*This parameter is sampled and not 100% tested.

A.C. CHARACTERISTICS ($T_A = -40°C$ to $85°C$, $V_{CC} = +5V \pm 5\%$)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
t_{PW}	Pulse Width	30			ns	
t_{PD}	Data to Output Delay			30	ns	Note 1
t_{WE}	Write Enable to Output Delay			40	ns	Note 1
t_{SET}	Data Set Up Time	15			ns	
t_H	Data Hold Time	20			ns	
t_R	Reset to Output Delay			40	ns	Note 1
t_S	Set to Output Delay			30	ns	Note 1
t_E	Output Enable/Disable Time			45	ns	Note 1
t_C	Clear to Output Delay			55	ns	Note 1

SWITCHING CHARACTERISTICS

Conditions of Test

Input Pulse Amplitude = 2.5V
Input Rise and Fall Times 5ns
Between 1V and 2V Measurements made at 1.5V
with 15mA and 30pF Test Load

Note 1:

Test	C_L^*	R_1	R_2
t_{PD}, t_{WE}, t_R, t_S, t_C	30pF	300Ω	600Ω
t_E, ENABLE↑	30pF	10KΩ	1KΩ
t_E, ENABLE ↓	30pF	300Ω	600Ω
t_E, DISABLE↑	5pF	300Ω	600Ω
t_E, DISABLE↓	5pF	10KΩ	1KΩ

*Includes probe and jig capacitance.

A.C. TESTING LOAD CIRCUIT

C_L INCLUDES JIG CAPACITANCE