



Support : Display & Systems Solution

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Tentative Product Specification

Module name: C0283QGLC-T

Issue date: 2007/05/21

Version: 1.0

Customer		
Approved by Customer		
Approved by CMEL		
PD Division	ENG Division	QA Dept

Note:

- The information contained herein may be change without prior notice. Its therefore advisable to contact Chi MEI ELCorp before designed your product based on this specification.



Reversion History

Version	Date	Page	Description
Ver.1.0	2007,5,21	All	Tentative specification was first issued



1. Purpose:

This documentation defines general product specification for OLED module supplied by CMEL. The information described in this technical specification is tentative. Please Contact CMEL's representative while your product is modified.

2. General Description:

■ Driving Mode: Active Matrix.

■ Color Mode: Full Color (262K color)

■ Driver IC: S6E63D6, COG Assembly

■ Interface:

1. MPU i80-system 18-/16-/9-/8-bit bus interface

2. MPU i68-system 18-/16-/9-/8-bit bus interface

3. Serial data transfer interface

4. RGB 18-/16-/6-bit bus interface (DOTCLK, VSYNC, HSYNC, DE, DB17-0)

■ Application: Cell phone etc..

3. Mechanical Data:

No.	Items	Specification	Unit
1	Diagonal Size	2.83"	Inch
2	Resolution	240 x RGB x 320	
3	Pixel Pitch	0.060 × 0.180	mm
4	Active Area	43.2 x 57.6	mm
5	Outline Area	49.1 x 67.3	mm
6	Thickness	2.75 (Typ) ; 2.95 (Max)	mm
7	Weight	20 (Max)	g



4. Absolute Maximum ratings:

(VSS=0V)

Item	Symbol	Unit	Value	Note
Power supply voltage 1	VDD3	V	-0.3 ~ + 5.0	
Power supply voltage 2	VCI	V	-0.3 ~ + 5.0	
Supply Voltage range	VLIN2-VLIN3	V	20	
Input Voltage range	Vin	V	-0.3 ~ VDD+0.5	

Notes:

(1) Absolute maximum rating is the limit value. When the IC is exposed operation environment beyond this range, the IC do not assure operations and may be damaged permanently, not be able to be recovered.

(2) Absolute maximum rating is guaranteed only when our company's package used.



5. Electrical Characteristic:

5.1 DC Characteristic

Characteristic	Symbol	CONDITION	MIN	TYP	MAX	Unit	Note
Driving voltage	VGH	-	3.0	-	8.0	V	
	VGL	-	-8.0	-	-3.0	V	
	VINT	-	-4.0	-	-1.0	V	
Logic Operating Voltage	RVDD	-	1.45	1.5	1.55	V	
Operating frequency	fosc	Frame frequency = 60Hz	1161.1	1290.2	1419.3	kHz	
1 st step-up input voltage	VCI1	-	2.1	-	2.75	V	
1 st step-up output voltage	VLOUT1	Without load	+4.6	-	+5.5	V	
1 st step-up output	VLOUT1	I_VLOUT1_LOAD = 2.3mA	90	95	-	%	
2 nd step-up output voltage	VLOUT2	Without load	-	8.1	-	V	
2 nd step-up output	VLOUT2	I_VLOUT2_LOAD = 0.1mA	90	93	-	%	
3 rd step-up output voltage	VLOUT3	Without load	-	-10.6	-	V	
3 rd step-up output	VLOUT3	I_VLOUT3_LOAD = 0.1mA	90	93	-	%	
Source Output voltage deviation	-	-	-	±TBD	-	mV	
Output voltage deviation	-	-	-	±TBD	-	mV	
Source driver output	Vso	-	0.96	-	4.2	V	
LTPS driver output voltage	-	-	-	-	TBD	V	
Driving voltage	dVGH	voltage deviation	-	-	TBD	V	
	dVGL		-	-	TBD	V	
Current consumption during normal operation	IVDD3	No load, Ta = 25 °C	-	-	TBD	uA	-
	IVCI	VCI=2.8V	-	-	TBD	mA	-



Characteristic	Symbol	CONDITION	MIN	TYP	MAX	Unit	Note
Power Supply Voltage	VCI	Operating Voltage	2.5	2.8	3.3	V	
Power Supply Voltage	VDD3	I/O supply Voltage	1.65	1.8	3.3	V	
Logic High level input	Vih		0.7*VDD3		VDD3	V	
Logic Low level input	Vil		0.0		0.3*VDD3	V	
Logic High level output	Voh	Iout=-1mA	0.8*VDD3		VDD3	V	
Logic Low level output	Vol	Iout=+1mA	0.0		0.2*VDD3	V	
Analog High level output	EL_ONoh	8uA	1.8		VCI	V	
Analog Low level output	EL_ONol	8uA	0		0.3	V	

(VDD3 = 1.65~3.3V, VCI = 2.5~3.3V, Ta = 25°C)

Characteristic	Symbol	CONDITION	MIN	TYP	MAX	Unit	Note
VREG1OUT		.	4.185	4.2	4.215	V	



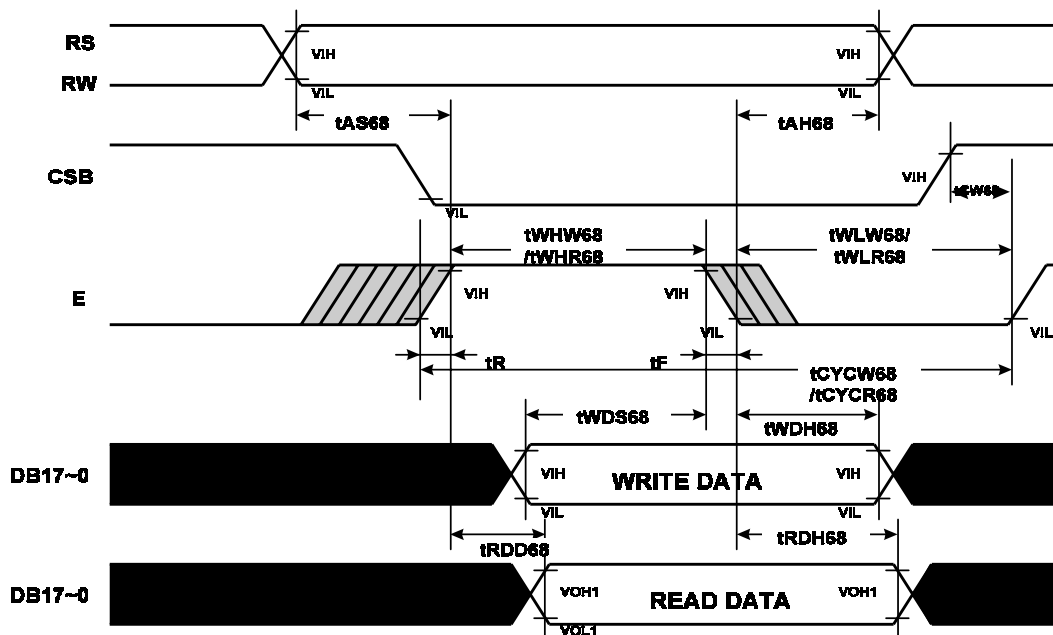
5.2 AC Characteristic

5.2.1 CPU interface M68

Table64: Parallel Write Interface Characteristics (68 Mode)

(VDD = 1.5V, VDD3 = 1.65 to 3.3V, T_A = -40 to +85°C)

Characteristic		Symbol	Specification		Unit
			Min.	Max.	
Cycle time	Write	t _{CYCW68}	85	-	ns
	Read	t _{CYCR68}	500	-	
Pulse rise / fall time		t _R , t _F	-	15	
Pulse width low	Write	t _{WHW68}	27.5	-	
	Read	t _{WHR68}	250	-	
Pulse width high	Write	t _{WLW68}	27.5	-	
	Read	t _{WLR68}	250	-	
RS,RW to CSB, E setup time		t _{AS68}	10	-	
RS,RW to CSB, E hold time		t _{AH68}	2	-	
CSB to F time		t _{CW68}	15	-	
Write data setup time		t _{WDS68}	40	-	
Write data hold time		t _{WDH68}	15	-	
Read data delay time		t _{RDD68}	-	200	
Read data hold time		t _{RDH68}	5	-	



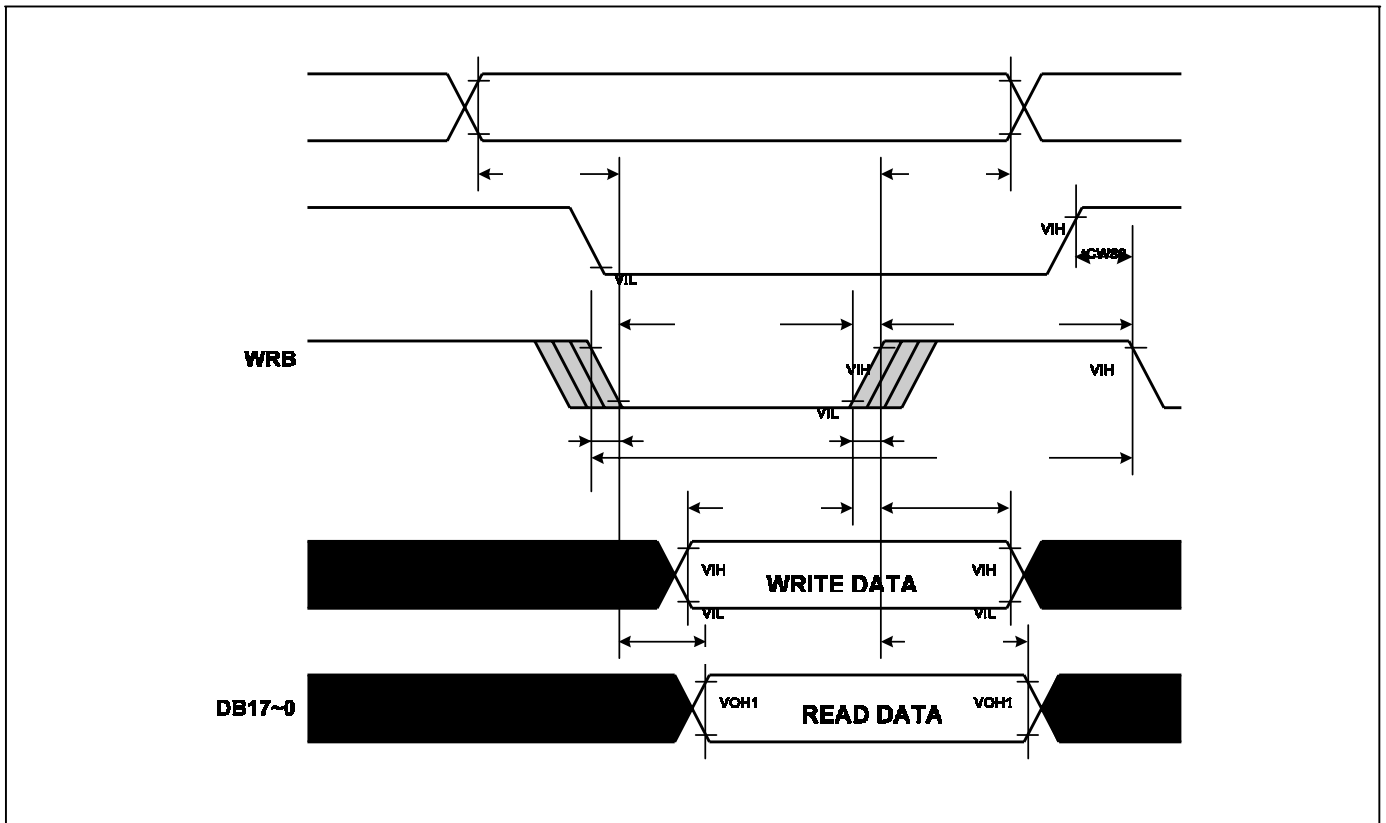


5.2.2 CPU interface M80

Table65: Parallel Write Interface Characteristics (80 Mode)

(VDD = 1.5V, VDD3 = 1.65 to 3.3V, T_A = -40 to +85°C)

Characteristic	Symbol	Specification		Unit	
		Min.	Max.		
Cycle time	Write	t _{CYCW80}	85	-	ns
	Read	t _{CYCR80}	500	-	
Pulse rise / fall time		t _r , t _f	-	15	
Pulse width low	Write	t _{WLW80}	27.5	-	
	Read	t _{WLR80}	250	-	
Pulse width high	Write	t _{WHW80}	27.5	-	
	Read	t _{WHR80}	250	-	
RS to CSB, WRB(RDB) setup time		t _{AS80}	10	-	
RS to CSB, WRB(RDB) hold time		t _{AH80}	2	-	
CSB to WRB(RDB) time		t _{cw80}	15	-	
Write data setup time		t _{WDS80}	40	-	
Write data hold time		t _{WDH80}	15	-	
Read data delay time		t _{RDD80}	-	200	
Read data hold time		t _{RDH80}	5	-	

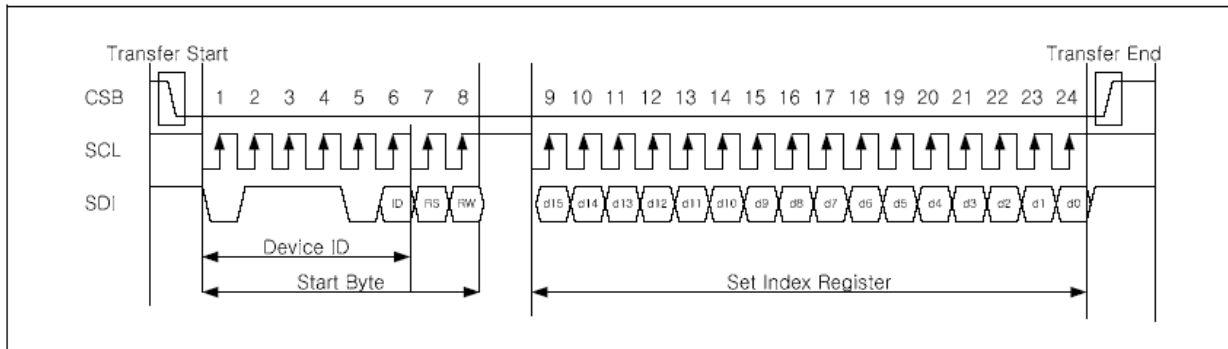




5.2.1 SPI

(VDD = 1.5V, VDD3 = 1.65 to 3.3V, T_A = -40 to +85°C)

Characteristic	Symbol	specification		Unit
		Min.	Max.	
Serial clock write cycle time	tscvc	130	-	ns
Serial clock read cycle time	tscvc	250	-	ns
Serial clock rise / fall time	t _R , t _F	-	15	ns
Pulse width high for write	tsCHW	50	-	ns
Pulse width high for read	tsCHR	110	-	ns
Pulse width low for write	tsCLW	50	-	ns
Pulse width low for read	tsCLR	110	-	ns
Chip Select setup time	tcSS	20	-	ns
Chip Select hold time	tcSH	60	-	ns
Serial input data setup time	tsIDS	30	-	ns
Serial input data hold time	tsIDH	30	-	ns
Serial output data delay time	tsODD	-	130	ns
Serial output data hold time	tsODH	5	-	ns

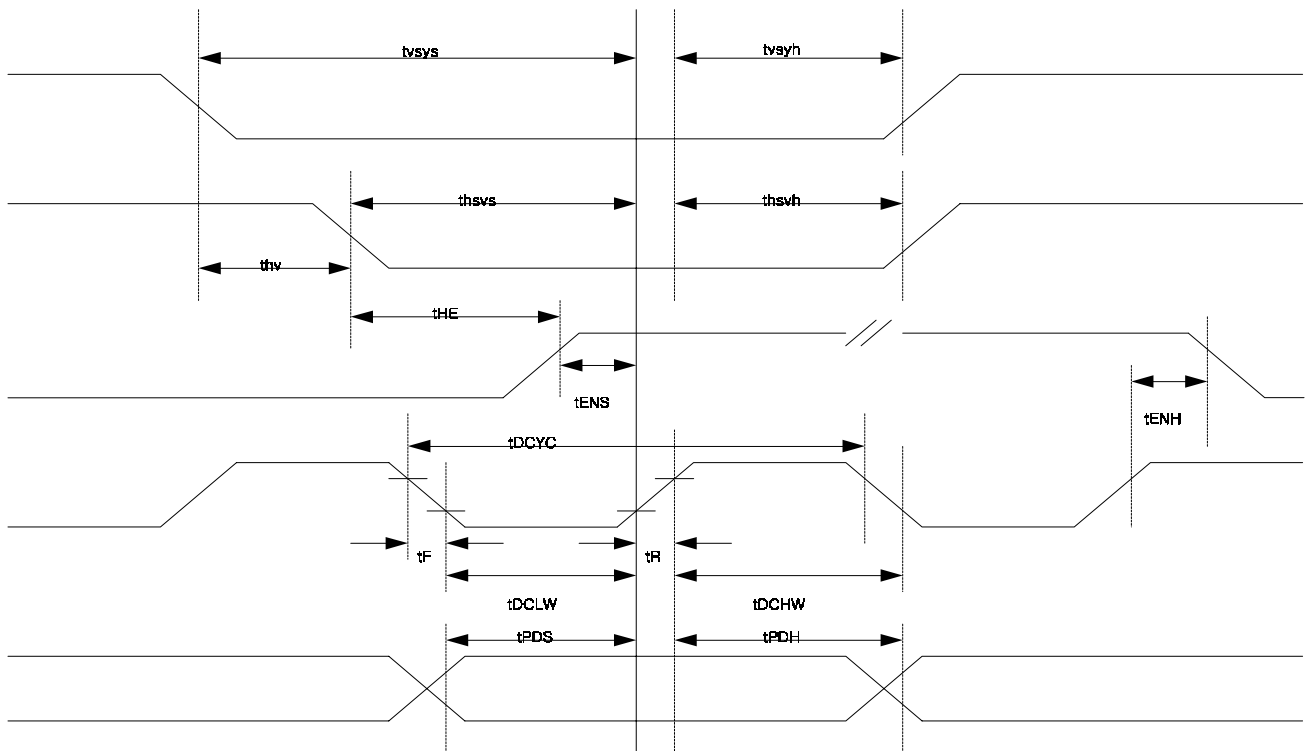




5.2.2 RGB Interface

(VDD = 1.5V, VDD3 = 1.65 to 3.3V, T_A = -40 to +85°C)

Characteristic	Symbol	18/16bit RGB interface		6bit RGB interface		Unit	
		Min.	Max.	Min.	Max.		
DOTCLK cycle time	tDCYC	100	-	100	-	ns	
DOTCLK rise / fall time	tR, tF	-	15	-	15		
DOTCLK Pulse width high	tDCHW	40	-	40	-		
DOTCLK Pulse width low	tDCLW	40	-	40	-		
Vertical Svnc Setup Time	tvsys	30	-	30	-		
Vertical Sync Hold Time	tvsyh	30	-	30	-		
Horizontal Svnc Setup Time	thsvs	30	-	30	-		
Horizontal Sync Hold Time	thsyh	30	-	30	-		
ENABLE setup time	tENS	30	-	30	-		
ENABLE hold time	tENH	20	-	20	-		
PD data setup time	tpDS	30	-	30	-		
PD data hold time	tpDH	20	-	20	-		
HSYNC-ENABLE Time	tHE	1	HBP	1	HBP		tDCYC
VSYNC-HSYNC Time	thv	1	175	1	527		



(When VSPL=0, HSPL=0, DPL=0, EPL=1)

6. Electro-Optical Characteristic:

Items	Symbol	Min	Typ.	Max	Unit	Remark
Operating Luminance	L	-	200	-	Cd/m ²	(1)(5)
Power Consumption	Pon	-	TBD	-	mW	30% pixels on (1)
Response Time	Tres	-	-	50	uS	(2)
CIEx (White)	Wx	0.25	0.30	0.35	-	(5)
CIEx(White)	Wy	0.29	0.34	0.39	-	(5)
Viewing Angle	VA	160	170	-	Degree	(3)
Contrast	CR	-	10000:1	-		(4)
Operation Lifetime	LTop	10000	-	-	Hrs	(1)(6)

Note:

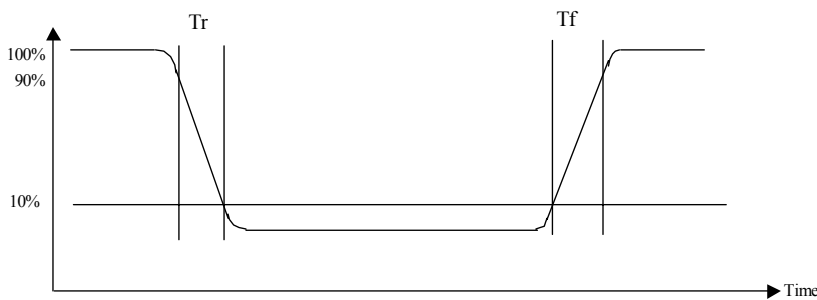
Measuring surrounding: dark room

Surrounding temperature: 25°C

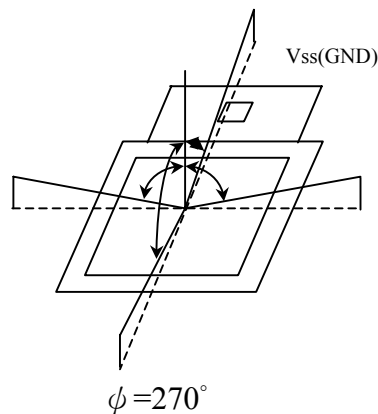
1. test condition:

TBD

2.response Time test condition



3.Viewing angle test condition:





4. Contrast

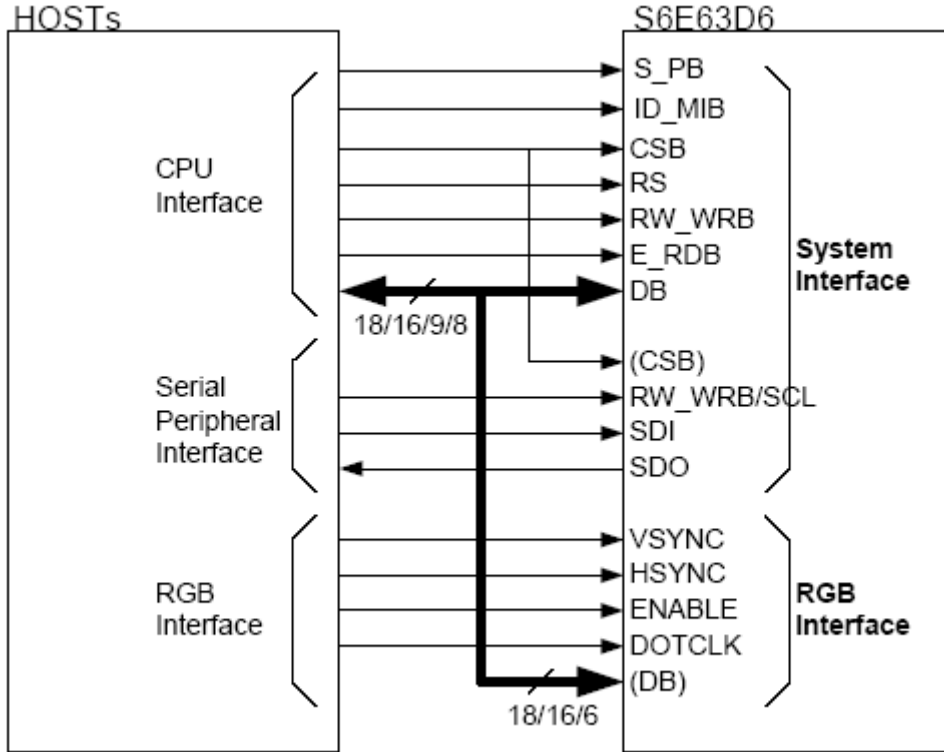
$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

5. Optical tester: Topcon SR3

6. Full White with check board at 85Hz frame rate, 1/96 duty. Operating Life Time is defined when the luminance has decayed to less than 50% of the initial measured luminance before life test.



7. System Diagram:





8. Pin Assignment:

PIN	Symbol	I/O	Description	Remarks
1	AR_VDD	I	Positive voltage for OLED	
2	AR_VSS	I	Negative voltage for OLED	
3	VCI	I	Power supply for analog circuit(2.5v~3.3v)	
4	VCI1	O	A reference voltage for 1 st booster	
5	GND	I	Ground	
6	C12M	I	External capacitance connect pin between C12M and C12P	
7	C12P	I		
8	C11M	I	External capacitance connect pin between C11M and C11P	
9	C11P	I		
10	VLOUT1	O	1 st booster output pin.	
11	C31P	I	External capacitance connect pin between C31M and C31P	
12	C31M	I		
13	C32P	I	External capacitance connect pin between C32M and C32P	
14	C32M	I		
15	VLOUT3	O	3 rd booster output pin.	
16	VLOUT2	O	2 nd booster output pin.	
17	C21P	I	External capacitance connect pin between C21M and C21P	
18	C21M	I		
19	VGS	I	A reference level for the grayscale voltage generation circuit.	
20	IOVCC	I	I/O power supply	
21	SPB	I	Select the CPU interface mode. (0=parallel interface 1=serial interface)	
22	ID_MIB	I	Select the CPU type (0=intel 80x-system 1=motorola 68x-system)	
23	DB17	I/O	BI-directional data bus. When CPU I/F, 18-bit interface : DB 17-0 16-bit interface : DB 17-10 , DB 8-1 9-bit interface : DB 8-0 8-bit interface : DB 8-1 When RGB I/F 18-bit interface : DB 17-0 16-bit interface : DB 17-0 16-bit interface : DB 17-10, DB 8-1 6-bit interface : DB 8-3 Fix unused pin to the VSS level	
24	DB16	I/O		
25	DB15	I/O		
26	DB14	I/O		
27	DB13	I/O		
28	DB12	I/O		
29	DB11	I/O		
30	DB10	I/O		
31	DB9	I/O		
32	DB8	I/O		
33	DB7	I/O		
34	DB6	I/O		



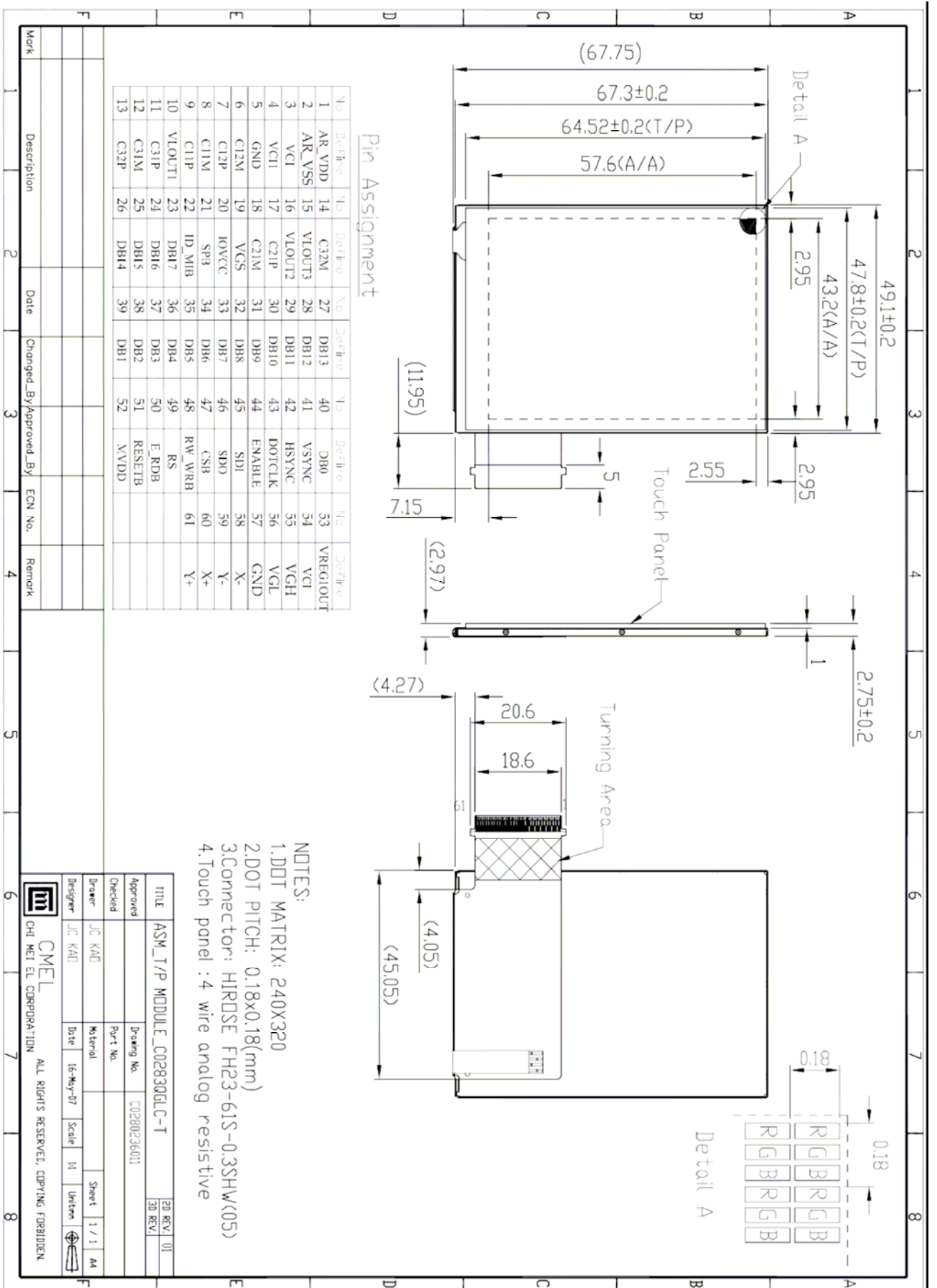
35	DB5	I/O				
36	DB4	I/O				
37	DB3	I/O				
38	DB2	I/O				
39	DB1	I/O				
40	DB0	I/O				
41	VSYNC	I	Frame-synchronizing signal. (VSPL=0 Low active, VSPL=1 High active) FIX this pin at VSS level if the pin is not used			
42	HSYNC	I	Line-synchronizing signal. (HSPL=0 Low active, HSPL=1 High active) FIX this pin at VSS level if the pin is not used			
43	DOTCLK	I	Input pin for clock signal of external interface : dot clock. DPL=0 Display data is fetched at DOTCLK's rising edge DPL=1 Display data is fetched at DOTCLK's falling edge Fix this pin at VSS level if the pin is not used.			
44	ENABLE	I	Data enablesignal pin for RGB interface.			
			EPL	ENABLE	GRAM write	GRAM address
			0	0	Valid	Updated
			0	1	Invalid	Held
			1	0	Invalid	Held
1	1	Valid	Updated			
45	SDI	I	For a serial peripheral interface(SPI), input data is fetched at the rising edge of the SCL signal, Fix SDI pin at VSS level if the pin is not used.			
46	SDO	I	For a serial peripheral interface (SPI), serves as the serial data olutput pin(SDO), Successive bits are output at the falling edge of the SCL signal.			
47	CSB	I	Chip select signal input pin. 0= driver IC is selected and can be accessed. 1= driver IC is not selected and cannot be accessed.			
448	RW_WRB	I	Pin function	CPU type	Pin description	
			RW	68-system	Read/Write operation selection pin 0=write 1=read	
			WRB	80_system	Write strobe signal.(Input pin) Data is fetched at the rising edge.	
			SCL	SPI	The synchronous clock signal	
49	RS	I	Register select pin. 0=Index/status, 1=instruction parameter, GRAM data Must be fixed at VDD3 level when not used.			
50	E_RDB	I	Pin Function	CPU type	Pin description	
			E	68-system	Read/Writeoperation enable pin	
			RDB	80_system	Read strobe signal. Read out data at the low level	
			When SPI mode is selected , fix this pin at VDD3 levle			
51	RESETB	I	Reset pin initializes the IC when low. Should be reset after power-on.			
52	MVDD	O	Internal power for RAM. Connect a capacitance to gnd.			
53	VREG1OUT	O	A reference level for the grayscale voltage.			
54	VCI	I	Power supply for analog circuit(2.5v~3.3v)			
55	VGH	O	The positive voltage used in the gate driver.			
56	VGL	O	The negative voltage used in the gate driver.			



57	GND		Ground	
58	TP1		For touch screen	
59	TP2		For touch screen	
60	TP3		For touch screen	
61	TP4		For touch screen	



9. External Dimension:





10. Reliability Test:

No.	Items	Specification
1	High Temp. Storage	85°C, 240hrs
2	Low Temp. Storage	-40°C, 240hrs
3	High Temp. Operation	70°C, 240hrs
4	Low Temp. Operation	-20°C, 240hrs
5	High Temp / Humidity Storage	85°C, 85%RH, 240hrs
6	High Temp / Humidity Operation	65°C, 90%RH, 240hrs
7	Thermal shock	-40°C ~85°C (-40°C /30min; transit /3min; 85°C /30min; transit /3min) 1cycle: 66min, 100 cycles
8	Peel strength	500g/cm (Speed~ 50mm/min)
9	Vibration	Frequency: 5~50HZ, 0.5G Scan rate : 1 oct/min Time : 2 hrs/axis Test axis : X, Y, Z
10	Drop	Height: 76cm Sequence : 1 angle 、3 edges and 6 faces Cycles: 1
11	ESD	Air discharge model, ±8kV, 10 times

Evaluation Criteria

- No damage to glass or encapsulation
- No drastic change to display
- Pixel / Line defects : no increased
- Luminance: Within +/-50% of initial value
- Uniformity: (Max-Min) / Min <15%
- Current consumption: within +/-50% of initial value



11.Package:

TBD