CMOS Analog Multiplexers

The DG506A, DG507A, DG508A and DG509A are CMOS Monolithic 16-Channel/Dual 8-Channel and 8-Channel/Dual 4-Channel Analog Multiplexers, which can also be used as demultiplexers. An enable input is provided. When the enable input is high, a channel is selected by the address inputs, and when low, all channels are off.

A channel in the ON state conducts current equally well in both directions. In the OFF state each channel blocks voltages up to the supply rails. The address inputs and the enable input are TTL and CMOS compatible over the full specified operating temperature range.

The DG506A, DG507A, DG508A and DG509A are pinout compatible with the industry standard devices.

Features

- Low Power Consumption
- TTL and CMOS-Compatible Address and Enable Inputs
- 44V Maximum Power Supply Rating
- High Latch-Up Immunity
- Break-Before-Make Switching
- Alternate Source

Applications

- Data Acquisition Systems
- Communication Systems
- Signal Multiplexing/Demultiplexing
- Audio Signal Multiplexing

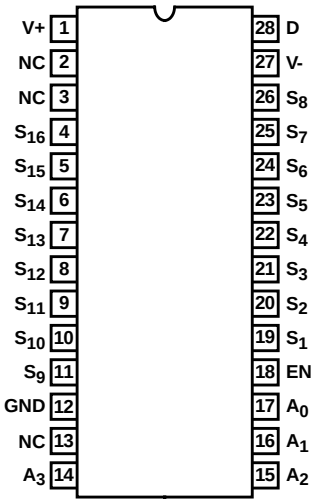
Ordering Information

PART NUMBER	TEMP. RANGE (^{O}C)	PACKAGE	PKG. NO.
DG506AAK	-55 to 125	28 Ld CERDIP	F28.6
DG506ACJ	0 to 70	28 Ld PDIP	E28.6
DG506ACY	0 to 70	28 Ld SOIC	M28.3
DG507ABK	-25 to 85	28 Ld CERDIP	F28.6
DG507ACJ	0 to 70	28 Ld PDIP	E28.6
DG507ACY	0 to 70	28 Ld SOIC	M28.3

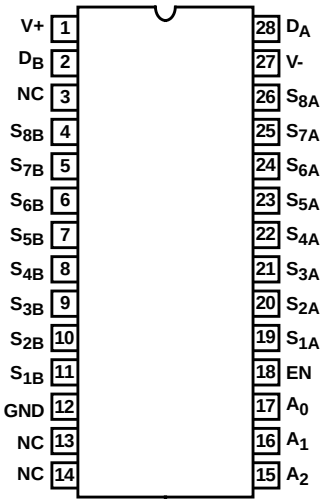
PART NUMBER	TEMP. RANGE (^{O}C)	PACKAGE	PKG. NO.
DG508AAK	-55 to 125	16 Ld CERDIP	F16.3
DG508ABK	-25 to 85	16 Ld CERDIP	F16.3
DG508ACJ	0 to 70	16 Ld PDIP	E16.3
DG509ACJ	0 to 70	16 Ld PDIP	E16.3
DG509ACY	0 to 70	16 Ld SOIC	M16.3

Pinouts

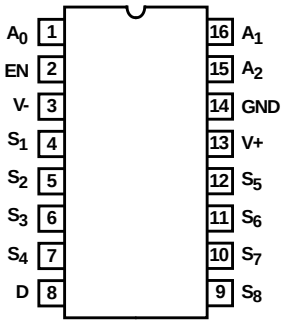
DG506A (PDIP, CERDIP, SOIC)
TOP VIEW



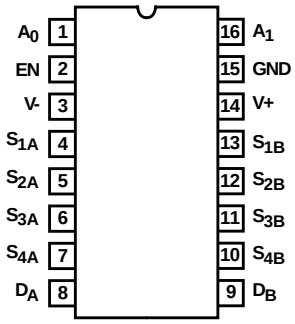
DG507A (PDIP, CERDIP, SOIC)
TOP VIEW



DG508A (PDIP, CERDIP)
TOP VIEW



DG509A (PDIP, SOIC)
TOP VIEW



Truth Tables

DG506A

A_3	A_2	A_1	A_0	EN	ON SWITCH
X	X	X	X	0	None
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16

Logic “0” = V_{AL}, $V_{ENL} \leq 0.8V$, Logic “1” = V_{AH}, $V_{ENH} \geq 2.4V$.

DG508A

A_2	A_1	A_0	EN	ON SWITCH
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

A_0, A_1, A_2, EN
Logic “1” = $V_{AH} \geq 2.4V$, Logic “0” = $V_{AL} \leq 0.8V$

DG507A

A_2	A_1	A_0	EN	ON SWITCH
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

Logic “0” = V_{AL}, $V_{ENL} \leq 0.8V$, Logic “1” = V_{AH}, $V_{ENH} \geq 2.4V$.

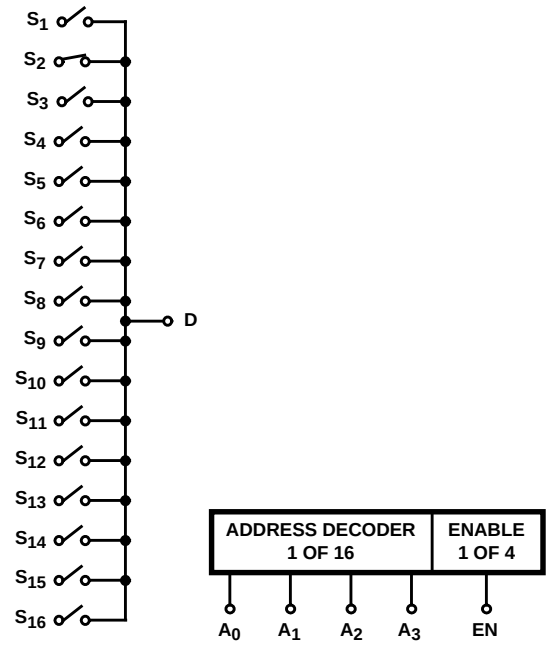
DG509A

A_1	A_0	EN	ON SWITCH
X	X	0	None
0	0	1	1A, 1B
0	1	1	2A, 2B
1	0	1	3A, 3B
1	1	1	4A, 4B

A_0, A_1, EN
Logic “1” = $V_{AH} \geq 2.4V$, Logic “0” = $V_{AL} \leq 0.8V$.

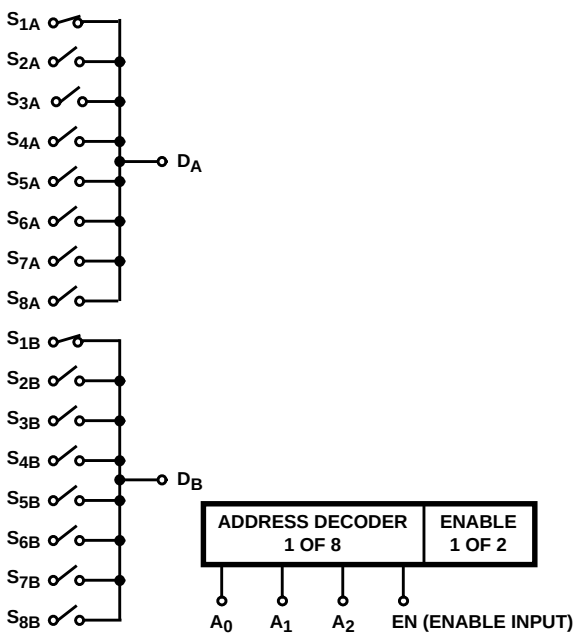
Functional Diagrams

DG506A



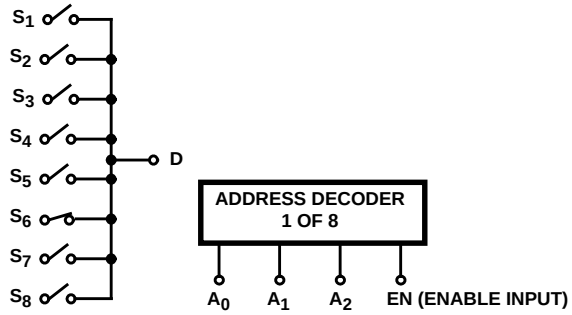
4 Line Binary Address Inputs
(0 0 0 1) and EN = 5V
Above example shows channel 2 turned ON.

DG507A



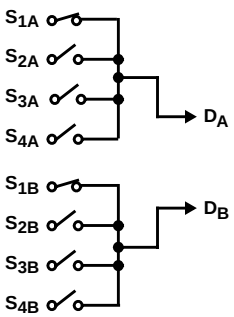
3 Line Binary Address Inputs
(0 0 0) and EN = 5V
Above example shows channels 1_A and 1_B turned ON.

DG508A



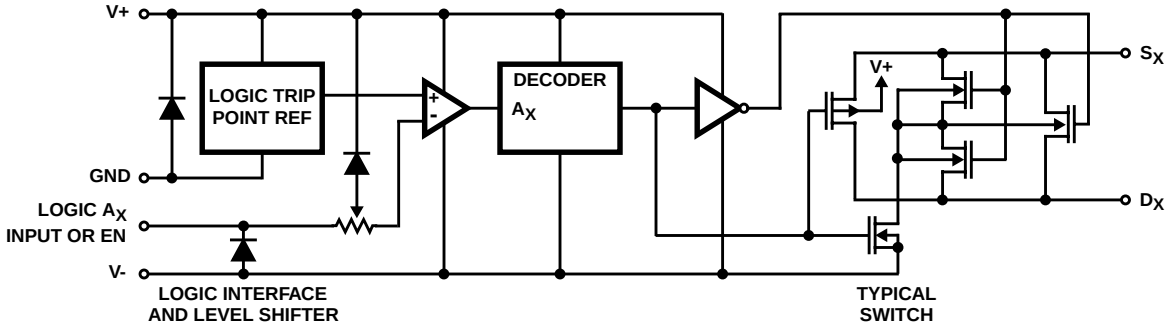
3 Line Binary Address Inputs
(1 0 1) and EN = 1
Above example shows channel 6 turned ON.

DG509A



2 Line Binary Address Inputs
(0 0) and EN = 1
Above example shows channels 1_A and 1_B turned ON.

Schematic Diagram



Absolute Maximum Ratings

V+ to V- 44V
V- to Ground. 25V
Digital Inputs, V_S, V_D (Note 1). . . . . .(V- -2V) To (V+ +2V)
Continuous Current, (Any Terminal Except S or D) 30mA
Continuous Current, (S or D) 20mA
Peak Current, S or D (Pulsed 1ms, 10% Duty Cycle Max) 40mA

Operating Conditions

Temperature Range
"A" Suffix. . . . . -55^{o}C to 125^{o}C
"B" Suffix. . . . . -25^{o}C to 85^{o}C
"C" Suffix . . . . . 0^{o}C to 70^{o}C

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (^{o}C/W)	θ_{JC} (^{o}C/W)
16 Ld CERDIP Package	75	20
28 Ld CERDIP Package	55	18
16 Ld PDIP Package	90	N/A
28 Ld PDIP Package	55	N/A
16 Ld SOIC Package	100	N/A
28 Ld SOIC Package	70	N/A

Maximum Junction Temperature
CERDIP Package. . . . . .175^{o}C
PDIP Package . . . . . .150^{o}C
Maximum Storage Temperature
"A" and "B" Suffix . . . . . -65^{o}C to 150^{o}C
"C" Suffix . . . . . -65^{o}C to 125^{o}C
Maximum Lead Temperature (Soldering 10s) . . . . . .300^{o}C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Signals on S_X, D_X, E_N, or A_X exceeding V+ or V- are clamped by internal diodes. Limit diode current to maximum current ratings.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

T_A = 25^{o}C, V+ = +15V, V- = -15V, GND = 0V, V_{EN} = 2.4V, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	"A" SUFFIX (NOTE 4) MIN	"A" SUFFIX (NOTE 3) TYP	"A" SUFFIX (NOTE 4) MAX	"B" AND "C" SUFFIX (NOTE 4) MIN	"B" AND "C" SUFFIX (NOTE 3) TYP	"B" AND "C" SUFFIX (NOTE 4) MAX	UNITS
DYNAMIC CHARACTERISTICS								
Switching Time of Multiplexer, $t_{TRANSITION}$	See Figure 1	-	0.6	1	-	0.6	-	µs
Break-Before-Make Interval, t_{OPEN}	See Figure 3	-	0.2	-	-	0.2	-	µs
Enable Turn-ON Time, $t_{ON(EN)}$	See Figure 2	-	1	1.5	-	1	-	µs
Enable Turn-OFF Time, $t_{OFF(EN)}$	See Figure 2	-	0.4	1.0	-	0.4	-	µs
OFF Isolation, OIRR	V_{EN} = 0V, R_L = 1kΩ, C_L = 15pF, V_S = 7V_{RMS}, f = 500kHz (Note 5)	-	68	-	-	68	-	dB
Source OFF Capacitance, $C_{S(OFF)}$	V_S = 0V, V_{EN} = 0V, f = 140kHz							
DG506A, DG507A		-	6	-	-	6	-	pF
DG508A, DG509A		-	5	-	-	5	-	pF
Drain OFF Capacitance, $C_{D(OFF)}$	V_D = 0V, V_{EN} = 0V, f = 140kHz							
DG506A		-	45	-	-	45	-	pF
DG507A		-	23	-	-	23	-	pF
DG508A		-	25	-	-	25	-	pF
DG509A		-	12	-	-	12	-	pF
Charge Injection, Q	See Figure 4							
DG506A, DG507A		-	6	-	-	6	-	pC
DG508A, DG509A		-	4	-	-	4	-	pC
DIGITAL INPUT CHARACTERISTICS								
Address Input Current, Input Voltage High, I_{AH}	V_A = 2.4V	-10	-0.002	-	-10	-0.002	-	µA
	V_A = 15V	-	0.006	10	-	0.006	10	µA
Address Input Current Input Voltage Low, I_{AL}	V_{EN} = 2.4V, V_A = 0V	-10	-0.002	-	-10	-0.002	-	µA
	V_{EN} = 0V, V_A = 0V	-10	-0.002	-	-10	-0.0002	-	µA

Electrical Specifications $T_A = 25^oC$, V+ = +15V, V- = -15V, GND = 0V, V_{EN} = 2.4V, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS		"A" SUFFIX (NOTE 4) MIN	"A" SUFFIX (NOTE 3) TYP	"A" SUFFIX (NOTE 4) MAX	"B" AND "C" SUFFIX (NOTE 4) MIN	"B" AND "C" SUFFIX (NOTE 3) TYP	"B" AND "C" SUFFIX (NOTE 4) MAX	UNITS
ANALOG SWITCH CHARACTERISTICS									
Analog Signal Range, V_{ANALOG}	(Note 7)		-15	-	+15	-15	-	+15	V
Drain-Source ON Resistance, $r_{DS(ON)}$	Sequence Each Switch ON V_{AL} = 0.8V V_{AH} = 2.4V	I_S = -200µA, V_D = +10V	-	270	400	-	270	450	Ω
		I_S = -200µA, V_D = -10V	-	230	400	-	230	450	Ω
$r_{DS(ON)}$ Matching Between Channels	-10V ≤ V_S ≤ +10V $\Delta r_{DS(ON)} = \frac{r_{DS(ON)MAX} - r_{DS(ON)MIN}}{r_{DS(ON)AVG}}$		-	6	-	-	6	-	%
Source OFF Leakage Current, $I_{S(OFF)}$	V_{EN} = 0V	V_S = +10V, V_D = -10V	-1	0.002	1	-5	0.002	5	nA
		V_S = -10V, V_D = +10V	-1	-0.005	1	-5	-0.005	5	nA
Drain OFF Leakage Current, $I_{D(OFF)}$	V_{EN} = 0V								
DG506A		V_S = -10V, V_D = +10V	-10	0.02	10	-20	0.02	20	nA
		V_S = +10V, V_D = -10V	-10	-0.03	10	-20	-0.03	20	nA
DG507A		V_S = -10V, V_D = +10V	-5	0.007	5	-10	0.007	10	nA
		V_S = +10V, V_D = -10V	-5	-0.015	5	-10	-0.015	10	nA
DG508A		V_S = -10V, V_D = +10V	-	0.01	10	-	0.01	20	nA
		V_S = +10V, V_D = -10V	-10	-0.015	-	-20	-0.015	-	nA
DG509A		V_S = -10V, V_D = +10V	-	0.005	10	-	0.005	20	nA
		V_S = +10V, V_D = -10V	-10	-0.008	-	-20	-0.008	-	nA
Drain ON Leakage Current, $I_{D(ON)}$	(Note 6) Sequence Each Switch ON V_{AL} = 0.8V V_{AH} = 2.4V								
DG506A		$V_D = V_{S(ALL)}$ = +10V	-10	0.03	10	-20	0.03	20	nA
		$V_D = V_{S(ALL)}$ = -10V	-10	-0.06	10	-20	-0.06	20	nA
DG507A		$V_D = V_{S(ALL)}$ = +10V	-5	0.015	5	-10	0.015	10	nA
		$V_D = V_{S(ALL)}$ = -10V	-5	-0.03	5	-10	-0.03	10	nA
DG508A		$V_D = V_{S(ALL)}$ = +10V	-	0.015	10	-	0.015	20	nA
		$V_D = V_{S(ALL)}$ = -10V	-10	-0.03	-	-20	-0.03	-	nA
DG509A		$V_D = V_{S(ALL)}$ = +10V	-	0.007	10	-	0.007	20	nA
		$V_D = V_{S(ALL)}$ = -10V	-10	-0.015	-	-20	-0.015	-	nA
POWER SUPPLY CHARACTERISTICS									
Positive Supply Current, I+	V_{EN} = 5.0V, V_A = 0V (Enabled)		-	1.3	2.4	-	1.3	2.4	mA
Negative Supply Current, I-			-1.5	-0.7	-	-1.5	-0.7	-	mA
Positive Supply Current, I+ Standby	V_{EN} = 0V, V_A = 0V (Standby)		-	1.3	2.4	-	1.3	2.4	mA
Negative Supply Current, I- Standby			-1.5	-0.7	-	-1.5	-0.7	-	mA

Electrical Specifications

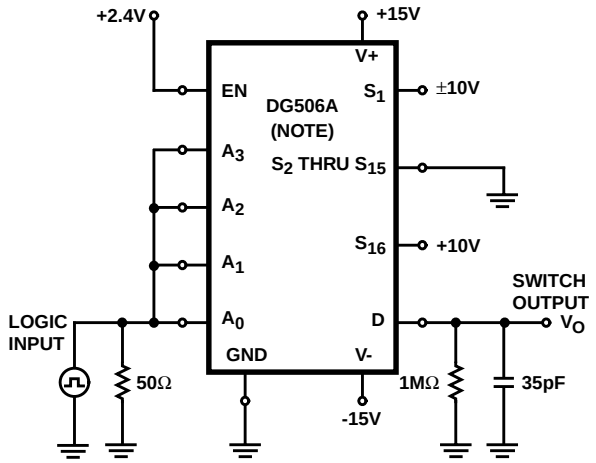
T_A = Over Operating Temperature Range, V+ = +15V, V- = -15V, GND = 0V, V_{EN} = 2.4V, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS		"A" SUFFIX MIN	"A" SUFFIX (NOTE 3) TYP	"A" SUFFIX MAX	"B" AND "C" SUFFIX MIN	"B" AND "C" SUFFIX (NOTE 3) TYP	"B" AND "C" SUFFIX MAX	UNITS
DIGITAL INPUT CHARACTERISTICS									
Address Input Current, Input Voltage High, I_{AH}	V_A = 2.4V		-30	-	-	-	-	-	µA
	V_A = 15V		-	-	30	-	-	-	µA
Address Input Current Input Voltage Low, I_{AL}	V_{EN} = 2.4V	V_A = 0V	-30	-	-	-	-	-	µA
	V_{EN} = 0V		-30	-	-	-	-	-	µA
ANALOG SWITCH CHARACTERISTICS									
Analog Signal Range, V_{ANALOG}	(Note 7)		-15	-	+15	-	-	-	V
Drain-Source ON Resistance, $r_{DS(ON)}$	Sequence Each Switch ON V_{AL} = 0.8V V_{AH} = 2.4V	I_S = -200µA, V_D = +10V	-	-	500	-	-	-	Ω
		I_S = -200µA, V_D = -10V	-	-	500	-	-	-	Ω
Source OFF Leakage Current, $I_{S(OFF)}$	V_{EN} = 0V	V_S = +10V, V_D = -10V	-	-	50	-	-	-	nA
		V_S = -10V, V_D = +10V	-50	-	-	-	-	-	nA
Drain OFF Leakage Current, $I_{D(OFF)}$ DG506A	V_{EN} = 0V	V_S = -10V, V_D = +10V	-	-	300	-	-	-	nA
		V_S = +10V, V_D = -10V	-300	-	-	-	-	-	nA
DG507A		V_S = -10V, V_D = +10V	-	-	200	-	-	-	nA
		V_S = +10V, V_D = -10V	-200	-	-	-	-	-	nA
DG508A		V_S = -10V, V_D = +10V	-	-	200	-	-	-	nA
		V_S = +10V, V_D = -10V	-200	-	-	-	-	-	nA
DG509A		V_S = -10V, V_D = +10V	-	-	100	-	-	-	nA
		V_S = +10V, V_D = -10V	-100	-	-	-	-	-	nA
Drain ON Leakage Current, $I_{D(ON)}$ DG506A	(Note 6) Sequence Each Switch ON V_{AL} = 0.8V V_{AH} = 2.4V	$V_D = V_{S(ALL)}$ = +10V	-	-	300	-	-	-	nA
		$V_D = V_{S(ALL)}$ = -10V	-300	-	-	-	-	-	nA
DG507A		$V_D = V_{S(ALL)}$ = +10V	-	-	200	-	-	-	nA
		$V_D = V_{S(ALL)}$ = -10V	-200	-	-	-	-	-	nA
DG508A		$V_D = V_{S(ALL)}$ = +10V	-	-	200	-	-	-	nA
		$V_D = V_{S(ALL)}$ = -10V	-200	-	-	-	-	-	nA
DG509A		$V_D = V_{S(ALL)}$ = +10V	-	-	100	-	-	-	nA
		$V_D = V_{S(ALL)}$ = -10V	-100	-	-	-	-	-	nA
POWER SUPPLY CHARACTERISTICS									
Positive Supply Current, I+		V_{EN} = 5.0V, V_A = 0V	-3.2	-	4.5	-	-	-	mA
Negative Supply Current, I-			-3.2	-	4.5	-	-	-	mA
Positive Standby Supply Current, I+		V_{EN} = 0V, V_A = 0V	-3.2	-	4.5	-	-	-	mA
Negative Standby Supply Current, I-			-3.2	-	4.5	-	-	-	mA

NOTES:

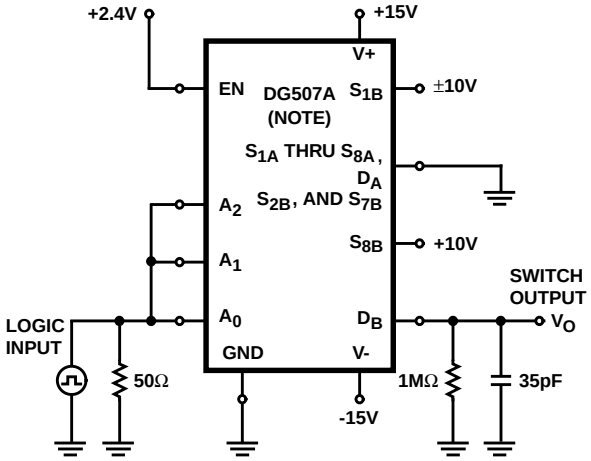
3. Typical values are for design aid only, not guaranteed and not subject to production testing.
4. The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.
5. Off isolation = 20Log $|V_S|/|V_D|$, where V_S = input to Off switch, and V_D = output due to V_S.
6. $I_{D(ON)}$ is leakage from driver into "ON" switch.
7. Parameter not tested. Parameter guaranteed by design or characterization.

Test Circuits and Waveforms



NOTE: Similar connections for DG508A.

FIGURE 1A. DG506A TEST CIRCUIT



NOTE: Similar connections for DG509A.

FIGURE 1B. DG507A TEST CIRCUIT

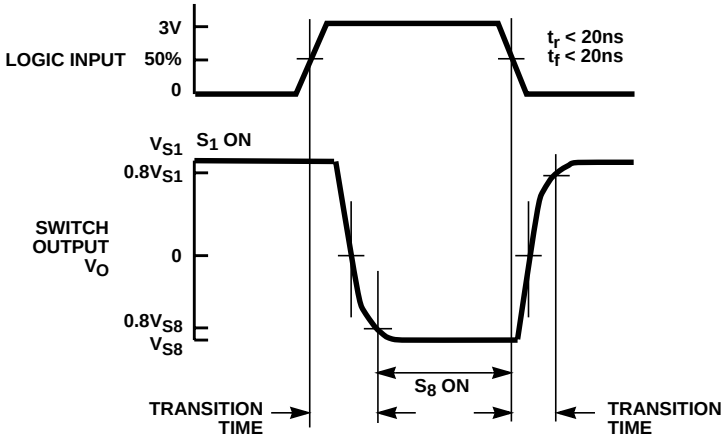
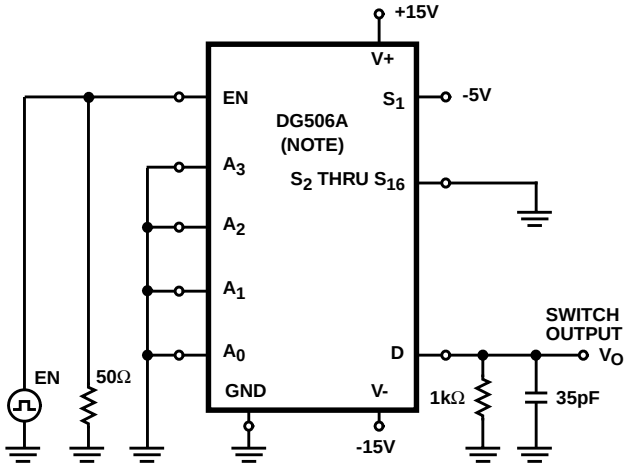


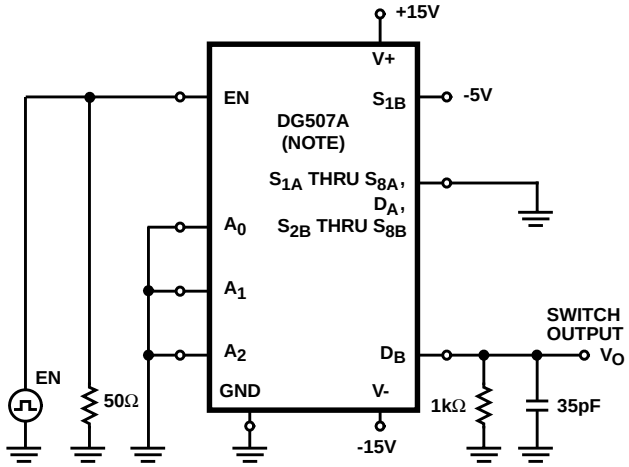
FIGURE 1C. MEASUREMENT POINTS

FIGURE 1. SWITCHING TIME



NOTE: Similar connections for DG508A.

FIGURE 2A. DG506A TEST CIRCUIT



NOTE: Similar connections for DG509A.

FIGURE 2B. DG507A TEST CIRCUIT

Test Circuits and Waveforms (Continued)

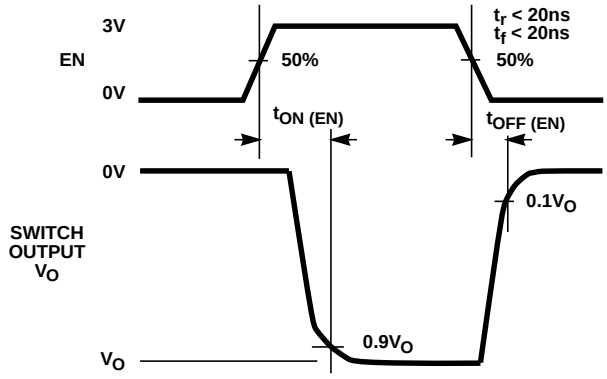
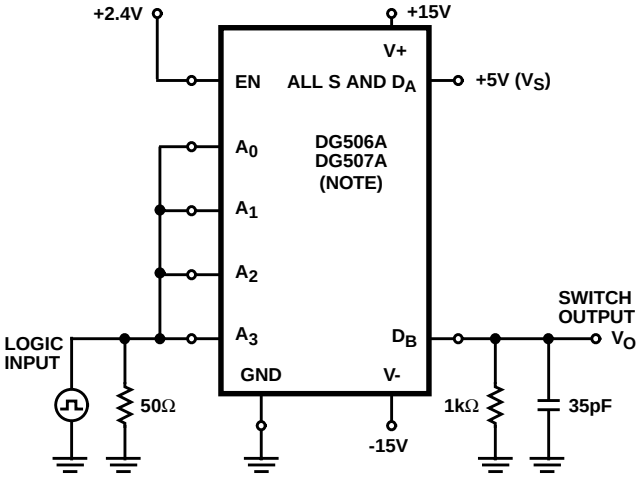


FIGURE 2C. MEASUREMENT POINTS

FIGURE 2. ENABLE TIMES



NOTE: Similar connections for DG508A, DG509A.

FIGURE 3A. TEST CIRCUIT

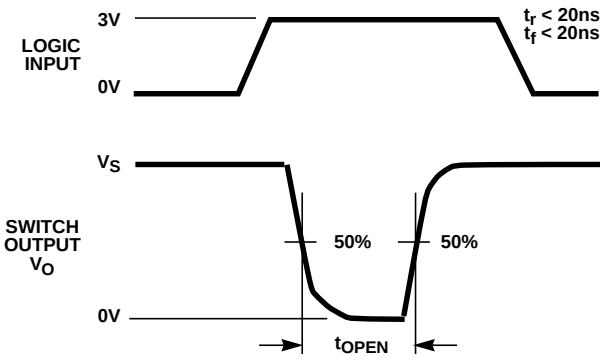
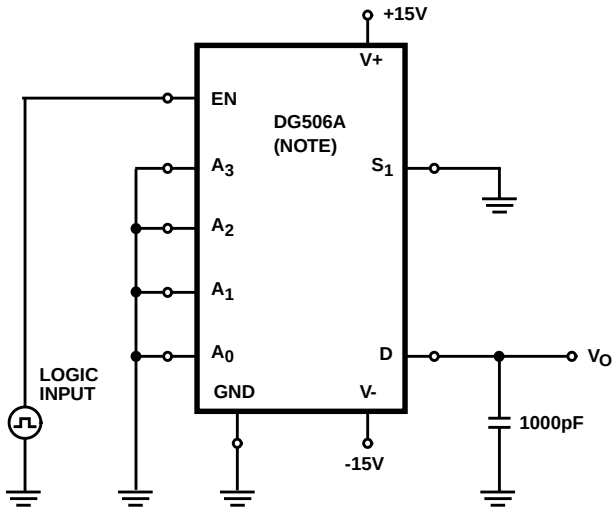


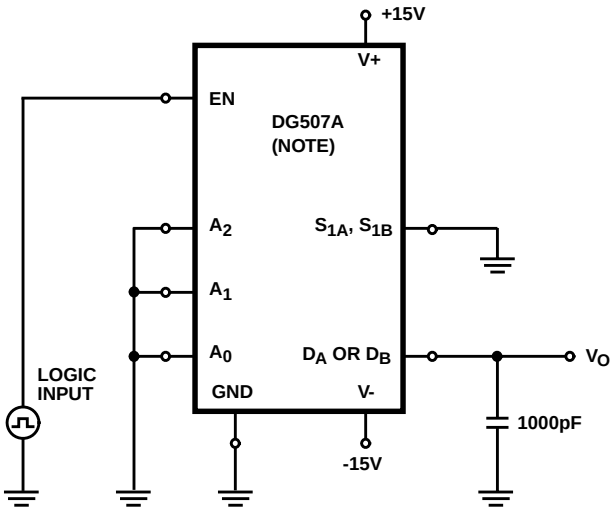
FIGURE 3B. MEASUREMENT POINTS

FIGURE 3. BREAK-BEFORE-MAKE INTERVAL



NOTE: Similar connections for DG508A.

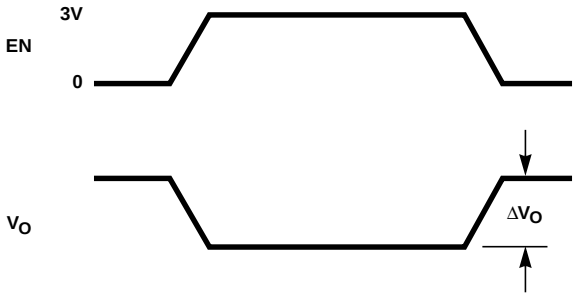
FIGURE 4A. DG506A TEST CIRCUIT



NOTE: Similar connections for DG509A.

FIGURE 4B. DG507A TEST CIRCUIT

Test Circuits and Waveforms (Continued)



ΔV_O is the measured voltage error due to charge injection.
The charge transfer error in Coulombs is $Q = C_L \times \Delta V_O$.

FIGURE 4C. CHARGE INJECTION WAVEFORMS

FIGURE 4. CHARGE INJECTION

Typical Performance Curves

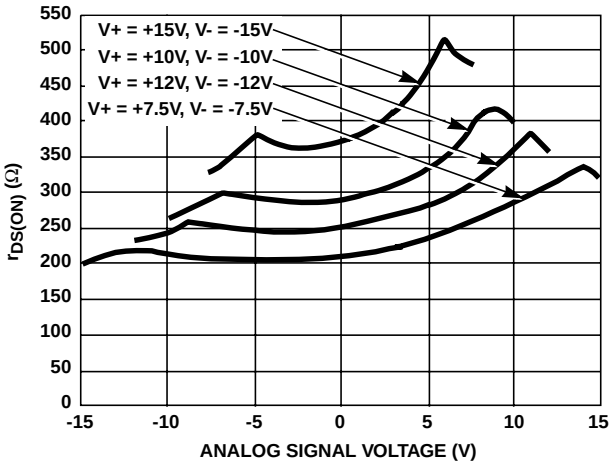


FIGURE 5. $r_{DS(ON)}$ vs ANALOG SIGNAL VOLTAGE vs SUPPLY VOLTAGE

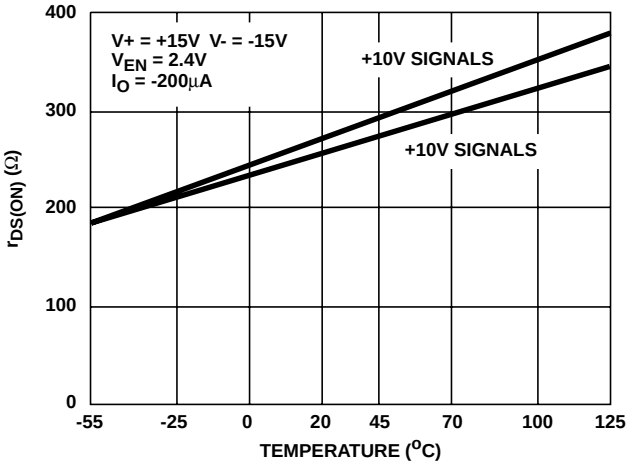


FIGURE 6. TYPICAL $r_{DS(ON)}$ VARIATION WITH TEMPERATURE

Die Characteristics

DIE DIMENSIONS:

3810µm x 2770µm

METALLIZATION:

Type: Al
Thickness: 10kÅ ±1kÅ

PASSIVATION:

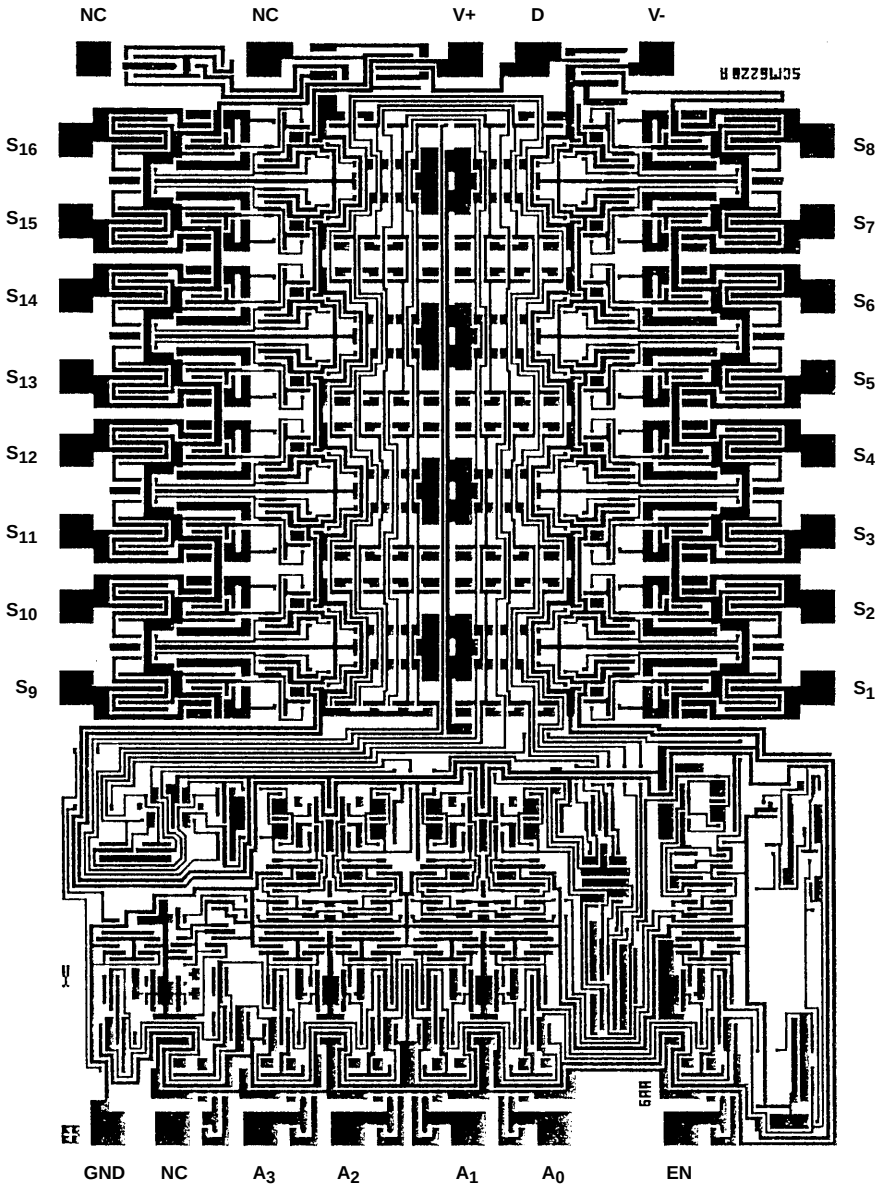
Type: PSG/Nitride
Thickness: PSG: 7kÅ ±1.4kÅ
Nitride: 8kÅ ±1.2kÅ

WORST CASE CURRENT DENSITY:

9.1×10^4 A/cm^2

Metallization Mask Layout

DG506A



Die Characteristics

DIE DIMENSIONS:

3810µm x 2770µm

METALLIZATION:

Type: Al
Thickness: 10kÅ ±1kÅ

PASSIVATION:

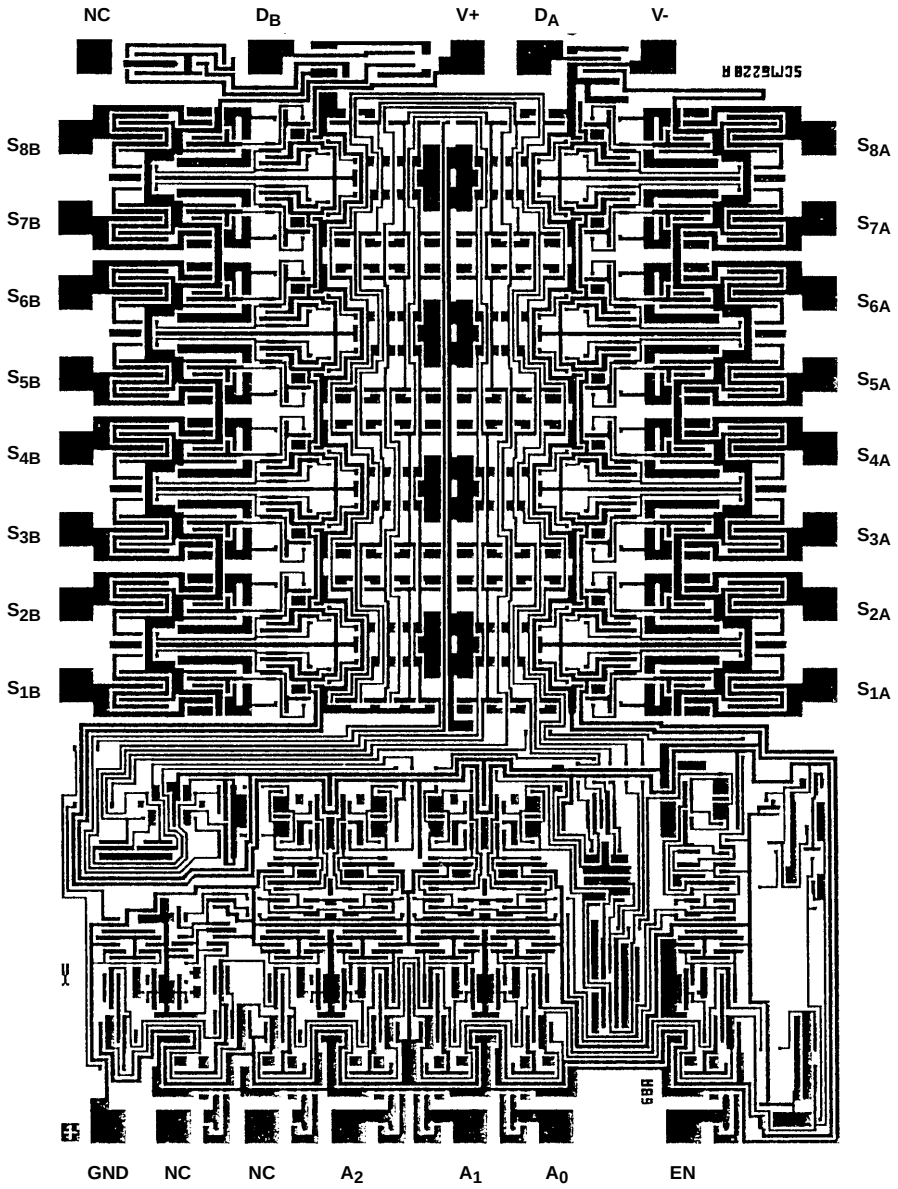
Type: PSG/Nitride
Thickness: PSG: 7kÅ ±1.4kÅ
Nitride: 8kÅ ±1.2kÅ

WORST CASE CURRENT DENSITY:

9.1×10^4 A/cm^2

Metallization Mask Layout

DG507A



Die Characteristics

DIE DIMENSIONS:

3100µm x 2083µm

METALLIZATION:

Type: Al
Thickness: 10kÅ ±1kÅ

PASSIVATION:

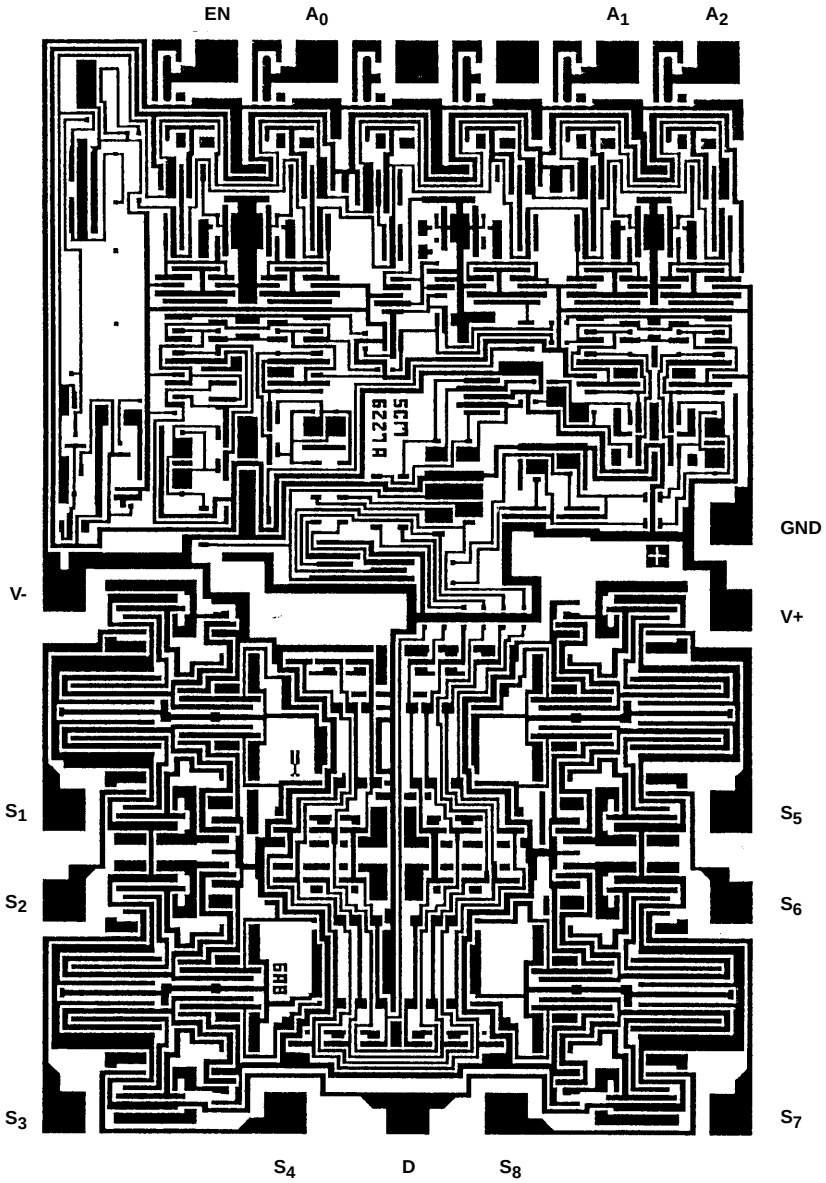
Type: PSG/Nitride
Thickness: PSG: 7kÅ ±1.4kÅww
Nitride: 8kÅ ±1.2kÅ

WORST CASE CURRENT DENSITY:

9.1×10^4 A/cm^2

Metallization Mask Layout

DG508A



Die Characteristics

DIE DIMENSIONS:

3100µm x 2083µm

METALLIZATION:

Type: Al
Thickness: 10kÅ ±1kÅ

PASSIVATION:

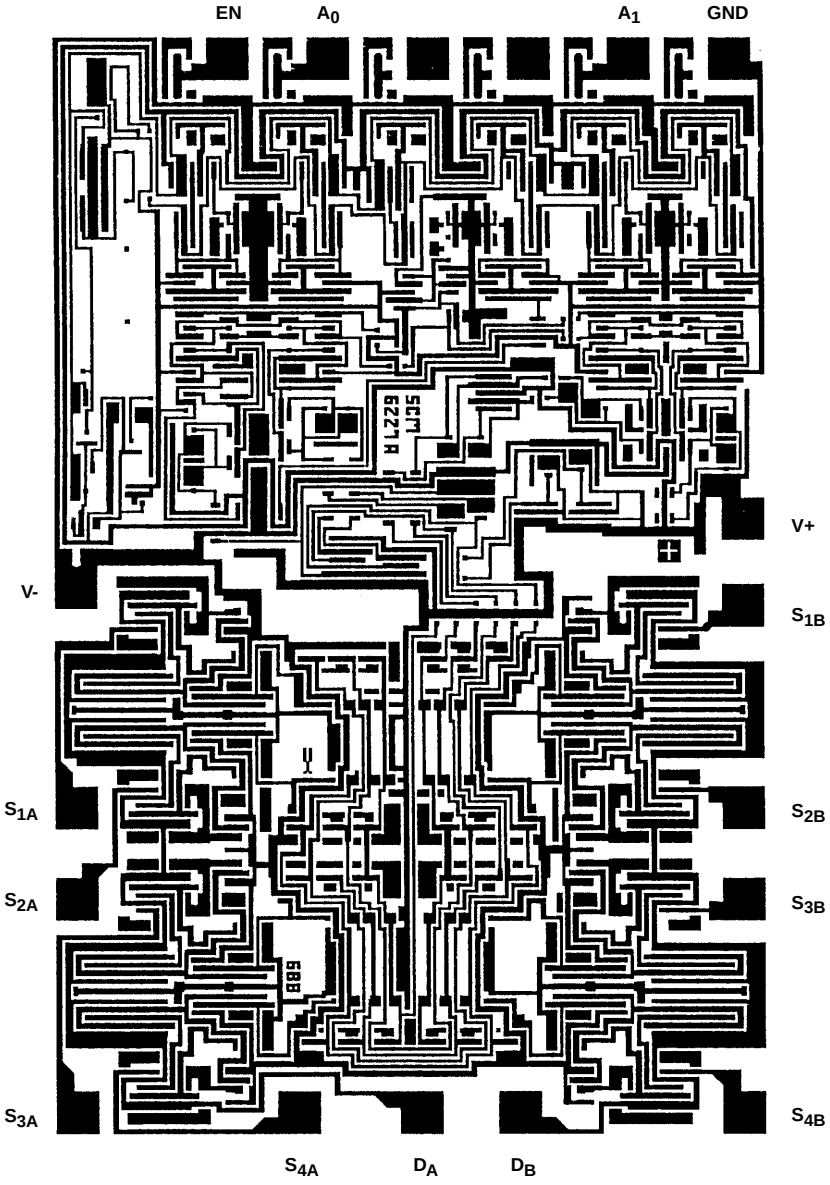
Type: PSG/Nitride
Thickness: PSG: 7kÅ ±1.4kÅ
Nitride: 8kÅ ±1.2kÅ

WORST CASE CURRENT DENSITY:

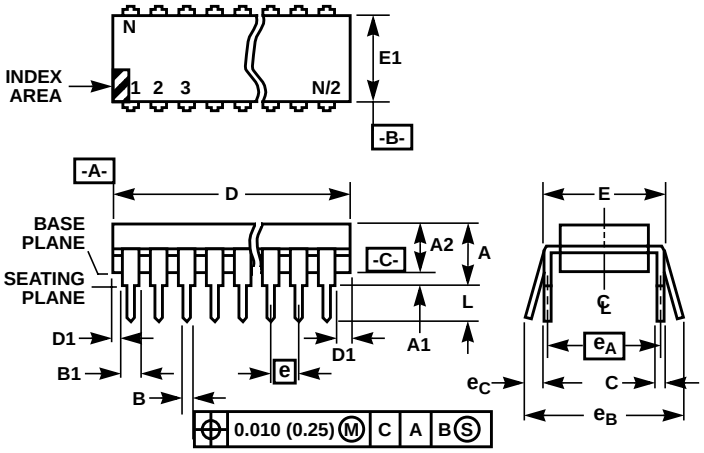
9.1×10^4 A/cm^2

Metallization Mask Layout

DG509A



Dual-In-Line Plastic Packages (PDIP)



NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E16.3 (JEDEC MS-001-BB ISSUE D)
16 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.735	0.775	18.66	19.68	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	16		16		9

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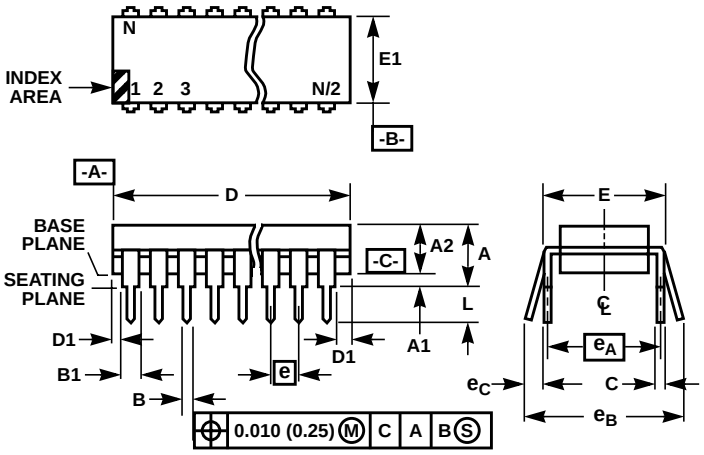
Dual-In-Line Plastic Packages (PDIP)



NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E28.6 (JEDEC MS-001-BF ISSUE D)
28 LEAD NARROW BODY DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.250	-	6.35	4
A1	0.015	-	0.39	-	4
A2	0.125	0.195	3.18	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.030	0.070	0.77	1.77	8
C	0.008	0.015	0.204	0.381	-
D	1.380	1.565	35.1	39.7	5
D1	0.005	-	0.13	-	5
E	0.600	0.625	15.24	15.87	6
E1	0.485	0.580	12.32	14.73	5
e	0.100 BSC		2.54 BSC		-
e_A	0.600 BSC		15.24 BSC		6
e_B	-	0.700	-	17.78	7
L	0.115	0.200	2.93	5.08	4
N	28		28		9

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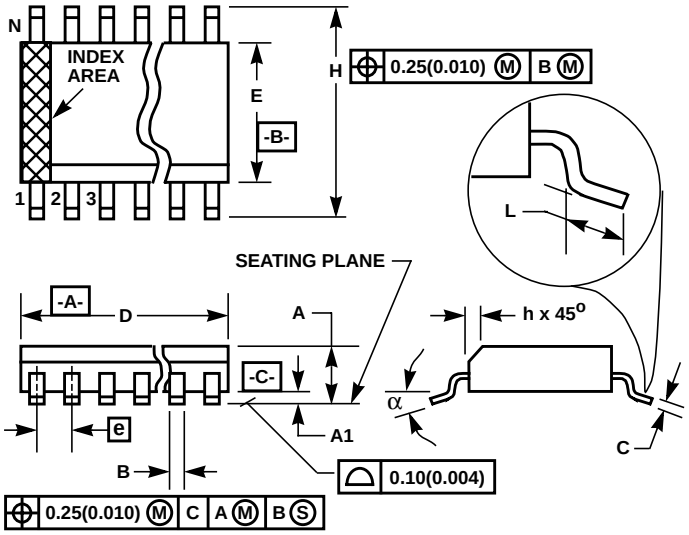
Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M16.3 (JEDEC MS-013-AA ISSUE C)
16 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.3977	0.4133	10.10	10.50	3
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0^o	8^o	0^o	8^o	-

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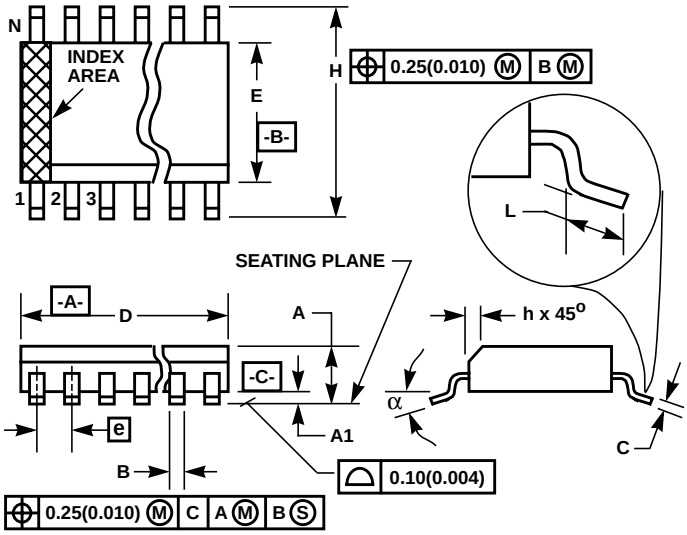
Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M28.3 (JEDEC MS-013-AE ISSUE C)
28 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

	INCHES		MILLIMETERS		
SYMBOL	MIN	MAX	MIN	MAX	NOTES
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.6969	0.7125	17.70	18.10	3
E	0.2914	0.2992	7.40	7.60	4
e	0.05 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.01	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	28		28		7
α	0^o	8^o	0^o	8^o	-

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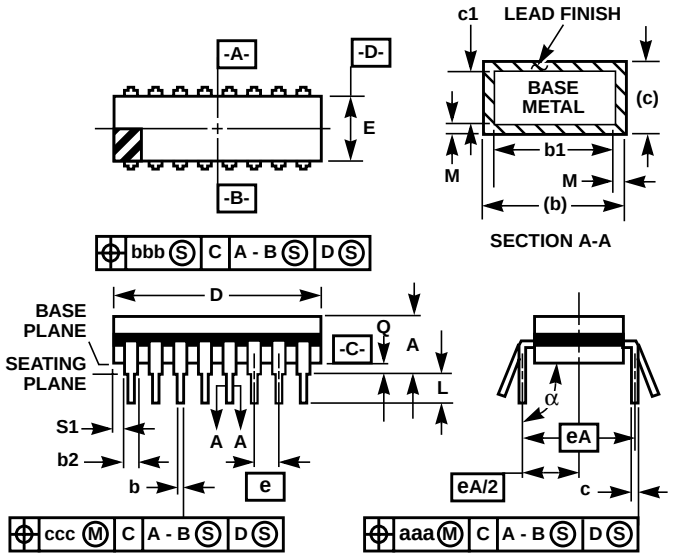
Ceramic Dual-In-Line Frit Seal Packages (CERDIP)



NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

F16.3 MIL-STD-1835 GDIP1-T16 (D-2, CONFIGURATION A)
16 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.840	-	21.34	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
α	90^o	105^o	90^o	105^o	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	16		16		8

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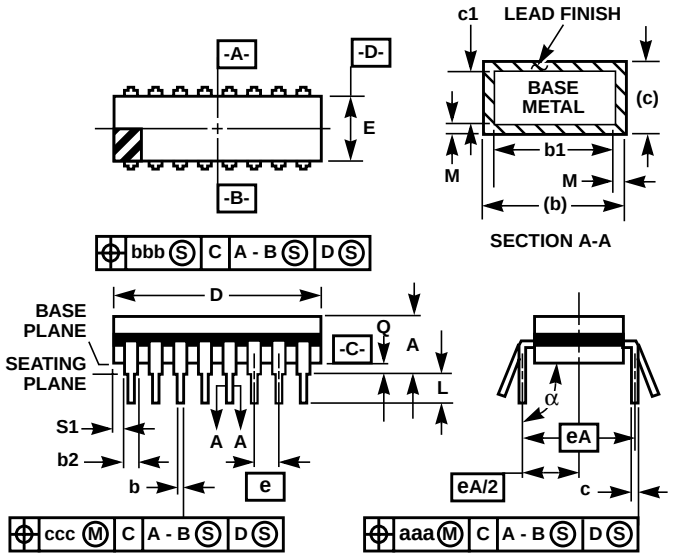
Ceramic Dual-In-Line Frit Seal Packages (CERDIP)



F28.6 MIL-STD-1835 GDIP1-T28 (D-10, CONFIGURATION A)
28 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.232	-	5.92	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	1.490	-	37.85	5
E	0.500	0.610	12.70	15.49	5
e	0.100 BSC		2.54 BSC		-
eA	0.600 BSC		15.24 BSC		-
eA/2	0.300 BSC		7.62 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
α	90^o	105^o	90^o	105^o	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	28		28		8

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NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

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