Opto-electrical isolation of the I²C-Bus

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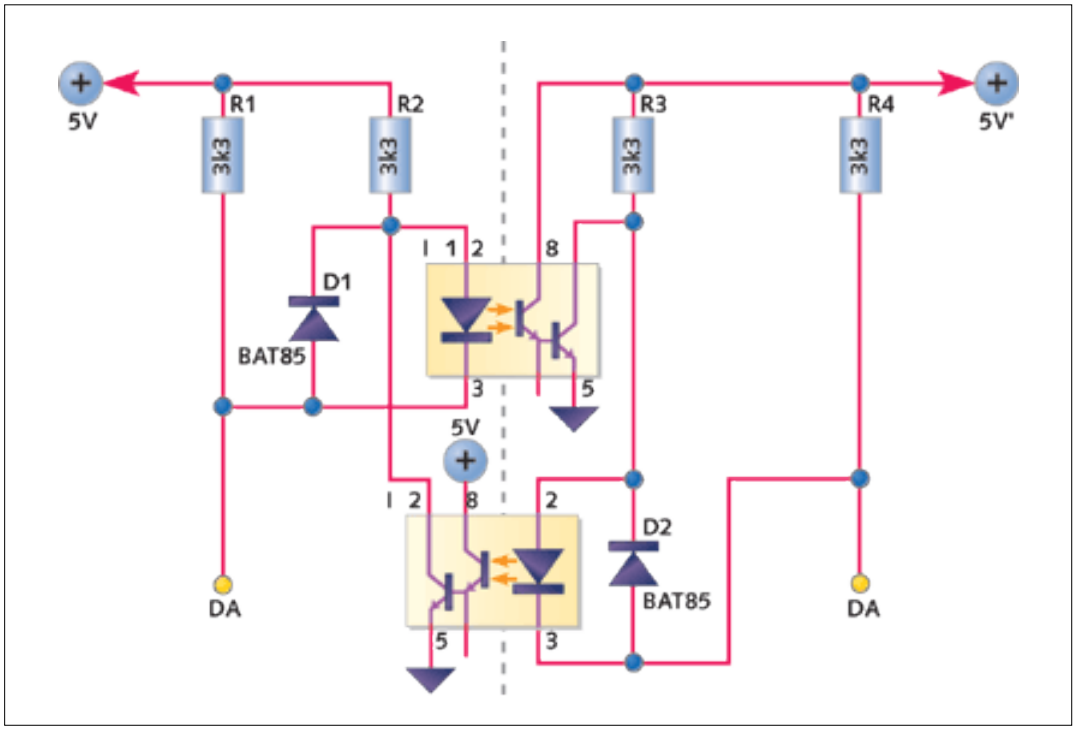

Figure 1: National Semiconductor Application circuit circa 1998

The inter-integrated circuit bus (I2C-bus) provides an attractive maintenance and control communication interface between parts of a system since it uses only two signal wires yet has powerful addressing and a reasonably fast, up to 400kHz bidirectional data handling capability. Some of these systems are connected to telephone lines or to electronic switches that are directly connected to the high-voltage AC main power supply and should be electrically isolated. Additionally, medical patient-monitoring equipment needs to operate without any common physical interconnection wiring to form a safety isolation barrier to prevent any chance of electrocution.

These and similar applications need galvanic isolation, so including opto-couplers in I2C-bus signal wires is obviously attractive. Unfortunately it's not so simple to provide opto-isolation of the I2C-bus because the I2C clock and data signals are both bidirectional signals while opto-couplers can only handle unidirectional signals. The challenge to optically isolate the I2C-bus has always been to effectively split the bidirectional I2C signals into unidirectional data streams and recombine them again.

Many circuits have been published over the last decade attempting to opto-isolate parts of an I2C-bus system. All result in, and most admit to, problems with glitches resulting from signal propagation delays. All the circuits are based upon the concept of temporarily blocking the bidirectional I2C signal propagation in one direction to prevent bus latch-up caused by feedback of the logic signals. As a result these circuits all produce a bus "glitch" during the propagation time of the logic signals that must clear the blocking process when the bus-driving signals change. Figure 1 shows a circuit from a National Semiconductor Application, typical of published circuits for opto-isolating the I2C-bus.

You can apply a simple test to check whether an isolating circuit will generate unwanted glitches on the bus. Drive one side of the isolating circuit low, then, holding that first side low, drive the other side low. Then release the drive on the first side. If the system conforms to the I2C protocol the first side should just stay low, held low by the second side.

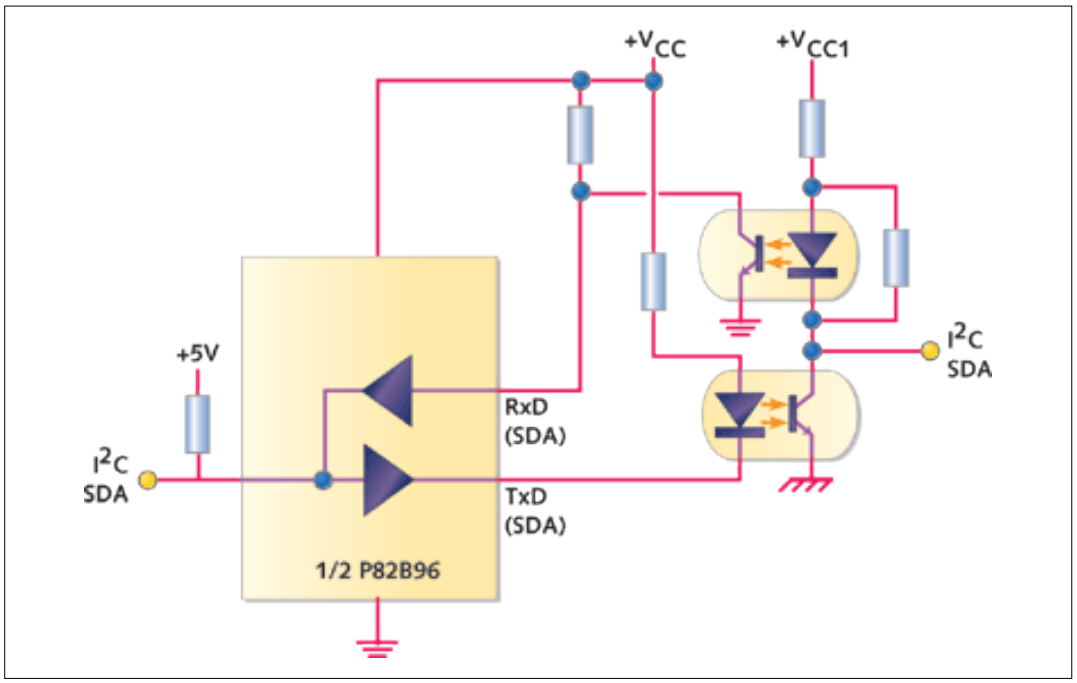

Figure 2: Simple 5kHz opto-electrical isolation circuit

Let's try this test on the circuit of Figure 1. Drive the left side SDA low. Current in R2 turns on the LED in opto-coupler IC1. The photo-transistor in IC1 turns on and the isolated -SDA is pulled low via diode D2. Now drive the right hand side -SDA low. It's already low so the -SDA bus doesn't change state. The photo-transistor in IC1 remains on, so there is no current in the LED of IC2. Now release SDA. SDA immediately goes high because there's nothing to hold it low; the photo-transistor in IC2 isn't on. This represents the start of an unwanted "glitch" of the I2C-bus at SDA. With SDA high, the LED of opto-coupler IC1 turns off and after some delay time its photo-transistor turns off. After IC1 turns off, R3 can source current to pin 2 of the LED in opto-coupler IC2 and current flows, via the LED, to -SDA that's being held low. After another switch-on delay the photo-transistor in IC2 turns on and SDA is pulled down again to the correct state, ending the unwanted "glitch." But notice SDA was high during the time taken for IC2 to turn off plus the time taken for IC1 to turn on. This is a false bus signal that can lead to problems.

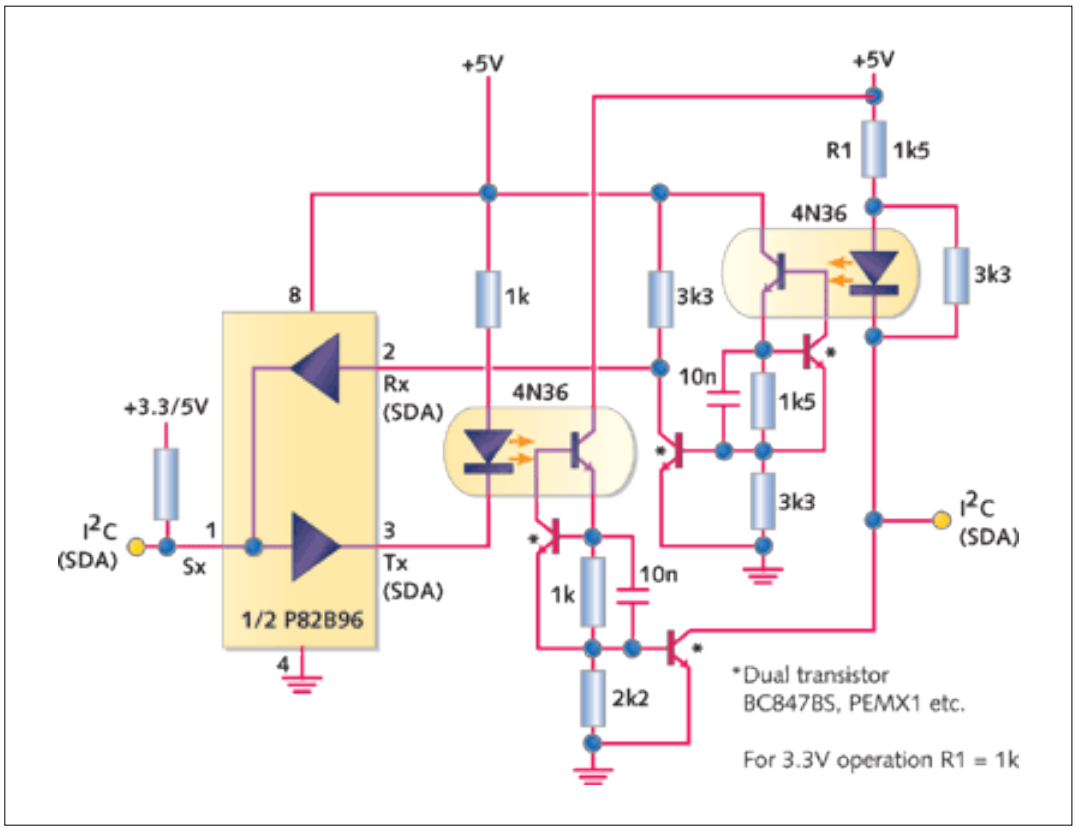

Figure 3: 50kHz application with general purpose low-speed opto-couplers

Eliminate bus glitches

The way to eliminate these glitches is by using an I2C opto-isolation buffer IC. It introduces special logic voltage levels on one of its inputs to prevent bus latching. It never blocks any signals, it uses instead different logic voltage levels that are all placed below the normal bus logic "low" level and are therefore transparent to the connected I2C chips. False bus glitches are eliminated, but of course some bus signal propagation delays are still introduced and these delays can act to limit the maximum bus clock speed.

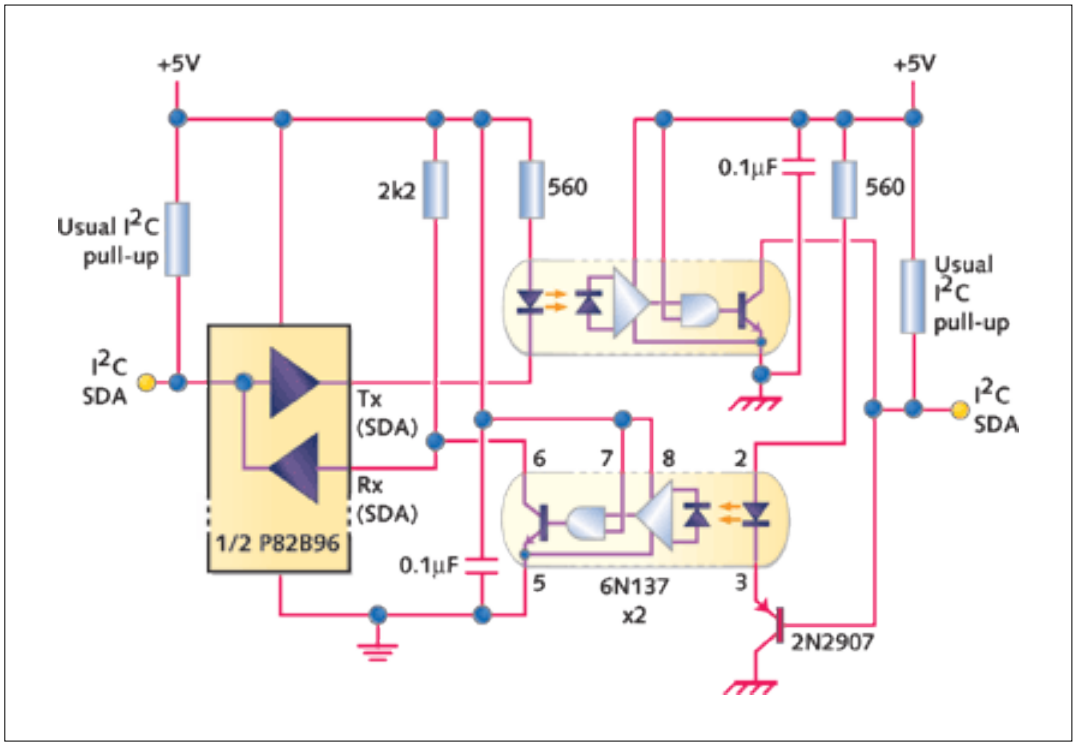

Figure 4: High-speed opto-couplers achieve 100kHz operation

Figure 2 shows the simple circuit that uses the opto-isolation of I2C-bus signals using low-cost 4N36 opto-couplers. This simple circuit allows saturation of the photo-transistor in the opto-coupler, resulting in long turn-off delays caused by charge storage effects. The total switching delays will be around 50µs and this limits the bus speed of this circuit to around the 5kHz clock rate.

Achieve higher bus speeds Increasing the LED drive current can reduce the turn-on delay of an opto-coupler, but unless steps are taken to prevent the consequent deeper saturation of its photo-transistor, the turn-off delay will increase and the total signal delays will increase. To reduce the turn-off delay a traditional technique to prevent saturation of the photo-transistor is to apply a Schottky diode clamp between its collector and base, as used in Schottky TTL logic.

An alternative approach is to apply feedback to regulate (limit) the current in the photo-transistor so it will be unsaturated and operating in a linear mode, with a relatively higher collector-emitter voltage, at the instant when it's

required to switch off. The circuit of Figure 3 shows a low cost dual transistor added to each opto-coupler to prevent saturation of the photo-transistor and reduce the turn-on and turn-off delays to less than 5µs each, extending bus operation to 50kHz. The circuit can be adapted to a wide range of couplers, providing a choice of isolating voltage specification. It offers reasonable bus speed for about a third of the cost of using true high-speed couplers.

The resistor values in Figure 3 are selected for 5V operation, setting LED drive to around 2mA to stay within the 3mA maximum sink allowed in an I2C system. For operation on 3.3V, only resistor R1 needs to be reduced to maintain the 2mA drive, taking account of the published diode voltage drop for the opto used. For 4N36, R1 should be reduced to 1kΩ.

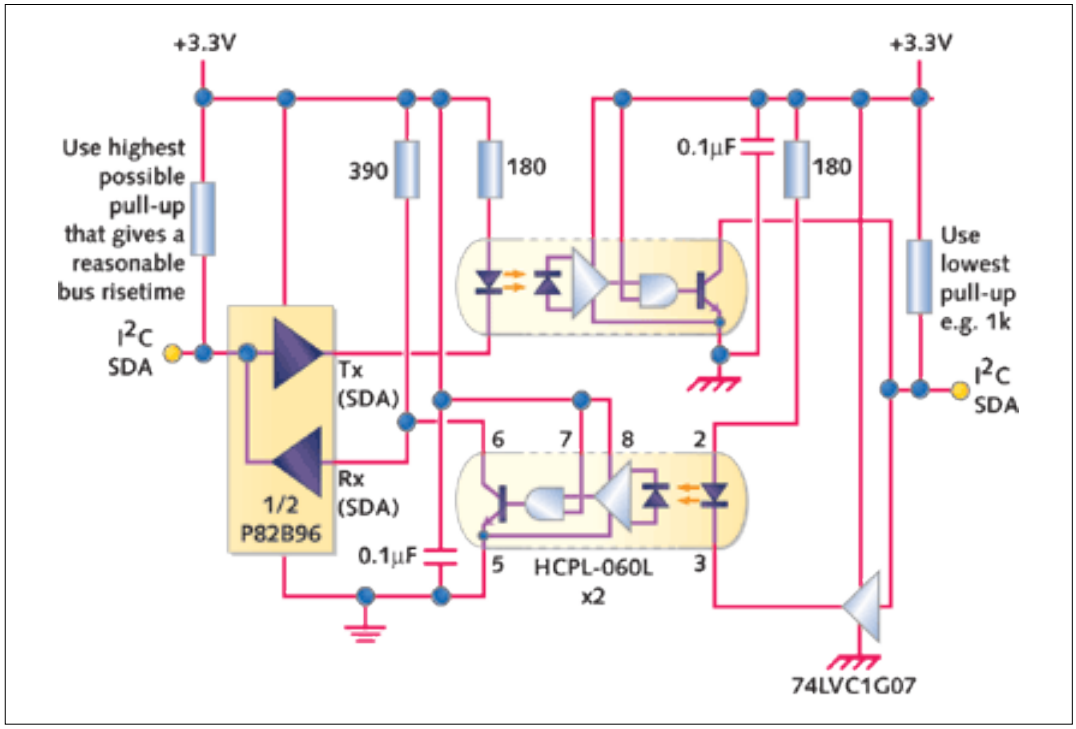

Figure 5: Suggested circuit for 400kHz applications

Figure 3 shows two 10nF capacitors added to the feedback path to further improve switching times. During turn-on of the photo-transistor this capacitor delays the feedback, increasing the drive and improving the turn-on time. When the photo-transistor drive is removed the delay caused by the 10nF again delays the removal of the feedback. This causes an excess base current to be drawn out of the base of the photo-transistor by the current regulating transistor during switch-off, further improving the fall-time of the current. The opto-coupler propagation delays measured with 4N36 were reduced to around 2 to 3µs each, giving some safety margin on the recommended 50kHz bus speed to take account of different components that might be used. The bus speed recommendation is also based on conforming to 100kHz Standard mode bus timings when using ICs specified for use in 100kHz systems. The allowed clock speed specification is calculated by simply adding the delay introduced by P82B96 and the opto-couplers to the minimum SCL "low" period and calculating a new frequency based on a symmetrical clock. The typical system performance may be found to be much better, especially when using components specified for 400kHz bus operation because their maximum response delays are smaller, but 100kHz operation remains theoretically impossible with these low-cost couplers.

This speed-up technique should prove economical when applied to any opto-switching application where a higher speed is an advantage but higher speed couplers cannot be justified. If there's no restriction on the available LED drive you can achieve even smaller turn-on delays. Turn-off delays remain limited by the fall-time of the current in the photo-transistor.

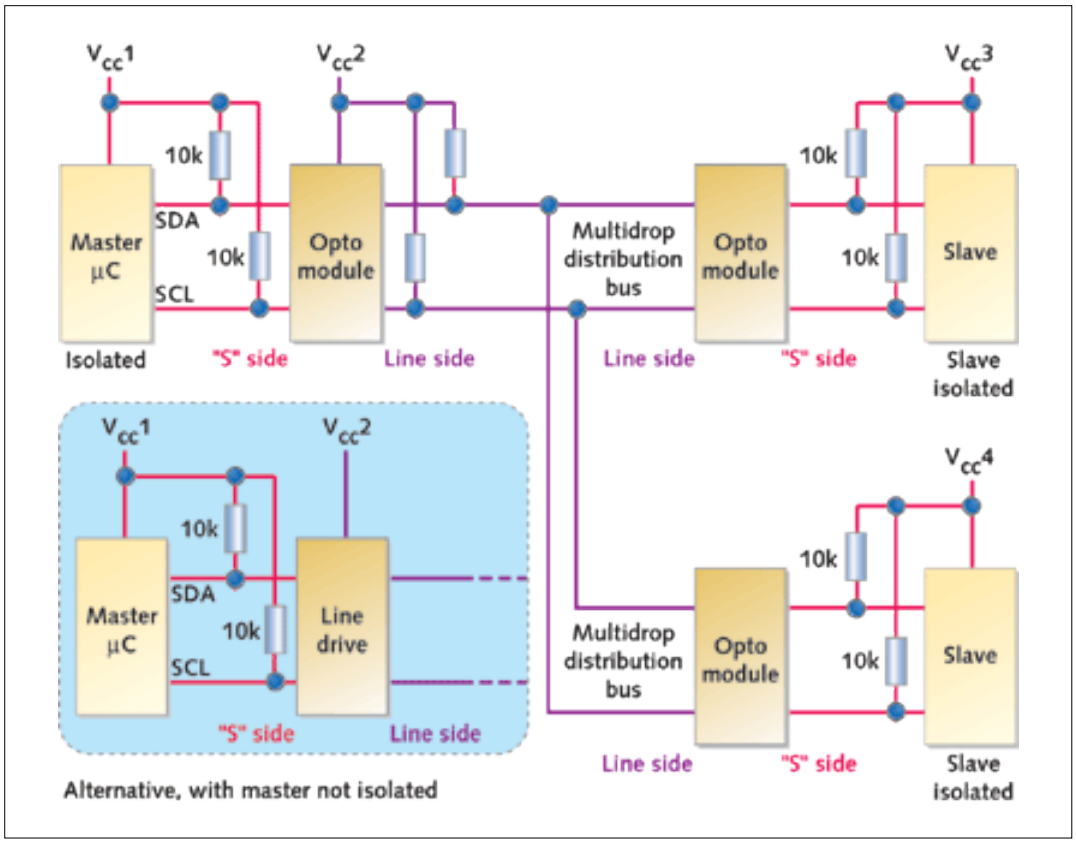

Figure 6: Suggested circuit for multi-point applications

Run at full 100kHz speed

Obviously faster system speeds require faster opto-couplers and parts such as 6N137 re-

duce the switching delays to less than 100ns each when operating in a 5V bus system as shown in Figure 4.

Is 400kHz possible?

Because the original I2C specifications didn't envisage the development of bus buffering components or the possibilities for signal propagation delays in the system, it's strictly not allowed to introduce any delays other than those anticipated in the bus rise and fall times. In practice typical I2C parts do not use up all of the allowed response time that can be calculated from the bus specifications. For example, the typical response time for ICs specified for 400kHz application are mostly under 700ns while the bus specifications allow for 1.3µs delays. This means that in practice delays up to 600ns can be tolerated. P82B96 introduces delays around 400ns and fast couplers will have delays less than 100ns so in practical systems, when the designer checks the actual bus timings, 400kHz opto-coupling can be achieved. The fastest circuit, designed for interfacing 3.3V logic, is shown in Figure 5.

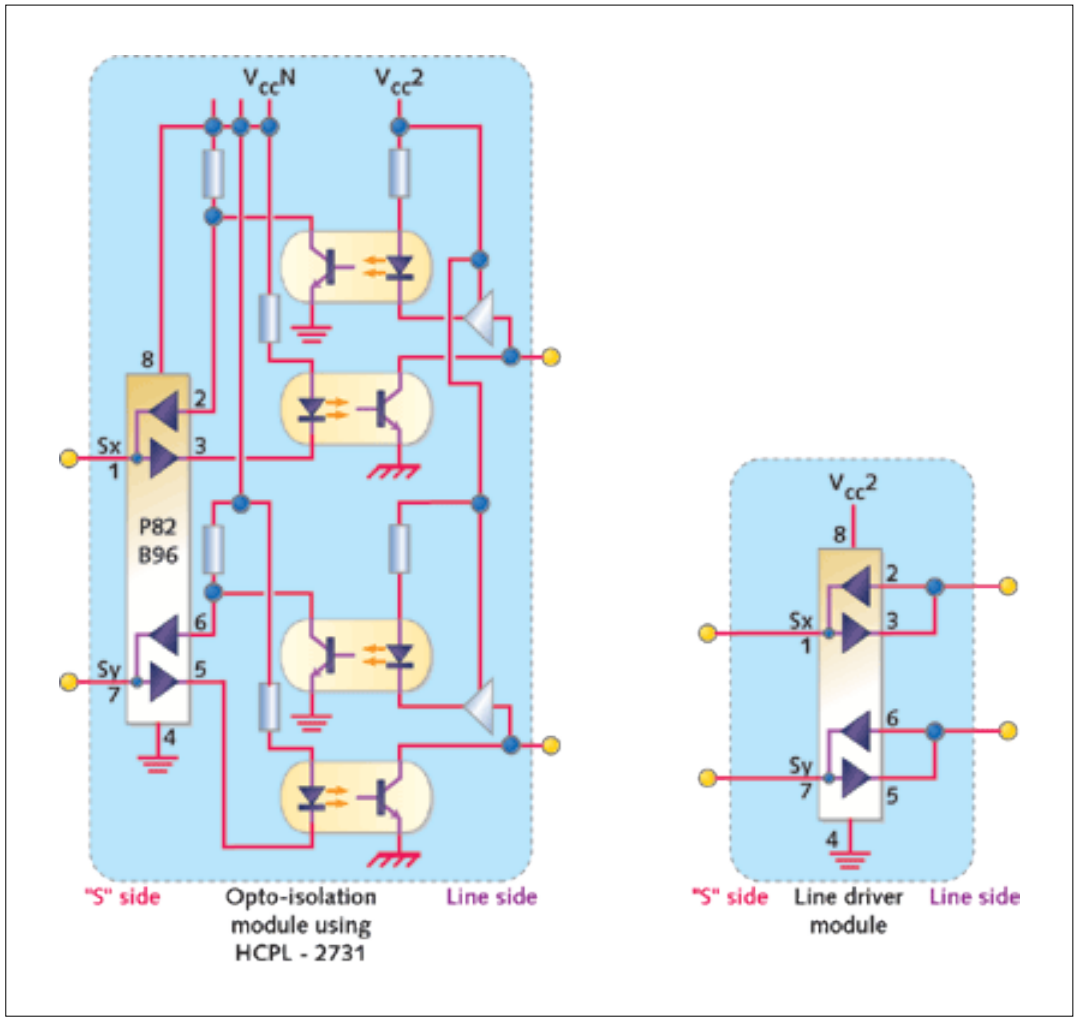

Figure 7: Suggested modules for use in the system of Figure 6

Multi-node opto-electrical isolation

Figure 6 shows a general arrangement for a multi-drop system in which isolated and nonisolated modules can be mixed as required. The coupler shown in the example in Figure 7 is the Darlington-type HCPL-2731 that has an 18V rating and guarantees when sinking 24mA. It can be used to drive lower impedance higher voltage distribution bus lines exactly the same way P82B96 is used. It can interface with a P82B96 line driver module as shown in Figure 7 when isolation is not required or it can be used to isolate the master or any slaves from the bus wiring.

When many isolation modules are used in a system it's convenient to build the opto modules as shown in Figure 7 with a logic buffer (for example, HEF 4050B) driving the LED on the line side. That ensures each module imposes no load on the distribution bus and saves making calculations about loading. When only a small number of modules is used then a buffer is not needed, but just remember to include the LED drive current when calculating the pull-up resistor(s) for the line side distribution bus to stay under 24mA.

The distribution bus pull-ups should be calculated for no more than 24mA to have guarantees on the opto performance. That still allows 510Ω pull-ups to 12V and should be OK for about 2nF (say < 20 meters) of wiring capacitance. If the bus and its capacitance are small then it's not necessary to waste energy and larger resistance pull-ups can be used. The cheapest, simplest opto interface as shown is very slow and the warnings about 5kHz maximum for Figure 2 should be taken seriously. It's wise to monitor the waveforms around the opto devices and check that they're doing what the data sheet implies. For faster speeds it's necessary to adapt the faster opto circuits in Figures 3 through 5. In every case note it must be the opto-coupled side of the module that interfaces to the distribution bus because this side has normal I2C characteristics and full noise margins. Do not connect the Sx sides of an opto module to the distribution bus because that interface can have very low noise margins when two Sx pins are joined. The Sx interface is intended for connection only to standard I2C parts and not to other buffers. For details see AN255-03.

Safe and sure

Using P82B96 to split the bidirectional I2C signals into unidirectional signals enables simple opto-isolation of an I2C-bus, without generating any spurious glitches, and offering various cost/speed performance levels.