6.1.6 Power supply scheme

Backup circuitry Power 1.65 - 3.6 V (LSĖ, RTC, switch Wakeup logic, Backup registers) OUT GP I/Os I/O logic Kernel logic (CPU, digital & memories) $11 \times V_{DD}$ Regulator 11 x 100 nF 11 x V_{SS} + 1 x 4.7 µF V_{DDA} V_{DDA} Analog: RCs, 10 nF 10 nF V_{REF+} PLL,comparators, OPAMP, ADC/DAC + 1 µF V_{REF} V_{SSA} MS35524V1

Figure 12. Power supply scheme

 Dotted lines represent the internal connections on low pin count packages, joining the dedicated supply pins.

Caution:

Each power supply pair (V_{DD}/V_{SS} , V_{DDA}/V_{SSA} etc.) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below the appropriate pins on the underside of the PCB to ensure the good functionality of the device.