

Current Mode PWM Controller

FEATURES

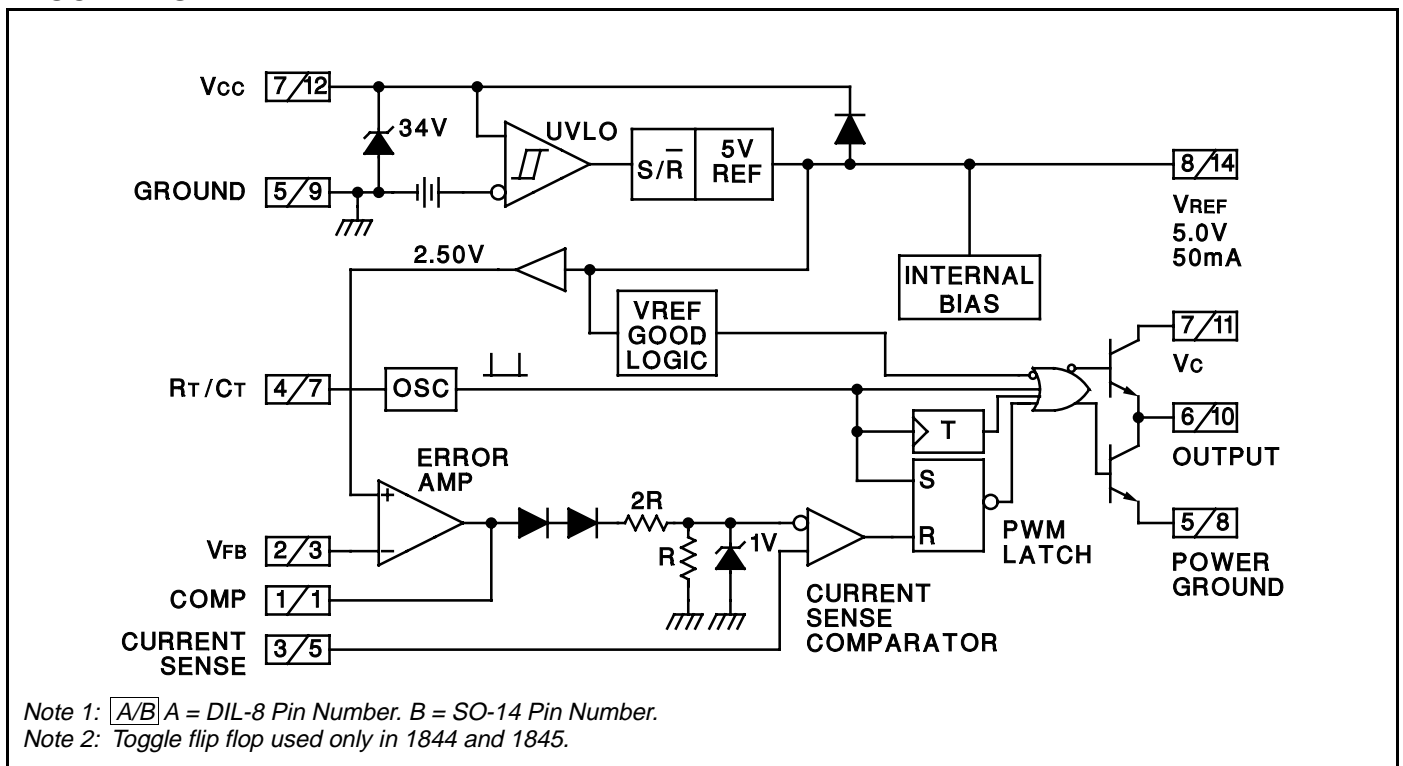
- Optimized For Off-line And DC To DC Converters
- Low Start Up Current (<1mA)
- Automatic Feed Forward Compensation
- Pulse-by-pulse Current Limiting
- Enhanced Load Response Characteristics
- Under-voltage Lockout With Hysteresis
- Double Pulse Suppression
- High Current Totem Pole Output
- Internally Trimmed Bandgap Reference
- 500khz Operation
- Low Ro Error Amp

DESCRIPTION

The UC1842/3/4/5 family of control ICs provides the necessary features to implement off-line or DC to DC fixed frequency current mode control schemes with a minimal external parts count. Internally implemented circuits include under-voltage lockout featuring start up current less than 1mA, a precision reference trimmed for accuracy at the error amp input, logic to insure latched operation, a PWM comparator which also provides current limit control, and a totem pole output stage designed to source or sink high peak current. The output stage, suitable for driving N Channel MOSFETs, is low in the off state.

Differences between members of this family are the under-voltage lockout thresholds and maximum duty cycle ranges. The UC1842 and UC1844 have UVLO thresholds of 16V (on) and 10V (off), ideally suited to off-line applications. The corresponding thresholds for the UC1843 and UC1845 are 8.4V and 7.6V. The UC1842 and UC1843 can operate to duty cycles approaching 100%. A range of zero to 50% is obtained by the UC1844 and UC1845 by the addition of an internal toggle flip flop which blanks the output off every other clock cycle.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Note 1)

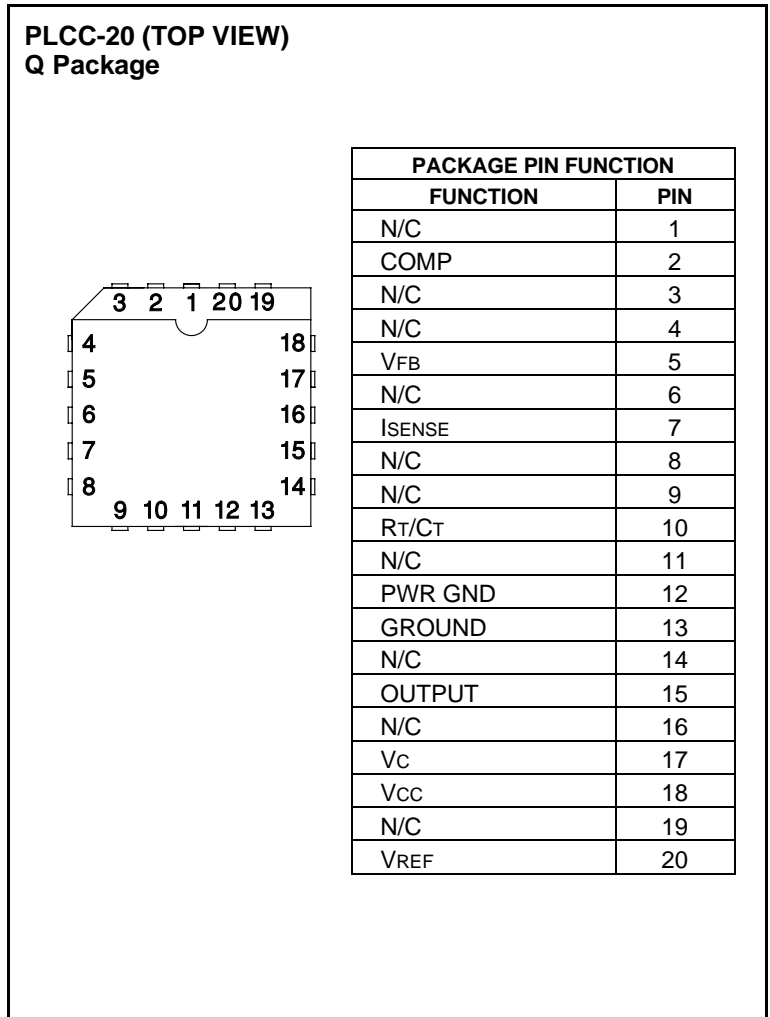
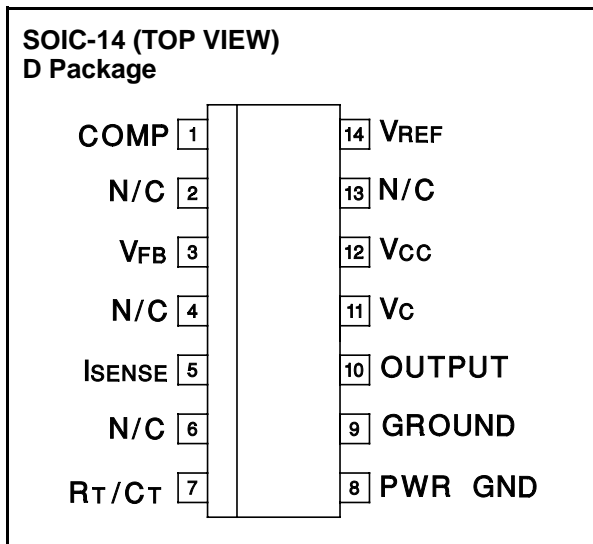
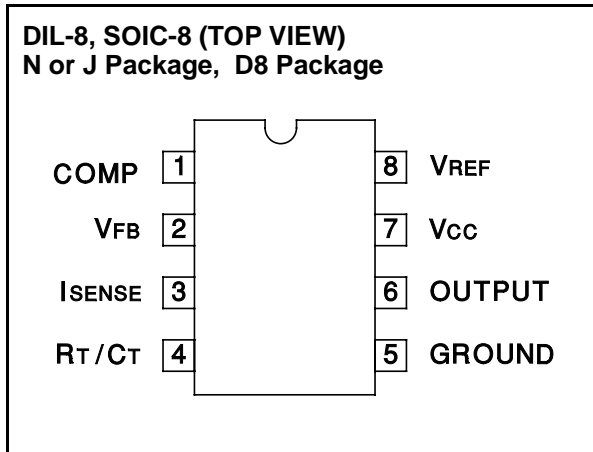
| | |
|--|-----------------|
| Supply Voltage (Low Impedance Source) | 30V |
| Supply Voltage (I _{cc} <30mA) | Self Limiting |
| Output Current | ±1A |
| Output Energy (Capacitive Load) | 5μJ |
| Analog Inputs (Pins 2, 3) | -0.3V to +6.3V |
| Error Amp Output Sink Current | 10mA |
| Power Dissipation at T _A ≤ 25°C (DIL-8) | 1W |
| Power Dissipation at T _A ≤ 25°C (SOIC-14) | 725mW |
| Storage Temperature Range | -65°C to +150°C |
| Lead Temperature (Soldering, 10 Seconds) | 300°C |

Note 1: All voltages are with respect to Pin 5.

All currents are positive into the specified terminal.

Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAMS



ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for $-55^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ for the UC184X; $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ for the UC284X; $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$ for the 384X; $V_{CC} = 15\text{V}$ (Note 5); $R_T = 10\text{k}$; $C_T = 3.3\text{nF}$, $T_A = T_J$.

| PARAMETER | TEST CONDITIONS | UC1842/3/4/5 UC2842/3/4/5 | | | UC3842/3/4/5 | | | UNITS |
|------------------------------|--|------------------------------|------|------|--------------|------|------|------------------------|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| Reference Section | | | | | | | | |
| Output Voltage | $T_J = 25^{\circ}\text{C}$, $I_o = 1\text{mA}$ | 4.95 | 5.00 | 5.05 | 4.90 | 5.00 | 5.10 | V |
| Line Regulation | $12 \leq V_{IN} \leq 25\text{V}$ | | 6 | 20 | | 6 | 20 | mV |
| Load Regulation | $1 \leq I_o \leq 20\text{mA}$ | | 6 | 25 | | 6 | 25 | mV |
| Temp. Stability | (Note 2) (Note 7) | | 0.2 | 0.4 | | 0.2 | 0.4 | mV/ $^{\circ}\text{C}$ |
| Total Output Variation | Line, Load, Temp. (Note 2) | 4.9 | | 5.1 | 4.82 | | 5.18 | V |
| Output Noise Voltage | $10\text{Hz} \leq f \leq 10\text{kHz}$, $T_J = 25^{\circ}\text{C}$ (Note 2) | | 50 | | | 50 | | μV |
| Long Term Stability | $T_A = 125^{\circ}\text{C}$, 1000Hrs. (Note 2) | | 5 | 25 | | 5 | 25 | mV |
| Output Short Circuit | | -30 | -100 | -180 | -30 | -100 | -180 | mA |
| Oscillator Section | | | | | | | | |
| Initial Accuracy | $T_J = 25^{\circ}\text{C}$ (Note 6) | 47 | 52 | 57 | 47 | 52 | 57 | kHz |
| Voltage Stability | $12 \leq V_{CC} \leq 25\text{V}$ | | 0.2 | 1 | | 0.2 | 1 | % |
| Temp. Stability | $T_{MIN} \leq T_A \leq T_{MAX}$ (Note 2) | | 5 | | | 5 | | % |
| Amplitude | $V_{PIN 4}$ peak to peak (Note 2) | | 1.7 | | | 1.7 | | V |
| Error Amp Section | | | | | | | | |
| Input Voltage | $V_{PIN 1} = 2.5\text{V}$ | 2.45 | 2.50 | 2.55 | 2.42 | 2.50 | 2.58 | V |
| Input Bias Current | | | -0.3 | -1 | | -0.3 | -2 | μA |
| AVOL | $2 \leq V_o \leq 4\text{V}$ | 65 | 90 | | 65 | 90 | | dB |
| Unity Gain Bandwidth | (Note 2) $T_J = 25^{\circ}\text{C}$ | 0.7 | 1 | | 0.7 | 1 | | MHz |
| PSRR | $12 \leq V_{CC} \leq 25\text{V}$ | 60 | 70 | | 60 | 70 | | dB |
| Output Sink Current | $V_{PIN 2} = 2.7\text{V}$, $V_{PIN 1} = 1.1\text{V}$ | 2 | 6 | | 2 | 6 | | mA |
| Output Source Current | $V_{PIN 2} = 2.3\text{V}$, $V_{PIN 1} = 5\text{V}$ | -0.5 | -0.8 | | -0.5 | -0.8 | | mA |
| VOUT High | $V_{PIN 2} = 2.3\text{V}$, $R_L = 15\text{k}$ to ground | 5 | 6 | | 5 | 6 | | V |
| VOUT Low | $V_{PIN 2} = 2.7\text{V}$, $R_L = 15\text{k}$ to Pin 8 | | 0.7 | 1.1 | | 0.7 | 1.1 | V |
| Current Sense Section | | | | | | | | |
| Gain | (Notes 3 and 4) | 2.85 | 3 | 3.15 | 2.85 | 3 | 3.15 | V/V |
| Maximum Input Signal | $V_{PIN 1} = 5\text{V}$ (Note 3) | 0.9 | 1 | 1.1 | 0.9 | 1 | 1.1 | V |
| PSRR | $12 \leq V_{CC} \leq 25\text{V}$ (Note 3) (Note 2) | | 70 | | | 70 | | dB |
| Input Bias Current | | | -2 | -10 | | -2 | -10 | μA |
| Delay to Output | $V_{PIN 3} = 0$ to 2V (Note 2) | | 150 | 300 | | 150 | 300 | ns |

Note 2: These parameters, although guaranteed, are not 100% tested in production.

Note 3: Parameter measured at trip point of latch with $V_{PIN 2} = 0$.

Note 4: Gain defined as

$$A = \frac{\Delta V_{PIN 1}}{\Delta V_{PIN 3}}, 0 \leq V_{PIN 3} \leq 0.8\text{V}$$

Note 5: Adjust V_{CC} above the start threshold before setting at 15V.

Note 6: Output frequency equals oscillator frequency for the UC1842 and UC1843.

Output frequency is one half oscillator frequency for the UC1844 and UC1845.

Note 7: Temperature stability, sometimes referred to as average temperature coefficient, is described by the equation:

$$\text{Temp Stability} = \frac{V_{REF(max)} - V_{REF(min)}}{T_J(max) - T_J(min)}$$

$V_{REF(max)}$ and $V_{REF(min)}$ are the maximum and minimum reference voltages measured over the appropriate temperature range. Note that the extremes in voltage do not necessarily occur at the extremes in temperature.

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| PARAMETER | TEST CONDITION | UC1842/3/4/5 UC2842/3/4/5 | | | UC3842/3/4/5 | | | UNITS |
|--------------------------------------|--|------------------------------|------|-----|--------------|------|------|-------|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| Output Section | | | | | | | | |
| Output Low Level | $I_{\text{SINK}} = 20\text{mA}$ | | 0.1 | 0.4 | | 0.1 | 0.4 | V |
| | $I_{\text{SINK}} = 200\text{mA}$ | | 1.5 | 2.2 | | 1.5 | 2.2 | V |
| Output High Level | $I_{\text{SOURCE}} = 20\text{mA}$ | 13 | 13.5 | | 13 | 13.5 | | V |
| | $I_{\text{SOURCE}} = 200\text{mA}$ | 12 | 13.5 | | 12 | 13.5 | | V |
| Rise Time | $T_J = 25^{\circ}\text{C}$, $C_L = 1\text{nF}$ (Note 2) | | 50 | 150 | | 50 | 150 | ns |
| Fall Time | $T_J = 25^{\circ}\text{C}$, $C_L = 1\text{nF}$ (Note 2) | | 50 | 150 | | 50 | 150 | ns |
| Under-voltage Lockout Section | | | | | | | | |
| Start Threshold | X842/4 | 15 | 16 | 17 | 14.5 | 16 | 17.5 | V |
| | X843/5 | 7.8 | 8.4 | 9.0 | 7.8 | 8.4 | 9.0 | V |
| Min. Operating Voltage After Turn On | X842/4 | 9 | 10 | 11 | 8.5 | 10 | 11.5 | V |
| | X843/5 | 7.0 | 7.6 | 8.2 | 7.0 | 7.6 | 8.2 | V |
| PWM Section | | | | | | | | |
| Maximum Duty Cycle | X842/3 | 95 | 97 | 100 | 95 | 97 | 100 | % |
| | X844/5 | 46 | 48 | 50 | 47 | 48 | 50 | % |
| Minimum Duty Cycle | | | | 0 | | | 0 | % |
| Total Standby Current | | | | | | | | |
| Start-Up Current | | | 0.5 | 1 | | 0.5 | 1 | mA |
| Operating Supply Current | $V_{\text{PIN } 2} = V_{\text{PIN } 3} = 0\text{V}$ | | 11 | 17 | | 11 | 17 | mA |
| V_{CC} Zener Voltage | $I_{CC} = 25\text{mA}$ | 30 | 34 | | 30 | 34 | | V |

Note 2: These parameters, although guaranteed, are not 100% tested in production.

Note 3: Parameter measured at trip point of latch with $V_{\text{PIN } 2} = 0$.

Note 4: Gain defined as:

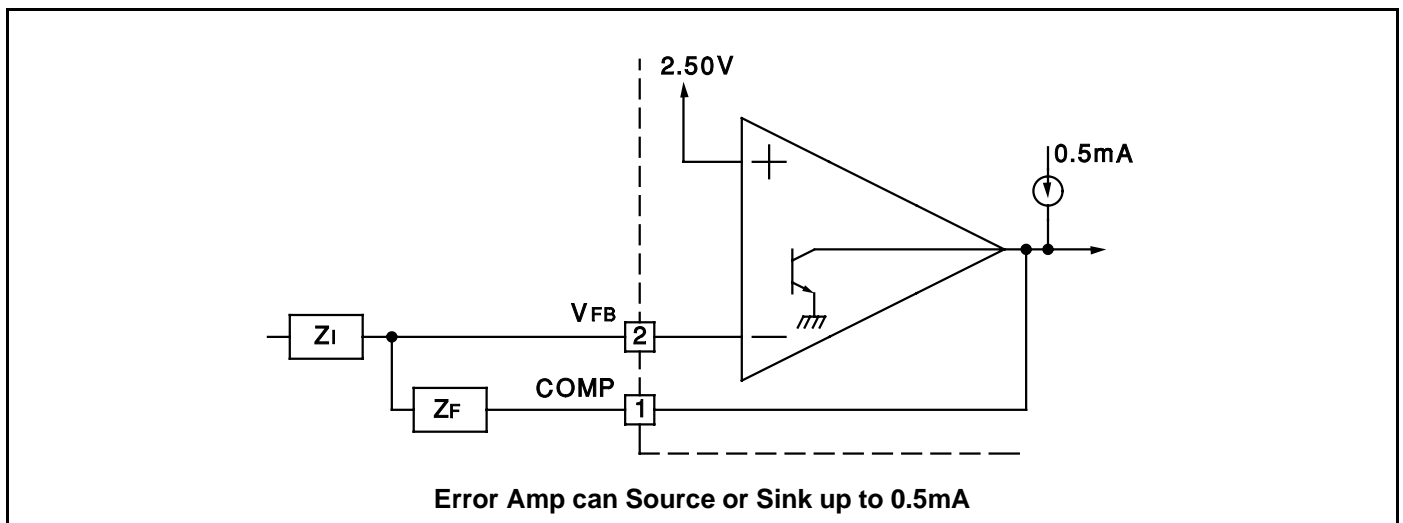
$$A = \frac{\Delta V_{\text{PIN } 1}}{\Delta V_{\text{PIN } 3}}; 0 \leq V_{\text{PIN } 3} \leq 0.8\text{V}.$$

Note 5: Adjust V_{CC} above the start threshold before setting at 15V.

Note 6: Output frequency equals oscillator frequency for the UC1842 and UC1843.

Output frequency is one half oscillator frequency for the UC1844 and UC1845.

ERROR AMP CONFIGURATION



UNDER-VOLTAGE LOCKOUT

| | | |
|------------------|------------------|------------------|
| | UC1842 UC1844 | UC1843 UC1845 |
| V _{ON} | 16V | 8.4V |
| V _{OFF} | 10V | 7.6V |

During under-voltage lock-out, the output driver is biased to sink minor amounts of current. Pin 6 should be shunted to ground with a bleeder resistor to prevent activating the power switch with extraneous leakage currents.

CURRENT SENSE CIRCUIT

Peak Current (I_S) is Determined By The Formula

$$I_{S\text{MAX}} \approx \frac{1.0\text{V}}{R_s}$$

A small RC filter may be required to suppress switch transients.

OSCILLATOR SECTION

For $R_T > 5k$ $f \approx \frac{1.72}{R_T C_T}$

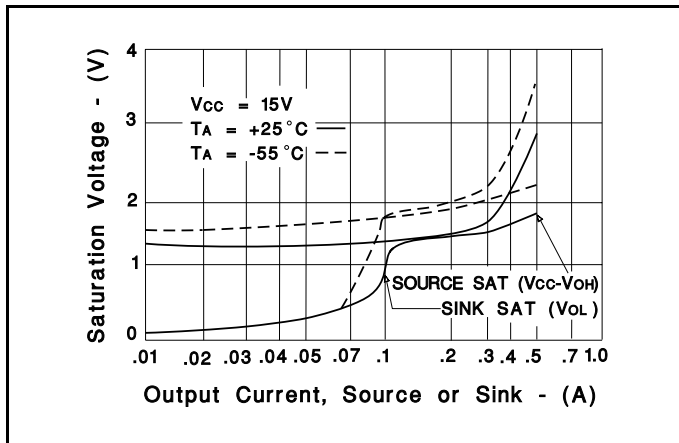
Deadtime vs C_T ($R_T > 5k$)

| C_T (nF) | t_d (μs) |
|------------|-------------------------|
| 1 | 0.3 |
| 2.2 | 0.6 |
| 4.7 | 1.2 |
| 10 | 2.4 |
| 22 | 4.8 |
| 47 | 9.6 |
| 100 | 19.2 |

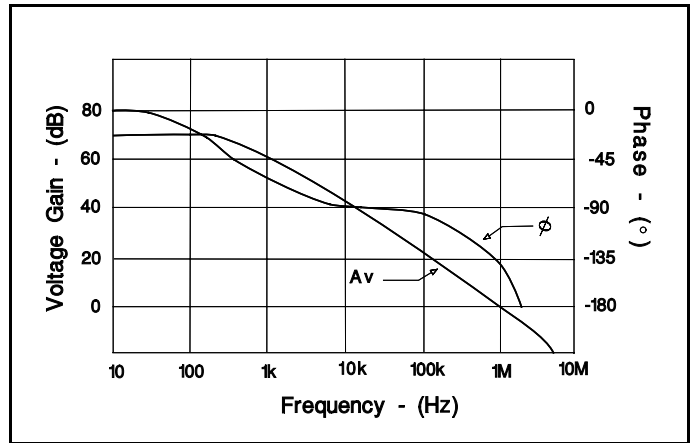
Timing Resistance vs Frequency

| FREQUENCY (Hz) | R_T ($k\Omega$) |
|----------------|---------------------|
| 100 | 100 |
| 1k | 10 |
| 10k | 1 |
| 100k | 0.1 |
| 1M | 0.01 |

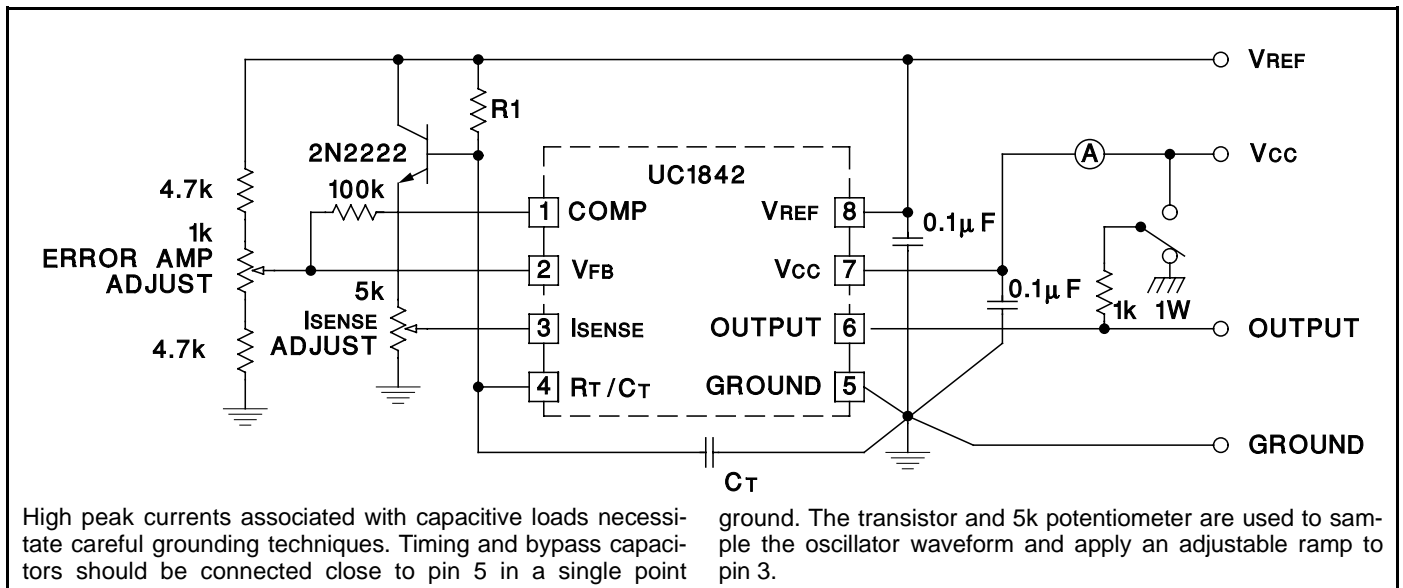
OUTPUT SATURATION CHARACTERISTICS



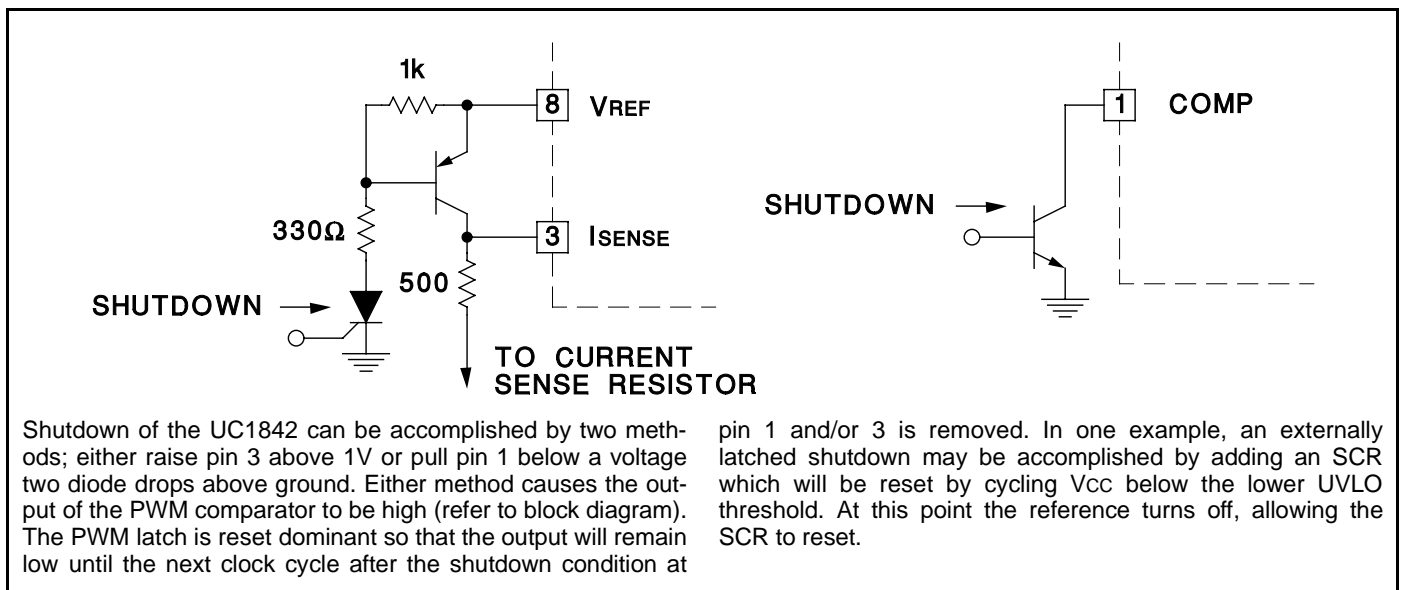
ERROR AMPLIFIER OPEN-LOOP FREQUENCY RESPONSE



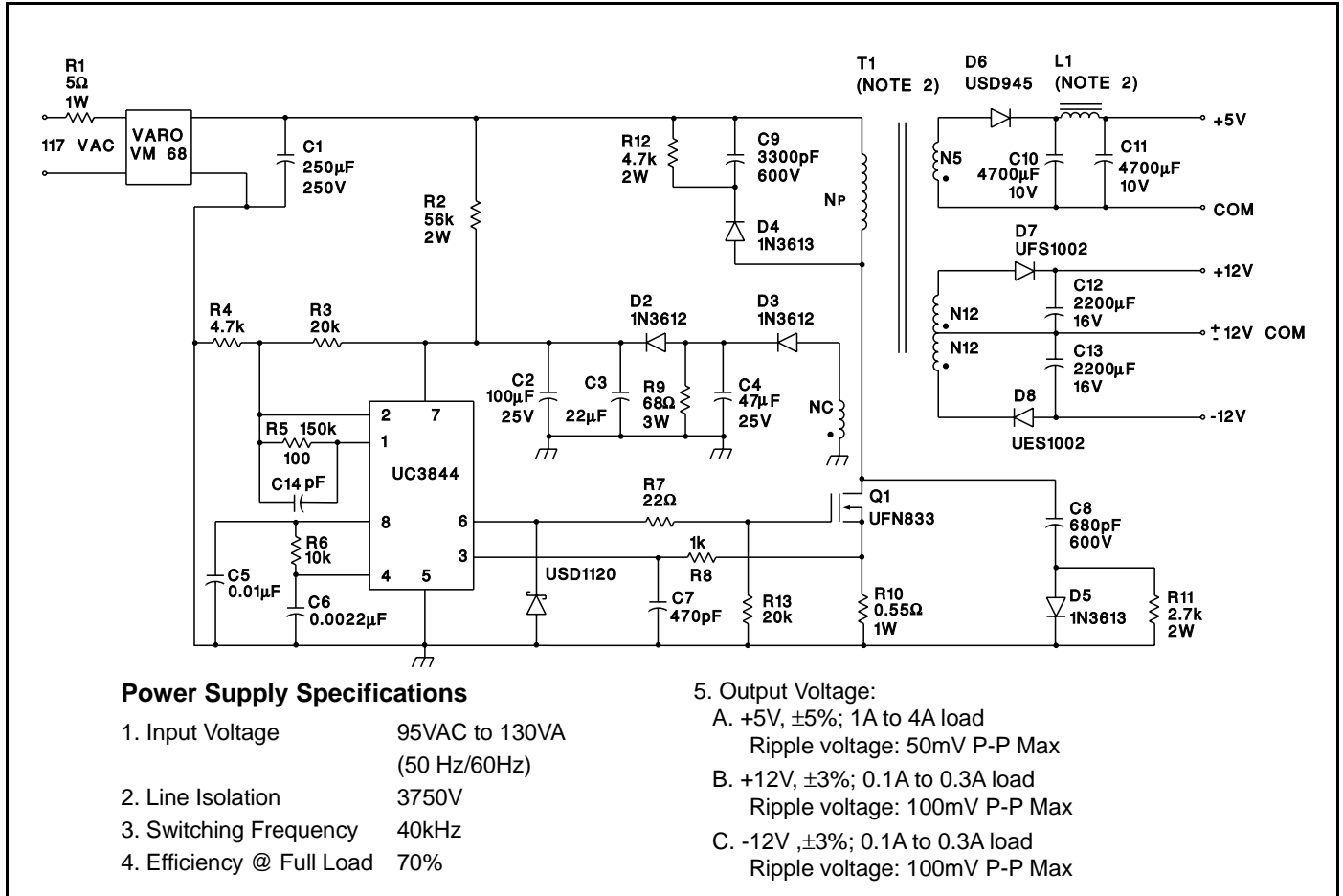
OPEN-LOOP LABORATORY FIXTURE



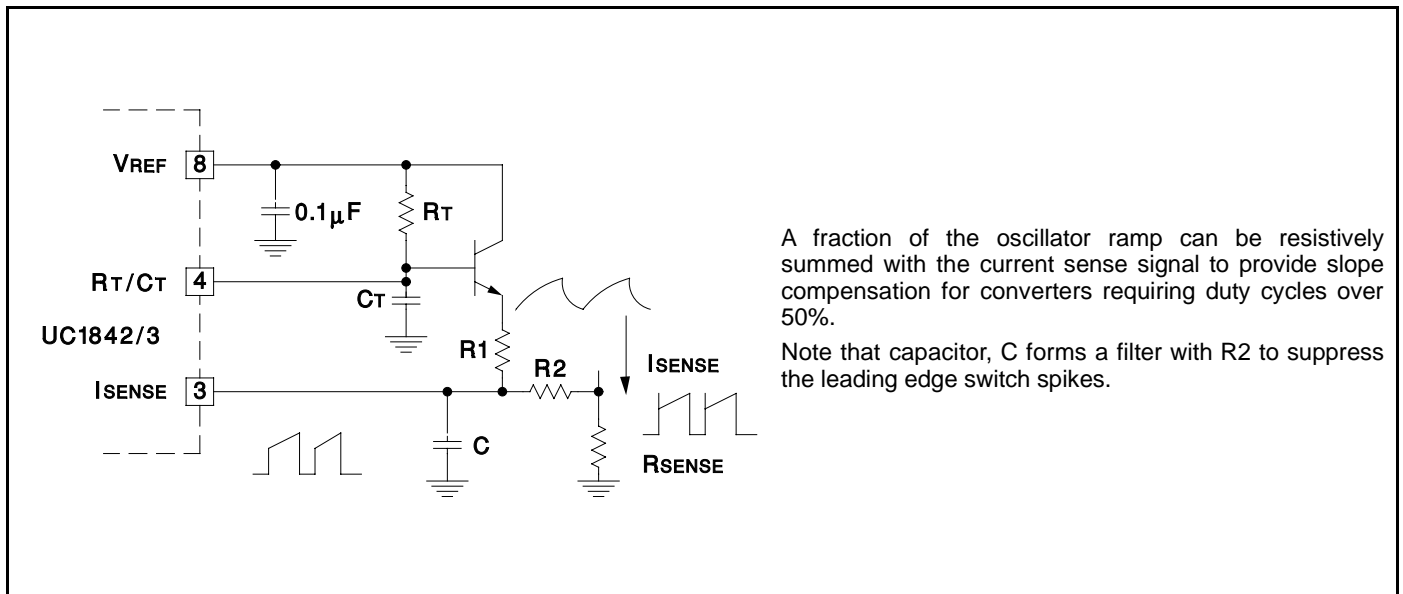
SHUT DOWN TECHNIQUES



OFFLINE FLYBACK REGULATOR



SLOPE COMPENSATION



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