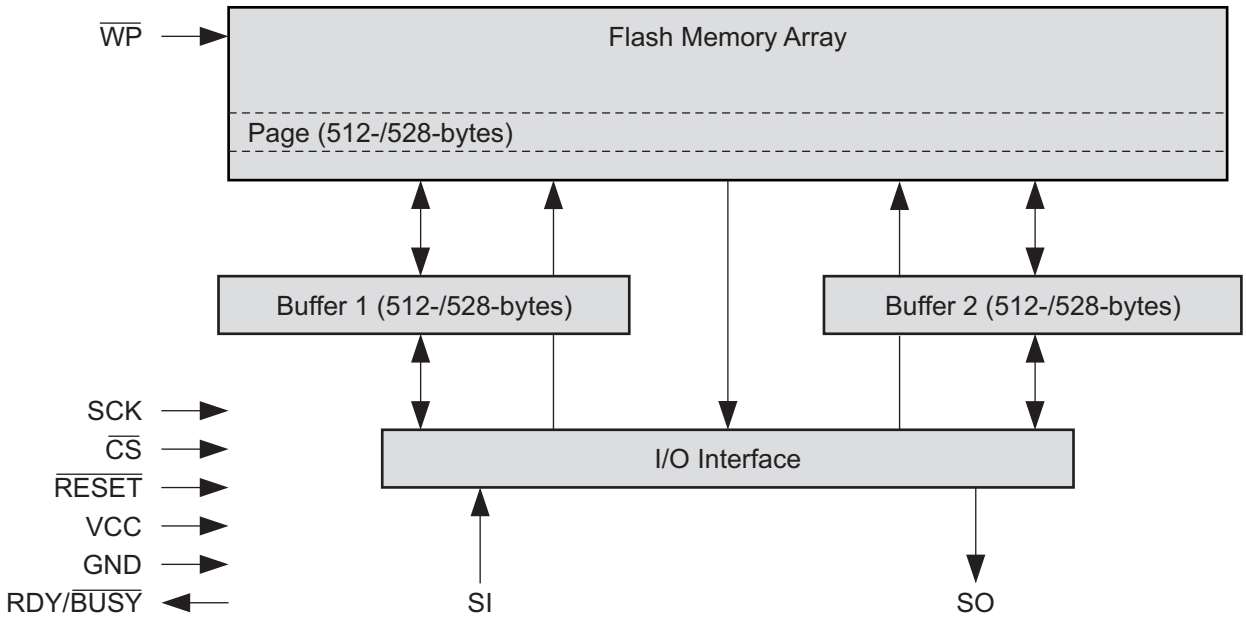
Figure 1-2. Block Diagram



2. Memory Array

To provide optimal flexibility, the AT45DB321D memory array is divided into three levels of granularity comprising sectors, blocks, and pages. The "Memory Architecture Diagram" illustrates the breakdown of each level, and details the number of pages per sector and block. All program operations to the DataFlash device occur on a page-by-page basis. The erase operations can be performed at the chip, sector, block, or page level.

Figure 2-1. Memory Architecture Diagram