VENABLE TECHNICAL PAPER # 5

Current Mode Control

Abstract:

Current mode control, one of the hot new subjects of power electronics, has actually been in use for many years under another name — the discontinuous mode fly back converter. This paper details the principle of current mode control, how it is supposed to work, what topologies come closest to truly representing the concept, and how to test a current mode converter to see if it is actually working as advertised. Description of an implementation of the concept in a commercially available integrated circuit is included, together with a description of the principles of operation of a little-used topology that is one of the few true implementations of the concept, the continuous-mode buck converter with constant off time.

Introduction

Switching regulators have been with us for many years, but it took Silicon General and the advent of the SG1524 Pulse Width Integrated Circuit to make them really take off in popularity. The 1524 drives a pair of switching transistors with a duty cycle which is proportional to a control voltage, and by using the switching transistors to switch a voltage source on and off into an L-C low pass filter, a relatively efficient voltage regulator can be produced. This technique has come to be known as "voltage-mode programming", since the duty cycle is proportional to the control voltage.

Another technique, which has also been around for a long time, senses the peak current in the power switch and turns the switch off at a programmed level of current. By pretending that the average current from the low-pass filter is proportional to the peak current in the power switch (a good assumption in most cases), a functional block is formed which uses local feedback to create what is essentially a voltage-to-current converter. By using this voltage-to-current converter block inside an overall voltage feedback loop, a voltage regulator can be produced where the control voltage sets the load current rather that the switch duty cycle. Figure 1 is a block diagram of the concept. The net result of the two approaches is the same, to regulate voltage, but this latter approach is called "current-mode programming" since the load current is the directly controlled variable and the output voltage is controlled only indirectly. Like switching regulators in general, this approach languished until an integrated circuit was developed to make the job easy. In this case Unitrode developed the 1842 and 1846 chips for single-ended and push-pull applications respectively, and the technique was off and running.

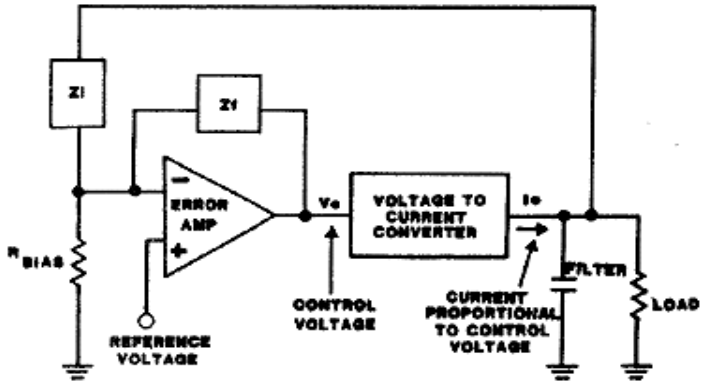

Figure 1. Ideal Current Mode Converter

Why Current-Mode Control?

Why bother with such a roundabout way to regulate output voltage anyway? Well, it turns out that the current-mode approach offers some advantages.

For one thing, since the output current is proportional to the control voltage, the output current can be limited simply by clamping the control voltage. In fact, since the current is controlled by sensing the peak current in the power switch (es), the current can be limited on a cycle-by-cycle basis. The two sides of a push-pull circuit can be forced to share, even if there are significant imbalances in circuit component values.

Another advantage is that the energy storage inductor is effectively absorbed into the current source. Provided the bandwidth of the local feedback in the voltage-to-current converter is sufficiently high, the transfer function from control voltage to output voltage has a single- pole rolloff, due to the current source driving the filter capacitor. With voltage-mode control, the inductor does not disappear and the control to output transfer function has a two-pole rolloff. Systems with a single-pole rolloff of the control-to-output transfer function can be stabilized with a simpler compensation network around the error amplifier.

For higher power applications, power stages can be connected in parallel. Since the output currents are proportional to the control voltages, the power stages can be forced to share equally by simply connecting the control voltages to a common bus.

A final advantage, which is touted, is automatic feed forward from the line voltage. This particular feature is actually more readily attained in voltage-mode converters by a technique known as "ramp compensation". In fact, in current-mode converters perfect feed forward is obtained only by a particular value of slope compensation (a concept which will be explained more fully later in the paper) and this value of compensation is not practical in actual practice.

Is Current-Mode Control Perfect?

Like almost everything, there is some bitter with the sweet. The hardest part of current-mode control is measuring the current accurately and with the required bandwidth.

There are also open-loop instabilities that have to be dealt with. The local current feedback loop is open-loop unstable for duty cycles over 50% unless some form of "slope compensation" is used. In the half- bridge topology, the circuit will unbalance the two filter capacitors. The transfer function of the voltage-to-current converter (essentially the transconductance) is not as wide-band as previously thought, and has recently been proven to have a bandwidth of at best 1/6 to 2/3 of the switching frequency. And finally, the familiar right-half-plane zeros of the buck and buck-boost topologies are still present, even with current-mode control. Figure 2 shows some of the problems associated with measuring the current. The sense resistor has parasitic inductance. The various capacitances around the power switch must charge and discharge through the current sense resistor. The R and C of the current signal filter could be chosen to match the L/R time constant of the sense resistor, if it were not for the parasitic capacitance currents. These currents are significant, and in most applications the C of the current signal filter is chosen large enough to filter out the spikes caused by these currents flowing through the R and L of the sense resistor. This causes the C of the filter to be much larger than required to match the L/R time constant, and causes another pole in the feedback loop, which must be accounted for in the compensation calculations.

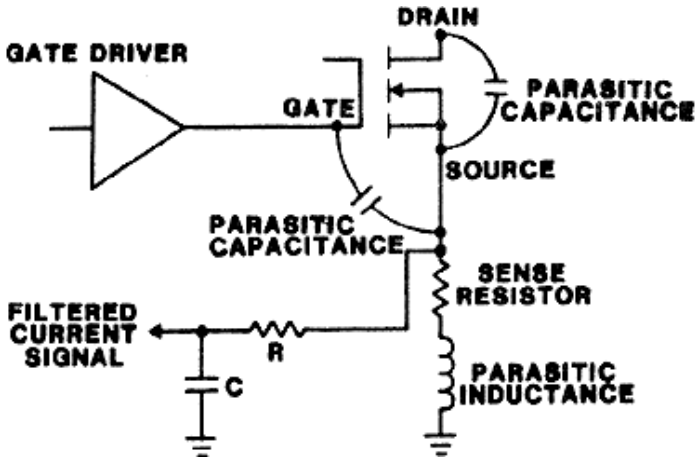

Figure 2. Parasitics Affect Accurate Current Measurement

Time delays cause the switch to turn off at a time later than indicated by the current crossing the threshold. Figure 3 shows this effect. Although a relatively minor effect, the present trend toward higher switching frequencies makes this parasitic increasingly important.

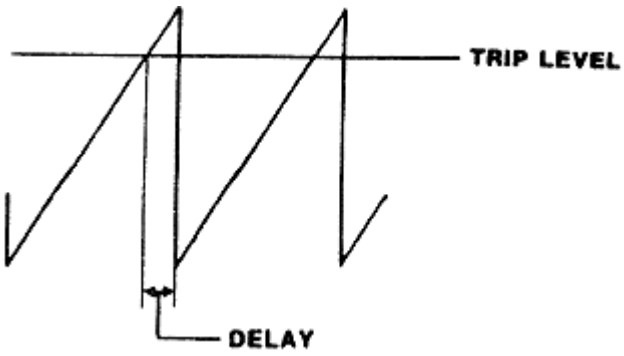

Figure 3. Time Delays Affect Accuracy of Peak Current Sensing

As the line voltage and duty cycle changes, the peak-to-peak and average current values of the inductor change, as indicated in Figure 4. This contributes to inaccuracies in the transconductance, since the average current does not track the peak and the peak is what is being controlled.

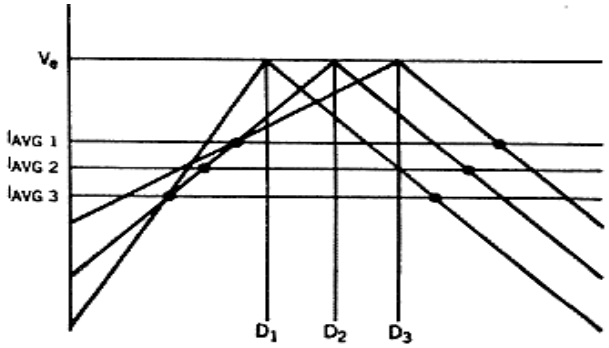

Figure 4. Average and Peak-to-Peak Values Change with Duty Ratio

4. Open Loop Instability

An early discovery in the development of current-mode control was that the current feedback loop became open loop unstable when the duty cycle was increased past 50%. This phenomenon has been thoroughly studied and analyzed. Disturbances in the operating point gradually die out when the duty

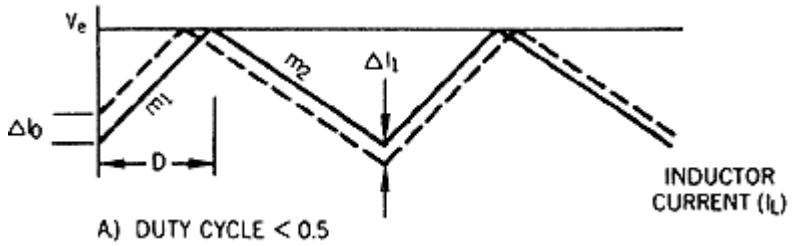

Figure 5. For Duty Ratio Less Than 0.5, Disturbances Die Out

For duty cycles greater than 50% however, a disturbance from the nominal operating point grows larger with each cycle. This leads to large deviations from the nominal operating point and a phenomenon known as "sub-cycle oscillation." Figure 6 shows the beginning of this process.

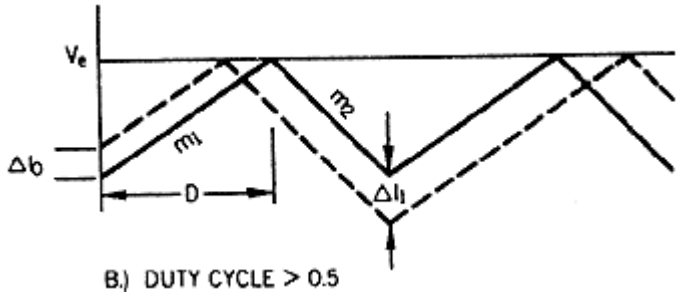

Figure 6. For Duty Ratio Greater Than 0.5, Disturbances Grow

By adding "slope compensation" to the trip level (or to the sensed current signal), the duty cycle at which a disturbance begins to grow can be increased. Figure 7 shows the effects of slope compensation.

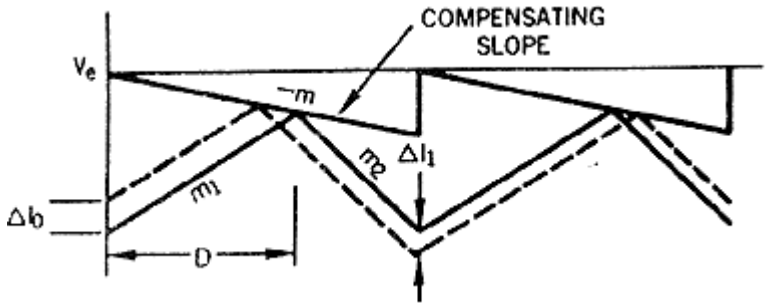

Figure 7. Slope Compensation Can Cause Disturbances to Die Out for Any Duty Ratio

If the slope of the falling current in the energy storage inductor is called m2, then a negative slope equal to half the slope of m2 will in theory cause a disturbance to die out for any duty cycle up to 100%. Two other advantages that occur with this particular amount of slope compensation are that the average current is no longer a function of duty cycle, and that line voltage changes are perfectly rejected without requiring action by the voltage loop. Figure 8 shows slope compensation where -m = m2/2, and the effect on average current. Although the advantages of having -m = m2/2 are significant, they are difficult to achieve in practice. In practice, it is better to have more compensation than -m = m2/2 to assure freedom from oscillation at high duty cycles.

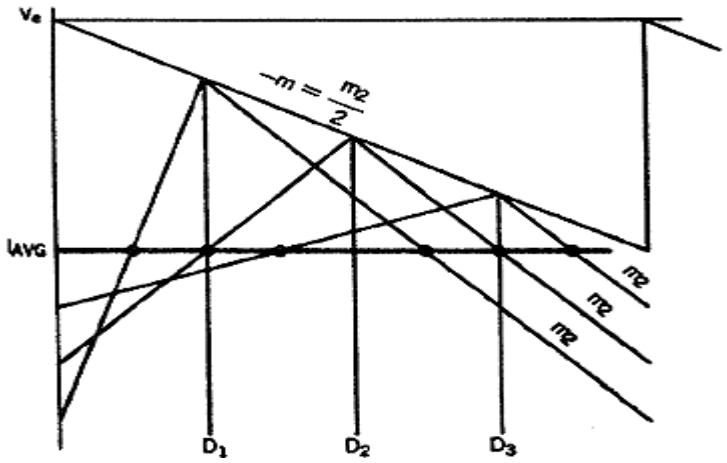

Figure 8. For -m = m2/2, Average Current Stays Constant

Slope compensation of -m = m2 gives perfect rejection of disturbances on the first cycle, but line rejection is no longer perfect, and the average current is again a function of duty cycle. Figure 9 shows the rejection of a disturbance.

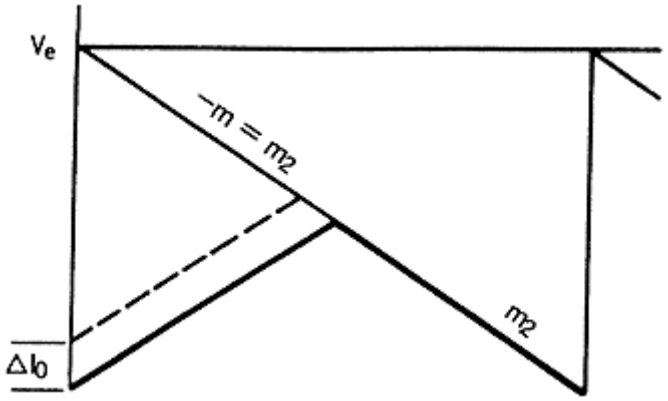

Figure 9. For -m = m2, Disturbances Die Out in One Cycle

Control To Output Transfer Function

If the voltage-to-current converter were a perfect, wideband transconductance amplifier, then the control to output transfer function would be flat at low frequency (due to the current flowing through the load resistor), breaking to a -1 slope (20 dB per decade) above the corner frequency of the filter capacitor and load resistor (due to the falling impedance of the filter capacitor with frequency). Stabilizing the voltage control loop would be a snap. Unfortunately, nothing is that perfect. The transconductance amplifier is not really all that wide band. Recent papers have shown that due to the limited gain of the current loop, the inductor does not really disappear, but the corner merely moves out in frequency. The effect of the current loop is to cause a large, lossless damping resistor to appear in series with the signal path, similar to the lossless damping caused by storage time modulation. The bandwidth of the voltage-to-current feedback loop is only 1/6 to 2/3 of the switching frequency. Above this frequency, the transconductance falls at a -1 slope, causing the control to output transfer function to fall at a -2 slope (40 dB per decade). This is shown in Figure 10.

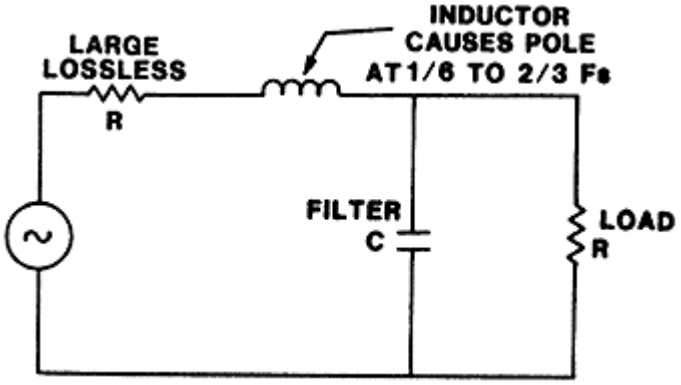

Figure 10. Control-to-Output Transfer Function has 2nd Pole

Other parasitic affect the transfer function as well. The equivalent series resistance (ESR) and equivalent series inductance (ESL) of the filter capacitor change the loading on the voltage-to-current converter. Extra output filter stages or remote sensing are both common, and have dramatic effects on the transfer function. As mentioned earlier, the amount of filtering of the current sense signal can also have a marked effect on the bandwidth of the voltage-to-current (transconductance) block.

The Advantages Of Fixed Off Time

Fixed frequency is by far the most popular mode of operation for PWM converters, because it allows them to be synchronized and simplifies the design of the magnetics. If the application permits a mode other than fixed frequency however, fixed off time presents significant advantages over any other mode of operation.

Disturbances Die Out In One Cycle

With fixed off time, disturbances in the nominal operating point die out in one cycle, as they would normally with slope compensation of -m = m2. Figure 11 shows this effect.

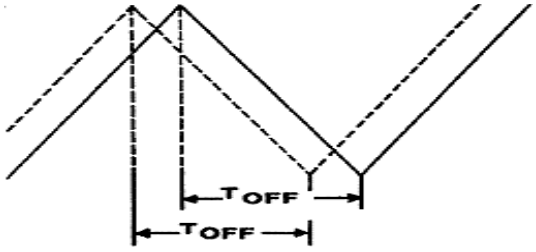

Figure 11. Disturbance Dies Out in One Cycle

Line Variations Are Rejected Totally

Figure 12 shows that changing line voltage causes the current to reach the trip level at a different time than otherwise, but once the transistor turns off the rate of fall of inductor current is constant and determined only by the output voltage. With fixed off time the change in current is constant, therefore

the average current does not change. Line ripple is totally rejected, as it would be with normal current mode and slope compensation of -m = m2/2.

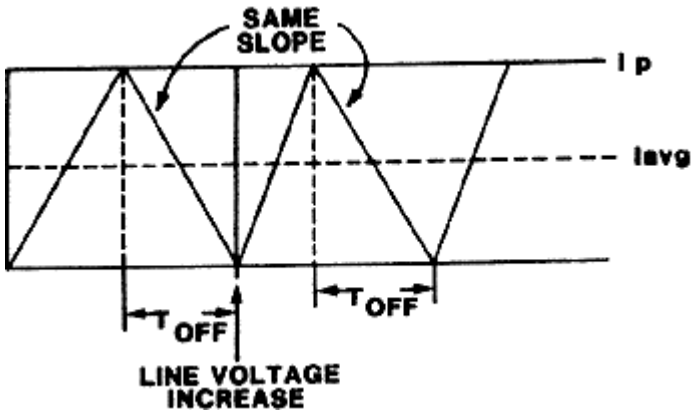

Figure 12. Total Line Variation Rejection

Critical Current Is Fixed

The critical current is the load current at which the energy storage inductor current just goes to zero at the lower peaks. Load currents below critical cause discontinuous operation. The critical current is half the peak-to-peak ripple of the current in the energy storage inductor. With fixed off time, the peak-to-peak current is constant, and therefore the critical current is constant.

Effects Of Right-Half-Plane Zero Are Minimized

Right-half-plane zeros cause the gain portion a transfer function to stop falling as fast, like a normal (left-half-plane) zero, while causing a phase lag instead of a lead. They are usually caused by parallel signal paths in a circuit, one inverting and one non-inverting, and happen at the transition in frequency where the dominant path changes from inverting to non-inverting or vice-versa.

In the case of boost and buck-boost converters, a sudden increase in duty cycle causes a momentary reduction in output since power flows to the output a smaller percentage of the time. Once the current level builds up, which may take several cycles, the duty cycle will revert to normal and the higher current coupled with the relatively normal duty cycle will cause more output. This dip before the rise in output voltage is effectively an inversion at higher frequencies. At low frequency, the output tracks the input and is in phase. The frequency where the phase transitions from in-phase to out-of-phase is the right- half-plane zero.

With fixed frequency, the increase of duty cycle causes a corresponding reduction in output conduction time. With constant off time, the output conduction time remains constant, although the on time increased and the output conduction time as a percentage of total time still decreased, it did not decrease as much as in the fixed frequency case. The effect of this is to increase the frequency where the right-half-plane zero occurs. Figure 13 shows the input and output current waveforms for the two modes of operation for an abrupt change in duty cycle.

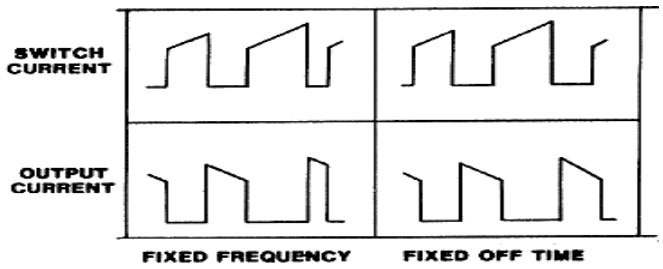

Figure 13. Effect of Right-Half-Plane Zero Minimized

7. Constant Off Time is Easy to Implement

Constant off time is easy to implement on existing current-mode PWM chips. Figure 14 shows an implementation on the single-ended 1842 chip and Figure 15 shows an implementation on the double-ended 1846 chip. In both cases the implementation consists of inhibiting the charging of the timing capacitor during the on time of the power switch (es). When the switch turns off, the clamp is released and the timing capacitor charges to the trigger level in a fixed amount of time.

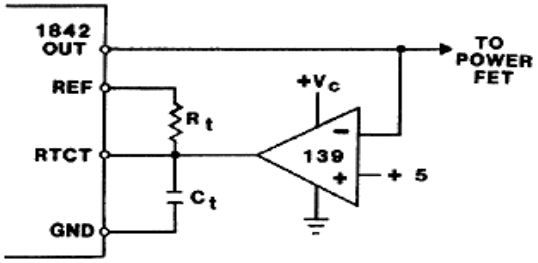

Figure 14. Easy to Implement on UC 1842

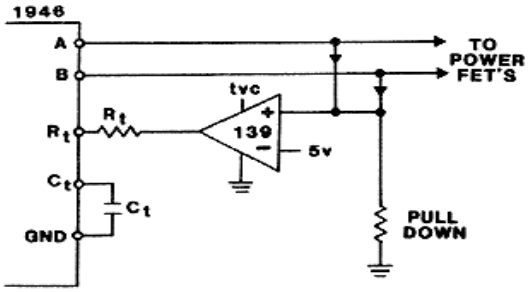

Figure 15. Easy to Implement on UC 1846

Summary

Current mode control was discussed in some detail, together with some of the practical difficulties in implementing the concept. An alternative mode of operation, fixed off time, was suggested which eliminates the problems of implementing slope compensation and simultaneously gives the disturbance rejection advantages of -m = m2 and the line rejection advantages of -m = m2/2.

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