VENABLE TECHNICAL PAPER # 18

New Techniques for Measuring Feedback Loop Transfer Functions in Current Mode Converters

Abstract:

In power supplies with current mode control topology, the current feedback forms an internal digital loop that cannot be directly measured. The phase margin of this loop is a function of duty cycle, and this loop can become unstable for duty cycles greater than fifty percent. Although techniques such as slope compensation can be used to adjust the stability of this internal feedback loop, measurement of this loop is essential to verify the effectiveness of the adjustment. This paper describes techniques for indirect measurement of the gain-phase characteristics (Bode plot) of this feedback loop. If also describes how to use this information to optimize the performance of the overall voltage feedback loop. Finally, the paper describes how to measure the feedback loop of power supplies where no single signal injection point is available.

Introduction

Figure 1 is the schematic of a power supply that seems to have become a de-facto world standard. There may be a few minor variations, such as using a flyback topology instead of the two-transistor forward converter shown, but we have seen this basic circuit produced by power supply companies the world over. It is simple, cheap, and works reasonably well, and these factors undoubtedly contribute to its popularity. The questions we are trying to pose and answer in this paper concern feedback loops and their stability. A major power supply manufacturer told us recently that customers are starting to ask for Bode plots and demanding that power supplies have a minimum 45 degrees of phase margin.

A Bode plot is a plot of feedback loop gain expressed as log gain and linear phase versus log frequency. The gain around the feedback loop varies with frequency. At some frequency a signal goes around the loop and comes back with the same amplitude the signal had when it entered the loop. This is called the unity gain frequency. This return signal lags the input signal in phase. If it lags the input signal by one whole cycle (360 degrees), the loop will oscillate. If the phase lag is less than 360 degrees, the loop will be stable. Phase margin is the difference between the actual phase lag and 360 degrees at the unity gain frequency.

To achieve a minimum phase margin of 45 degrees, the total loop phase lag at the unity gain frequency cannot exceed 315 degrees. The big questions are:

1. Where is the loop, and

2. How do you measure it?

The reasons we feel these questions are important to ask and to answer is that we have some indication power supply feedback loops are not being measured correctly. If quantities like phase margin are to be specified as performance parameters, they must be measured correctly or they are meaningless. We know these measurements can be difficult. Venable Industries pioneered the use of frequency response analyzers in the measurement of power supply loop stability. We developed the tools and techniques widely used today, and we have tried to educate power supply manufacturers about the proper use and application of these tools. This is a long process and this paper is one more step along that path.

Description of Operation and Signal Flow Analysis of the Feedback Loops

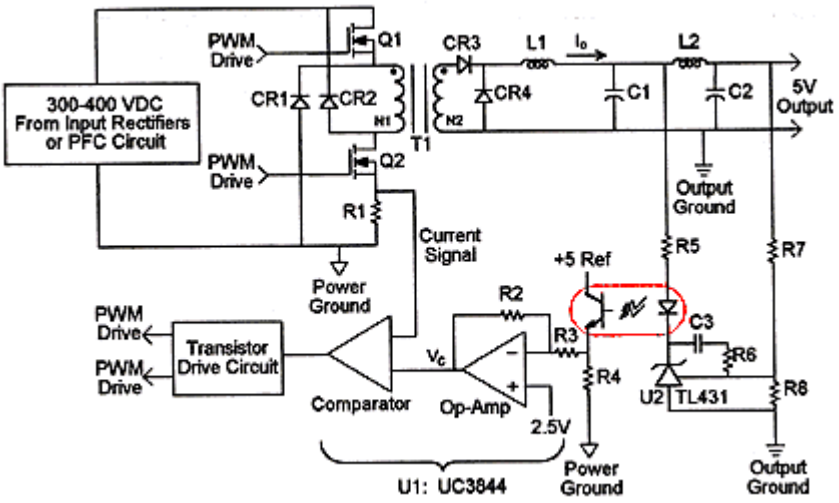

Figure 1. Schematic of typical current mode control power supply

The power supply shown in Figure 1 is a two-transistor forward converter. Transistors Q1 and Q2 turn on and off at the same time. When they are on, energy is delivered through CR3 to inductor L1. When they are off, leakage inductance energy in transformer T1 is returned to the source through diodes CR1 and CR2, and L1 delivers some of its stored energy to the load by drawing current through diode CR4. The waveform at the junction of CR3, CR4, and L1 is a pulse train with an average value equal to the DC output voltage. Inductor L1 and capacitor C1 form a low-pass filter, which removes most of the AC components and passes the DC value of the waveform.

The triangular ripple current through L1 passes through the equivalent series resistance (ESR) of C1 and generally creates more ripple voltage than allowed by the specification. A second filter consisting of L2 and C2 reduces the ripple voltage to an acceptable level, but creates an additional phase lag that cannot be compensated for by the feedback loop if the loop were closed at the output of the supply. This problem is sometimes avoided by connecting the optocoupler diode through R5 to the junction between the two filters, before the additional phase lag is incurred. There are two signal flow paths at this point. One is a high-frequency path through R5, and the other a low-frequency path through R7. The high-frequency path is created by C3 and R6 tending to make the cathode of programmable zener U2 a virtual AC ground. High-frequency AC voltage on the top of R5 pushes current through R5 and the optocoupler diode without any signal passing through the gate of U2 from R7. This path through R5 is actually more important to the stability of the feedback loop than the low-frequency path through R7. Current through the optocoupler diode, whether from

signal on the top of R5 or from additional current through U2 due to an increase in gate voltage, causes the transistor portion of the optocoupier to conduct more. This increases the voltage on R4 and reduces the voltage at the output of the operational amplifier (op-amp), which is the compensation pin of U1, the UC3844 current-mode controller chip. Transistors Q1 and 02 turn off when the voltage across R1, which is proportional to load current, is equal to the output voltage of the op-amp. This makes the output current proportional to the output voltage of the op-amp. The output voltage of the op-amp is called the control voltage, Vc, and the gain from this point to the output is called the control-to-output transfer function.

An internal feedback loop has thus been created which controls the output current, making it proportional to Vc. There has been a great deal of controversy about the significance of this loop. Our position at Venable Industries is that it is a minor loop; no more significant than the feedback around an op-amp, and the principal reason for examining it is that it can be unstable if improperly compensated. It is a sampled-data feedback loop because the only important instant of time is the moment when the voltage across R1 is equal to Vc. At all other times, there is no significance to the relationship between these two voltages. For this reason conventional analog signal measurement techniques, which assume the output is continuously proportional to the input, do not work. The way around this particular limitation is to measure the closed-loop transfer function and to use this data to calculate the open-loop transfer function from the closed-loop data. The open-loop transfer function is the gain around the loop. The closed-loop transfer function is the gain from input to output. In this case, the closed-loop transfer function is a transconductance, the ratio of output current (the current in L1) to control voltage (Vc) as a function of frequency, and can easily be measured using conventional analog techniques. Techniques for making this measurement and converting the closed-loop data to an open-loop Bode plot are one of the subjects of this paper.

Measuring Voltage Loop Gain

The classical method of measuring the gain of a feedback loop is to break the loop, terminate the input with the output impedance, terminate the output with the input impedance, and then connect the input to an AC source and measure the ratio of output voltage to input voltage. This technique presents a number of measurement problems. The input and output impedance are difficult to measure and to re-create for connecting to the open terminals, but the primary problem is that the loop gain is very high at DC and it is difficult if not impossible to maintain a stable operating point while measuring the loop. We solve both of these problems by finding a place in the circuit where the loop has a single path and the signal comes from a low impedance and drives a high impedance [1]. We insert a small resistor (small relative to the input impedance) in series with the loop at that point. We then connect a floating AC source (the output winding of a transformer) across the injection resistor to turn it into a floating AC error voltage in series with the feedback loop. The high gain does not matter because the open loop gain is being measured while the power supply isbeing operated closed-loop.

The open loop gain is the ratio of the voltages on either side of the injection point. It is measured with a frequency response analyzer that measures only at the frequency of the signal injection voltage and calculates the ratio of these two voltages in both amplitude (gain) and phase over a wide range of frequencies. A good frequency response analyzer will measure from millihertz to megahertz.

The big question still is "Where is the best place to measure the loop?"

A likely place many people choose is the top of R7. It meets the impedance criteria (the impedance of C2 is much lower than the resistance of R7 at all frequencies of interest), but this is only one of two parallel paths at this point. The top of R5 is a place to measure the other parallel path. This point is probably fine also from the impedance standpoint, although R5 is typically much lower in

value than R7 and it may be necessary to look at the frequency at which the impedance of C1 is equal to R5. The real problem is that neither of these loops by itself represents the total loop.

One power supply user (a large computer company) told us recently that they sometimes inject at the right side of R3. They said that the ratio of R3 to R4 was usually in the range of 1 – 5, which means the ratio of Zout to Zin is in the range of 0.2 to 1. The equation for actual loop gain Aactual in terms of measured loop gain Ameasured is:

$$A_{actual} = \frac{A_{measured} + \frac{Z_{out}}{Z_{in}}}{1 + \frac{Z_{out}}{Z_{in}}} \qquad (1)$$

Failure to meet the criterion Zout << Zin, can result in very large errors in actual loop gain. Bear in mind that the impedances are vectors, i.e., they have magnitudes and phase angles. It is possible that when Zout / Zin has a magnitude of 1, it could also be –1 since the phase angle of the ratio could be 180 degrees. This would make a big difference in the value of the denominator of the above equation.

The ideal place to measure loop gain is the connection between the output of the op-amp and the input to the comparator. This point meets both the single path criterion and the impedance ratio criterion. Unfortunately, both the op-amp and the comparator are contained within a single integrated circuit (IC) and this path cannot be broken easily. It is possible on a developmental basis to use two control ICs and use the op-amp from one driving the comparator of the other so you have access to the connection between them. This technique works well, but is not convenient and is especially not easy to do on a production testing basis.

About a year ago we developed an injection technique that is mathematically equivalent to injecting between the op-amp and the comparator. This technique is to inject in series with R2 on the side that connects to the output of the op-amp. R2 is an external component and the connection between the op-amp and the comparator always is available, as is the inverting input of the op-amp. The mathematics of this technique was presented in an earlier paper [2]. As before, we connect a signal injection resistor in series with the signal path, in this case in series with R2 on the side where it connects to the output of the op-amp. The value is not critical, but it should be small relative to R2. A good value for the injection resistor is 100 ohms. This is usually enough smaller than R2 to not cause a problem, and is high enough to present a reasonable load to the error signal source.

We strongly recommend that this injection resistor be designed in as part of the circuit. One additional resistor will not add significantly to the cost, even in high volume applications, and it will make it easy to measure loop gain at any time. Almost every component associated with the normal operation of a power supply has some effect on the Bode plot. Loop gain testing is an excellent way to check the correctness of the assembly operation, marking and value of components, and to discover damaged components such as cracked transformer or inductor cores or incorrect turns ratios.

Measuring Current Loop Gain

The discussion so far has primarily concerned measurement of the voltage loop gain, since this is the loop that controls external performance such as transient response. The current loop is an internal loop that makes the output current track the control voltage. In current mode control, the output voltage is regulated by sensing whether the output voltage is high or low, and then decreasing or increasing the output current as required to maintain the output voltage at the desired level. As pioneers in the field of current mode power supply design quickly discovered, the current loop is inherently unstable for duty ratios greater that 0.5. Duty ratio is the ratio of on time to cycle time for the power switching transistors. In forward converters such as the example shown in Figure 1, the duty ratio cannot exceed 0.5 since at least that much time is needed to reset the flux in the core of power transformer T1. At low line voltage the duty ratio does approach 0.5 and the current loop can be on the verge of oscillation at that operating point.

In addition to the question of stability of the current loop, it is also instructive to know the bandwidth of this loop. It is common knowledge that the control-to-output transfer function of current mode control falls at a –1 slope (–20 dB per decade). The reason for this –1 slope may not be so commonly known. It is because the current loop creates a transconductance block that takes a control voltage and puts out a current, and the ratio of current to voltage is constant with frequency (up to the bandwidth of the current loop). This transconductance block drives an impedance consisting of the power supply output filter capacitor in parallel with the load. A current driving an impedance creates a voltage, so the control voltage to output voltage transfer function is the product of the transconductance of the current loop and the impedance of the output filter capacitor. Since the transconductance is constant with frequency and the impedance of a capacitor falls at a –1 slope, the product of the two falls at a –1 slope also. This is why the control voltage to output voltage transfer function falls at a –1 slope. Above the bandwidth of the current loop, the transfer function of the voltage to current converter is no longer flat with frequency. Above this bandwidth, the control voltage to output voltage falls at a steeper slope than –1. The power supply designer must make sure the voltage loop crossover frequency stays well below the bandwidth of the current loop. This is easier to do when the power supply designer knows the bandwidth of the current loop, but this is not usually the case.

The current loop is measured by connecting one channel of a frequency response analyzer to the compensation pin of the current mode control IC (Vc) and another channel of the analyzer to the output of a current probe. The current probe is clipped around one lead of the energy storage inductor L1. An appropriate scale factor must be applied if the current probe gain is anything other than one volt per amp. The loop is then disturbed by injecting an error voltage in series with the loop exactly as is the case when measuring the voltage loop. The frequency response analyzer measures the control voltage and output current only at the frequency of signal injection, rejecting all other frequencies and noise. The ratio of current to voltage is then plotted as a function of frequency. This is the plot of transconductance versus frequency, and is the closed-loop gain of the current loop. If the output current is not directly available, as is the case with converters using a flyback topology, it may be necessary to measure the control voltage to output voltage transfer function instead. The output impedance can then be modeled (it is simply the actual components of the output filter together with the load), and the control voltage to output voltage transfer function can be divided by the filter and load impedance transfer function to calculate the closed-loop transconductance of the voltage-to-current converter block. We assume these functions are available as part of any good modeling and test system. We know that the modeling, testing, and transfer function math features are part of the Venable Model 350 Frequency Response Analysis System, for example.

You all know about the block diagram consisting of a logical series of steps leading from beginning to end except for one block labeled "Then a miracle occurs!" We are not going to require that particular block, but there are some assumptions that may fall in the "Leap of Faith" category. We are going to point each of these out as they occur, and try to estimate the possible error that mayresult from the assumption.

Figure 2 shows more detail of the internal connections within the UC3844 control chip. The error amplifier (labeled op-amp) actually drives two diodes and then a resistive voltage divider. From an AC standpoint (which is the only standpoint we will use) the diodes do not have any effect, but the divider makes the voltage applied to the comparator only 1/3 of the op-amp output voltage. This voltage is compared to the voltage across R1, except that a high frequency filter is used in practice. This filter is not shown in Figure 1 but it is shown in Figure 2 and consists of the two components Rf and Cf. Leap of Faith #1 is that the control chip manufacturer actually has a 3:1 voltage divider inside the chip.

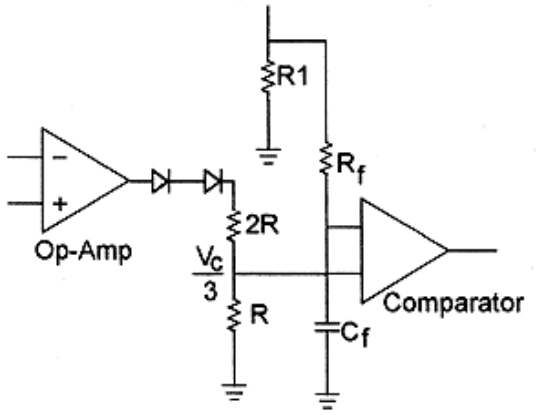

Figure 2. Detail of UC3844 Comparator

Leap of Faith #2 is that the high frequency filter has no effect on the comparator. If you accept these two leaps of faith, then the peak value of the output current is given by the equation

$$I_o \text{ peak} = \frac{V_c}{3 \times R1} \times \frac{N1}{N2} \text{ amps} \qquad (2)$$

Figure 3 shows how the voltage across R1 relates to the output current. The peak current in the output is directly proportional to the peak current in (and peak voltage across) R1. The output current of transformer T1 is the input current times the transformer turns ratio N1 / N2. Figure 3 shows this portion of the schematic of Figure 1 together with waveforms for the voltage across R1 and the current through L1.

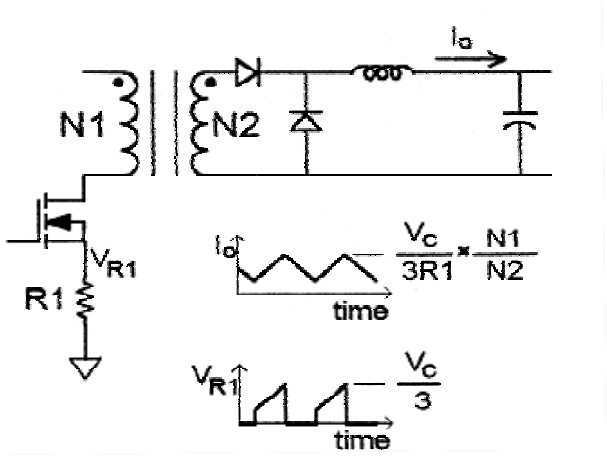

Figure 3. Relationship of output current to control voltage

The whole concept of current mode control is based on the average value of the output current being proportional to the control voltage. As you can see from the analysis so far, it is actually the peak value of the output current that is directly controlled. The average value of the output current is lower than the peak value by half the peak-to-peak ripple current value. In the biggest Leap of Faith so far, Leap of Faith #3 says that the average value of output current is proportional to the peak value of output current. This particular assumption does not have to be taken blindly like the other two. It is actually possible to calculate the peak-to-peak ripple current as a function of the input voltage and the particular design parameters. In Figure 4, we made some assumptions about operating conditions that resulted in peak-to-peak output current ripple of 1 amp at an input voltage of 300 volts. We then varied the input voltage from 150 volts (the voltage that caused 50% duty cycle) to 450 volts to see the effect on output current ripple. As you can see, the peak-to-peak value is relatively constant, within ±10% over the 2:1 voltage range from 225 volts to 450 volts. The peak-to-peak ripple drops off somewhat at lower line voltages, but bear in mind that it is not just the half the peak-to-peak current we are concerned with. It is this current plus the average DC current. If the average DC current were 5 amps, and the peak-to-peak dropped from 1 amp to 0.7 amps (the lowest value on the chart), it would only represent an error of 0.35 amps out of 5, or 7%. On a log current scale, this is a change of less than 1 dB. Based on these numbers, the assumption that the average output current tracks the control voltage seems like a reasonably good assumption.

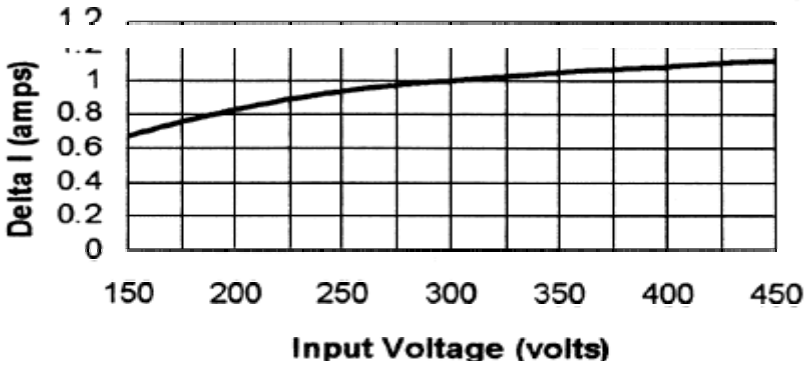

Figure 4. Plot of peak-to-peak ripple current in L1 versus input voltage

For the mathematically inclined, the formula for the above plot is:

$$\Delta I = \frac{V_o}{f \times L1}\left(1 - \frac{V_o \times N1}{V_i \times N2}\right) \text{amps p-p} \quad (3)$$

We used the following variables:

Vo = 5V
f = 100 kHz
L1 = 37.5 µHz
N1 / N2 = 15

A Little Bit About Signals

Figure 5 is a block diagram of a circuit with feedback that you may have seen in one of your early electrical engineering courses.

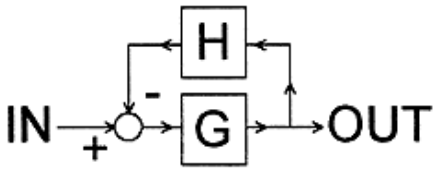

Figure 5. Block diagram of circuit with feedback

If you work out the algebra of the gain from input to output it comes out

$$\text{Gain} = \frac{G}{1+GH} \quad (4)$$

Another more useful way of expressing the same thing is

$$\text{Gain} = \frac{1}{H} \times \frac{GH}{1+GH} \quad (5)$$

Where $\frac{1}{H}$ is a scaling factor and $\frac{GH}{1+GH}$ appears to be (but is not) $\frac{\text{Loop Gain}}{1+\text{Loop Gain}}$.

Here is an important point that is not emphasized in school:

Loop gain is not GH.

Loop gain is –GH.

The reason for this is the "–" sign at the summing node of the diagram where the feedback from gain block H is summed with the input signal. The reason we emphasize this point is that there is a common misunderstanding that loop gain is GH. When a frequency response analyzer is used to measure loop gain by the method described earlier in this paper, it measures true loop gain, –GH. In equations (4) and (5), GH refers to Figure 5, not to real life or to measured data. The true equation for closed loop gain is:

$$\text{Gain} = \frac{1}{H} \times \frac{\text{Loop Gain}}{\text{Loop Gain} - 1} \qquad (6)$$

We should also note that each of these quantities, G and H, are functions of frequency and should really be denoted G(s) and H(s). In what may be the biggest Leap of Faith so far, we are going to assume in Leap of Faith #4 that 1 / H can be considered the DC scaling factor of output current divided by control voltage and that it is not a significant function of frequency. Since there is no frequency shaping components in this loop, this may be a good assumption. Based on Leap of Faith #4,

$$\frac{1}{H} = \frac{I_o}{V_c} = \frac{1}{3 \times R1} \times \frac{N1}{N2} \text{ amps per volt} \qquad (7)$$

We now come to the final and worst assumption of all, that the open loop gain of the current loop is high at low frequency so that the ratio of Loop Gain / (Loop Gain – 1) is approximately 1 at DC. In fact, we know from work done by Dr. David Middlebrook of the California Institute of Technology that the DC gain of the current loop is low, on the order of 3. This Leap of Faith, #5, is so big that we will have to factor in a correction in the final calculations. We can do that by adjusting the scaling factor of the closed loop test data. What we would normally do is to measure the closed-loop gain, then divide the transfer function by the low frequency value so that the curve is asymptotic to a gain of 1 (0 dB) at low frequency. Remember the formula for closed loop gain, excluding the scaling factor of 1 / H, is:

$$\text{Closed Loop Gain} = \frac{\text{Open Loop Gain}}{\text{Open Loop Gain} - 1} \qquad (8)$$

Also recalling that open loop gain has 180 degrees of phase shift at very low frequencies, the formula for Closed Loop Gain (CLG) when the Open Loop Gain is 3 is:

$$CLG = \frac{-3}{-3-1} = \frac{-3}{-4} = +0.75 = -2.5dB \qquad (8a)$$

If we make the assumption that the open loop gain is low, on the order of three (3), then the closed loop gain data should be scaled so that the low frequency gain is –2.5 dB rather than O dB we would normally aim for after correcting for the scaling factor 1/H. If we make the low frequency value of closed loop gain equal to 0.75 (–2.5 dB), we will always have open loop gain of 3 (10 dB) when we do the closed loop to open loop conversion. The question is, how much error does that create in the two parameters we are really interested in, the unity gain frequency of the open loop gain and the phase margin of the open loop gain? To answer that question, let's take two hypothetical open loop plots of the voltage-to-current transconductance block with gains of 2 (6 dB) and 10 (20 dB), convert them to closed loop plots, then scale the closed loop plots for low frequency gain of –2.5 dB, then convert back to open loop plots to see the comparison between the original and the reconstructed plots. By the way, the formula for converting closed loop gain to open loop gain is the same as the formula for converting open loop gain to closed loop gain.

$$\text{Open Loop Gain} = \frac{\text{Closed Loop Gain}}{\text{Closed Loop Gain} - 1} \qquad (9)$$

We know that the low frequency gain will be wrong, it will always be 3 (10 dB), but we can get an answer to the real question of how does the unity gain frequency and loop phase margin compare to the original. If the results are comparable, then we can use the –2.5 dB number in all our calculations and Leap of Faith #5 is not such a great leap as it first appeared. Figures 6–9 show this process for a loop that started with a gain of 2 (6dB). Figures 10–13 show this process for a loop that started with a gain of 10 (20 dB). Choosing the wrong DC gain value causes almost no error in the reconstructed bandwidth of the current loop, and only a small error in the phase margin of theloop. The results are summarized in the tables below.

Table 1. Loop with 6 dB of Gain Bandwidth Phase

	Bandwidth	**Phase Margin**
Original	41.4 kHz	31.5 degrees
Reconstructed	41.6 kHz	27.8 degrees

Table 2. Loop with 20 dB of Gain Bandwidth Phase

	Bandwidth	Phase Margin
Original	41.3 kHz	12.0 degrees
Reconstructed	41.2 kHz	14.6 degrees

Based on these results, the various assumptions or "Leaps of Faith" are reasonable. It is possible to get a very accurate measure of bandwidth and a reasonably accurate measure of phase margin by measuring the closed loop gain of the current loop and then converting this data to open loop gain using these assumptions and techniques.

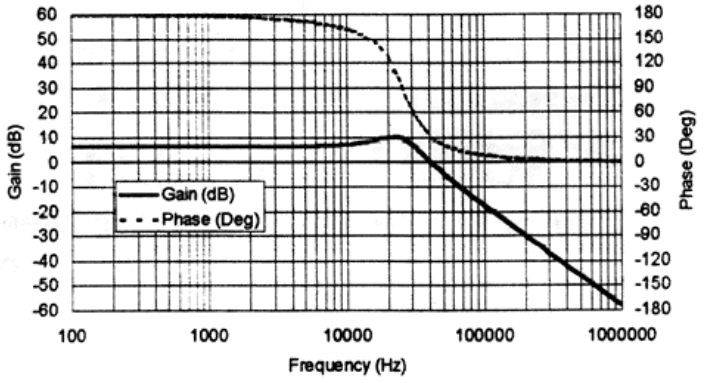

Figure 6. Open loop gain of a typical loop with 6 dB of gain

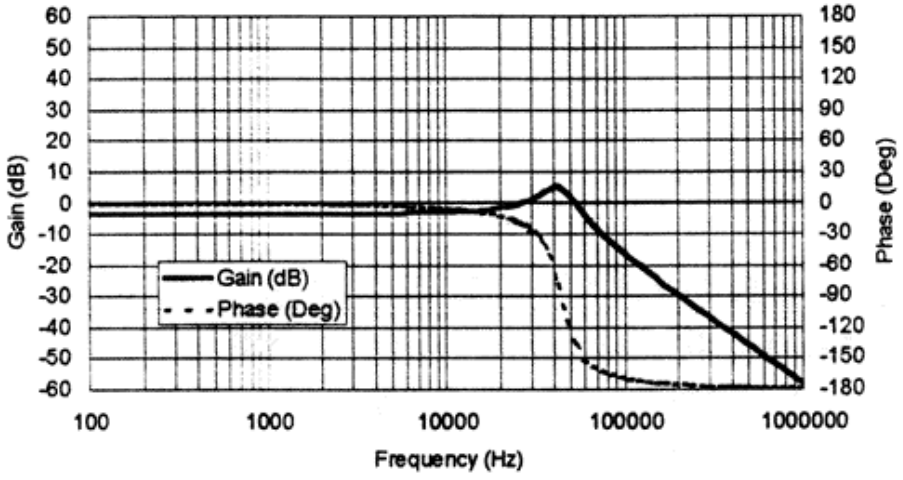

Figure 7. The loop of Figure 6 converted to closed loop

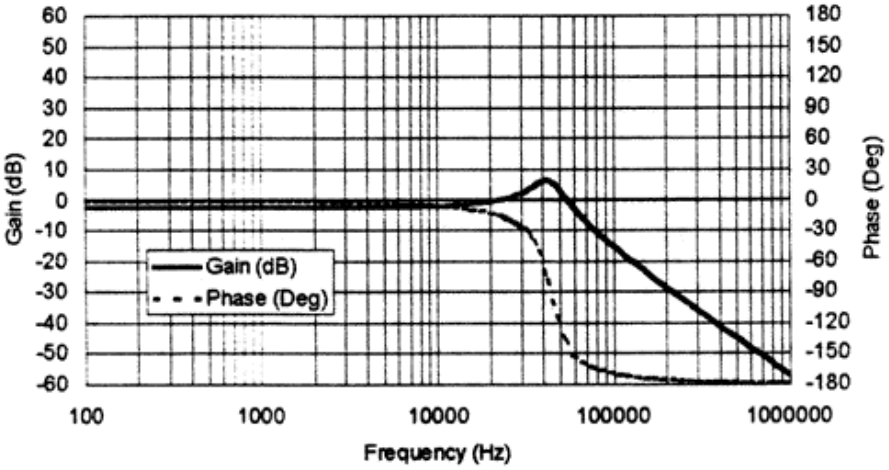

Figure 8. The closed loop gain of Figure 7 scaled to –2.5 dB at DC

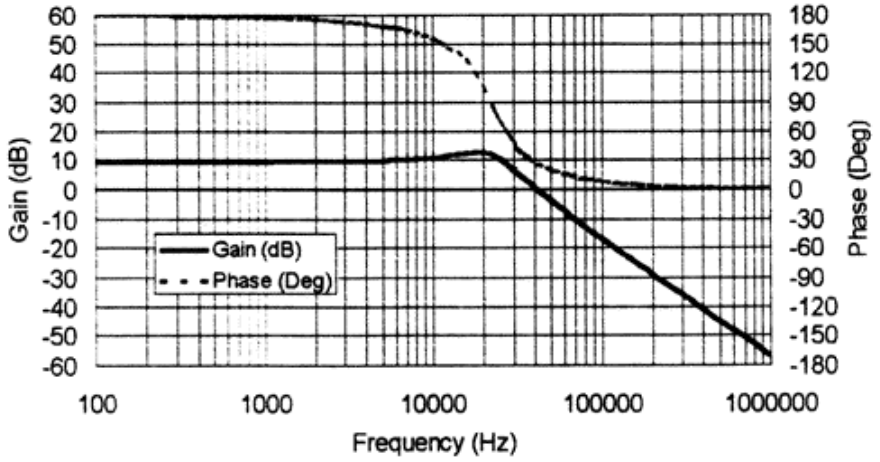

Figure 9. Figure 8 converted back to open loop (the original reconstructed)

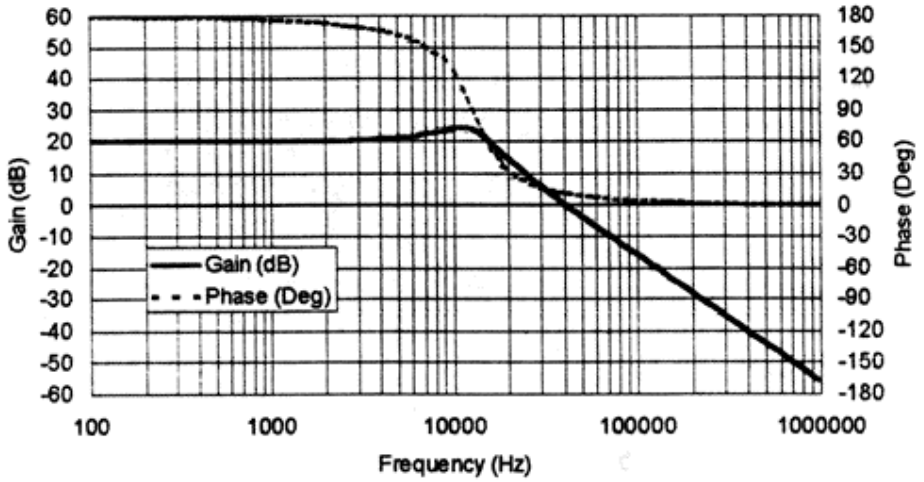

Figure 10. Open loop gain of a typical loop with 20 dB of gain

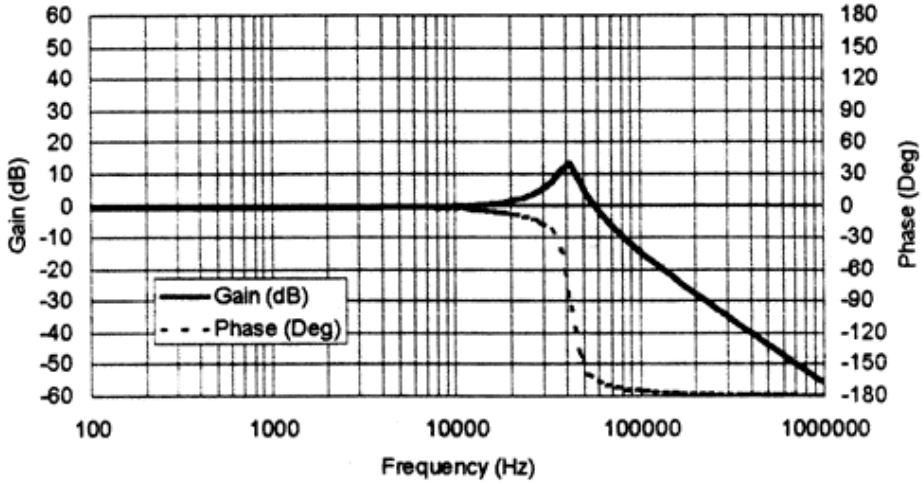

Figure 11. The loop of Figure 10 converted to closed loop

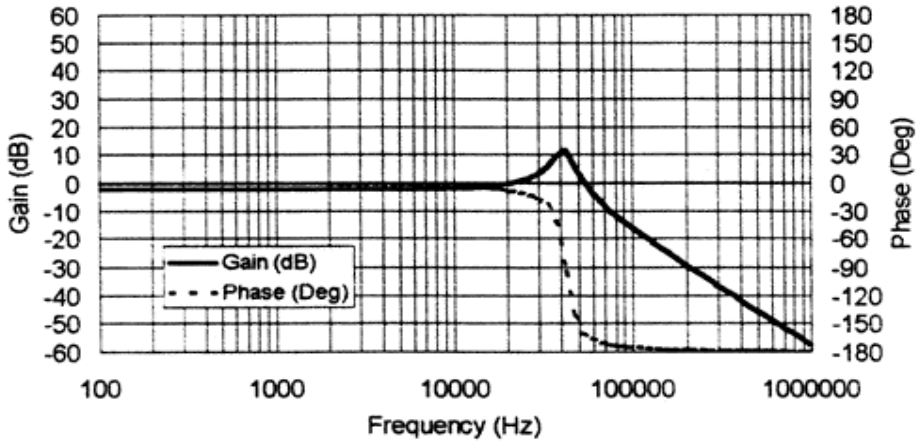

Figure 12. The closed loop gain of Figure 11 scaled to –2.5 dB at DC

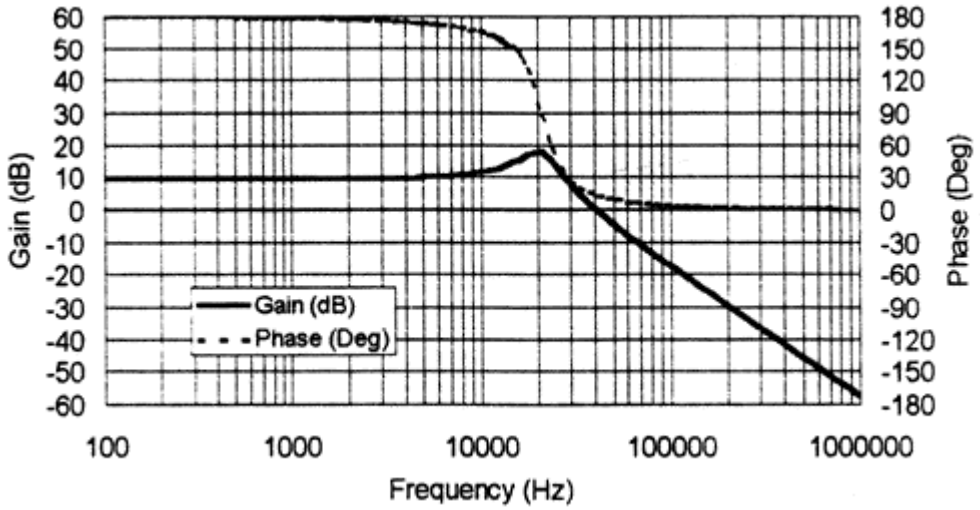

Figure 13. Figure 12 converted back to open loop (the original reconstructed)

Conclusions

If stability criteria such as phase margin are to be specified by power supply purchasers, measurement conditions and techniques need to be specified. In this paper we have described the signal paths of the voltage control loop, the loop that is most likely the object of any phase margin specification. There are frequently other loops in a power supply as well. In supplies with power factor correction, there are one or two additional loops, depending on the implementation of the power factor correction circuit. It is also common to have separate regulators on some critical outputs. This is especially common in recent computer power supply designs where the processor

chip operates at a voltage lower than 5 volts and requires a separate regulator. We feel that if these loops are specified they should be tested correctly also. The goal in all feedback loop testing is to locate a place in the loop where the signal is confined to a single path and where the source is a low impedance and the load is a high impedance. It is not always easy to find such a place, and many power supplies are being incorrectly tested. Guidelines for selecting the proper signal injection point are summarized in this paper and presented in more detail in an earlier paper that was also published as a magazine article [2].

In addition to the main voltage loop, there is also an internal current loop that can be unstable. This loop is not usually specified, and is in fact difficult to measure, at least directly. This paper details a step-by-step procedure for determining the bandwidth and phase margin of this loop.

References

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