SW017
ISO 11784-11785 read only transponder chip

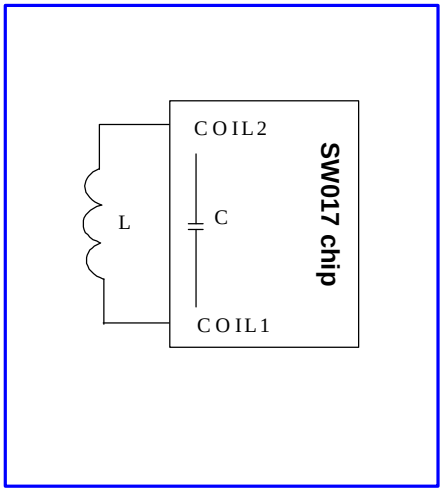
DATA SHEET

Typical Applications

- ➔ **Transponders with additional cap**
- ➔ **Transponder without additional cap**
- ➔ **Ferrite core modules, injectable glass tubes**
- ➔ **Air coil transponders**

Features

- ➔ **Fully compatible with industry-standard 134.2kHz ISO R/O chips.**
- ➔ **ID code memory array custom configurable**
- ➔ **In factory mixed mask and electrical coding simplify delivery**
- ➔ **Bit coding according to ISO FDX-B**
- ➔ **Full wave rectifier on chip**
- ➔ **Small size chip for any transponder types**
- ➔ **Long reading distance**
- ➔ **Bit duration: 32 periods- of RF field**
- ➔ **Low power consumption**
- ➔ **Optional on-chip resonant capacitor to obtain a resonant system with external adapted coil only**



Product Description

The SW017 is a fully integrated 134.2KHz RFID transponder circuit. It is specially designed for being a space and cost efficient kernel of a read-only tag module. SW017 is a monolithic CMOS ASIC which provides full compatibility with other industry-standard 134.2KHz read-only tags. Thanks to its on-chip integrated capacitor, SW017 can be mounted with additional coil only, in order to complete the resonant circuit necessary for inductive 134.2KHz reading.

General functional description

FUNCTIONAL DIAGRAM

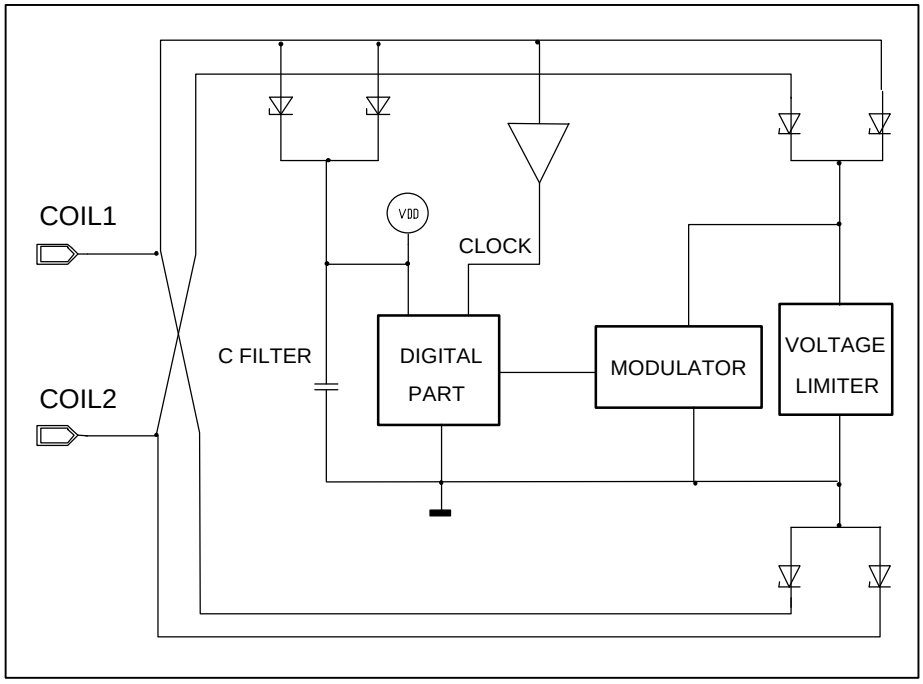


Figure 1 : Block diagram

GENERAL FEATURES

SW017A is supplied by means of an electromagnetic field induced on the attached coil. The chip gets its clock via the coil terminals.

The chip is divided in two parts – high power and low power parts, separated by two Graetz bridges, having a common ground.

The modulator is in the “high power” part of the chip, controlled by the digital part. Load modulation is implemented. The modulator acts directly on the voltage, limited by the voltage limiter, and, over the voltage drop on the diodes -– on the voltage on the coil. 128 bits of information, contained in a factory defined memory array, are transmitted continuously as long as the chip is powered.

Due to the low power consumption of the logic core, no supply capacitor other than the on-chip one is required.

VOLTAGE LIMITER

The voltage limiter, situated in the "high power" part of the chip, limits the voltage between 2.0V up to 4.5V with different AC coil currents.

A limited voltage (Vcoil) can be seen on the coil (Vcoil voltage is two diode voltage drops higher than the limited voltage Vlim). The digital part power supply VDD is close to Vlim. With small currents Vlim almost coincides with VDD. With high currents, because of the different diode voltage drops (high current flows only through the high power part diodes), the difference between Vlim and VDD increases. Digital part power supply VDD is limited between 2.0V up to 5.0V.

DIGITAL PART

The digital part consists of control logic, memory array and digital modulator.

- **Control Logic**

One coil terminal is used to obtain the clock signal for the logic. The output of the clock extractor drives a sequencer, thus providing all necessary signals to address the memory array and serially output the data. The data rate is set to 32 clocks per cycle.

- **Memory**

The memory contains 128 bits memory array custom configurable.

The in factory electrical coding is done according to a customer list of codes. The bits are read serially in order to control the modulator. The 128 bits output sequence is repeated continuously until power goes off.

- **Memory organization**

The structure of the 128 bits is presented in a memory map (Figure 3) and is as follows :

The header is sent first and is used to identify the start sequence. It is composed of 11 bits having a bit pattern which is unique in the data stream: 000 000 000 01

The header is followed by the identification code, which is composed of 64 bits organized in 8 blocks of 8 bits. Each block of 8 bits is trailed by a control bit set to logic "1" to prevent that the header is reproduced in the data. Bit 64 is transmitted first.

- ➔ Bit 1 is a flag for animal "1" or non-animal "0" application.
- ➔ Bit 2-15 are reserved code for future use.
- ➔ Bit 16 is a flag for additional data block "1" or no additional data block "0".
- ➔ Bits 17-26 ISO 3166 is the Numeric country code.
- ➔ Bits 27-64 is the National identification code.
- ➔ The next two 8 bits blocks contain the 16 CRC-CCITT error detection bits. LSB is transmitted first, and the 2 blocks are trailed with a binary "1'.

The data stream with 3 blocks of 8 bits is trailed with a logical “1” representing the extension bits. The extension bits are planned for the future extension in which for instance information from sensors or contents of trailing pages may be stored. In the current version, the standard coding will be:

000 000 001 000 000 001 000 000 001

… and the flag bit 16 of the identification code “0”.

- **Memory map**

Programming of bits is done in two ways – electrically and with mask.

The electrically programmed bits are:

➔ The 24 least significant bits from the National identification code, i.e. bits 41 to 64.
➔ The 16 CRC bits.

All the rest of the bits are mask programmed.

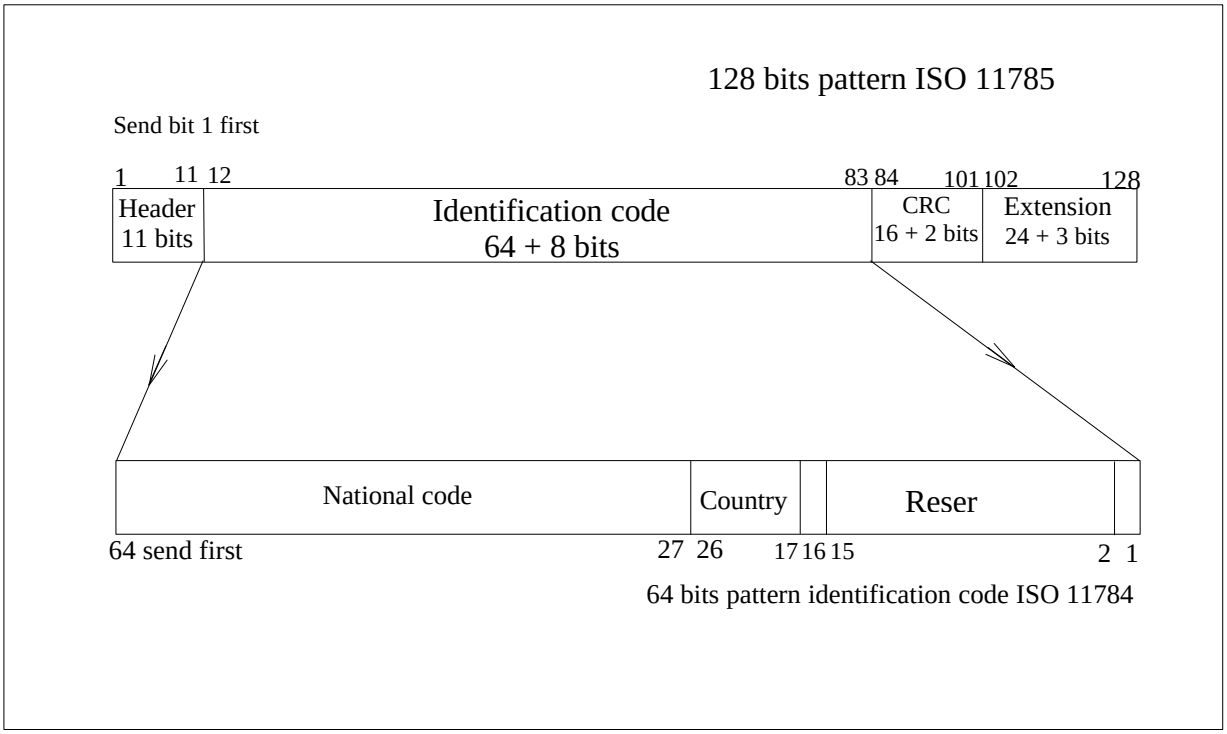


Figure 2 : Memory Map

- **Data encoder**

The data is coded according to the FDX-B scheme. At the beginning of each bit, a transition will occur. A logic bit “1” will keep its state for the whole bit duration and a logic bit “0” will show a transition in the middle of the bit duration (Figure 4).

The FDX-B allows in advance of up to 8 clocks in the ON to OFF transition. Due to its low power consumption, there is no difference in performance for SW017A when implementing a transition advance. No clock advance is provided on the standard version.

MODULATOR

As mentioned above, the modulator is in the “high power” part of the chip. It is controlled by the digital part, according to the data, programmed in the chip.

When the digital control signal is ON additional load is switched in the chip, higher current flows through the coil and the voltage on the coil (Vcoil) decreases – Figure 4.

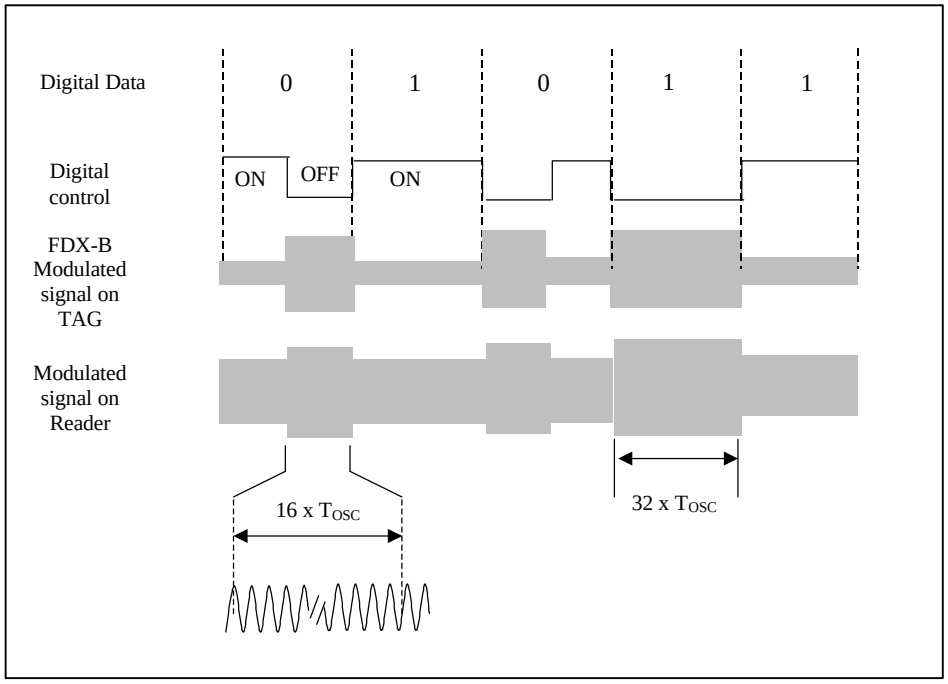


Figure 3 : Timing and Modulation Waveforms

RESONANCE CAPACITOR

An on chip custom adjusted ±10% capacitor is provided to obtain a resonant LC circuit together with the external coil. The integrated capacitor value varies from 0 (no cap) to 200pF, according to part number.

Electrical features

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions
Maximum AC peak current induced between COIL 1 and COIL 2	I_{COIL}	25mAp
Max storage temperature	$T_{STOREmax}$	+200 °C
Min storage temperature	$T_{STOREmin}$	-55 °C
Electrostatic discharge according to MIL-STD 883C method 3015	V_{ESD}	750 V

Stressed above these listed maximum ratings may cause permanent damage to the device. Exposure beyond specified conditions may affect device reliability or cause malfunction.

OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
Operating temperature	T_A	-40		+85	°C
AC supply voltage	V_{COIL}	5.1		*note	V_{PP}
AC coil current	I_{COIL}			15	mA
Supply frequency	f_{COIL}	100		200	kHz

*note : the supply voltage is internally limited for reliability purpose

ELECTRICAL CHARACTERISTICS

(V_{AC} = 5.8V_{PP}, V_{COIL} ≅ 5.1V_{PP}, R=1k*, L=1.5mH, C=1nF, f_{COIL} = 130 kHz sine wave, T_A = +25 °C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Demodulated voltage	U_{DEMOD}	fig.4	0.25			V
Coil1-Coil2 on-chip capacitance	C_S		±10% tolerance on typical value			pF
Capacitor series resistance	R_S		According to chosen part#			Ω

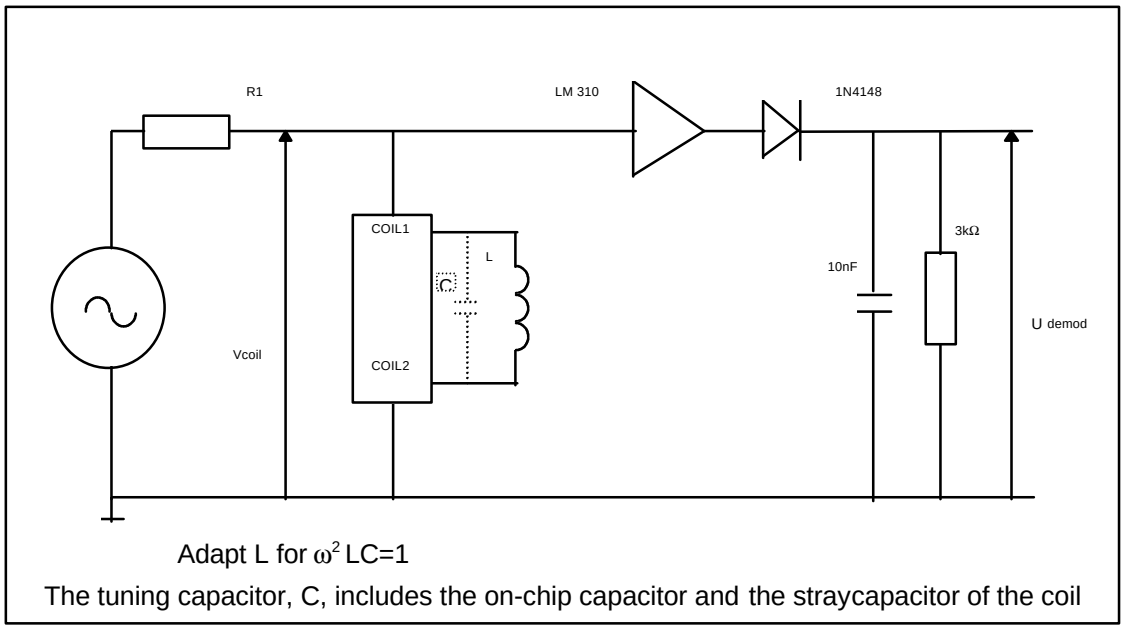


Figure 4 : Testing configuration of electrical parameters

TIMING CHARACTERISTICS

V_{COIL2} = 0V, V_{COIL1} = 5.1 V_{PP}, sine wave

Timings are derived from the field frequency and are specified as a number of RF periods.

Parameter	Symbol	Min	Typ	Max	Units
Coil clock frequency	f_{COIL}	100		300	kHz
Ratio between bit period and coil period (FDX-B coding)	R_{BCP}		32		

Handling Procedure

This device has built-in protection against high static voltages or electric fields. However, due to the unique properties of this device, anti-static precautions should be taken as for other CMOS component. Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the supply voltage range. Unused inputs must always be tied to a defined logic voltage level.

Ordering information

Product form	On-chip tuning cap value	Order Code
Chip form	no tuning cap	SW017AF-U/P(xx)*
	75pF	SW017BF-U/P(xx)*
	200 pF	SW017CF-U/P(xx)*
Package form in PDIP (sampling only)	no tuning cap	SW017AF-DC

* xx is the hex. value for customer/country code

DELIVERY FORMS: - Un-sawn wafers
- Sawn wafers on foil

Mechanical characteristics

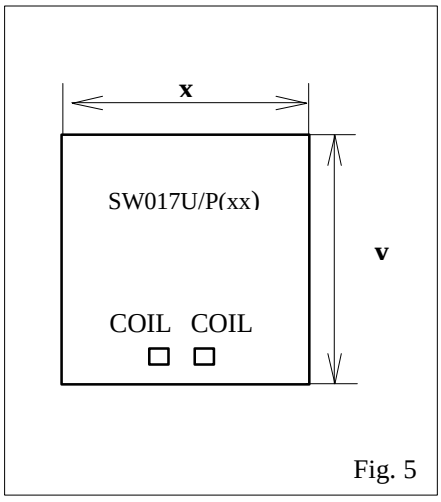


Fig. 5

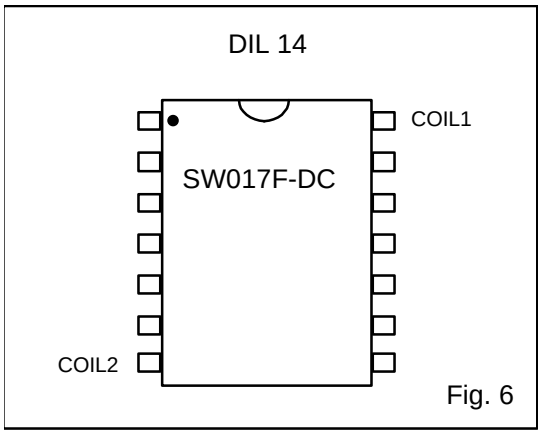


Fig. 6

Order Code	Dimension (mm)	
	x	y
SW017AF-U/P(xx)*	1.23	1.71
SW017BF-U/P(xx)*	1.23	1.79
SW017CF-U/P(xx)*	1.23	1.96

Notes:

- Standard die thickness is 450µm. Thinner circuits are available on request.

- Bonding pad size is 120 x 120 µm

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