Intel® Edison Compute Module

Hardware Guide

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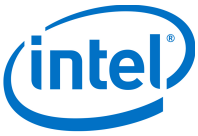

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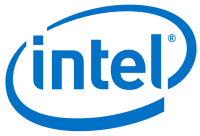

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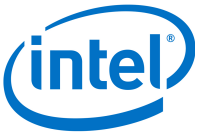

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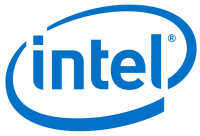

Revision History

Revision	Description	Date
ww32	Initial release	August 4, 2014
ww34	Minor edits.	August 20, 2014
001	First public release.	September 9, 2014
002	Minor corrections.	September 16, 2014
003	Added section on software recovery mode.	November 14, 2014
004	Major content additions to chapter 4.	January 30, 2015
005	Minor change in chapter 4.	June 13, 2015

§

1 Introduction

This document describes the hardware interface of the Intel® Edison compute module. It provides an overview of how to create an expansion board that connects directly to the Intel® Edison compute module.

1.1 References

Table 1 Product-specific documents

Reference	Name	Number/location
331188	Intel® Edison Board Support Package User Guide	
331189	Intel® Edison Compute Module Hardware Guide	(This document)
331190	Intel® Edison Breakout Board Hardware Guide	
331191	Intel® Edison Kit for Arduino* Hardware Guide	
329686	Intel® Galileo and Intel® Edison Release Notes	
[GSG]	Intel® Edison Getting Started Guide	W: *http://www.intel.com/support/edison/sb/CS-035336.htm* M: *http://www.intel.com/support/edison/sb/CS-035344.htm* L: *http://www.intel.com/support/edison/sb/CS-035335.htm*
331438	Intel® Edison Wi-Fi Guide	
331704	Intel® Edison Bluetooth* Guide	

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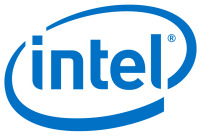


2 High-Level Functional Description

The Intel® Edison Compute Module is designed to lower the barriers to entry for anyone prototyping and producing IoT and wearable computing products. Intel® Edison contains core system processing and connectivity elements: Processor and processor power management IC, RAM, eMMC, and Wi-Fi/BT. Intel® Edison is a module that interfaces with end-user systems via a 70-pin connector. Intel® Edison relies on the end-user to provide input power, and overall system power management, such as battery recharging for battery-powered systems. Table 2 shows the main system components.

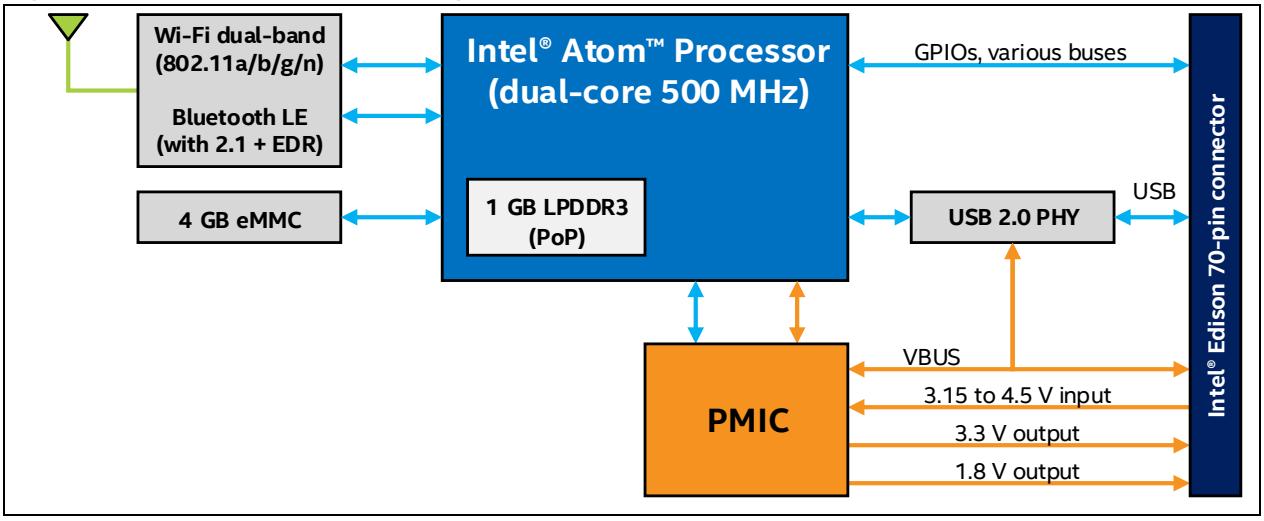
Table 2 Hardware features

Component	Description
Processor	22 nm Intel® SoC that includes a dual-core, dual-threaded Intel® Atom™ CPU at 500 MHz and a 32-bitIntel® Quark™ microcontroller at 100 MHz
RAM	1 GB LPDDR3 POP memory (2 channel 32 bits @ 800 MT/sec)
Internal storage	4 GB eMMC (v4.51 spec)
Power	TI SNB9024 power management IC
Wireless	Dual-band (2.4 and 5 GHz) IEEE 802.11a/b/g/n
Bluetooth*	BT 4.0 + 2.1 EDR
Antenna	Dual-band onboard chip antenna or u.FL for external antenna
Connector	70-pin Hirose DF40 Series (1.5, 2.0, or 3.0 mm stack height)
Size	35.5 × 25.0 × 3.9 mm maximum (to be verified)
Power input	3.15 to 4.5 V
I/O	40 general purpose GPIO which can be configured as: • SD card: 1 interface • UART: 2 controllers (one full flow control, one Rx/Tx) • I^2C: 2 controllers • SPI: 1 controller with 2 chip selects • I2S: 1 controller • GPIO: Additional 14 (with 4 capable of PWM)
USB 2.0	1 OTG controller
Clocks	19.2 MHz, 32 kHz

2.1 Block diagram

Figure 1 shows the basic Intel® Edison block diagram.

Figure 1 Intel® Edison block diagram



2.2 Module photos

Figure 2 Intel® Edison compute module top view

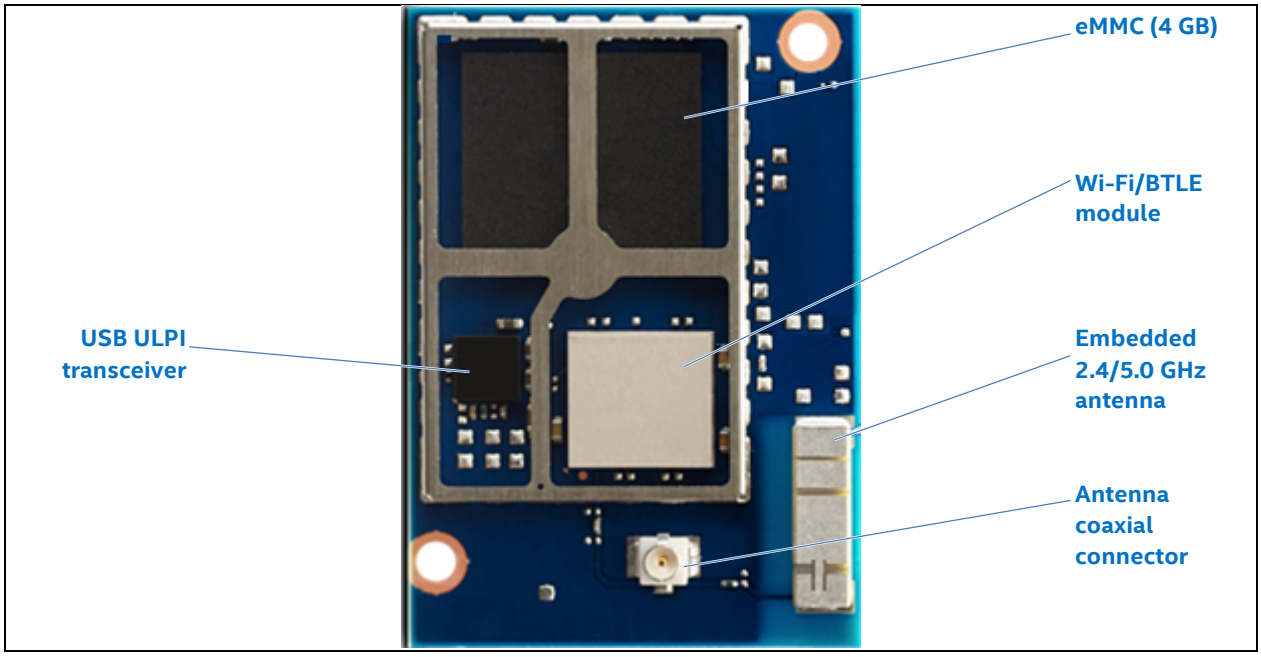
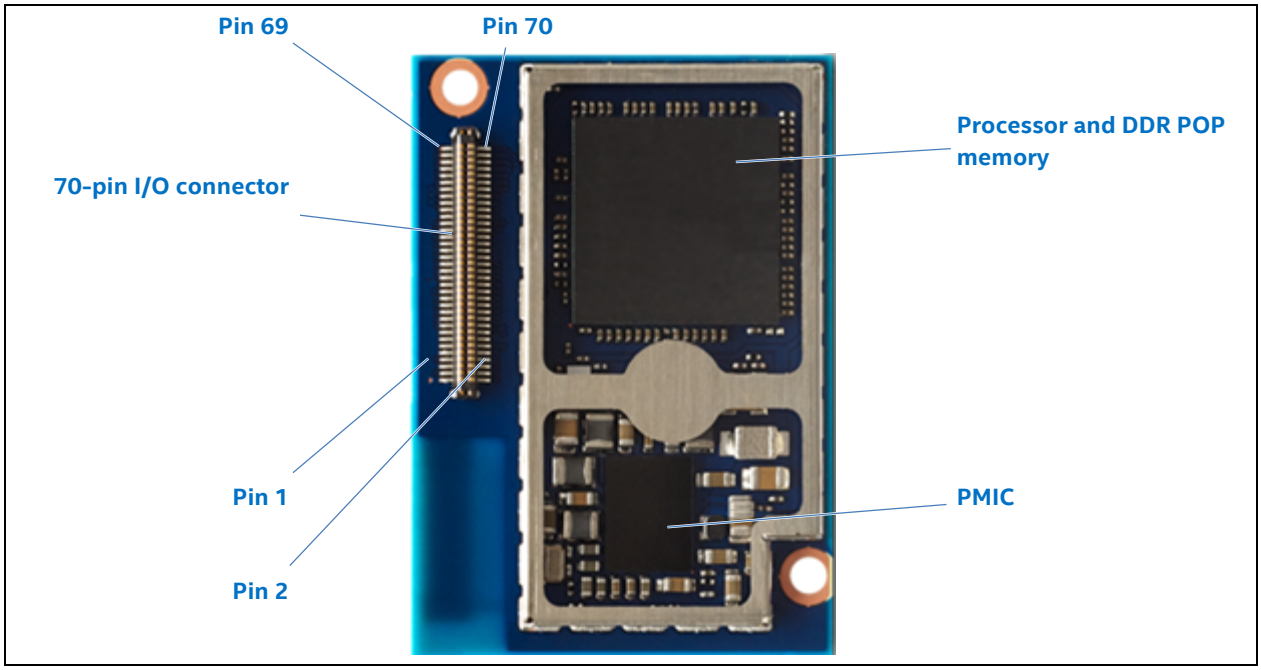


Figure 3 Intel® Edison compute module bottom view



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3 Component and Subsystem Details

3.1 Intel® Atom™ processor

Intel® Edison takes advantage of the Intel® Atom™ Processor 22 nm System-on-Chip, targeted for the smartphone market segment. The SoC contains dual IA-32 cores operating at 500 MHz. The architecture includes 2-wide instruction decode and Out Of Order Execution with 1 MB cache shared between the two CPU cores. It includes Intel SIMD Extensions 2, 3, 4 (SSE2, SSE3, SSE4.1/4.2).

3.2 Wi-Fi / BT module

The Murata integrated Wi-Fi BT module is built around a Broadcom BCM43340 Wi-Fi/BT device.

The Broadcom BCM43340 single-chip quad device provides a high level of integration for a mobile or handheld wireless system, with integrated dual-band (2.4 / 5 GHz) IEEE 802.11a/b/g/n MAC/baseband/radio with Bluetooth* 4.0.

- Dual-band 2.4 GHz and 5 GHz IEEE 802.11 a/b/g/n.
- Single-stream IEEE 802.11n support for 20 MHz and 40 MHz channels provides PHY layer rates up to 150 Mbps for typical upper layer throughput in excess of 90 Mbps.
- Supports standard SDIO v2.0 and gSPI (48 MHz) host interfaces.
- Complies with Bluetooth* Core Specification Version 4.0 with provisions for supporting future specifications. Bluetooth Class 1 or Class 2 transmitter operation.
- Security:
  - WPA and WPA2 (personal) support for powerful encryption and authentication.
  - AES in WLAN hardware for faster data encryption and IEEE 802.11i compatibility –Reference WLAN subsystem provides Cisco* Compatible Extensions (CCX, CCX 2.0, CCX 3.0, CCX 4.0, CCX 5.0).
  - Reference WLAN subsystem provides Wi-Fi protected setup (WPS).

3.3 Managed NAND (eMMC) flash

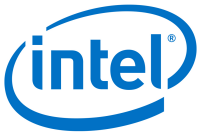
Intel® Edison uses 4 GB of managed NAND to store the file system and user data. Managed NAND flash contains a full MMC controller, wear-leveling firmware, and all the other features that are typically found in MMC cards, except it is available in a small BGA form-factor.

- Bus mode
  - Data bus width: 1 bit (default), 4 bits, 8 bits
  - Data transfer rate: up to 200 MBps (HS200)
  - MMC I/F clock frequency: 0~200 MHz
  - MMC I/F boot frequency: 0~52 MHz

3.4 DDR SDRAM

Intel® Edison supports 1 GB LPDDR3 memory at speeds up to 1033 MT/s.

- 8 banks
- Row addresses R0-R13
- Column addresses C0-C9
- Dual-channel 32 bits
- 400 MHz clock max (800 MT/s)



3.5 Power management IC (PMIC)

Intel® Edison uses the Texas Instruments* SNB9024 Power Management Integrated Circuit (PMIC). The SNB9024 PMIC is for mobile application processors platforms with high feature integration in order to minimize system board area. It includes subsystems for voltage regulation, A/D conversion, GPIOs, and RTC. The SNB9024 device is controlled and programmed using an I^2C interface. There is also a serial voltage ID interface between the SOC and PMIC for handling core voltage rail settings as well as system control signals.

- Four high-efficiency buck converters
  - – Two dual-phase 0.55 to 1.2 V @ 4.8 A with DVS
  - – One dual-phase 1.24 V @ 2.5 A
  - – One single-phase 1.8 V @ 1.1 A
- One 5 V 1.2 A boost converter
- One 3.3 V/3.4 V 1.4 A buck-boost converter
- Five low drop-out regulators
  - – Three programmable 1.05 to 2.85 V @ 100 to 300 mA
  - – One high precision 1 V @ 2 mA
  - – One DVS 0.75 to 0.95 V @ 220 mA
- Two load switches with slew rate control and external load switch control
- USB and AC/DC adapter power supply detection with external charger control (enable/disable and current limit)
- I^2C Interface and dedicated SVI
- Interrupt controller for PMIC events
- Seven general purpose 1.8 V I/Os, with two of them supporting up to 3.3 V
- 32.768 kHz RTC for backup time
- Alarm timer interrupt
- Sleep clock outputs (32.768 kHz)

3.6 USB 2.0 transceiver ULPI interface

The TUSB1211 is a USB 2.0 transceiver chip, designed to interface with a USB controller via a ULPI interface. It supports all USB 2.0 data rates (High-Speed 480 Mbps, Full-Speed 12 Mbps, and Low-Speed 1.5 Mbps) in both Host and Peripheral modes. TUSB1211 also supports the OTG (Ver1.3) optional addendum to the USB 2.0 specification, including Host Negotiation Protocol (HNP) and Session Request Protocol (SRP).

TUSB1211 also supports USB Battery Charging Specification v1.1 integrating a charger detection module for sensing and control on DP/DM lines, and ACA (Adaptive Charger Accessory) detection and control on ID line. ACA allows simultaneous connection of a USB Charger or Charging Downstream Port and an Accessory to a portable OTG device. Configuration bits allow an ACA-agnostic legacy link to correctly communicate with the connected accessory port through the ACA.

3.7 Integrated chip antenna or u.FL connector for external antenna

The Intel® Edison Compute Module has an integrated dual-band 2.4/5 GHz antenna built onboard. The onboard antenna is used primarily for small form factor plastic devices. For larger devices or a device which has a metal enclosure, another version of Intel® Edison is available with an industry standard u.FL connector for attachment to an external antenna. This will allow the end-user to locate the antenna for optimal performance.

Note: The internal antenna versions also have a u.FL connector on the board, but it is only used as a manufacturing test point. *Do not* connect an external antenna to a board with an internal antenna.

3.8 70-pin interface connector

The Intel® Edison Compute Module connects to the end user device via a 70-pin connector. The connector on Intel® Edison is a Hirose 70-pin DF40 Series “header” connector sometimes referred to as a “plug” connector. The Hirose part number for the “header” connector on the Intel® Edison compute module is DF40C-70DP-0.4V(51).

The mating Hirose connector on an expansion board is the “receptacle” connector. This mating “receptacle” connector is available in three different heights. The board-to-board mating stack height can be 1.5, 2.0, or 3.0 mm. Table 3 lists the Hirose part number for the “receptacle” connector and corresponding DigiKey and Mouser part numbers for an expansion board.

Table 3 Intel® Edison 70-pin connector part numbers

Hirose P/N	Mating stack height	DigiKey P/N	Mouser P/N
DF40C-70DS-0.4V(51)	1.5 mm	n/a	798-DF40C70DS04V51
DF40C(2.0)-70DS-0.4V(51)	2.0 mm	H11908CT-ND (low quantity) H11908TR-ND (tape and reel)	798-DF40C2070DS04V51
DF40HC(3.0)-70DS-0.4V(51)	3.0 mm	n/a	n/a

The Intel® Edison Arduino board utilizes the 2.0 mm board-to-board stack height connector.

The bottom side of the Intel® Edison compute module (side with 70-pin connector) has a component height (shield height) of 1.5 mm and will sit flush against the connecting PCB if a 1.5 mm connector is used. Table 3 lists the expansion board component height restrictions for components under the Intel® Edison compute module.

Table 4 Intel® Edison 70-pin connector board-to-board mating height

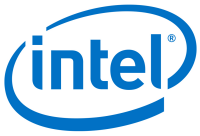
Hirose P/N	Board-to-board mating height	Available height under Intel® Edison
DF40C-70DS-0.4V(51)	1.5 mm	n/a
DF40C(2.0)-70DS-0.4V(51)	2.0 mm	0.5 mm
DF40HC(3.0)-70DS-0.4V(51)	3.0 mm	1.5 mm

Intel® Edison is secured to an expansion board via two mounting holes each with a diameter of 2.0 mm. Any mounting standoffs will also need to match the mating connector height (1.5, 2.0, or 3.0 mm).

Table 5 lists the Intel® Edison 70-pin connector pinouts and signals.

Table 5 Intel® Edison connector pinout and signal list

Pin	Signal name	Alternate function	Description
2, 4, 6	VSYS		System input power (3.3 to 4.5 V)
8, 10	3.3 V		System 3.3 V output
12	1.8 V		System 1.8 V output (same as I/O voltage levels)
14	DCIN		Input, connect to VSYS when powering from a DC power adapter (no connect if powering from a battery)
1,5,9,11,13,15	GND		Ground
7	MSIC_SLP_CLK3		32 kHz sleep clock output
3	USB_ID		USB OTG ID pin
16	USB_DP		USB D+
18	USB_DN		USB D-
20	USB_VBUS		USB VBUS input (does not power system)
17	PWRBTN#		Power/sleep button input (active low)
19	FAULT		USB power fault input (from external USB current limit switch)
21	PSW		USB power output enable (to external USB current limit switch)
23	V_VBAT_BKUP		Real-time clock (RTC) backup battery input
36	RESET_OUT#		System reset output (active low)
24	GP44		GPIO



Pin	Signal name	Alternate function	Description
25	GP165		GPIO
26	GP45		GPIO
28	GP46		GPIO
30	GP47		GPIO
32	GP48		GPIO
34	GP49		GPIO
42	GP15		GPIO
48	GP14		GPIO
35	GP12_PWM0	PWM_0	GPIO, capable of PWM output
33	GP13_PWM1	PWM_1	GPIO, capable of PWM output
37	GP182_PWM2	PWM_2	GPIO, capable of PWM output
39	GP183_PWM3	PWM_3	GPIO, capable of PWM output
41	GP19	I2C_1_SCL	GPIO, I2C1 clock (open collector when configured for I^2C)
43	GP20	I2C_1_SDA	GPIO, I2C1 data (open collector when configured for I^2C)
45	GP27	I2C_6_SCL	GPIO, I2C6 clock (open collector when configured for I^2C)
47	GP28	I2C_6_SDA	GPIO, I2C6 data (open collector when configured for I^2C)
50	GP42	I2S_2_RXD	GPIO, I2S2 receive data (input)
52	GP40	I2S_2_CLK	GPIO, I2S2 clock (output)
54	GP41	I2S_2_FS	GPIO, I2S2 frame sync (output)
56	GP43	I2S_2_TXD	GPIO, I2S2 transmit data (output)
22	GP134	UART_2_RX	GPIO, UART2 receive (input)
27	GP135	UART_2_TX	GPIO, UART2 transmit (output)
51	GP111	SPI_2_FS1	GPIO, SPI2 chip select 1 (output)
53	GP110	SPI_2_FS0	GPIO, SPI2 chip select 0 (output)
55	GP109	SPI_2_CLK	GPIO, SPI2 clock output
57	GP115	SPI_2_TXD	GPIO, SPI2 transmit data (output)
59	GP114	SPI_2_RXD	GPIO, SPI2 receive data (input)
46	GP131	UART_1_TX	GPIO, UART1 transmit (output)
61	GP130	UART_1_RX	GPIO, UART1 receive data (input)
63	GP129	UART_1_RTS	GPIO, UART1 ready to send (output)
65	GP128	UART_1_CTS	GPIO, UART1 clear to send (input)
44	GP84	SD_0_CLK_FB	GPIO, SD clock feedback
58	GP78	SD_0_CLK	GPIO, SD clock output
60	GP77	SD_0_CD#	GPIO, SD card detect input (active low)
62	GP79	SD_0_CMD	GPIO, SD command
66	GP80	SD_0_DAT0	GPIO, SD data 0
70	GP81	SD_0_DAT1	GPIO, SD data 1
64	GP82	SD_0_DAT2	GPIO, SD data 2
68	GP83	SD_0_DAT3	GPIO, SD data
67	OSC_CLK_OUT_0		19.2 MHz high speed clock output
31	RCVR_MODE		Firmware recovery mode
69	FW_RCVR		Firmware recovery (active high on boot)
29,38,40,49	Unused.		

§

4 External Interface Pins and Electrical Characteristics

Every Intel® Edison I/O (with the exception of USB and Power Button) uses 1.8 V signaling.

4.1 Clocks

Intel® Edison has two clock outputs. A 32 kHz sleep clock connected to pin 7 and a high frequency 19.2 MHz clock connected to pin 67. The sleep clock has ±5 mA drive capability, and may be programmed to provide an output when the SoC is in a sleep state. Refer to the GPIO buffer (1.8 V) DC specification, mentioned in Table 28.

You might need to buffer the clocks, depending on external trace lengths.

4.1.1 19.2 MHz OSC clock output specification

Table 6 provides specifications for clocks labeled OSC_CLK[4:0].

Table 6 19.2 MHz OSC_Clock output

Symbol	Parameter	Min	Typ	Max	Unit	Figure	Notes
	Frequency		19.2	–	MHz		2, 4
T_{RISE}/T_{FALL}	Rise and fall time	1	–	5	ns		1, 3
Duty cycle	Duty cycle	45	–	55	%		2
C2C-J	Cycle to cycle jitter (peak)	–	–	300	ps	Figure 4	2, 5
PJ	Period Jitter (peak to peak)	–	–	350	ps	Figure 4, Figure 5	2, 6
	Long term accuracy	–100	0	+100	ppm		7

NOTE:

1. Edge rate is measured from 20 to 80% of 1.8 V supply.
2. Frequency and duty cycle are measured with respect to 50% of the 1.8 V supply. Duty cycle is measured over three measurements of the of 10 K cycles.
3. Output is based on trace length of 25 to 200 mm, Far End Load of 2 to 5 pF, ESD of 10 pF, and board impedance of 30 to 75 ohm.
4. Divide by two (to achieve frequency of 9.6 MHz) and divide by four (to achieve frequency of 4.8 MHz) options available. Refer to *Merrifield Platform Firmware Architecture Specification (FAS) for Selected Targeted Accounts* for more details.
5. Cycle-to-cycle jitter represents how much the clock period changes between any two adjacent cycles. It can be found by applying a first-order difference operation to the period jitter, as shown by C2 and C3 in Figure 4.The peak cycle-to-cycle jitter is the maximum over 10 measurements of absolute values of 1000 cycles, per JEDEC Specification (JESD65B) *Definition of Skew Specifications for Standard Logic Devices*.
6. Period jitter value is measured by adjusting an oscilloscope to display a little more than one complete clock cycle with the display set to infinite persistence. Scope trigger is set on the first edge, and the period jitter is captured by measuring spread/peak-peak value of the second edge. Period jitter is the maximum over three measurements of the 10,000 cycles, per JEDEC Specification (JESD65B) *Definition of Skew Specifications for Standard Logic Devices*.
7. Long-term accuracy is a function of crystal and platform design. Meeting short term accuracy of ±50 ppm satisfies long term accuracy specification.

Figure 4 Clock jitter definitions

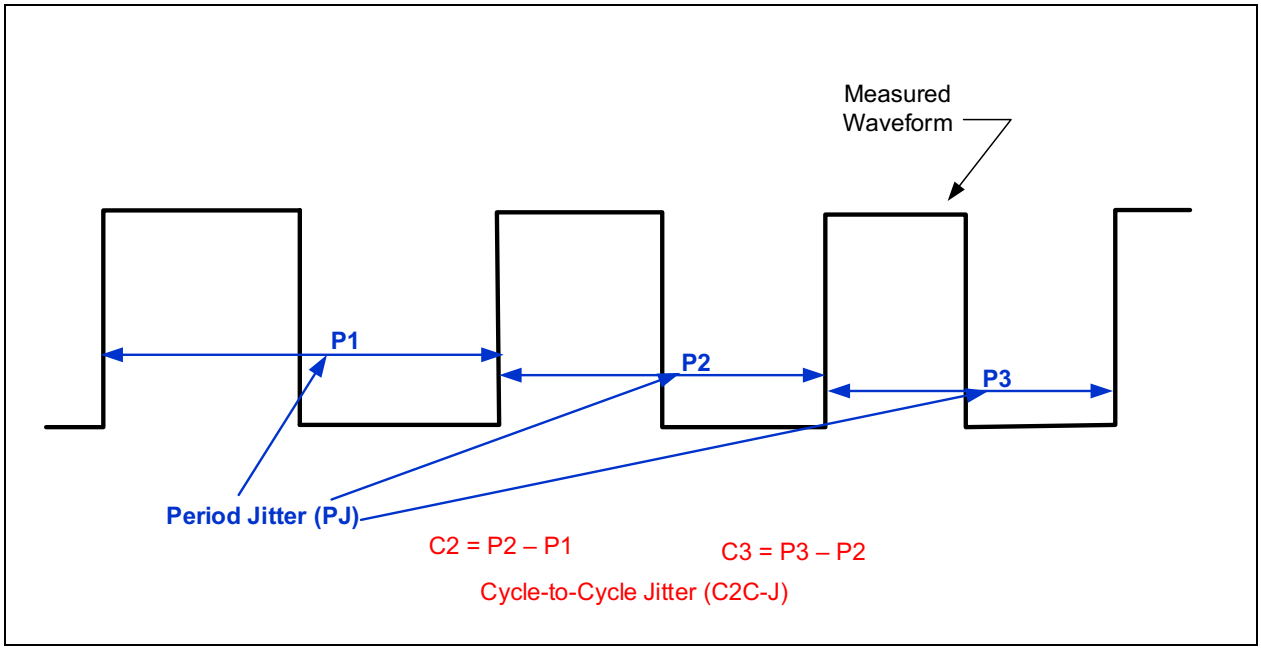
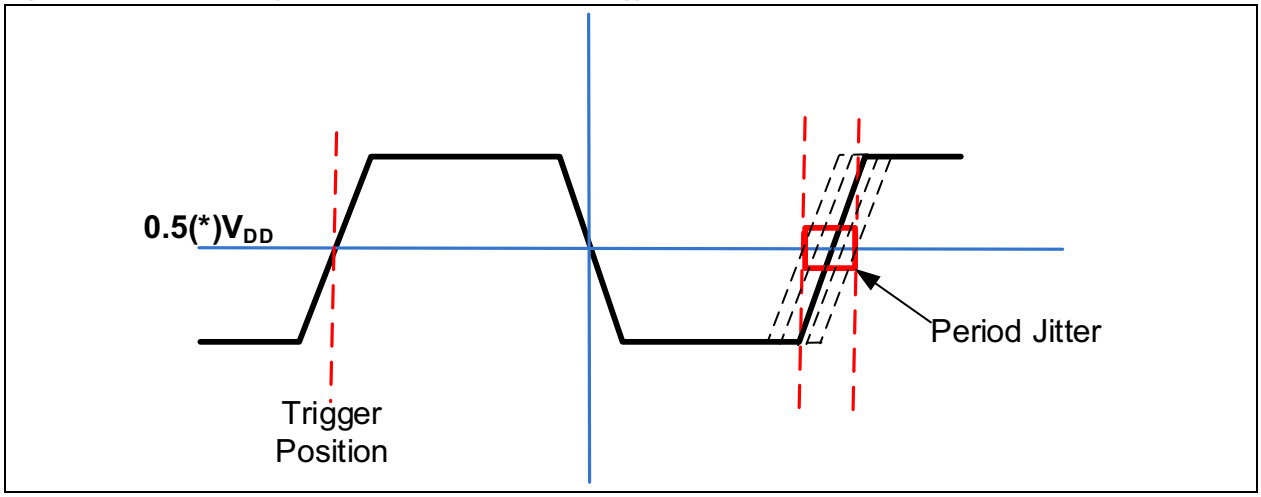


Figure 5 Period jitter measurement methodology



4.1.2 RTC clock specification

Table 7 shows the 32.768 kHz clock specifications to the SoC driven by PMIC.

Table 7 RTC clock input specification

Symbol	Parameter	Min	Typ	Max	Unit	Notes
	Frequency	–	32.768		kHz	
	Long term accuracy	-100	0	+100	ppm	

4.2 I²C Interfaces

Intel® Edison has two available I²C interfaces, I2C1 and I2C6. I2C1 on pins 41 and 43 is a general purpose I²C interface that connects directly to the IA cores. I2C6 on pins 45 and 47 can be configured as I2C6 which connects to the IA cores or as I2C8 which connects to a system controller fabric (controlled by MCU). For the initial release of Intel® Edison, only I2C1 and I2C6 are available. Both of these interfaces are open collector when configured as I²C. When configured as GPIO, they can be standard push pull outputs.

The I²C module can operate in the following modes:

- Standard mode (with data rates up to 100 kbps).
- Fast mode (with data rates up to 400 kbps).
- High-speed mode (with data rates up to 3.4 Mbps).
- The SoC is always I²C master, it does not support multimaster mode.
- The SoC can support clock stretching by slave devices.
- Both 7-bit and 10-bit addressing modes are supported.

When I2C6 is configured as I2C8, it can only run in standard or fast mode.

4.2.1 Standards specification compliance

- I²C–Bus Specification and User Manual Revision 03 dated June 2007.

4.2.2 I²C standard/fast mode electrical characteristics

4.2.2.1 I²C standard/fast mode AC specification

Table 8 AC specification for standard/fast mode I²C bus devices

Symbol	Parameter	Standard		Fast		Unit	Notes
		Min	Max	Min	Max		
fSCL	SCL clock frequency	0	100	0	400	KHz	
tHD: STA	Hold time (repeated) START condition. After this period, the first clock pulse is generated	4.0	–	0.6	–	µs	
tLOW	LOW period of the SCL clock	4.7	–	1.3	–	µs	
tHIGH	HIGH period of the SCL clock	4.0	–	0.6	–	µs	
tSU: STA	setup time for a repeated START condition	4.7	–	0.6	–	µs	
tHD: DAT	Data hold time: I2C-bus devices	0	–	0	–	ns	3
tSU: DAT	Data setup time	250	–	100	–	ns	1
tr	Rise time of both SDA and SCL signals	–	1000	20 + 0.1C_b	300	ns	2, Table 9
tf	Fall time of both SDA and SCL signals	10	300	1	300	ns	4, Table 9
tSU: STO	Setup time for STOP condition	4.0	–	0.6	–	µs	
tBUF	Bus free time between a STOP and START condition	4.7	–	1.3	–	µs	
Cb	Capacitive load for each bus line (=trace capacitance + device load)	–	400	–	400	pF	I
VnL	Noise margin at the LOW level for each connected device (including hysteresis)	0.1 VDD	–	0.1 VDD	–	V	
VnH	Noise margin at the HIGH level for each connected device (including hysteresis)	0.2 VDD	–	0.2 VDD	–	V	

NOTE:

1. A fast-mode I2C-bus device can be used in a standard mode I2C-bus system, but the requirement tSU; DAT ≥ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line tr max + tSU; DAT = 1000 + 250 = 1250 ns (according to the standard-mode I2C-bus specification) before the SCL line is released.

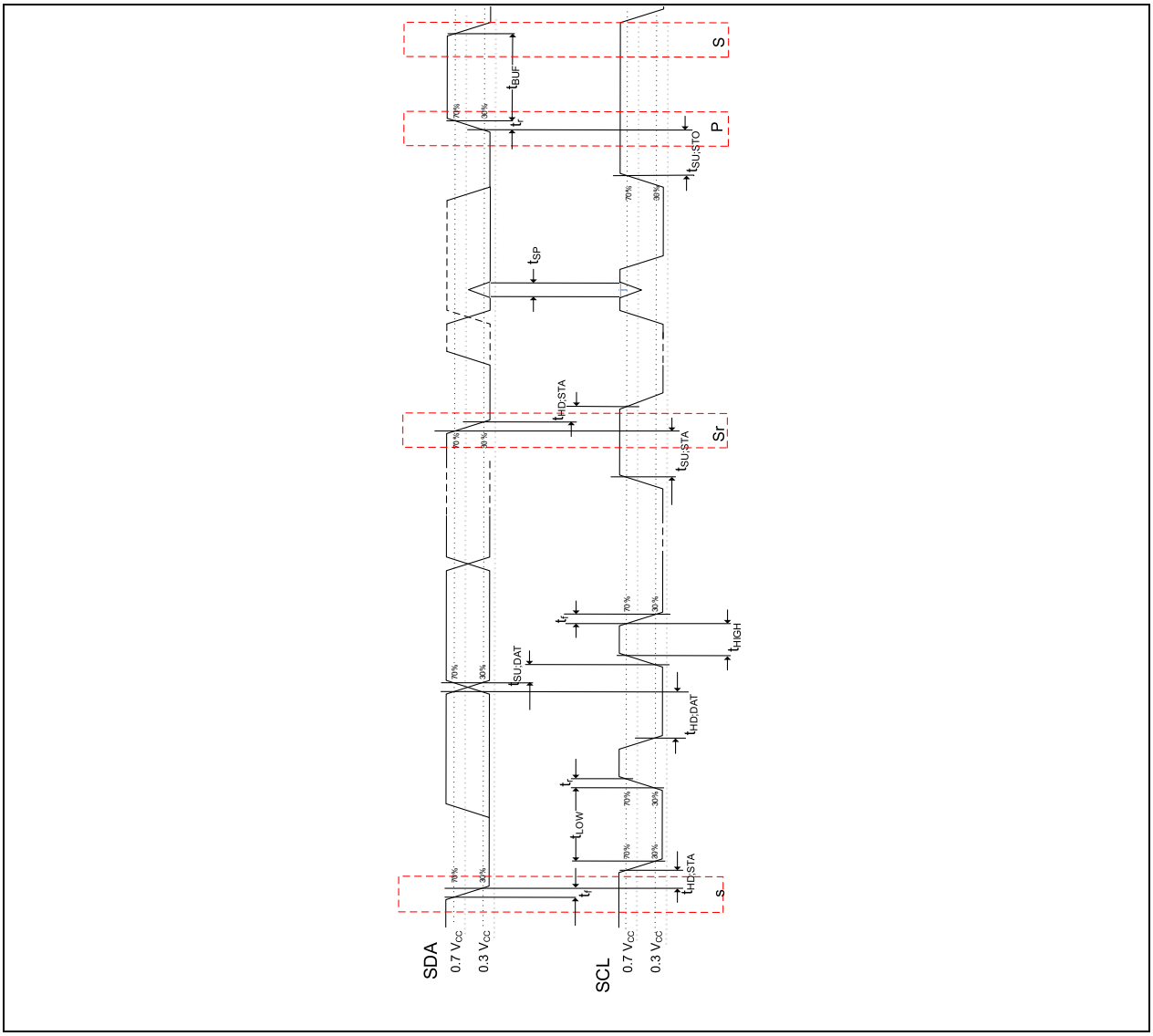
2. C_b = total capacitance of one bus line, in picofarads.
3. The maximum tHD;DAT could be 3.45 µs and 0.9 µs for standard-mode and fast-mode, but must be less than the maximum of tVD;DAT or tVD;ACK by a transition time. This maximum must only be met if the device does not stretch the LOW period (tLOW) of the SCL signal. If the clock stretches the SCL, the data must be valid by the setup time before it releases the clock.
4. Deviates from the I^2C specification, which has a minimum fall time of 20 + 0.1 C_b.

Table 9 I^2C standard/fast mode pullup strength settings for SCL and SDA

C_b	Internal pullup value	Current assist setting	Note
$C_b \leq 14$ pF	20,000	NA	1
14 pF ≤ $C_b \leq 144$ pF	2000	NA	1
40 pF ≤ $C_b \leq 400$ pF	910	NA	1, 2

NOTE:
1. The internal pullup values need to be programmed in the MIP Header of the firmware depending on the value of Cb.
2. Cb greater than 350 pF may require external pulls on the board. Contact your Intel Representative for further guidance.

Figure 6 Definition of timing for standard/fast mode devices on I^2C bus



4.2.2.2 I²C standard/fast mode DC specification

Table 10 DC specification for I²C standard/fast mode devices

Symbol	Parameter	Standard (100 kHz)			Fast (400 kHz)			Unit	Notes[1]
		Min	Typ	Max	Min	Typ	Max		
TSP	Pulse width of the spikes which are suppressed by the input filter.	0	–	54	0	–	54	ns	2
VOL	Output low voltage.	–	–	VDD * 0.2	–	–	VDD * 0.2	V	Ports 0 to 2 and 4 to7
VOL	Output low voltage.	–	–	90	–	–	NA	mV	Port 3
VOH	Output high voltage.	VDD * 0.9	–	–	VDD * 0.9	–	–	V	

NOTE:
1. For all other DC specifications, refer to the GPIO buffer DC specification mentioned in Table 28.
2. Deviates from the I²C specification, which states maximum TSP of 50 ns for fast mode.

4.2.2.3 I²C high speed mode electrical characteristics

Note: I²C high speed mode AC specification based on $C_b \leq 100$ pF, where C_b = trace capacitance + device load.

Table 11 AC specification for high speed mode I²C bus devices

Symbol	Parameter	High speed mode		Unit	Figure	Notes
		Min	Max			
fSCL	SCL clock frequency	0	2.8	MHz		
tSU:STA	Setup time for a repeated START condition	160	–	ns		
tHD:STA	Hold time (repeated) START condition	160	–	ns		
tLOW	LOW period of the SCL clock	160	–	ns		
tHIGH	HIGH period of the SCL clock	60	–	ns		
tHD:DAT	Data hold time: I2C-bus devices	0	–	ns		
tSU:DAT	Data setup time	10	–	ns		
tr CL	Rise time of SCL signals	10	40	ns		
tf CL	Fall time of SCL signals	1	40	ns		
trCL1	Rise time of SCL signal after repeated START condition and after acknowledge bit	10	40	ns		
tr DA	Rise time of SDAH signals	10	80	ns	Table 12	
tf DA	Fall time of SDAH signals	1	80	ns	Table 12	1
tSU:STO	Setup time for STOP condition	160	–	ns		
VnL	Noise margin at the LOW level for each connected device (including hysteresis)	0.1 VDD	–	V		
VnH	Noise margin at the HIGH level for each connected device (including hysteresis)	0.2 VDD	–	V		

NOTE:
1. Deviates from the I²C Specification, which has a minimum fall time of 20 + 0.1 C_b.

Table 12 I²C high speed mode pullup strength settings for SDA

C_b	Internal pullup value	Current assist settings
$C_b < 40$ pF	2 kohm	NA
40 pF $\leq C_b \leq$ 100 pF	910 ohm	NA

NOTE:
1. Internal pullup values must be programmed in the MIP Header of the firmware depending on the C_b for the SDA signals.

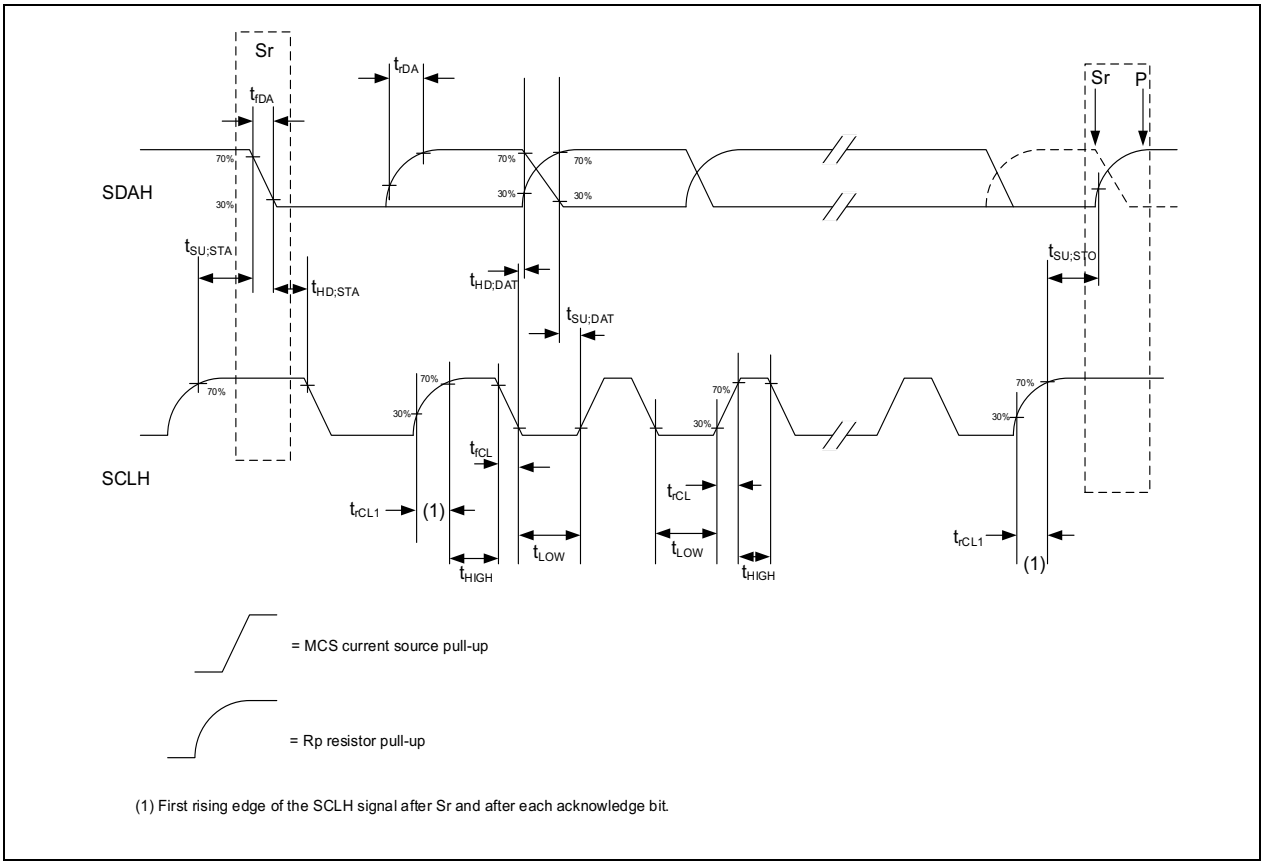
Table 13 I²C high speed mode pullup strength settings for SCL

C_b	Internal pullup value	Current assist settings [1]	Notes
Cb< 30pF	2 kohm	0x1	
30 pF ≤ Cb ≤ 40 pF	2 kohm	0x4	2
40 pF ≤ Cb ≤ 70 pF	2 kohm	0x5	
70 pF ≤ Cb ≤ 90 pF	2 kohm	0xD	
90 pF ≤ Cb ≤ 100 pF	2 kohm	0xE	

NOTE:

1. The internal pullup values and current assist setting need to be programmed in the MIP Header of the firmware depending on the Cb.
2. This setting would apply to I2C Port 0 used to communicate to PMIC.

Figure 7 Definition of timing for high speed-mode devices on I²C bus



4.2.2.4 I²C high speed mode DC specification

Table 14 DC specification for high-speed mode—I²C bus device

Symbol	Parameter	High speed 2.8 MHz			Unit	Notes[1]
		Min	Typ	Max		
TSP	Pulse width of the spikes, which are suppressed by the input filter.	–	–	12	ns	2
VOL	Output low voltage.	–	–	VDD * 0.2	V	
VOH	Output high voltage.	VDD * 0.9	–	–	V	

NOTE:

1. For all other DC Specifications, refer to GPIO Buffer DC Specification, mentioned in Table 28.
2. Deviates from the I²C Specification, which has a max T_{SP} = 10 ns.

4.3 SD card interface

An SD 3.0 compliant interface is available on pins 44, 58, 60, 62, 64, 66, 68, and 70. SD memory key features:

- Host clock up to 50 MHz.
- Supports card detection (insertion/removal) with dedicated card detection signal only.
- Meets SD Host Controller Standard Specification version 3.0.
- Only supports SD memory.
- Requires external level shifter for support of 2.85 V devices.

4.3.1 Standards specification compliance

- SD Specifications Physical Layer Specification—v3.01

4.3.2 SD/SDIO AC specification

Table 15 SD AC specification

Symbol	Parameter	Port 0 (SD)		Port 1 (SDIO)		Unit	Figure	Notes
		Min	Max	Min	Max			
$T_{wc(DDR50)}$	CLK cycle time for DDR50 mode	20	–	20	–	ns	Figure 8.	
$T_{wc(SDR25)}$	CLK cycle time for SDR25 mode	20	–	20	–	ns	Figure 9.	
$T_{wc(SDR12)}$	CLK cycle time for SDR12 mode	40	–	40	–	ns		
T_{DC}	Clock duty cycle	45	55	45	55	%		
$T_{ODLY(DDR50)}$	SD_CLK transitioning edge to SDIO_D	1.9	4.6	2.0	4.5	ns	Figure 8.	4
$T_{ODLY(SDR25)}$	SD_CLK rising edge to SDIO_D	1.9	11.6	3.2	11.5	ns	Figure 9.	4
$T_{ODLY(SDR12)}$	SD_CLK rising edge to SDIO_D	1.9	11.6	3.2	11.5	ns		4
T_{SU_SOC}	SoC setup time (data valid before clock launched)	2.4	–	1.3	–	ns	SDR12/25: Figure 10 DDR50: Figure 8	4
T_{HD_SOC}	SoC hold time (data valid after clock launched)	1.7	–	2.2	–	ns	SDR12/25: Figure 10 DDR50: Figure 8	4
$T_{RISE\ CLK}/T_{FALL\ CLK}$	Clock rise and fall time	0.5	4	0.5	4	ns		1, 2, 3, 5

NOTE:

1. Based on trace length of 0.25 to 4.0 inch, 2 to 5 pF far end load for Port 0, AND 2 to 10 pF far end load (for Port 1) and board impedance of 25 to 75 ohm. This corresponds to a lump load of 35 pF on Port 0 and 40 pF on Port 1.
2. Minimum time deviates from SDIO Specification 3.0, which is not defined in the specification.
3. Measured from 0.58 to 1.27 V.
4. Measured at SoC.
5. Measured at level shifter for Port 0 and at end device for Port 1.

Figure 8 SD/SDIO timing diagram (DDR50)

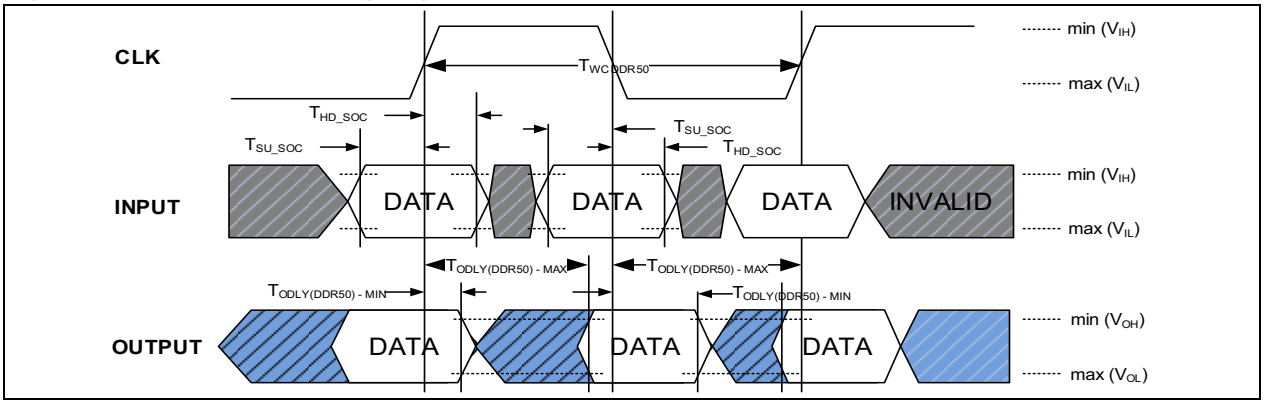


Figure 9 SD/SDIO output timing diagram (SDR 12/25)

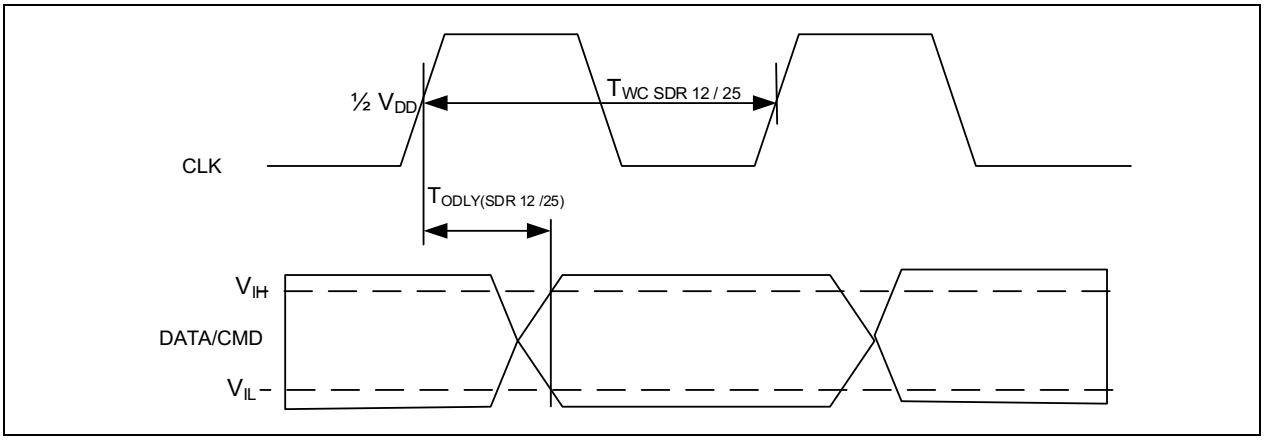
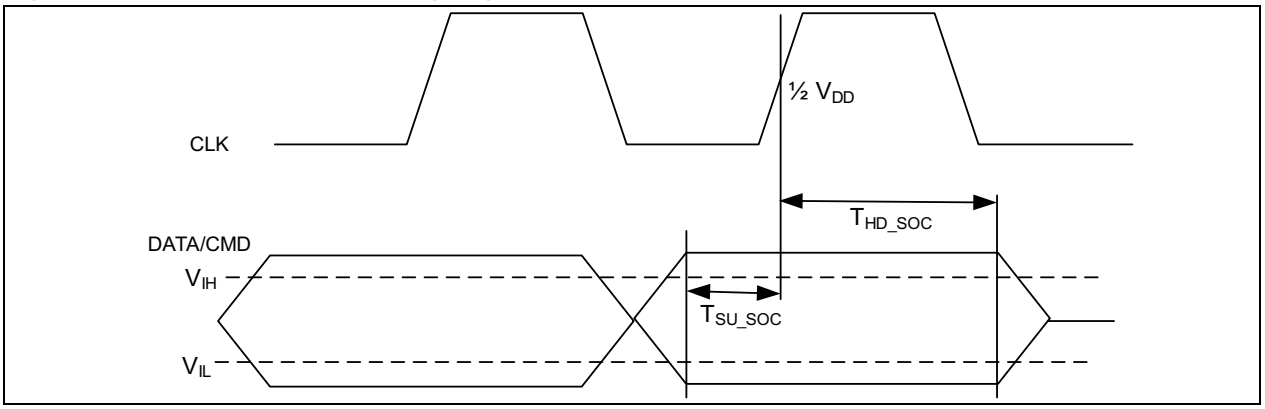


Figure 10 SD/SDIO input timing diagram (SDR12/25)



4.3.3 SD/SDIO DC specification

Table 16 provides the SD/SDIO DC specification. For all other DC specifications not listed here, refer to Table 28.

Table 16 SD/SDIO DC specification

Symbol	Parameter	Min	Typ	Max	Unit	Notes
V_{OL}	Output low voltage.	–	–	0.125*VDD1	V	1, 2. Port 0.
V_{OH}	Output high voltage.	0.75*VDD1	–	–	V	1, 2. Port 0.
V_{OL}	Output low voltage.	–	–	0.45	V	1, 2. Port 1.
V_{OH}	Output high voltage.	1.4	–	–	V	1, 2. Port 1.

NOTE:

1. Assuming a I_{OH}/I_{OL} of 2 mA.
2. Measured at level shifter for port 0 and at end device for port 1.

4.4 UART interfaces

There are two UARTs available: UART1 with flow control and UART2 without flow control. The UART1 interface is available on pins 46, 63, 61, and 54. UART2 is on pins 22 and 27. The UARTs are:

- 16550 compliant
- 64-byte buffer size
- Baud rate from 300 bps to 3.686 Mbps.

The UART2 alternate function is as the Linux* debug serial port.

The SoC supports three instances of a 16550 compliant UART controller (The buffering for this IP is 64 bytes, which makes it 16750 compliant. The register set remains compatible with the 16550.).

Each of the UART interfaces supports the following baud rates (T_{BAUD}): 3.6864 M, 921.6 k, 460.8 K, 307.2 K, 230.4 K, 184.32 K, 153.6 K, 115.2 K, 57.6 K, 38.4 K, 19.2 K, 9.6 K, 7.2 K, 4.8 K, 3.6 K, 2.4 K, 1.8 K, 1.2 K, 600, and 300.

4.4.1 UART AC specification

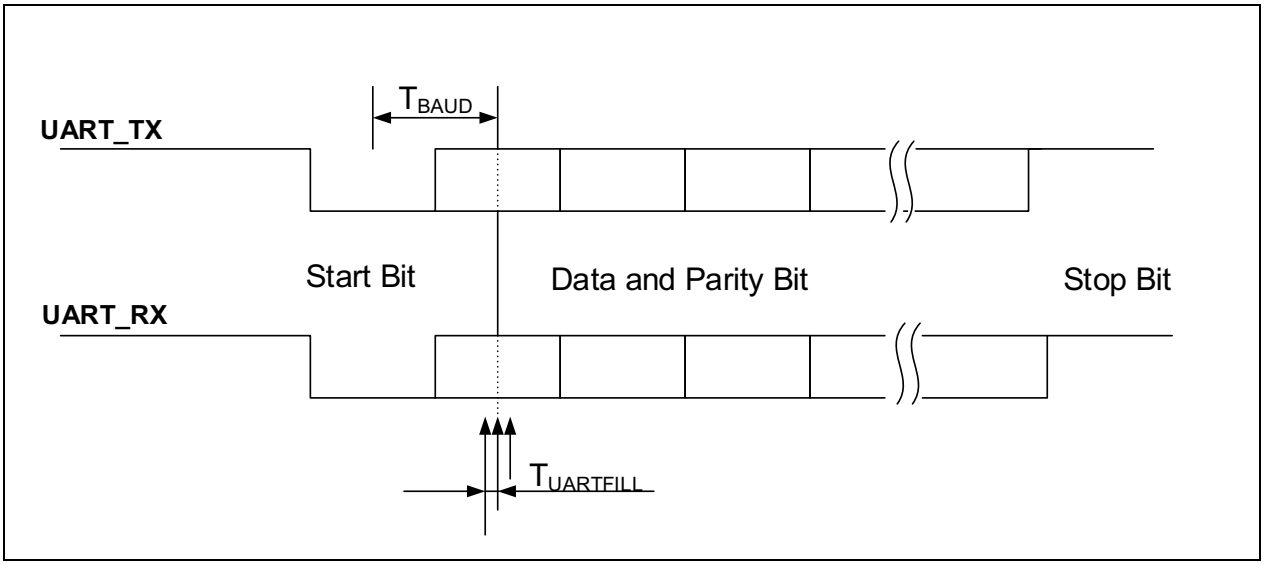
Table 17 UART AC specification

Symbol	Parameter	Min	Max	Unit	Notes
T_{RISE}	Maximum Rise Time	5	25	ns	1, 2
T_{FALL}	Maximum Fall Time	5	25	ns	1, 2
$T_{UARTFIL}$	UART Sampling Filter Period	26	–	ns	3

NOTE:

1. Based on total load capacitance of 5 to 65 pF (trace length up to 100 mm) and board impedance of 25 to 75 ohm.
2. Measured from 10 to 90%.
3. Each bit including start and stop bit are sampled at one-quarter of the prescalar value. Each prescalar cycle has a period of TUARTFIL.

Figure 11 UART timing diagram



4.4.2 UART DC specification

Refer to the GPIO buffer (1.8 V) DC specification, mentioned in Table 28.

4.5 I²S interface

An I²S interface is available on pins 50, 52, 54, and 56. All of the I²S modes below have not been verified and are subject to change. Table 18 lists the available formats available on the I²S port.

Table 18 Intel® Edison I2S available formats

Mode	Priority	Frame rate	Bits/ sample	Number of slots	Frame-to-data offset	Frame polarity	Frame width	Frame rate inaccuracy	Notes
I²S master	1	192K, 96K, 48K, 16K, 8K	16, 24	2	1	0-left, 1-right	50/50	0%	Standard I²S protocol. 50% duty cycle on frame.
PCM slave - SFS	1	192K, 96K, 48K, 44.1K, 16K, 8K	16, 24	192 kHz: 2 96 kHz: 4 All else: 1 to 6	0	High			
PCM slave - LFS	1	192K, 96K, 48K, 44.1K, 16K, 8K	16, 24	192 kHz: 2 96 kHz: 4 All else: 1 to 6	0	High			
PCM master - SFS	1	192K, 96K, 48K, 16K, 8K	16, 24	192 kHz: 2 All else: 1 to 4	0	High	1 bit clockwide	0%	Rising edge frame sensitive. Design supports more frame-to-data offset options.
PCM master - LFS	1	192K, 96K, 48K, 16K, 8K	16, 24	192 kHz: 2 All else: 1 to 4	0	High	1-bit to *n*-bit clocks	0%	*n* is the width of one slot. Design supports width > 1 slot.
Left justified master	2	192K, 96K, 48K	16, 24	2	0	0-left, 1-right	50/50	0%	Design supports flipping polarity on the frame signal.
I²S slave	3	192K, 96K, 48K, 44.1K	16, 24	2	0	0-left, 1-right	50/50	0%	
Left justified slave	3	192K, 96K, 48K	16, 24	2	0	0-left, 1-right	50/50	0%	
Right justified	Not supported.								

The SoC has three I²S ports (labeled I²S 0, 1, 2).

Table 19 I²S ports overview (reference design implementation)

Port #	Mode supported	Nominal voltage	Max operational frequency	Notes
0	Master and Slave	1.8 V	9.6 MHz	Used to interface with the Modem on Reference Design and is used in Slave Mode. Modem uses PCM Short Frame Mode.
1	Master and Slave	1.8 V	9.6 MHz	Used to interface with Bluetooth*/FM Module on Reference Design in Slave Mode.
2	Master and Slave	1.8 V	9.6 MHz	Used to interface with Audio codec in Reference Design and used in Slave Mode.

4.5.1 I²S AC specification

4.5.1.1 I²S master mode AC specification

Table 20 I²S master AC timings

Symbol	Parameter	Min	Max	Unit	Figure	Notes
T_{DC}	Clock duty cycle	45	55	%	I, I, I	
T_{I2S}	Clock frequency	–	9.6	MHz	I, I, I	
T_{S-RXD}	Setup for RXD with respect to the I²S CLK active edge.	10	–	ns	I, I, I	1, 2, 3, 4
T_{H_RXD}	Hold for RXD with respect to the I²S CLK active edge.	10	–	ns	I, I, I	1, 2, 3, 4
T_{CO_TXD}	Tco of TXD with respect to I2S CLK active edge at the SoC.	–	10	ns	I, I, I	1, 2, 3, 4
T_{CO-FS}	Tco of FS with respect to CLK at the SoC.	–	10	ns	I, I, I	1, 2, 3, 4

NOTE:

1. Active edge refers to the mode selected.
2. For I²S mode:
   a. I2S_TXD - SoC launches data after falling clock edge.
   b. I2S_RXD - SoC latches data on rising clock edge.
3. For PCM mode SoC:
   a. I2S_TXD - SoC launches after rising clock edge.
   b. I2S_RXD - SoC latches data on falling clock edge.
4. PCM Mode has two different modes, Short Frame Mode and Long Frame Mode:
   a. Short Frame Mode - Master asserts I2S-FS one clock before it drives data.
   b. Long Frame Mode - Master asserts I2S_FS and data on the same clock

Figure 12 I²S master port timings in I²S mode

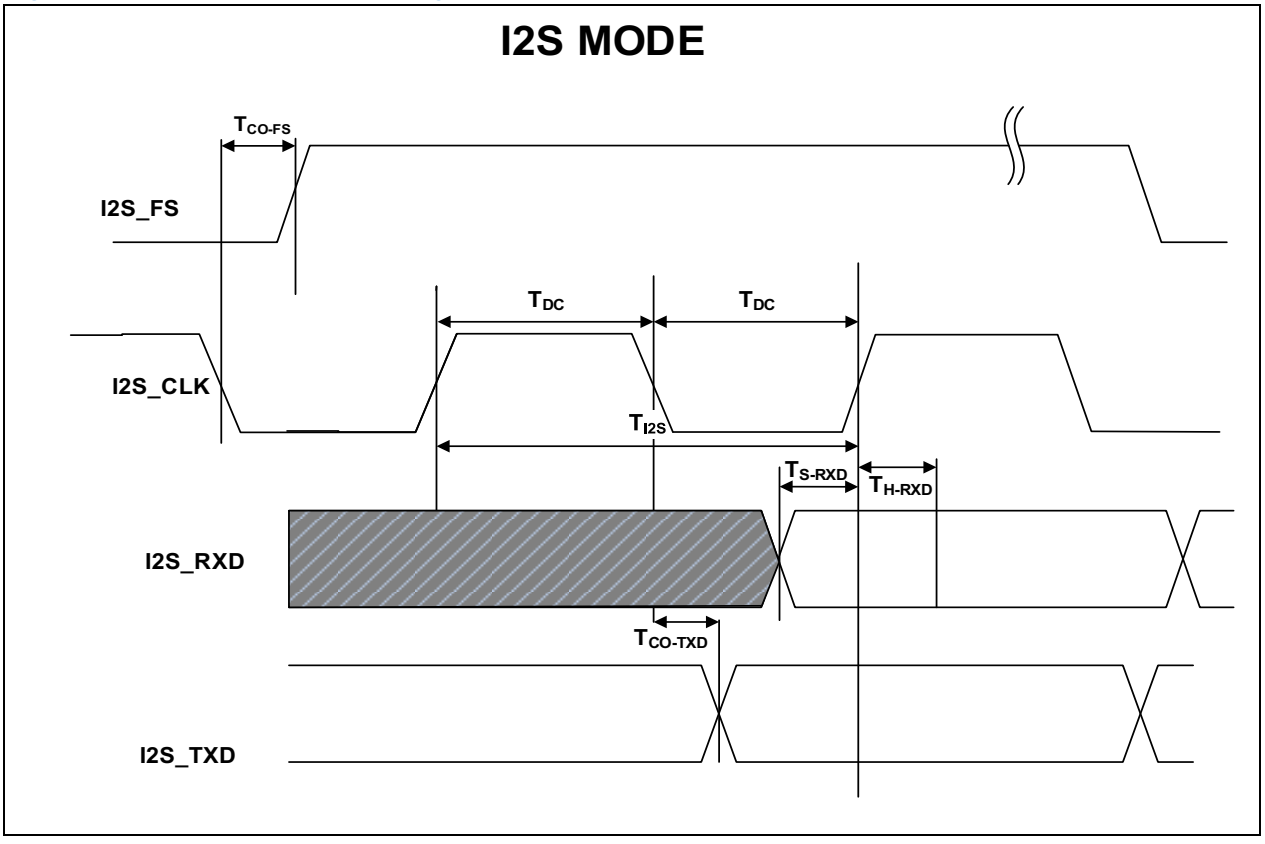


Figure 13 I²S master port timings in PCM short frame mode

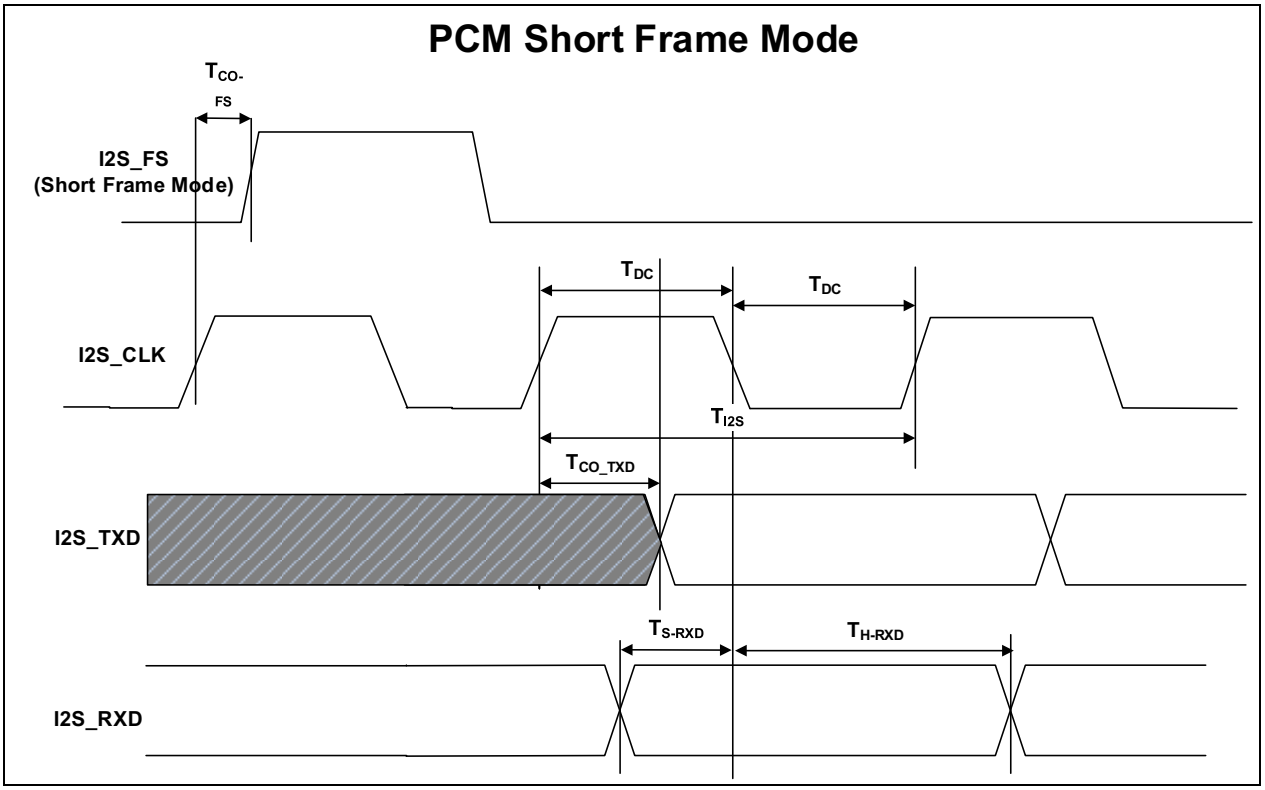
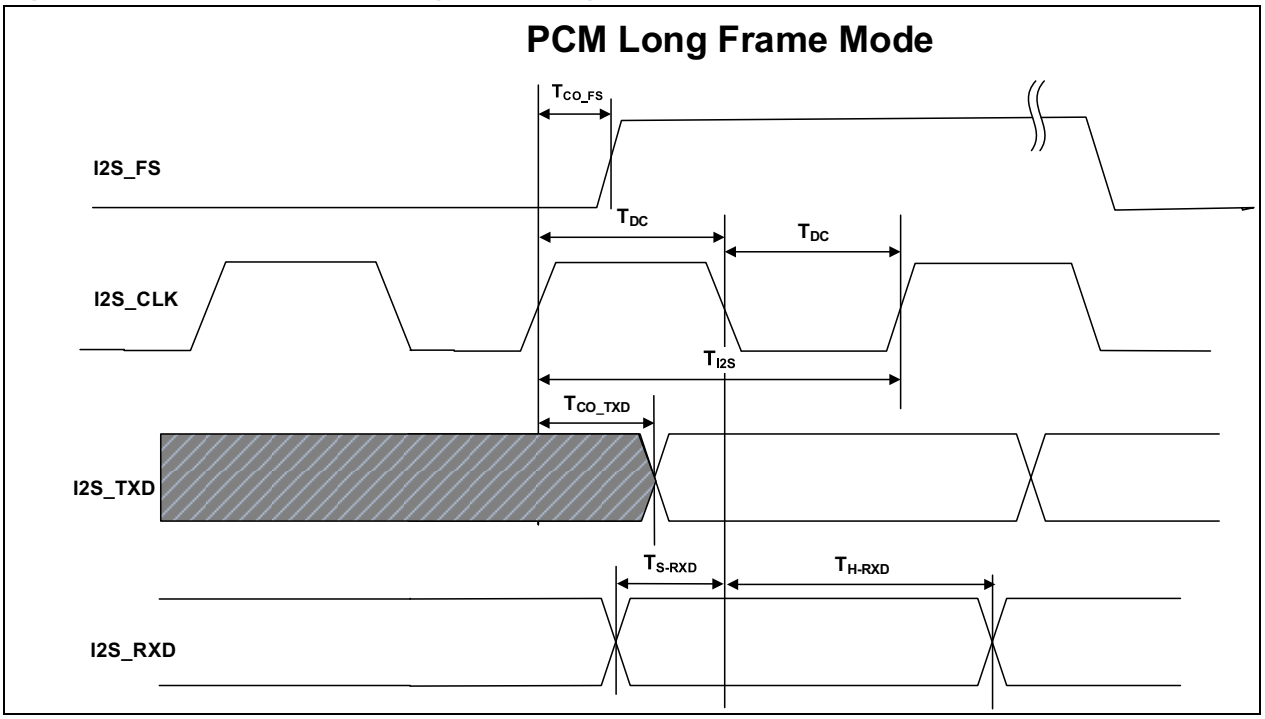


Figure 14 I²S master port timings in PCM long frame mode



4.5.1.2 I²S slave mode AC specification

Table 21 I²S slave mode AC timing parameters

Symbol	Parameter	Min	Max	Unit	Figure	Notes
T_{DC}	Clock Duty Cycle	40	60	%	Figure 15, Figure 16, Figure 17	
T_{I2S}	Clock Frequency	–	9.6	MHz	Figure 15, Figure 16, Figure 17	
T_{S-RXD}	Setup for RXD with respect to the I²S CLK active edge.	18	–	ns	Figure 15, Figure 16, Figure 17	1, 2, 3, 4
T_{H_RXD}	Hold for RXD with respect to the I²S CLK active edge.	0	–	ns	Figure 15, Figure 16, Figure 17	1, 2, 3, 4
T_{S-FS}	Setup for FS with respect to the I²S CLK active edge.	5.1	–	ns	Figure 15, Figure 16, Figure 17	1, 2, 3, 4
T_{H_FS}	Hold for FS with respect to I²S CLK active edge.	5.1	–	ns	Figure 15, Figure 16, Figure 17	1, 2, 3, 4
T_{CO_TXD}	Tco of TXD with respect to I²S CLK active edge at the host	3.3	29.2	ns	Figure 15, Figure 16, Figure 17	1, 2,3, 4
T_{CO-FS}	Tco of TXD with respect to FS at the host	3.3	29.2	ns	Figure 15, Figure 17	1, 2, 3, 4, 5

NOTE:

1. Active edge refers to the mode configuration.
2. For I2S mode:
   a. I2S_TXD – SoC launches data after falling clock edge.
   b. I2S_RXD – SoC latches data on rising clock edge.
3. For PCM mode SoC:
   a. I2S_TXD – SoC launches after rising clock edge.
   b. I2S_RXD – SoC latches data on falling clock edge.
4. PCM Mode has two different modes, Short Frame Mode and Long Frame Mode:
   a. Short Frame Mode – Master asserts I2S-FS one clock before it drives data.
   b. Long Frame Mode – Master asserts I2S_FS and data on the same clock.
5. TCO-FS does not apply to I2S mode and PCM-short frame mode.

Figure 15 I²S slave port timing parameters in I2S mode

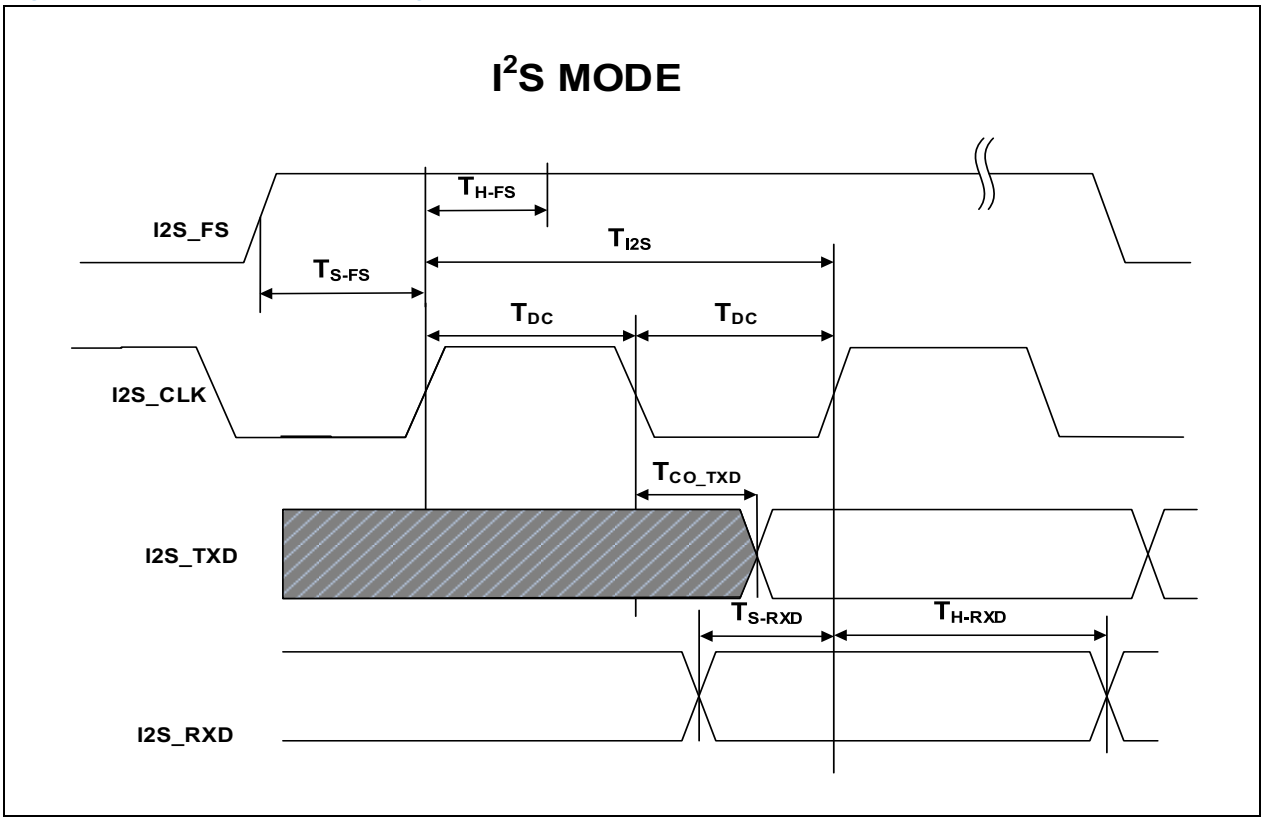


Figure 16 I²S slave port timing parameters in PCM short frame mode

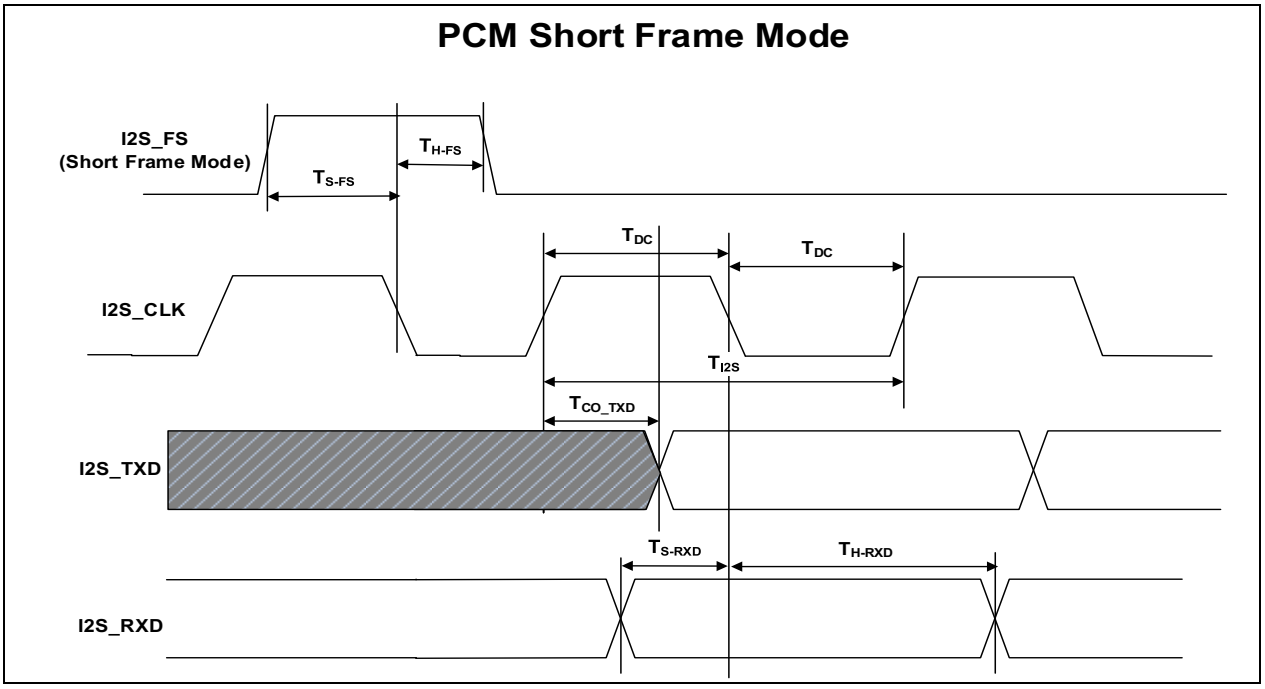
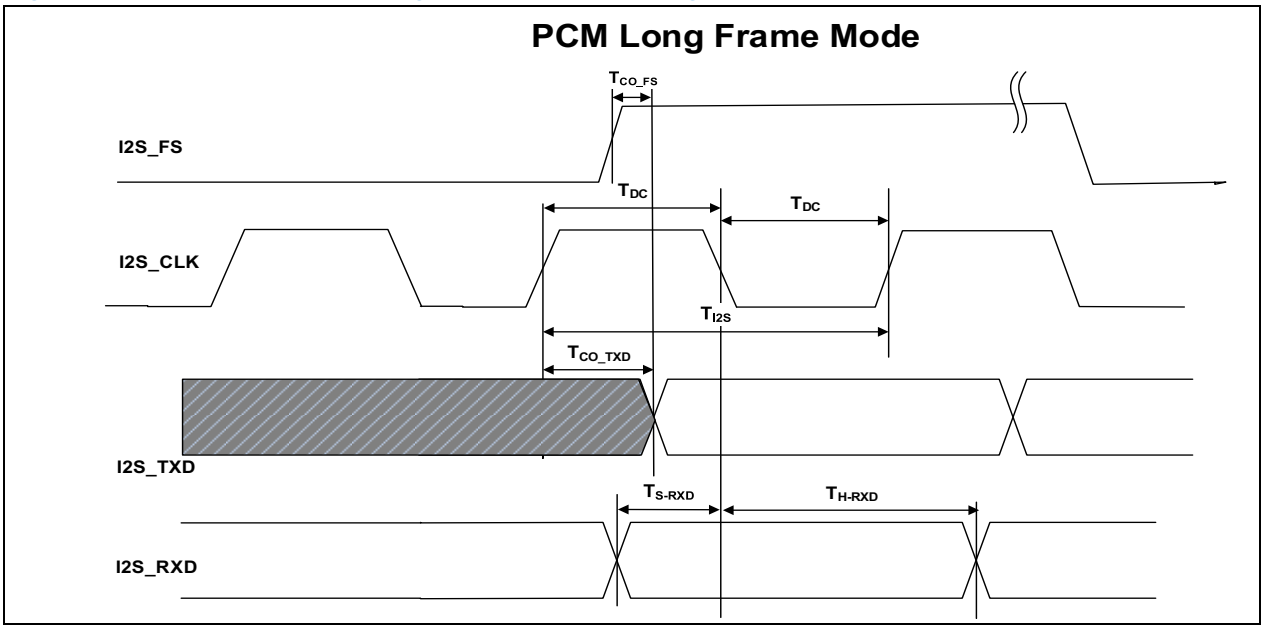


Figure 17 I²S slave port timing parameters in PCM long frame mode



4.5.2 I²S DC specifications

For I²S DC specifications not listed in Table 22, refer to GPIO buffer DC specifications listed in Table 28.

Table 22 I²S buffer DC specification

Symbol	Parameter	Min	Typ	Max	Unit	Notes
VOH	Output high voltage	0.8 * VDD	–	–	V	Measured at IOH maximum.
VOL	Output low voltage	–	–	0.2 * VDD	V	Measured at IOL maximum.

4.6 SPI interface

An SPI interface is available on pins 51, 53, 55, 57, and 59. The interface has two available chip selects.

- In a single-frame transfer, the SoC supports all four possible combinations for the serial clock phase and polarity.
- In multiple frame transfer, the SoC supports SPH=1 and SPO= 0 or 1.
- The SoC may toggle the slave select signal between each data frame for SPH=0.
- 25 MHz Master mode, 16.67 MHz slave mode.

The SoC contains four SPI ports: SPI 0, 1, 2, and 3.

Table 23 SPI ports overview

Port #	Mode	Nominal voltage	Max frequency
0 to 3	Master and slave	1.8 V	25 MHz (master mode) 16.67 MHz (slave mode)

Table 24 SPI modes

Port #	SPO	SPH
0	0	0
1	0	1
2	1	0
3	1	1

Note: SPO and SPH can be configured by SSP Control Register CTRL1 (SSCR1).

4.6.1 SPI master AC specification

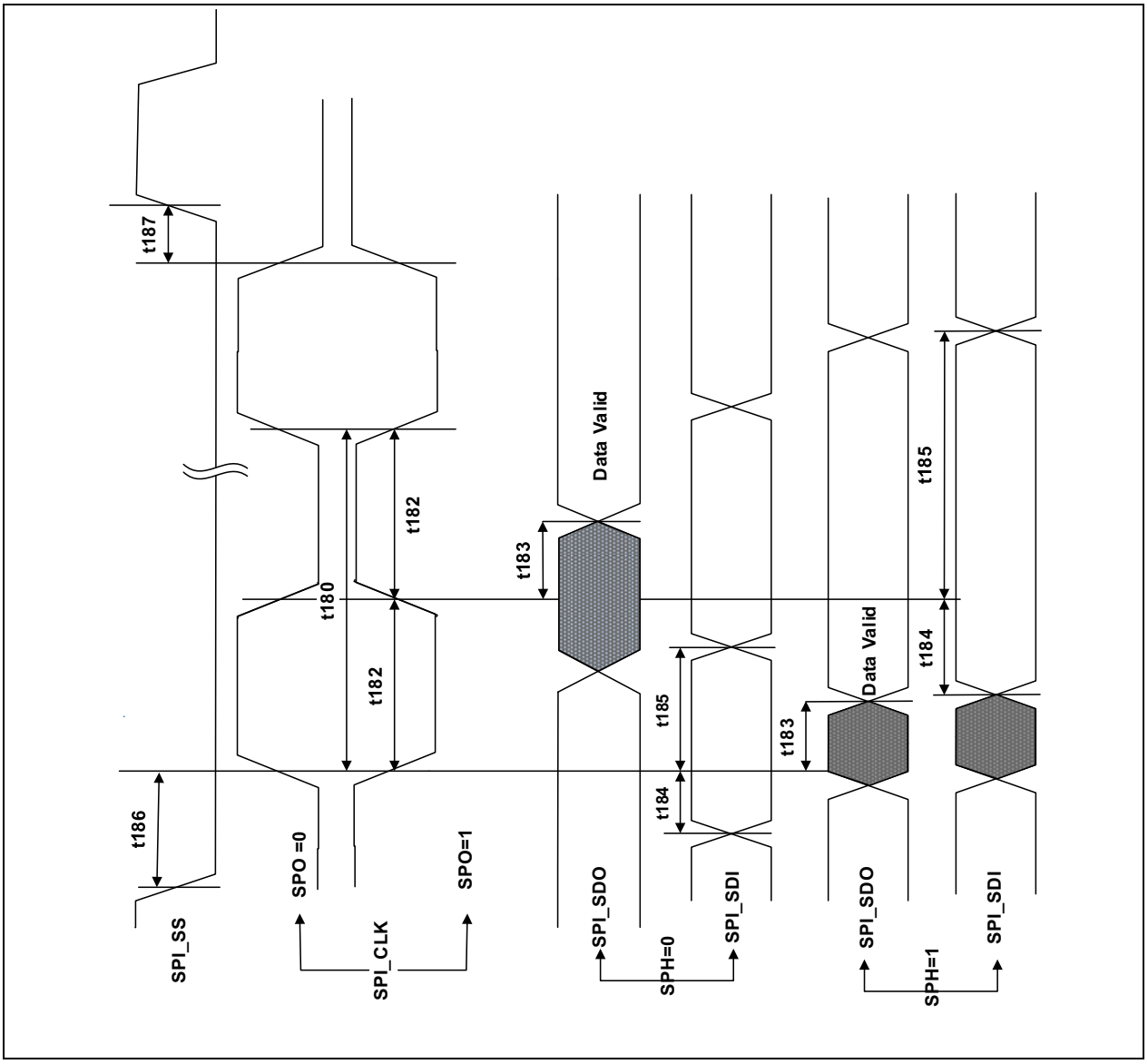
Table 25 SPI master AC timings

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t180	Serial clock frequency		25	MHz	Figure 18	
t182	SPI clock duty cycle at the host	45	55	%	Figure 18	
t183	Tco of SPI_SDO (SPI_MOSI) with respect to serial clock edge at the host.	0	5.4	ns	Figure 18	3
t184	Setup of SPI_SDI (SPI_MISO) with respect to the serial clock edge at the host.	5.2	–	ns	Figure 18	3
t185	Hold of SPI_SDI (SPI_MISO) with respect to serial clock edge at the host.	14.3	–	ns	Figure 18	3
t186	Setup of SPI_SS assertion with respect to serial clock edge at the host.	5.2	–	ns	Figure 18	3
t187	Hold of SPI_SS deassertion with respect to serial clock edge at the host.	14.3	–	ns	Figure 18	3
T_{RISE}/T_{FALL}	Maximum rise/fall time	0.85	10	ns		1
T_{RISE}/T_{FALL}	Maximum rise/fall time	0.6	3	ns		2

NOTE:

1. Based on:
   a. Trace length of up to six inches
   b. Board impedance of 25–75 ohm.
   c. Total maximum far end capacitance of 40 pF (4 loads at 10 pF per load)
   d. Measured from 35–65%
2. Based on:
   a. Trace length of up to four inches
   b. Board impedance of 25–75
   c. Total maximum far end capacitance of 10 pF
   d. Measured from 35 to 65%
3. Clock edge depends on the mode being used on SPI ports.

Figure 18 SPI master timing



4.6.2 SPI slave AC specification

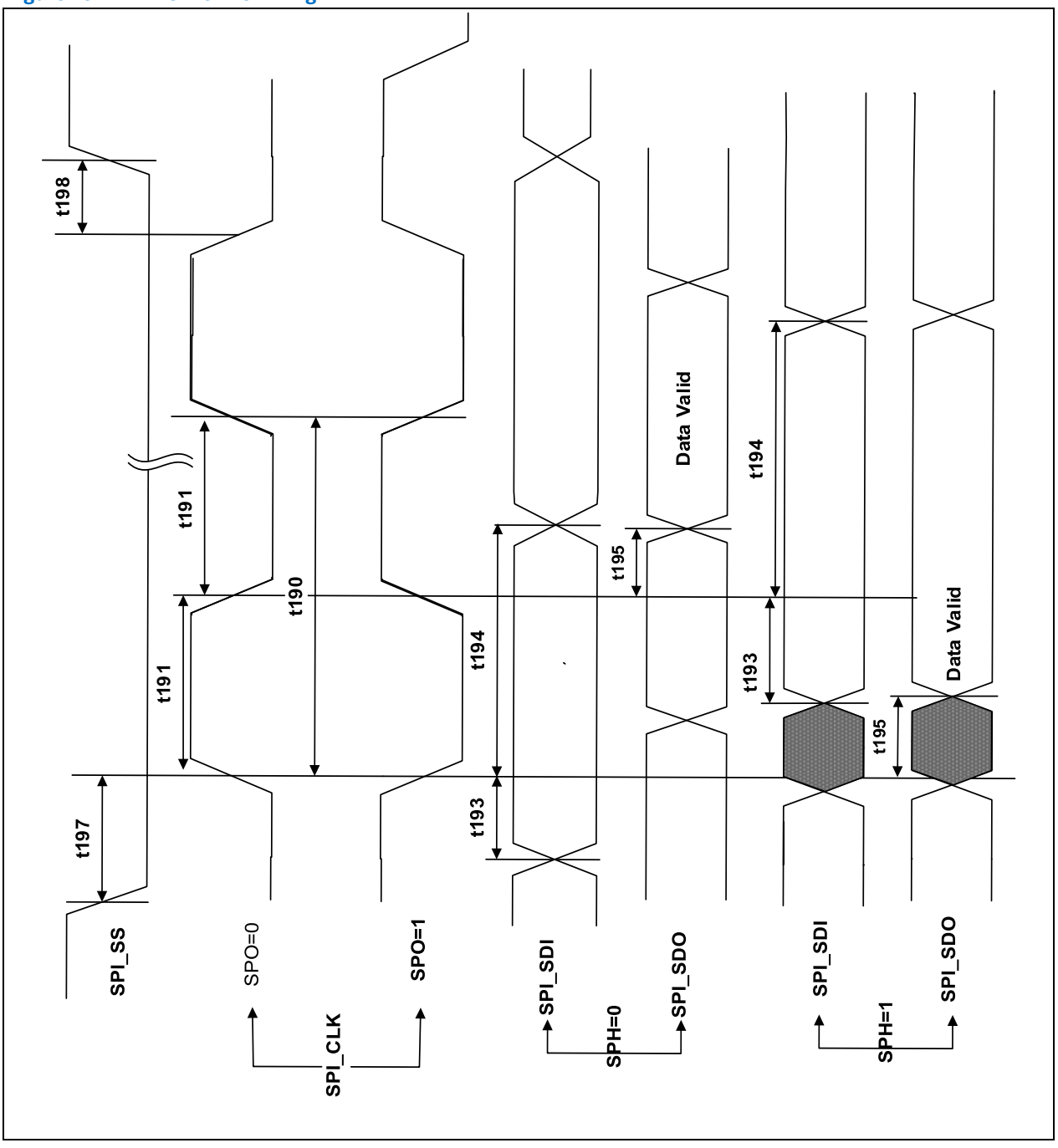
Table 26 SPI slave AC timings

Symbol	Parameter	Min	Typ	Max	Unit	Figure	Notes
t190	Serial clock frequency	–	–	16.67	MHz	Figure 19	
t191	Clock duty cycle	45	–	55	%	Figure 19	
t193	Setup of SPI_SDI (MOSI) with respect to the serial clock edge.	5	–	–	ns	Figure 19	1
t194	Hold of SPI_SDI (MOSI) with respect to serial clock edge.	5	–	–	ns	Figure 19	1
t195	TCO of SPI_SDO (MISO) with respect to the serial clock edge.	5	–	21	ns	Figure 19	1
t197	Setup of SPI_SS assertion with respect to serial clock edge.	5	–	–	ns	Figure 19	1
t198	Hold of SPI_SS deassertion with respect to serial clock edge.	5	–	–	ns	Figure 19	1

NOTE:

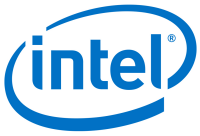
1. Clock edge depends on the mode being used.

Figure 19 SPI slave timing



4.6.3 SPI DC Specification

For SPI master and slave DC Specifications, refer to Table 28.



4.7 GPIO

A number of general purpose I/Os are available on the external interface. These are found on pins: 24, 25, 26, 28, 30, 32, 34, 42, and 48. Some of these serve alternate functions of interrupts for external sensor support. All the interfaces listed in Section 4 (I2C, I2S, UART, etc.) if not used, can be turned into general purpose I/Os.

When the pin mode is chosen as GPIO, it can be programmed as an output or input. When programmed as an input, a GPIO can serve as an interrupt or wake source. Inputs have programmable pullups or pulldowns. Pullup value can be 2, 20, or 50 kohm. I^2C pins also have an additional 910 ohm value. When in general purpose mode, input GPIO signals enter a glitch filter by default, before reaching the edge detection registers.

To ensure that a pulse is detected by the edge detection register, the pulse should be five clock cycles long.

- 100 ns for a 50 MHz clock when SoC is in S0 state.
- 260 ns for 19.2 MHz clock when SoC is in S0i1 or S0i2 State.
- 155.5 µs for 32 kHz clock (RTC) when SoC is in S0i3 State.

Most GPIO-capable pins are configured as GPIO inputs during the assertion of all resets, and they remain inputs until configured otherwise. As outputs, the GPIOs can be individually cleared or set. They can be preprogrammed to either state when entering standby. Output drive is ±3 mA.

GPIO buffer is used across various interfaces on the SoC such as, GPIOs, I^2C, I^2S, MIPI PTI, SPI, SDIO, SVID, UART, PWM, CAMERA SB, JTAG and ULPI, FAST-INT, OSC_CLK_OUT, OSC_CLK_CLTRL.

4.7.1 GPIO AC specification

GPIO buffer AC specifications, AC specifications apply to signals when used as GPIOs.

Table 27 GPIO buffer AC specifications

Symbol	Parameter	Min	Max	Unit	Notes
T_{RISE}	Maximum rise time	5	45	ns	1, 2
T_{FALL}	Maximum fall time	5	45	ns	1, 2

NOTE:

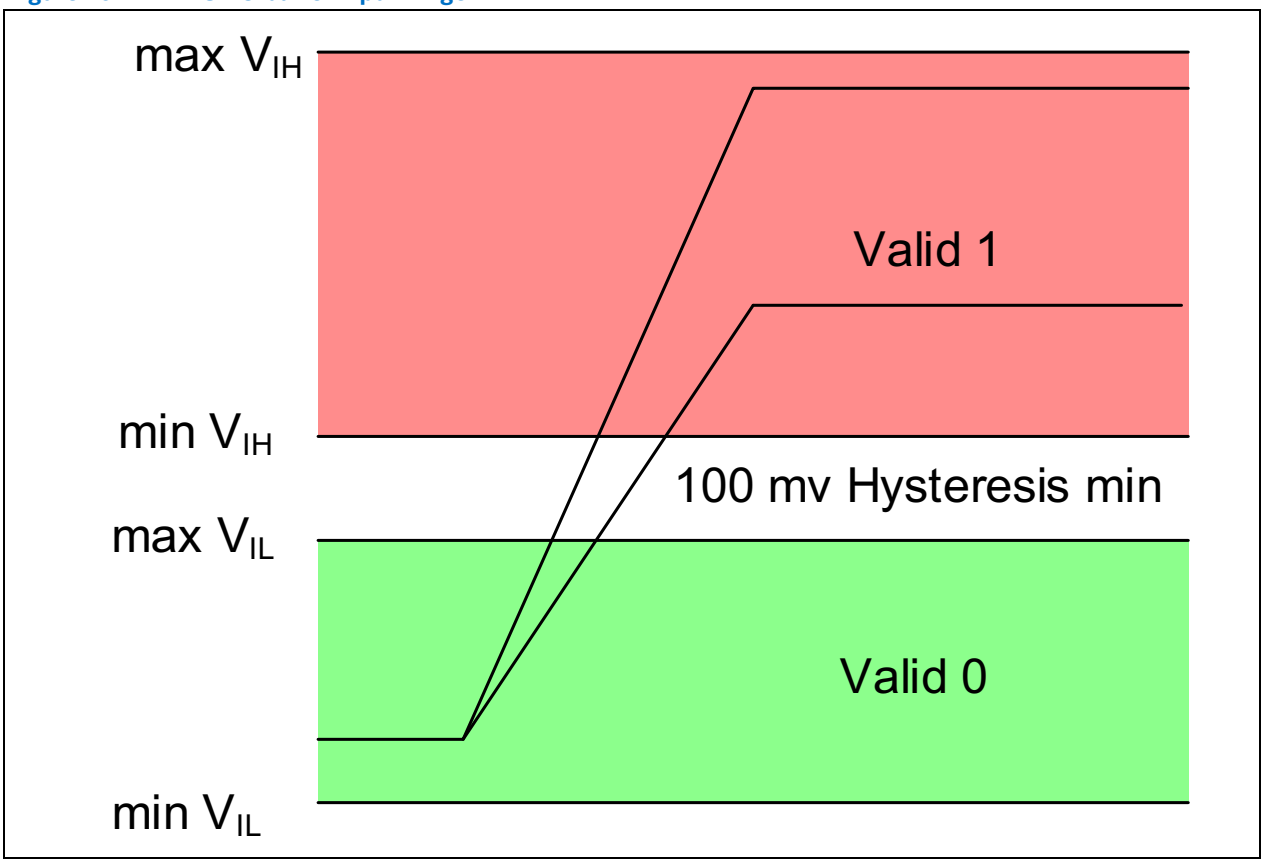
1. Based on total maximum capacitance of 150 pF.
2. Measured from 10 to 90%.

4.7.2 GPIO DC specification

Table 28 GPIO buffer DC specifications

Symbol	Parameter	Min	Typ	Max	Unit	Notes
V_{DD}	Supply voltage	1.71	1.8	1.89	V	
V_{IH}	Input high voltage	0.65 * VDD	–	–	V	
V_{IL}	Input low voltage	–	–	0.35 * VDD	V	
V_{OH}	Output high voltage	VDD – 0.45	–	–	V	Measured at IOH maximum.
V_{OL}	Output low voltage	–	–	0.45	V	Measured at IOL maximum.
$V_{HYSTERESIS}$	Input hysteresis	100	–	–	mv	
IOH/IOL	Current at V_{OL}/V_{OH}	-3	–	3	mA	
ILI	Input leakage current	-2	–	2	µA	
ILO	Output leakage current	-2	–	2	µA	
C pin	Input pin load capacitance	2	–	5	pF	

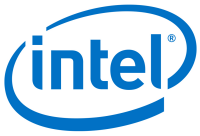
Figure 20 GPIO buffer input range



4.7.3 GPIO pullup and pulldown specification

Table 29 GPIO pullup and pulldown specification

Pullup and pulldown options	Tolerance	Notes
2 kohm, 20 kohm, 50 kohm	±30%	Available for all pins which can be used as GPIOs.
910 ohm	±30%	Available only for I^2C pins.



4.8 PWM

There are four available GPIO that can be configured as PWM outputs. These are found on pins 33, 35, 37, and 39. The PWM resolution is 8 bits.

The main PWM variables that control PWM output are:

- The PWM output frequency and duty cycle can be estimated by the equations:
  - Target frequency ~= 19.2 MHz * Base_unit value/256
  - Target PWM duty cycle ~= PWM_on_time_divisor / 256

Table 30 shows some examples of PWM programming.

Table 30 Intel® Edison PWM programming examples

Integer part of PWM_base_unit (bits 29:22)	Fractional part of PWM_base_unit (bits 21:8)	Decimal base unit value	Base unit type	PWM frequency (Hz)	PWM period (µs)	Bits of resolution	PWM steps
0000_0000b	00_0100_0000_0000b	0.0625	fractional	4,688	213	8	0.39%
0000_0000b	00_0010_0000_0000b	0.03125	fractional	2,344	427	8	0.39%
0000_0000b	00_0001_0000_0000b	0.015625	fractional	1,172	853	8	0.39%
0000_0000b	00_0000_1000_0000b	0.0078125	fractional	586	1,707	8	0.39%
0000_0000b	00_0000_0100_0000b	0.00390625	fractional	293	3,413	8	0.39%
0000_0000b	00_0000_0010_0000b	0.00195325	fractional	146	6827	8	0.39%
0000_0000b	00_0000_0001_0000b	0.0009765625	fractional	73.2	13,653	8	0.39%
0000_0000b	00_0000_0000_1000b	0.00048828125	fractional	36.6	27,307	8	0.39%
0000_0000b	00_0000_0000_0100b	0.000244140625	fractional	18.3	54,613	8	0.39%
0000_0000b	00_0000_0000_0010b	0.0001220703125	fractional	9.2	109,227	8	0.39%
0000_0000b	00_0000_0000_0001b	0.00006103515625	fractional	4.6	218,453	8	0.39%
0000_0000b	00_0000_0010_0001b	0.00201416015625	fractional	151	6619	8	0.39%

The SoC consists of four PWM drivers with programmable frequency and duty cycle, operating at 1.8 V.

The operating frequency can be set from 0 to 9.6 MHz. The frequency selection is based on system clock (19.2 MHz). Refer to the SoC technical reference manual for the PWM registers configuration.

4.8.1 PWM AC specification

For PWM AC specifications, refer to Table 27.

4.8.2 PWM DC specification

For PWM DC specifications, refer to Table 28.

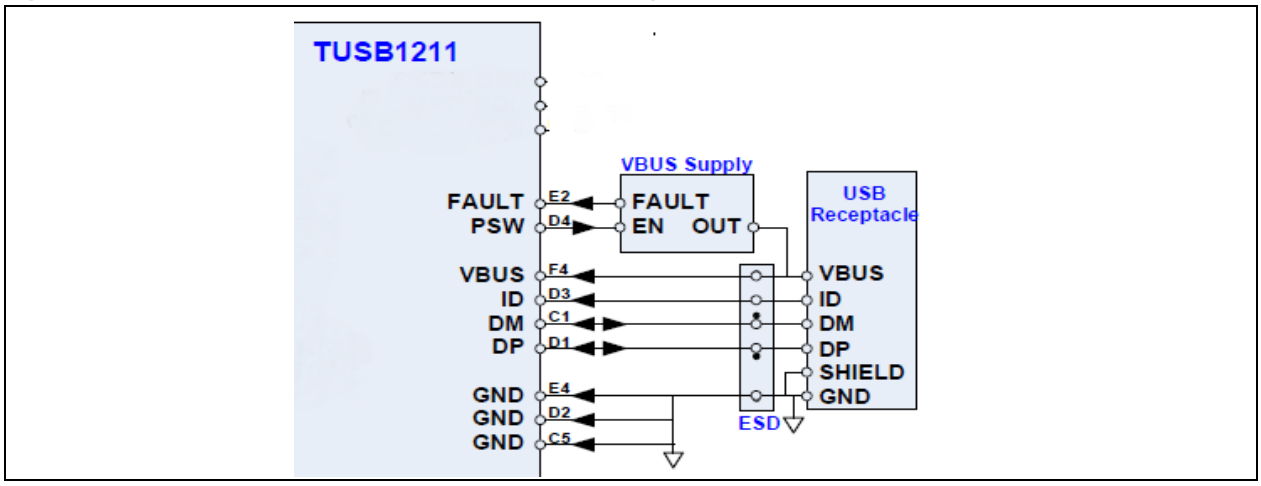
4.9 USB

The Intel® Edison Compute Module has a single USB 2.0 interface. This interface is the primary method for downloading code. The interface is found on pins: 3, 16, 18, and 20.

Note: The USB_VBUS signal should be applied to pin 20. This signal is only used to alert the Intel® Edison that it has been connected to a host port.

The Intel® Edison compute module does not use power applied to pin 20 to power the device. Intel® Edison is designed to support OTG, using the ID signal on pin 3. The OTG power function is offboard. Two signals PSW (pin 21), and FAULT (pin 19) from the ULPI controller are used to control the external power switch and monitor the overcurrent condition on VBUS. Figure 21 shows the configuration of the **external hardware**.

Figure 21 Example Intel® Edison external USB design



The PSW signal is active high and controls an external VBUS power switch or charge pump.

The FAULT signal is active low. **FAULT should be connected to GND if USB host mode is not used**.

The SoC contains one ULPI interface with labeled ULPI which is used for OTG operation.

The SoC features a 12-bit UTMI+ Low Pin Interface Specification (ULPI) interface with a USB 2.0 OTG v2.0 transceiver that is a discrete component external to the SoC on the platform.

4.9.1 Standards specification compliance

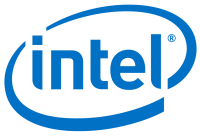
- On-the-Go Supplement to the USB 2.0 Specification, Revision 2.0 (May 2009).

4.10 System reset

Intel® Edison has two system reset signals PWRBTN# (pin 17) and RESET_OUT# (pin 36). The PWRBTN# pin is an active low input which can cause the Intel® Edison module to transition into and out of sleep, or cause a power-off , depending on the configuration of the software. RESET_OUT# is open-drain, and driven low by default out of system reset. This signal can be used by external hardware to indicate system reset. The Intel® Edison I/Os are undefined until RESET_OUT# transitions high.

4.11 Software recovery (FWR_RCVR and RCVR_MODE)

The Intel® Edison board has two signals, used during boot, to cause the SoC to force firmware and OS image download. These are for factory use only.



4.12 Power input and output

There are five power rails on the Intel® Edison: VSYS, 3.3 V, 1.8 V, USB_VBUS, and V_VBAT_BKUP. VSYS is the only input power rail to the Intel® Edison module, and the voltage range is 3.15 to 4.5 V. USB_VBUS is a standard USB VBUS input from 4.75 to 5.25 V. This rail is not used to power the device; it is only used by the USB ULPI PHY to determine a host device has attached to the Intel® Edison device. The 3.3 and 1.8 V are power outputs from the Intel® Edison module that source a maximum of 100 mA each.

DCIN is a signal that indicates whether the Intel® Edison device is being powered from a battery or from an external power source. DCIN also sets the voltage level required on VSYS in order to boot. When DCIN is floating or tied to ground, the voltage on VSYS MUST rise from 2.5 to 3.5 V in 100 ms, otherwise the boot is aborted. When the boot is aborted, power must be cycled below 2.5 V. If DCIN is connected to VSYS, the Intel® Edison device will start to boot when VSYS is above 2.5 V for 100 ms.

Note: The absolute minimum voltage to assure Wi-Fi and Bluetooth functionality is 3.15 V.

4.13 V_VBAT_BKUP

The PMIC has a dedicated charging subsystem for a backup battery supply that could be either a rechargeable coin cell batteries or super-capacitors. This backup subsystem allows for interruption of the main supply for a short period of time, such as changing a main system battery. The external cell should be connected to pin 23, V_VBAT_BKUP. The PMIC can be programmed with a charge voltage of 2.5, 3.0, 3.15, or 3.3 V. The charge current is programmable to 10, 50, 100, or 500 µA. The default settings are 2.5 V and 10 µA.

To change these settings, the BBCHGRCFG register (Table 31) will need to be modified. To read and write the 8-bit value of the BBCHGRCFG register from within the Linux kernel using the following functions that are provided by the drivers/platform/x86/intel_scu_pmic.c driver:

```
// Read BBCHGRCFG into bbchgrcfg_value
uint8_t bbchgrcfg_value;
int ret;
ret = intel_scu_ipc_ioread8(0x52, &bbchgrcfg_value);
if (ret)
error;

// Set BBCHGRCFG to NEW_BBCHGRCFG_VALUE
int ret;
ret = intel_scu_ipc_iowrite8(0x52, NEW_BBCHGRCFG_VALUE);
if (ret)
error;
```

D5, D6, and D7 should remain 0.

Table 31 BBCHGRCFG - Backup battery charger and main battery charger IC configuration registers

Register name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
BBCHGRCFG	R/W	RSVD		CHGDIS_ACT	BBCHGI[1:0]		BBCHGV[1:0]		BBCHGEN	0x01	0x52 (0x5E)

Bit	Name	Function	Default
D[7:6]	RSVD	Reserved.	00
D5	CHGDIS_ACT	**Charger IC disable pin action.** Set according to how the main battery charger IC responds to the CHGDIS pin being asserted. What this bit's tile value is set to depends entirely on charger IC selection. This bit is read only. 0 = The main battery charger IC is disabled when asserted. (Power-path is not available.) 1 = Only the battery charging function within the main battery charger IC will be disabled when asserted. (Power-path is still available.)	0 (NVM)
D[4:3]	BBCHGI[1:0]	Sets the backup supply charger current limit. 00 = 10 µA 01 = 50 µA 10 = 100 µA 11 = 500 µA	00 (NVM)
D[2:1]	BBCHGV[1:0]	Sets the backup supply charging limit. 00 = 2.5 V 01 = 3.0 V 10 = 3.15 V 11 = 3.3 V	00 (NVM)
D0	BBCHGEN	0 = Disable charging of backup supply. 1 = Enable charging of backup supply.	1 (NVM)

Example implementation:

- Register setting: BBCHGRCFG=19
- Voltage: 2.5 V (default value)
- Current: 500 µA

- Charging current: 500 µA
- Discharge current (consumption): 8.0 µA
- Charge voltage: 2.5 V
- Minimum RTC retention voltage: 2.05 V
- Capacitance of supercap: 0.014F (PAS3225P2R6143/Taiyo Yuden)

- Theoretical backup times = 0.014F * (2.5 to 2.05) V / 8 µA = 787.5 s = 13 min
- Measured (actual) backup time = 15 min 20 sec
- Measured chargeup time (0 to 2.5 V) = 2 min 24 sec

4.14 Electrostatic discharge (ESD) specification

Table 32 ESD performance

Model	Passing voltages	Notes
Human body model (HBM)	±1 kV	
Charged device model (CDM)	±500 V	For all pins, other than mentioned below.
Charged device model (CDM)	±250 V	For USB3, HDMI, DSI, CSI, and LPDDR3 pins.

Note: Passing voltage applies to all signal and power pins.

§

5 Powering Intel® Edison

Intel® Edison may be embedded in a number of devices either battery powered, or AC wall powered. Therefore, Intel® Edison was designed not to support a specific power delivery method or specific battery chemistry and capacity range. This portion of the design is left to the end-user. With the interfaces available, smart battery coulomb counters and smart rechargers could be placed onto one of the available I^2C buses. Porting of the software to the specific bus would be the responsibility of the end-user.

5.1 Main power supply VSYS

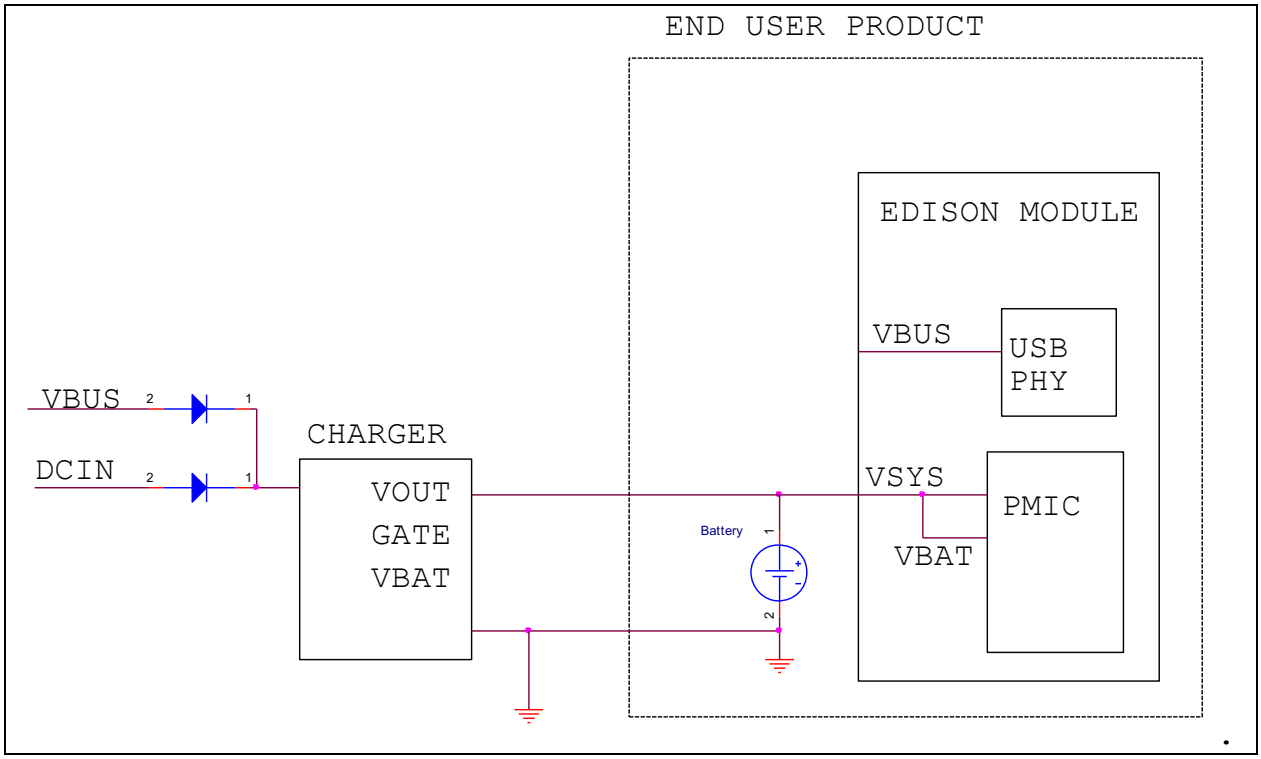
Intel® Edison uses VSYS (pins 2, 4, and 6) as the only power input path. Internal to Intel® Edison, this signal is also connected to the VBAT path. Application of power to VSYS is interpreted as a battery insertion and will cause Intel® Edison to boot. The VSYS power range is 3.15 min to 4.5 V max (see section 4.12). This allows VSYS to run off a standard lithium-ion battery. There are a number of possible power configurations for Intel® Edison, based on the size and cost sensitivity of the end-user's product.

5.2 Lithium-polymer battery direct attach

The simplest battery power connection to Intel® Edison is to directly attach a battery to VSYS, as shown in Figure 22. We do not recommend this configuration as the charging system cannot distinguish between charge current and total system current.

Note: If Intel® Edison is prevented from booting by holding the power button signal PWRBTN# (pin 17) low, then the power input can be assumed to be the battery charging current.

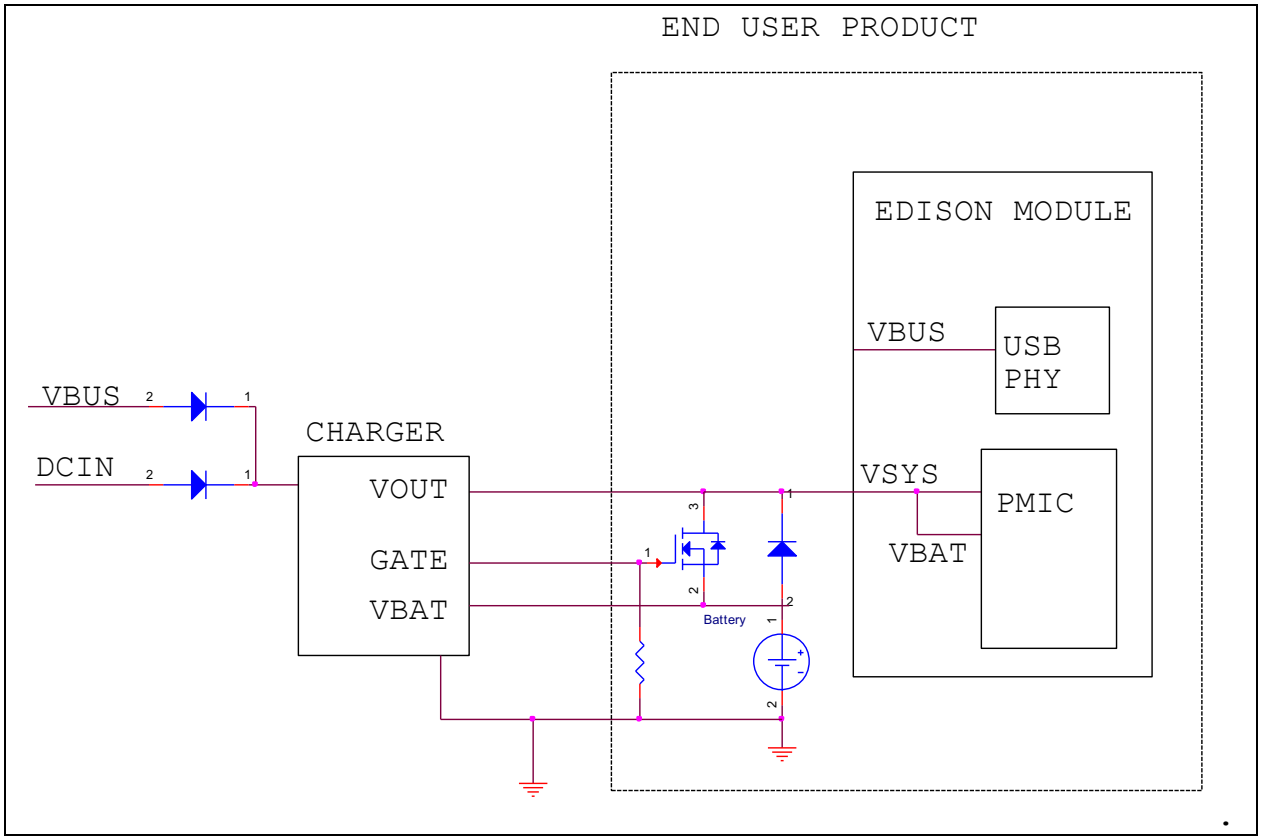
Figure 22 Example Intel® Edison lithium-polymer battery direct attach



5.3 Lithium-polymer battery with diode or FET isolation

In this configuration, Intel® Edison will see a diode drop during normal operation. This configuration allows the system to boot even with a dead battery. This configuration requires an additional pin to the external world to control the charging. Replacing the diode with a PFET, and pulling the gate low will remove the diode drop power loss. The external charger would require a gate control pin for an external PFET. This function is found on rechargers like the Texas Instruments* BQ24073.

Figure 23 Example Intel® Edison lithium-polymer battery with FET isolation



5.4 Connection to USB VBUS

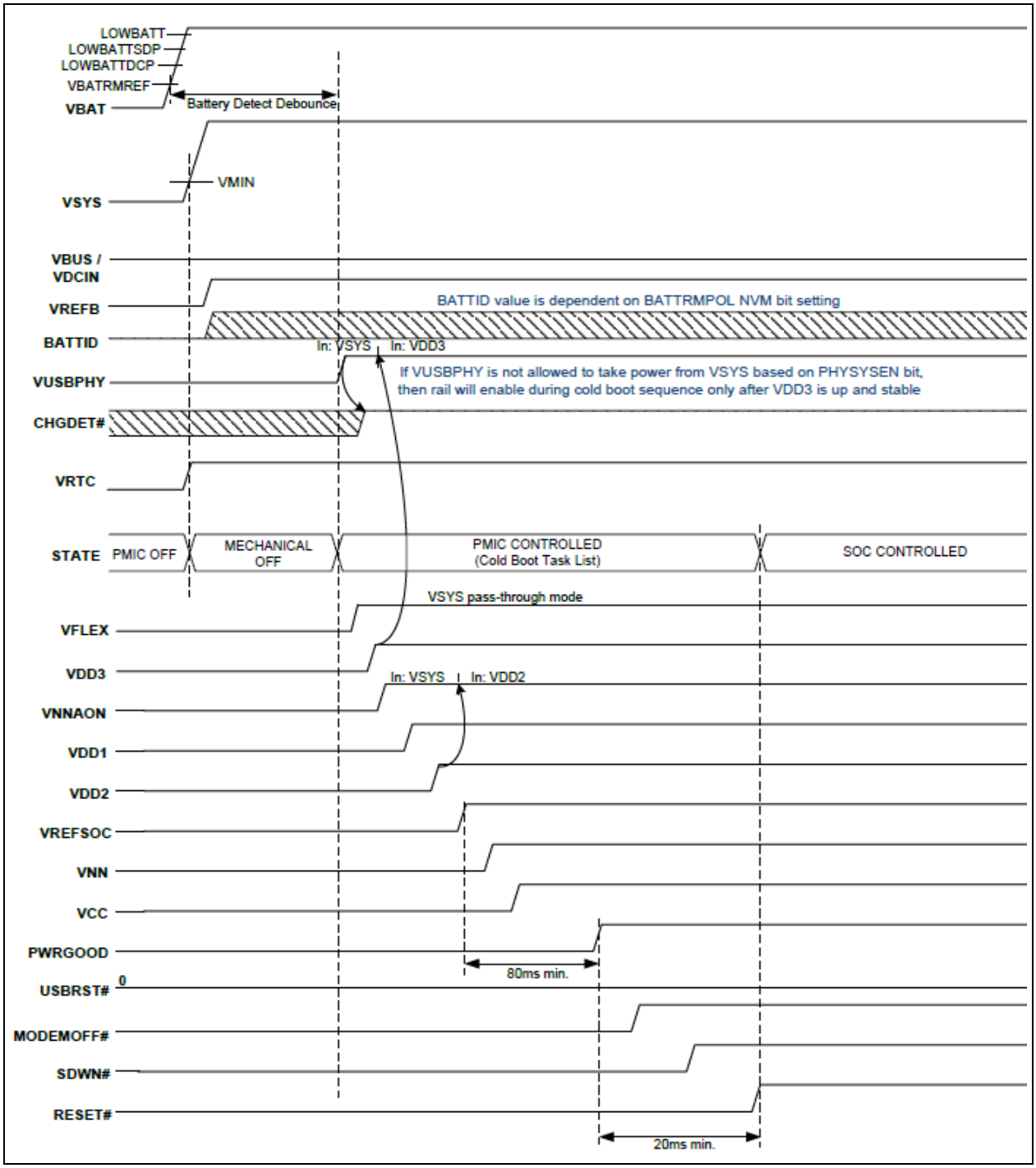
It is ***not*** possible to run an Intel® Edison compute module directly off a USB power supply. The maximum input voltage to VSYS should be less than 4.5 V. The USB power supply specification (4.75 to 5.25 V) exceeds the safe operational range of Intel® Edison. USB power must be down converted with an LDO or small buck switching converter or a recharger like the Texas Instruments* BQ24074.

5.5 Cold boot sequence

Figure 24 shows the signal sequence from a cold boot.

Note: The reset# signal in Figure 24 is accessible on the 70-pin connectors as RESET_OUT# on pin 36.

Figure 24 Intel® Edison cold boot sequence



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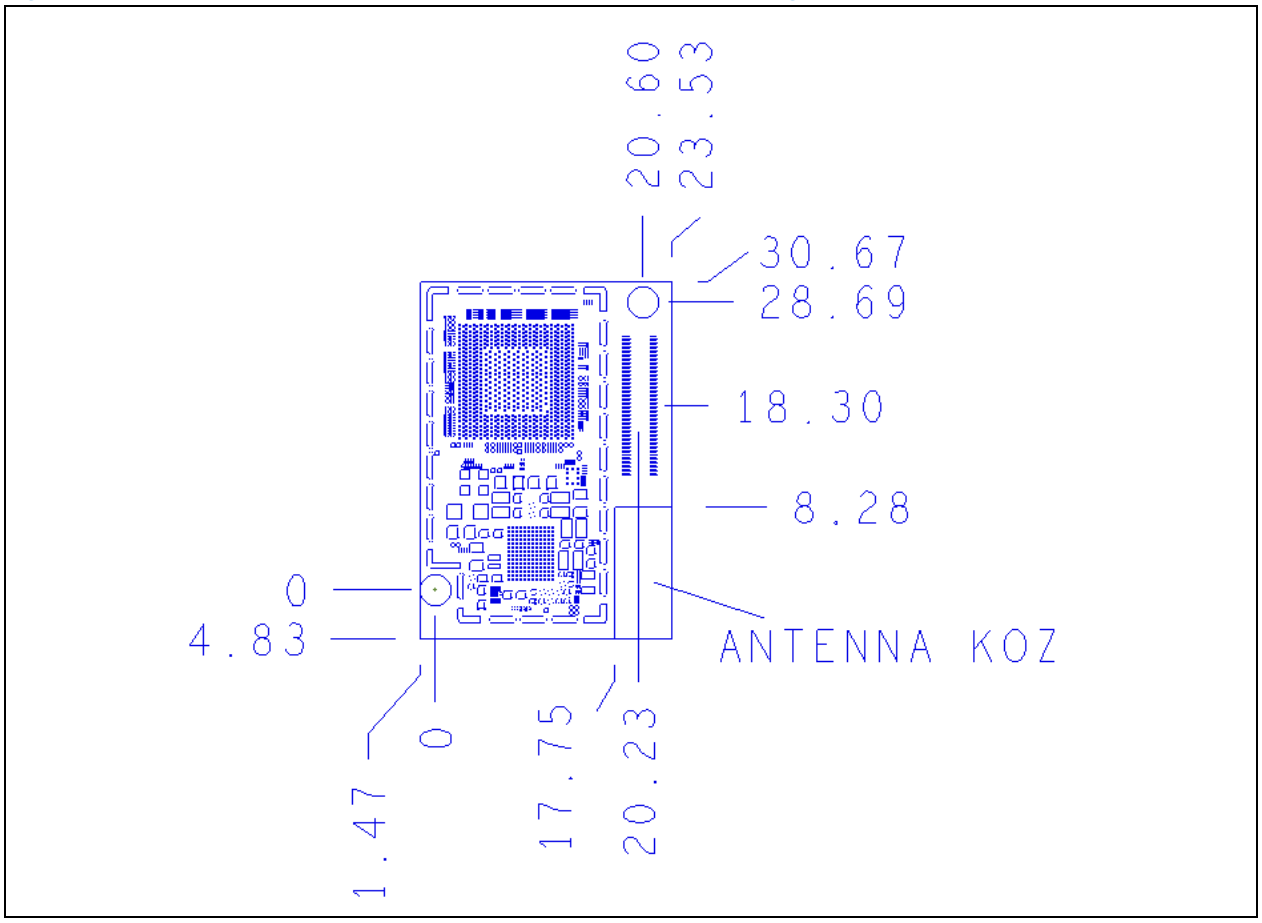
6 Intel® Edison Mechanicals

Figure 25 shows the dimensions (in millimeters) of the Intel® Edison module.

Figure 25 Intel® Edison mechanical dimensions (top view through PCB)



The location for pin 1 of the 70-pin connector is the lower right corner of the connector. The location of pin 2 is across the connector at the lower left corner. Consequently, the location of pin 69 is the upper right corner of the connector and the location of pin 70 is the upper left corner of the connector. The center point of the connector is specified in the drawing.

The diameters of the two mounting holes are 2.0 mm. Screw heads should be less than 3.0 mm. The mounting holes were designed for a T1.6 mm screw.

Note: The onboard chip antenna is in the lower right corner of Intel® Edison is denoted in the drawing as "ANTENNA KOZ". User-designed expansion PCBs should not place components or metallic objects close to the antenna keepout zone.

Most components on both sides of Intel® Edison will be covered with a shield. The height of the shields on both sides of the board, as measured from the surface of the PCB, is approximately 1.5 mm. The PCB thickness is specified as 0.8 mm ±0.1 mm. Therefore, the total maximum thickness of Intel® Edison is 3.9 mm. These values are verified with DVT modules.

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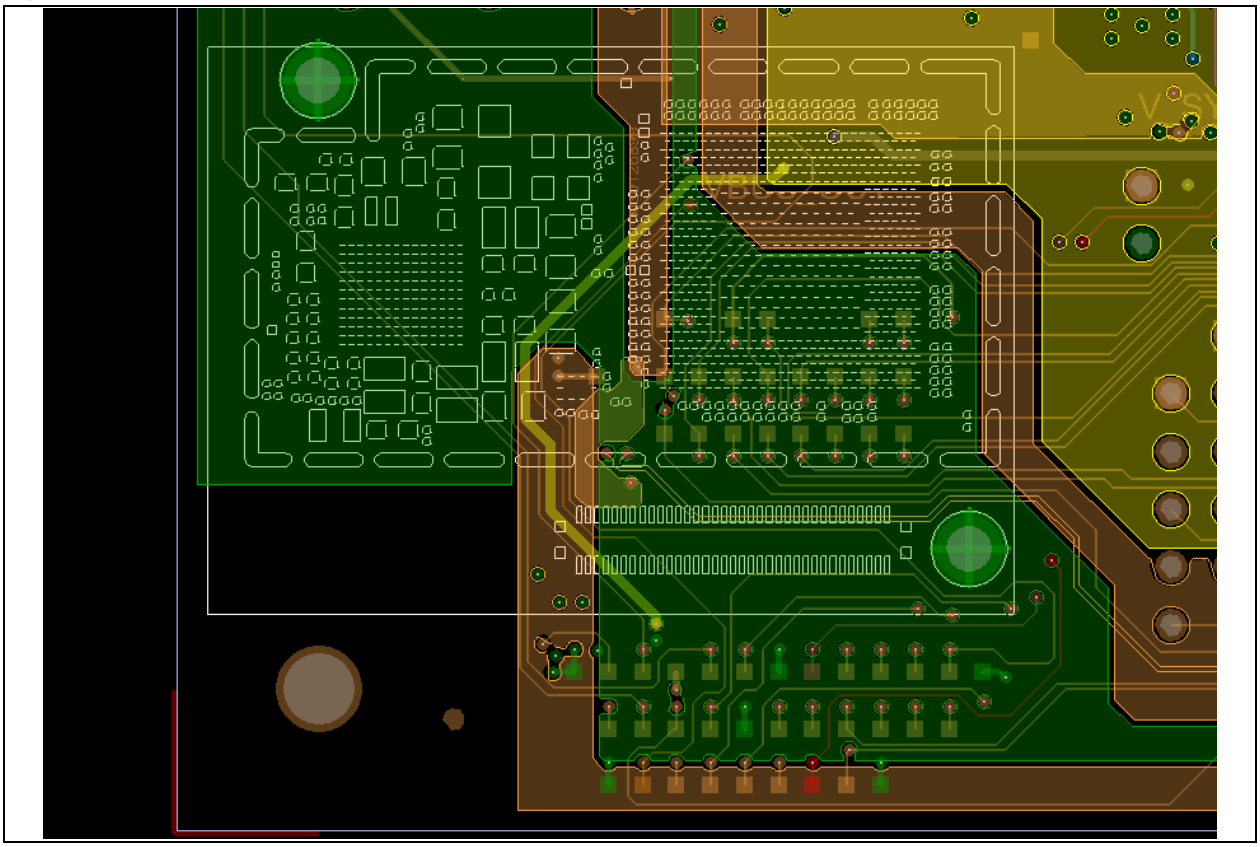
7 Layout

7.1 Antenna keepout

The area under and around the antenna should be kept free of all components, routes, and ground plane. An example is shown here with the Intel® Edison Compute Module DXF in white with antenna keepout shown in the Intel® Edison Kit for Arduino* trace layers. See Figure 26.

Figure 26 Area around antenna



7.2 Layout SD card, I2S, SPI, I2C

Table 33 Layout SD card

Signal parameter	Metric (mm)	Standard (mils)
Total length L1	0.254 to 101.6 mm	10 to 4000 mils
DATA/CMD/CTRL to CLK maximum pin-to-pin length mismatch	±2.54 mm	±100 mils
Minimum main route spacing ratio	60 × 60 µm. 1:1 trace width/space.	
CLK to DATA/CMD/CTRL matching	±200 mils	
Characteristic single ended impedance	42 to 45 ohm (±10%)	
Load capacitance	2 to 5 pF	

Note: 1) For SPI, total length is 6000 mils.
2) For I^2C, total length is 8000 mils.

7.3 Layout DXF

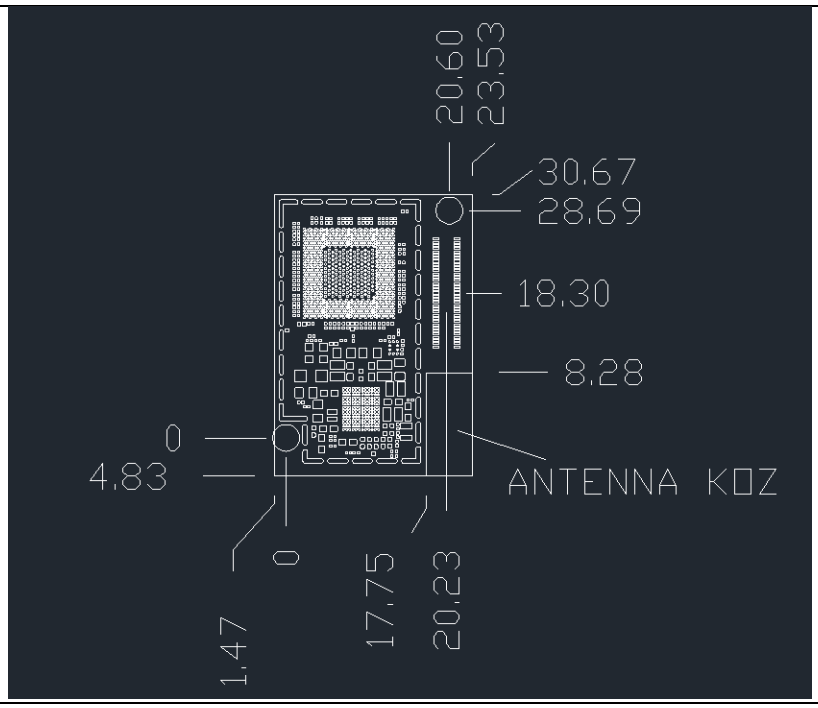
The following embedded file is a DXF of the Intel® Edison compute module as shown in Figure 27.

Note: KOZ stands for “keepout zone”.

Figure 27 Layout DXF

Package

(See attachment: *Edison_DVT.dxf*)



7.4 Layout PTC EMN files

Figure 28 PTC EMN graphic

H38489-005_R02 _emn.emn

(See attachment: *H38489-005_R02 _emn.emn*)

H38489-005_R02 _emn.emp

(See attachment: *H38489-005_R02 _emn.emp*)

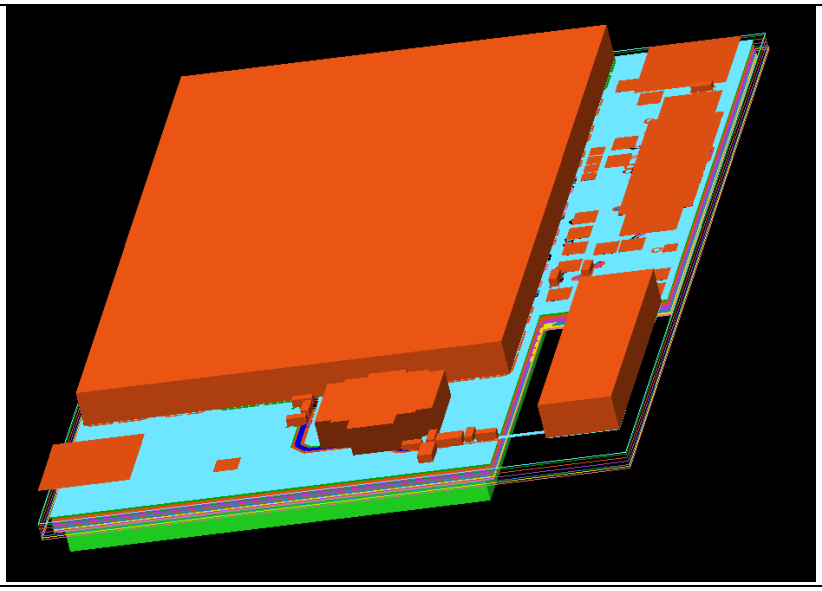
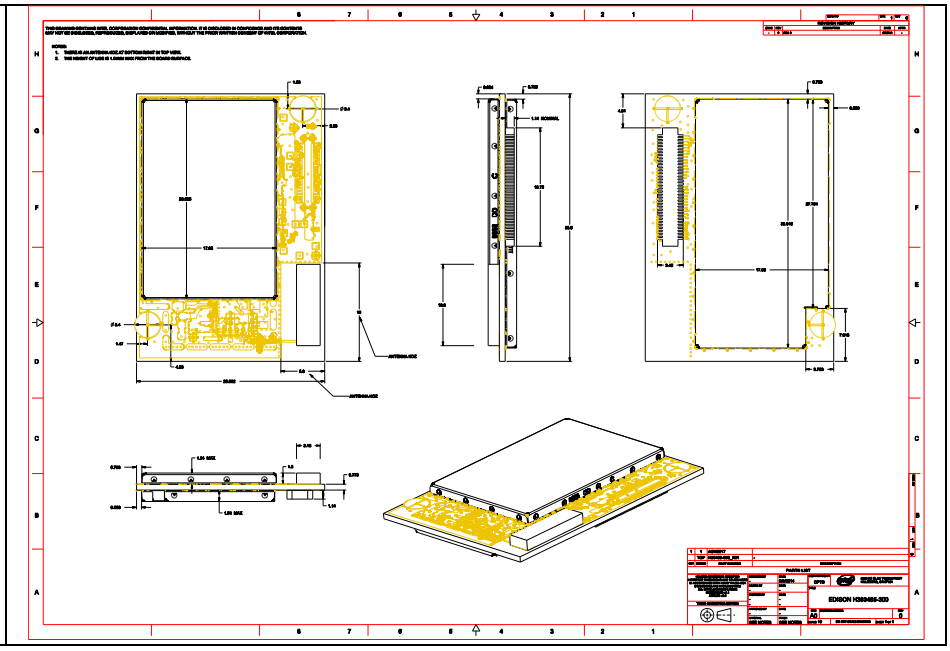


Figure 29 H383485-300

Adobe Acrobat Document

(See attachment: *H383485-300.pdf*)



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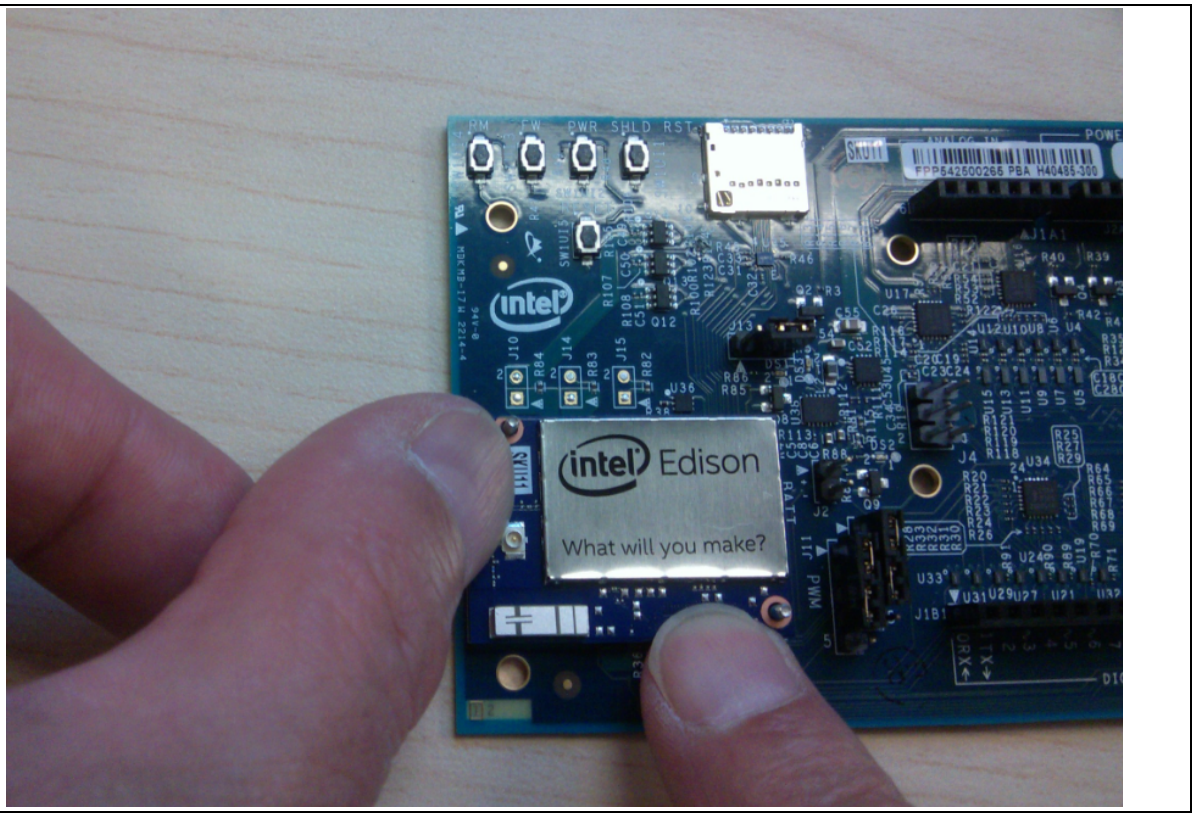
8 Handling

When assembling an Intel® Edison Compute Module to a carrier board such as the Intel® Edison Arduino* board, handle the Intel® Edison Compute Module by the PCB edges. Avoid holding or exerting pressure to the shields. To mate the Intel® Edison Compute Module to the Intel® Edison Arduino* board, apply pressure directly above the connector and to the left corner, as shown in Figure 30.

Figure 30 Inserting an Intel® Edison module



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