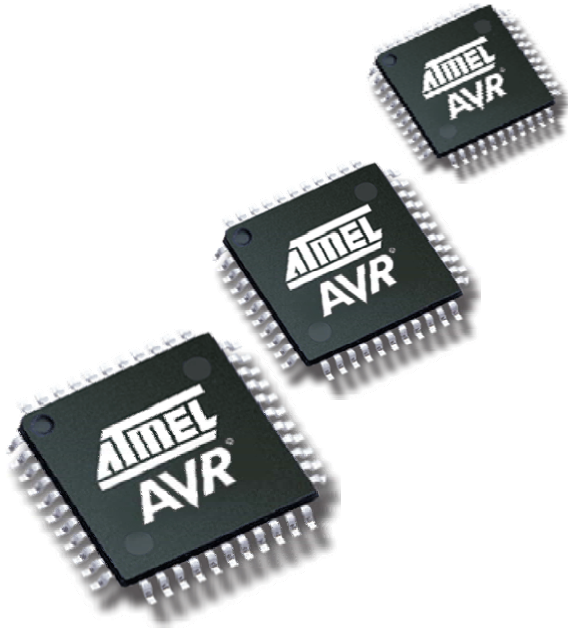
XMEGA Introduction

XMEGA™

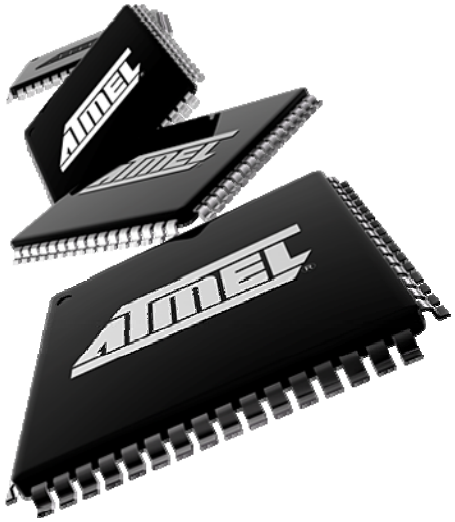
- XMEGA targets
  - Leadership on Peripheral Performance
  - Leadership in Low Power Consumption
  - Extending AVR market reach



- XMEGA AVR family
  - 44 - 100 pin packages
  - 16K – 512K devices
  - Launch: Q1 2008

- #1 in Low Power, Integration and Peripheral Performance

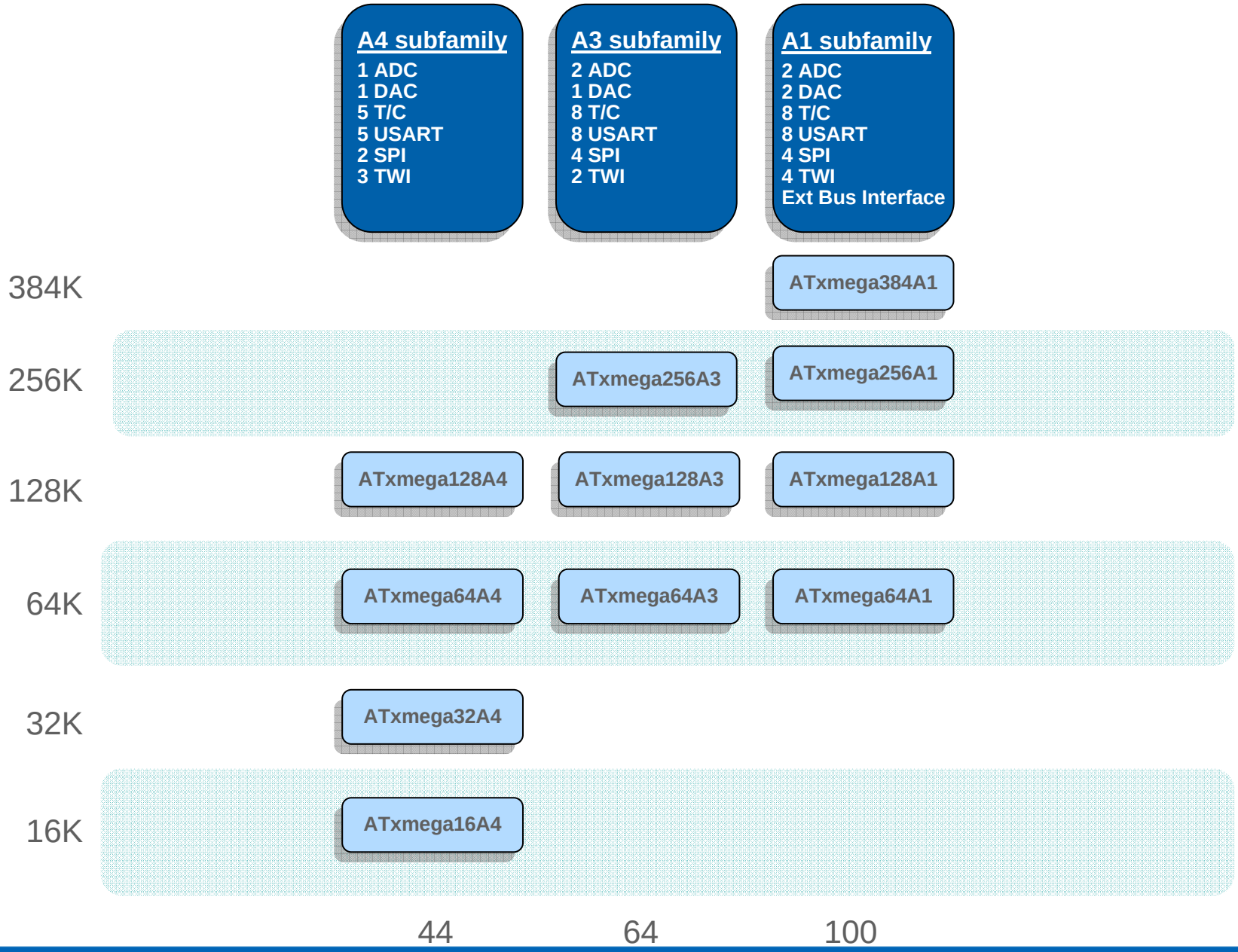
- Performance Boost
  - DMA Controller
  - Multilevel Interrupt Controller
  - Event System
  - 32 MHz @ 2.7 V
  - 12 MHz @ 1.8 V



- Advanced Peripherals
  - Analog
    - 12-bit fast ADC
    - 12-bit DAC
    - Multiple Analog Comparators
  - Digital
    - 16-bit Timers, high-speed PWM
    - TWI Interface
      - I2C and SMbus compliant
    - USART, SPI, IrDA

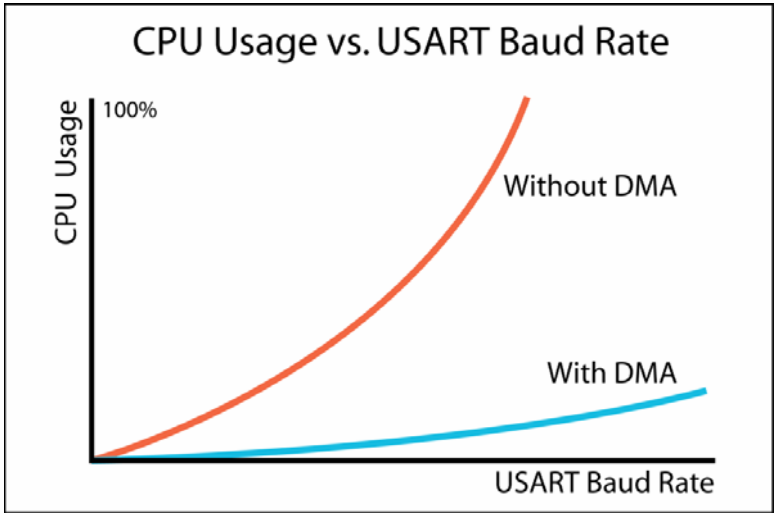
- Lowest power consumption
  - 2 µA with Watchdog, BOD and Real Time Counter running
  - picoPower technology
  - New watchdog timer
  - New brownout detector

XMEGA A Family



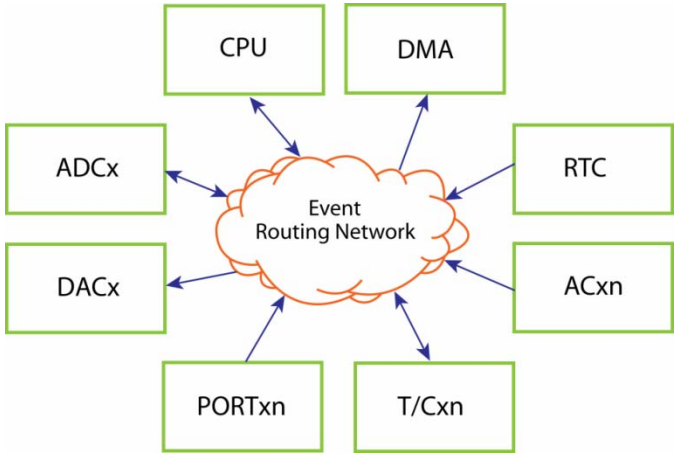
DMA Controller

- Highlights
  - 4 channels
  - Optional interrupt at end of transaction
  - 1, 2, 4 or 8 byte Burst modes
    - Programmable priority between channels
- DMA transfers done when core is not using the data bus
  - Very few instructions use the databus on AVR
    - load, store; in, out; push and pop only instructions using databus
- Allows high-speed data transfer
  - Memory <-> Peripheral
  - Memory -> Memory
  - Peripheral -> Peripheral



Event System

- Highlights
  - 8 Event Routing Channels
  - CPU and DMA independent operation
  - Quadrature Decoding
  - Digital Filtering



- Peripherals specify how to generate events
  - Ex: Pin change, Timer overflow, ADC complete
- Peripherals specify how to use events
  - Ex: Increment Timer, Output signal, Start ADC conversion
- Reduces the use of interrupts
- Ensures control of critical functions

Interrupt Controller

- Highlights
  - 4 levels of interrupts
  - Non Maskable Interrupts - NMI
    - Can be enabled, but not disabled by SW
    - System functions. Ex: Oscillator stop
  - High, Medium and Low level selectable for each source
    - Priorized interrupts will interrupt lower level interrupts
- Round robin priority possible for low level interrupts
  - Ensures all interrupts are serviced
- High priority interrupts are executed immediately
- Ensures immediate service of important interrupts
  - Even when MCU is heavily loaded

picoPower technology

- All the highlights of picoPower
- Enhanced Watchdog timer
  - 1 kHz ULP clock source
  - Windowed watchdog
- Sampled BOD
  - Trade-off reaction time vs Power Consumption
- 16-bit Real Time Counter
  - Programmable wake-up time up to 18 Hours
- EEPROM and Flash Power Down
- Event system and DMA reduces time in active mode significantly

Highest Integration

- Accurate RC and PLL
  - Eliminates need for external resonator in most systems
- VREF with less than 1% variation
  - No need for external VREF
- Low power highly programmable BOD
  - No need for external BOD for increased accuracy or reduced power
- DAC
  - Eliminates need for external components
- Crypto engine
  - Enables high-speed encrypted data transfer
- Reduces BOM cost and area significantly
- Increases market reach

Memories

- Flash
  - Application area for main program
  - Boot area for bootloader
  - Application Table area for fail safe EEPROM emulation
  - Built in CRC Check
- EEPROM
  - EEPROM on all devices
  - Byte and page accessible
  - Optional memory mapped
- SRAM
  - Internal on all devices
  - Optional external on some devices
    - Up to 16 MB directly addressable
    - Optional multiplexed address and data
- SDRAM
  - Optional external on some devices
    - Up to 128 Mbit directly addressable
    - 4-bit and 8-bit supported
- **Typical memory setup**

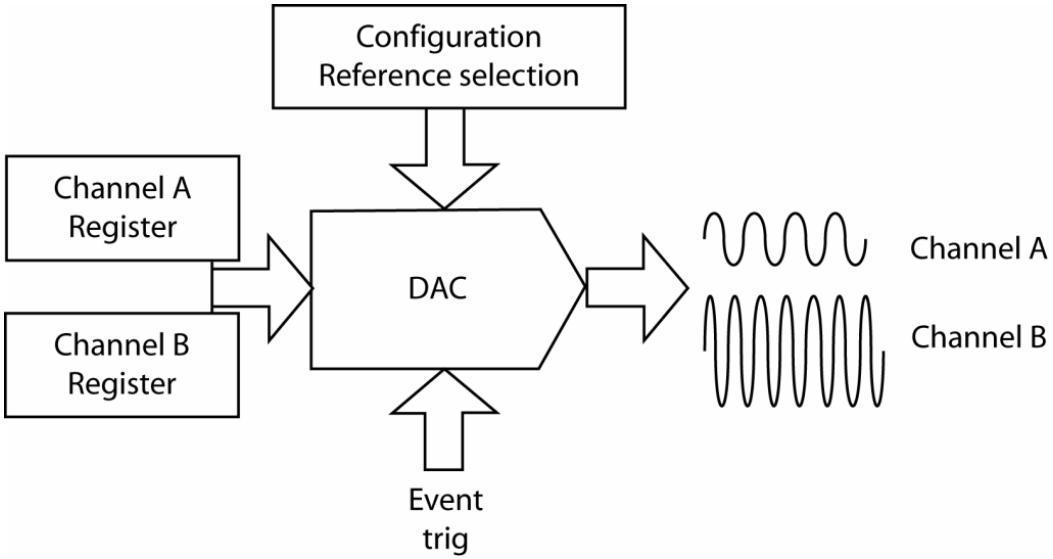
Flash	SRAM	EEPROM
16K + 4K	2K	512
32K + 4K	4K	512
64K + 4K	4K	1K
128K + 8K	8K	2K
256K + 8K	16K	2K

Analog to Digital Converter

- 12 bit, 2 Msps ADC
- Single or continuous conversion modes
- 8- or 12-bit accuracy SW selectable
  - 8-bit result has 2.5 µs propagation delay
  - 12-bit result has 3.0 µs propagation delay
- Connected to Event System and DMA Controller
- Internal and External reference voltages
- Interrupt/event on compare result
  - Interrupt if lower or equal
  - Interrupt if higher or equal
- Interrupt/event on conversion complete
- Improves throughput by 3000X and accuracy by 4X

Digital to Analog Converter

- Features:
  - 12 Bit resolution
  - Up to 1 Msps conversion rate, 1 µs settling time
  - Flexible conversion range (from 0V to up to VCC-0.3V)
  - Connected to Event System and DMA Controller
  - 1 continuous or 2 S/H outputs



Analog Comparators

- Selectable power vs. speed
  - 30 ns propagation delay in high-speed mode (130 µA)
  - 20 µA current consumption in low-power mode (500 ns)
- Selectable hysteresis
  - 0, 20mV, 50mV selectable
- Flexible input selections
  - Input pin (several options for each AC)
  - Output of DAC module
  - Bandgap voltage reference
  - Scaled version of VCC
- Flexible interrupts and events generation
- Window compare function by combining 2 comparators
- Possible to have comparator output on a pin

Timer/Counters

- Multiple 16-bit Timer/Counters in each device
  - 4 (2) Output Compare on each Timer/Counter
  - 4 (2) Input Capture on each Timer/Counter
  - Inverted and Non-inverted Outputs
  - Flexible event and interrupt generations
  - Multiple Frequency and PWM generation modes
- High-Resolution Extension
  - Increase waveform generation resolution by 4x (2 bit)
  - High frequency PWM gives lower cost
- Advanced Waveform Extension
  - Dead-Time Insertion
  - Fault Protection
  - Perfect for 3-phase inverters, power applications and variable frequency drives

Multiple Serial Communication Modules

- USART
  - Full duplex asynchronous or synchronous operation
  - SPI master mode
  - Baud Rate Generator with fractional divider
    - UART frequency crystals not needed
  - IrDA 1.4 physical compatible up to 115.2 kbps
- SPI – Serial Peripheral Interface
  - Full duplex, three-wire synchronous data transfer
- TWI – Two Wire Interface
  - I^2C and SMbus compliant
  - Fast data rate on slow chip clock
    - Clock / 10 for master operation
    - Asynchronous slave operation with no clock restrictions

XMEGA Schedule

Device	Eng Samples	Samples	Mass Prod
ATxmega128A1	Q1-08	Q1-08	Q2-08
ATxmega64A1	Q1-08	Q1-08	Q2-08
ATxmega256A3	Q2-08	Q3-08	Q4-08
ATxmega32A4	Q2-08	Q3-08	Q4-08
ATxmega16A4	Q2-08	Q3-08	Q4-08
ATxmega256A1	Q3-08	Q4-08	Q1-09
ATxmega128A3	Q3-08	Q4-08	Q1-09
ATxmega64A3	Q3-08	Q4-08	Q1-09