APPLICATION NOTE

ATA6836C/ATA6838C Open Load Detection

ATAN0013

References

- Atmel ATA6836C Datasheet
- Atmel ATA6838C Datasheet

Description

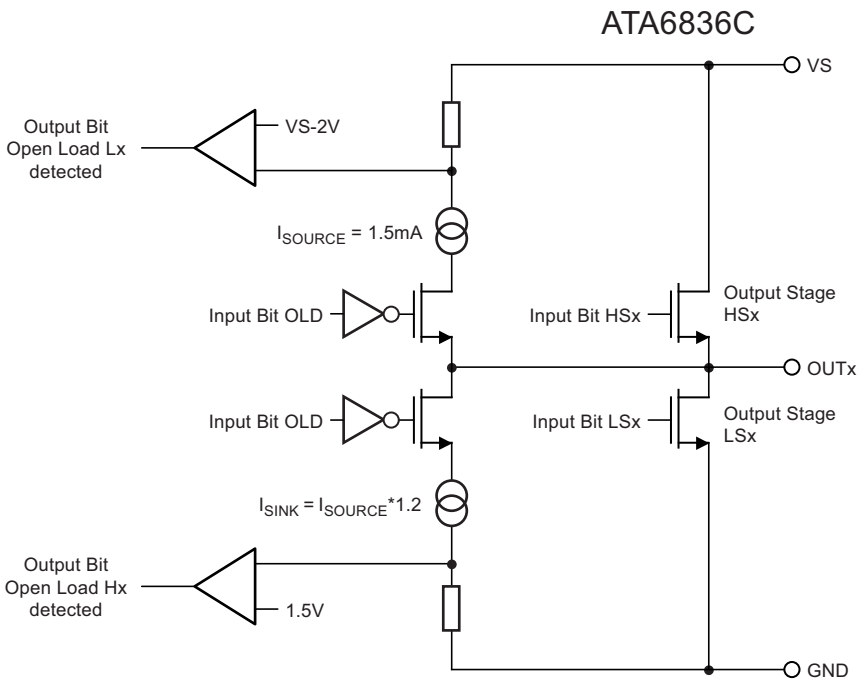
The Atmel® ATA6836C/ATA6838C high-voltage drivers employ internal protection circuitry to protect against short-circuit, overtemperature, undervoltage and open-load. The open-load detection feature will be discussed in this application note.

1. Open-Load Detection

1.1 Circuit Overview

Open-load monitoring of the high-voltage driver IC is controlled by the OLD (open-load detection) bit, bit 13, of the input data register. The open-load monitoring circuit for each output driver is defined in Figure 1-1.

Figure 1-1. Atmel ATA6836 Output Driver Open-load Detection Circuit



When the OLD bit is set LOW, open-load detection is enabled. In this mode of operation, a pull-up current (I_{source}) for each high-side switch (I_{HSx}) and a pull-down current (I_{sink}) for each low-side switch (I_{LSx}) will be activated simultaneously. The low-side open-load current is set to a level 25% greater than that of the high-side current in order to establish the high-side/low-side open-load thresholds. An open-load condition is detected when the difference between the supply voltage (VS) and the high-side voltage (V_{HSx}) or the low-side voltage (V_{LSx}) is lower than the open-load detection threshold for the output stage:

$V_{HS\_th} = V_{VS} – V_{HSx}$

$V_{LS\_th} = V_{LSx}$

Note: Please refer to the specific device datasheet for the high-side/low-side open-load threshold levels V_{HS_th} and V_{LS_th}.

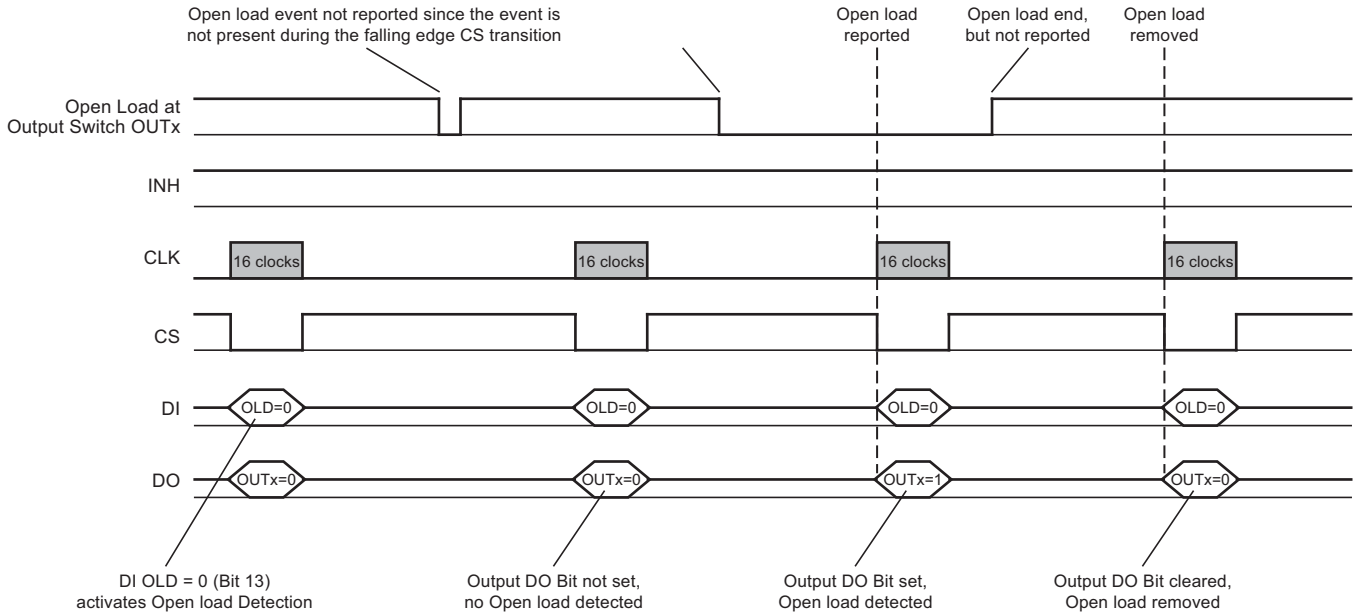
When an open-load has been detected, the corresponding output bit (LSx or HSx) in the output data register will be set HIGH.

Note: Switching on an output stage with OLD bit set to HIGH disables the open-load function for this output.

1.2 SPI Data Timing

Data transfer on the SPI begins with each falling edge of the CS (chip select) signal. Given the case where an open-load condition begins and ends between two falling CS edge cycles, as represented by the first open-load event in Figure 1-2, the open-load will not be reported and the corresponding DO bit will not be set. Only when the open-load event is present during the falling CS edge will open-load be reported (see Figure 1-2, second open-load event). Once the open-load is removed, the corresponding DO bit will be cleared, indicating the end of the open-load event.

Figure 1-2. SPI Reporting of Open-load Events



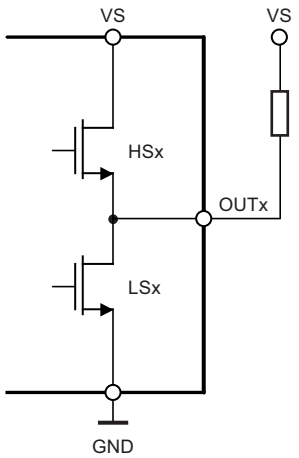
Notes:
1. When OLD = 1, the HSx/LSx DO bits report the Switch Status of the outputs
2. When OLD = 0, the HSx/LSx DO bits report the Open Load Status of the outputs
3. OUTx refers to the HSx/LSx bits in the Data Output Register

1.3 Examples

1.3.1 Single-ended High-side Open-load

A high-side load as shown in Figure 1-3 can be directly monitored for an open-load condition. In this case, if the connected load is open, activating open-load detection (OLD = 0) will indicate a high-side open-load at the dedicated low-side output register (LSx) for the associated output (OUTx).

Figure 1-3. High-side Load Configuration

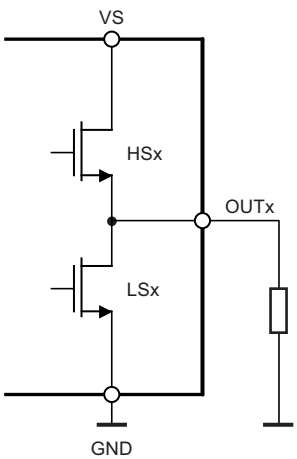


If LSx = 1, then the high-side load is open. Conversely, if LSx = 0, then the high-side load is properly connected.

1.3.2 Single-ended Low-side Open-load

A low-side load as shown in Figure 1-4 cannot be monitored for an open-load condition. In this case, regardless of the state of the load, open or closed, the result will be the same when activating open-load detection (OLD = 0). The corresponding HSx = 1 for the associated output (OUTx) in both instances.

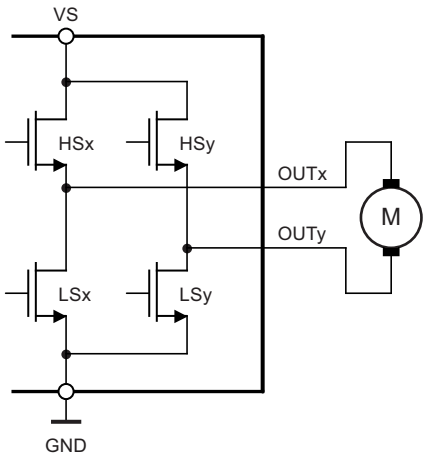
Figure 1-4. Low-side Load Configuration



1.3.3 Low-side Open-load: H-bridge Configuration

A low-side load configured in an H-bridge as shown in Figure 1-5 can be directly monitored for an open-load condition. Testing for the open-load is a two step process. First, switch off all high-side (HSx/HSy) and low-side (LSx/LSy) drivers. The voltage at both clamps in this condition will be pulled-down (as shown in Figure 1-1 on page 2) due to the higher low-side open-load detection current sources. Next, with both low-side drivers off, switch on one high-side driver (HSx or HSy). Since the DC motor has a relatively low internal resistance, the voltage of the inactive high-side output should be at the same level as the activated high-side output. In the case of an open-load, the inactive high-side output register will report a “0” if the active high-side output is “1”. Conversely, if the load is connected, the inactive high-side output will report a “1”.

Figure 1-5. H-bridge Load Configuration



The register configuration to perform open-load test of the H-bridge is as follows:

1. Step #1, program all drivers OFF
    a. Input register command
        i. OLD = 0, HSx = 0, LSx = 0, HSy = 0, LSy = 0
    b. Output register result
        i. LSx = 1, LSy = 1 indicates “Open-load” at LSx/LSy, which is expected
2. Step #2, program HSy ON:
    a. Input register command
        i. OLD = 0, HSx = 0, LSx = 0, HSy = 1, LSy = 0
    b. Check output register result
        i. HSy = 1, HSx = 1 indicates “Motor connected”
        ii. HSy = 1, HSx = 0 indicates “Motor disconnected”

2. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

Revision No.	History
9251E-AUTO-04/15	• Put document in the latest template
9251D-AUTO-02/14	• Type ATA6836 updated in ATA6836C • Type ATA6837 removed • Type ATA6838 updated in ATA6838C
9251C-AUTO-11/12	• Section “References” on page 1 updated • Section “Description” on page 1 updated • Figure 1-1 “Atmel ATA6836 Output Driver Open-load Detection Circuit” on page 2 updated

Atmel Corporation 1600 Technology Drive, San Jose, CA 95110 USA **T:** (+1)(408) 441.0311 **F:** (+1)(408) 436.4200 | **www.atmel.com**