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Building on his earlier fast driver amplifier work, Giovanni Stochino has now developed what is possibly the fastest high-power audio amplifier of its type. More impressively, he has done so without sacrificing audio purity.

300V/µs power

In my previous article[1] I described how the basic architecture of high-speed voltage feedback amplifiers can be applied to the design of high-performance audio-power equipment. Detailed design information for a non-slewing 100 watt into 8Ω mosfet power amplifier was given. It featured a linear output speed of ±170V/µs and its rated output power total harmonic distortion figures were 0.004% and 0.045% at 1kHz and 20kHz, respectively.

Subsequent investigations have shown that further evolution of the basic architecture can provide higher speed and better thd figures – comparable with top-class hi-fi amplifiers – relative to the basic configurations.

This article reports the results of my recent investigations and experiments and provides design details for a new low-distortion, very high speed 100W into 8Ω audio power amplifier, which features a slew rate higher than ±300V/µs and rated power thd figures of less than 0.002 % and 0.020% at 1kHz and 20kHz, respectively.

Improved high-speed architectures

In my last article, I demonstrated that the thd and speed performances of the basic high speed voltage-feedback architectures appear to be influenced by the low, i.e. unity to two, current gain of the intermediate stage. This implies that a substantial improvement of both thd and speed figures can be obtained when a higher current gain class AB intermediate stage is incorporated in the original schemes[1].

The problem here is that this change has to be done without degrading the other performances and, more importantly, the robustness of the basic design.

With this requirement in mind, my investigations have focused on the topologies shown in **Figs 1** and **2**.

The input stages are designed to provide class AB operation and the simultaneous availability of large push-pull currents, I_R and I_L, with the appropriate phase, at nodes A and B, Fig. 2. I have already shown [2] that this feature is very important to avoid the dangerous simultaneous conduction of the upper and lower half of the intermediate stage. During simultaneous conduction there is a risk of driving intermediate stage transistors out of the dynamic safe operating area.

Avoiding simultaneous conduction contributes to the robustness of the amplifier. It is particularly important in very fast high-power amplifiers, where the feedback loop forces the intermediate stage to provide high peak currents during large/fast input transients.

Another key feature of these schemes is the use of common-base transistors $Tr_{10,11}$. These play a twofold role:

- to allow the use of low voltage high current gain transistors Tr_9 and Tr_{12}, which increases the available gain and peak current of the intermediate stage;
- to improve amplifier linearity.

Relative to Fig. 2, the configuration of Fig. 1 potentially provides higher input stage large signal transconductance and less power consumption. As is well known, large signal transconductance in both schemes is determined mainly by cross coupling resistor R. However, while in Fig. 2 the value of R is mainly governed by the need to provide the level shifting voltage with reasonable power consumption, in Fig. 1 this limitation does not apply. As a result, R can be set as low as convenient.

Because of the above, Fig. 1 promises better speed and lower power consumption than Fig. 2, although at the expense of offset and noise precision and distortion performance. Differences in the two schemes are only in the input stage. Intermediate and output stages are exactly the same for both designs.

Compared with the simplified circuit diagram presented in my March '96 article, the clamping network at the output of the input stage in these designs shows one additional diode, which has been introduced to increase the intermediate stage peak output current to about 80mA. Accordingly, higher maximum output rates of change are to be expected. In order to produce comparable results, the two amplifiers are designed with as close as possible phase margins and unity gain frequencies under closed-loop conditions.

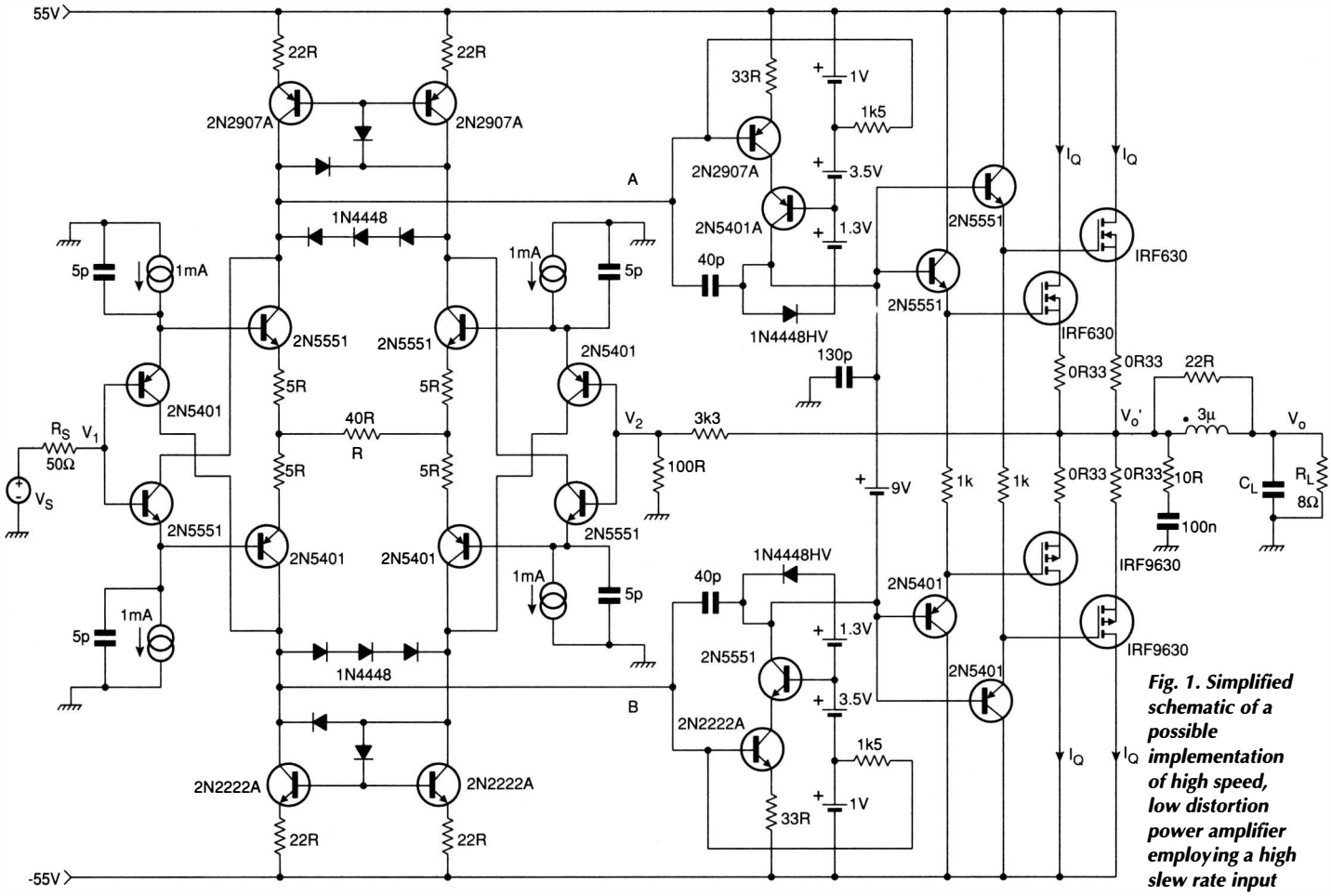

Fig. 1. Simplified schematic of a possible implementation of high speed, low distortion power amplifier employing a high slew rate input stage.

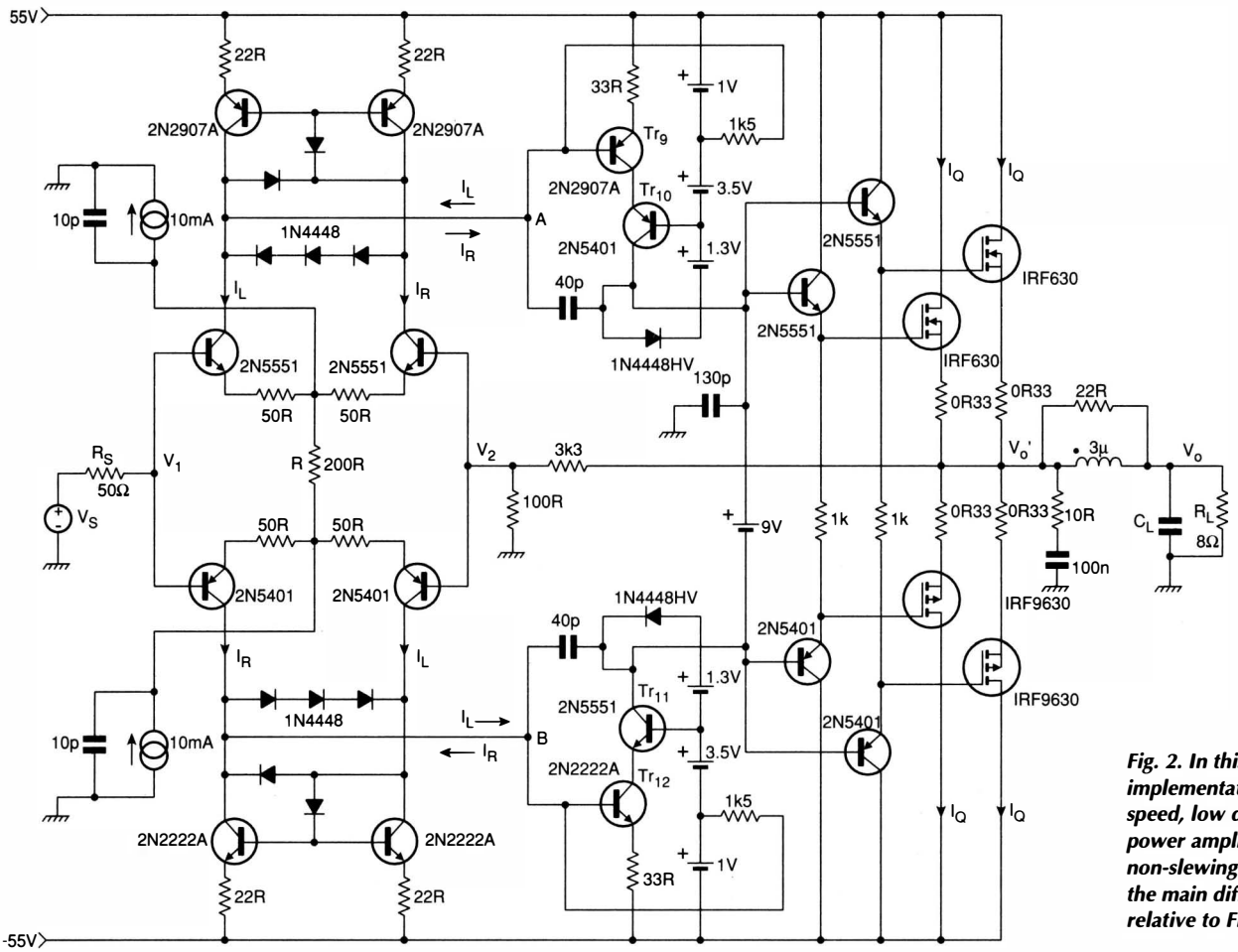

Fig. 2. In this preferred implementation of a high speed, low distortion power amplifier, a non-slewing input stage is the main difference relative to Fig. 1.

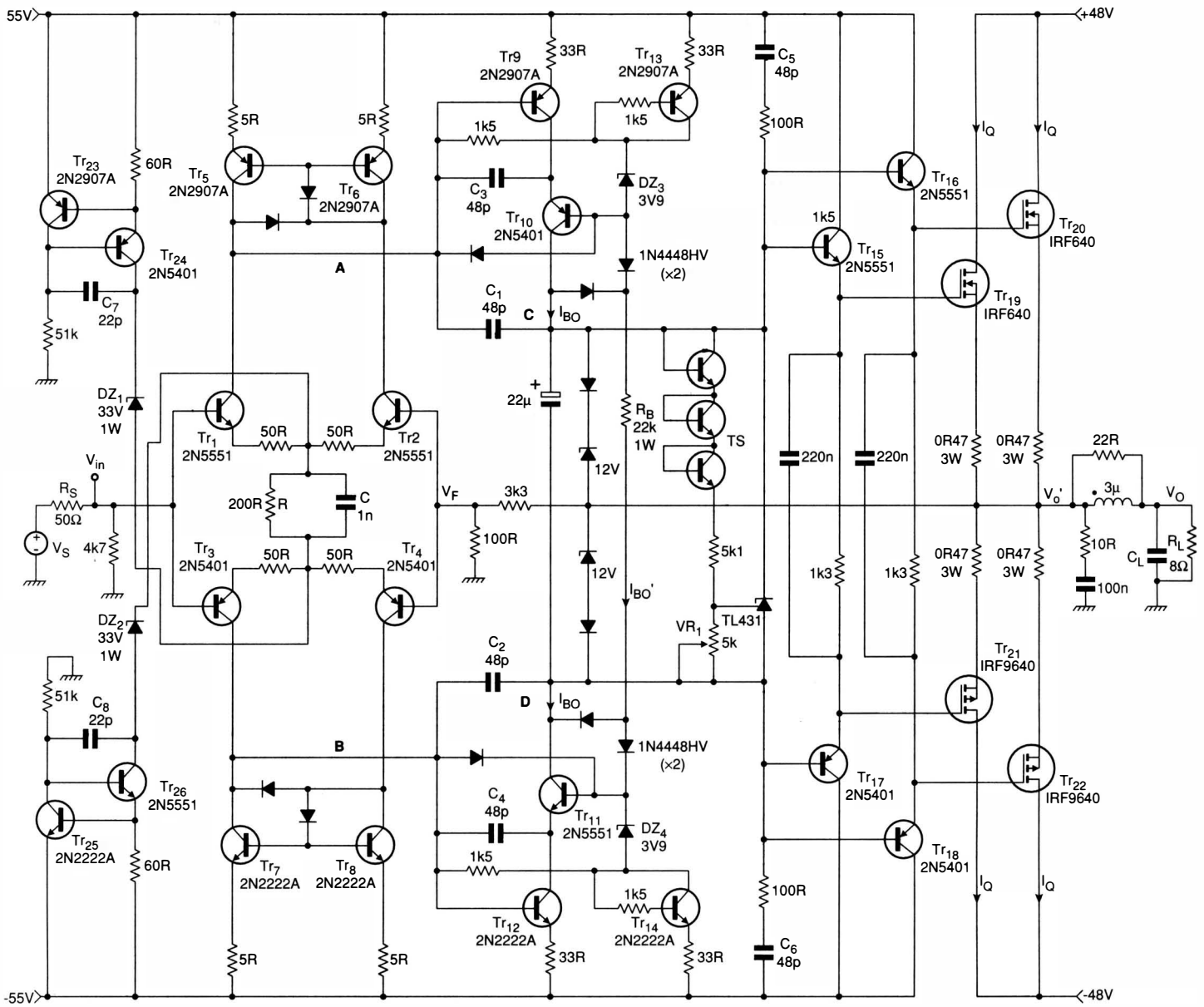

Fig. 3a). Detailed circuit diagram of the final 100W/8Ω audio-power amplifier, featuring a speed higher than ±300V/µs, and a rated power thd of 0.002% at 1kHz and 0.018% at 20kHz. Note that all diodes are 1N4448 Diodes 1N4448HV are 1N4448 selected for a reverse voltage higher than 120V. Add 100µF//100nF decoupling to each 55V rail and 1000µF//2×100nF to each 48V rail.

Some Spice simulation results are reported in **Tables 1** and **2**. Here, the main characteristics of the two new amplifier configurations are compared with the basic non-slewing architecture, with similar characteristics.

It is clear that the new implementations provide better speed and thd performances than the basic non-slewing architecture design, confirming the theoretical predictions.

Figure 1 and 2 have very similar closed-loop performances. However, due to the reduced number of transistors in the input stage, Fig. 2 offers better open-loop performance, in terms of frequency response and phase margin, as well as less noise.

In the light of the above, Fig. 2 seems to represent the best candidate for the design of a high-performance audio power amplifier, although power consumption is higher due to the level shifting current needed to bias the input stage. Moreover, this topology can be expected to provide reduced sensitivity to layout and parasitics, as well as load impedance variations. Consequently it will simplify design and implementation.

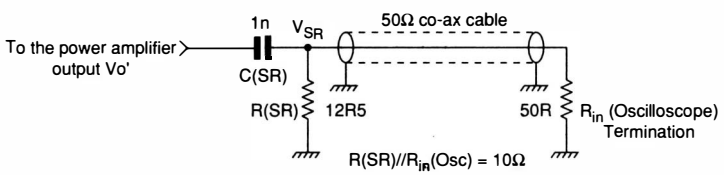

Fig. 3b). Slew rate test circuit from D. Self[3]. Component values and circuit have been adapted to high-speed measurement. Slew rate, SR, can be determined by the following; $SR \approx V_{SR(max)}/(C_{SR}R_P)=100\pi V_{SR(max)}$, in V/µs, where $R_P=R_{(SR)}//R_{IN(OSC)}=10\Omega$. Oscilloscope bandwidth is higher than 200MHz.

Implementing the power amplifier

Design has been optimised through intensive simulation work and verification tests on the experimental prototype. Measurements have substantially confirmed simulation results.

Discrepancies only occur when simulation data are close to or below the limits of available test equipment, the readings from which include noise, as well as thd. This is the case

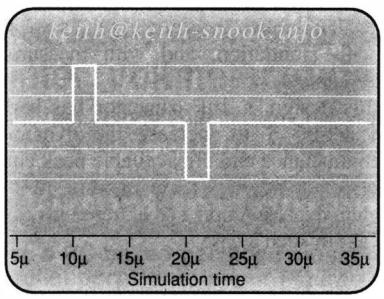

Fig. 4. Input stimulus type used for verifying the amplifier's speed, during simulation and experiments. Vertical scale is 3V/div. Maximum speed measurements were made using both standard and Self methods.

for thd at 1kHz. The differences at 20kHz can be explained by layout problems in the experimental prototype and/or by the influence of component mismatches.

Final design

Figure 3a shows the complete circuit diagram of the final low thd, high speed 100W, 8Ω audio power amplifier.

Compared with Fig. 2, extra capacitors C_3 to C_8 are introduced in the assembled prototype. These components compensate for layout parasitics and achieve a clean step response in all operating conditions, **Figs 4, 5** and **6**.

The diode clamping network on the collectors of the input stage transistor has been simplified. Two diodes connected to zener diodes DZ_3 and DZ_4 perform the same task of the original circuit. Here, positive and negative peak currents of the intermediate stage are slightly higher and symmetrical than in Fig. 2.

The biasing network of the intermediate stage is made from Tr_{13}, Tr_{14}, DZ_3 and DZ_4, in addition to current setting resistor R_E. Nominal bias current, given by,

$$I_{BO} \approx I_{BO}' = (V_{CC}+V_{EE}-2V_Z-4V_{BE(on)})/R_B$$

and is about 6mA.

Bias setting and stabilisation of output power mosfets is achieved by means of the *TL431* shunt regulator and temperature sensing network *TS* in Fig. 3a. This network consists of three diode-connected *2N5551*s and is mounted very close to the output mosfets on the same heatsink to provide thermal coupling.

This scheme provides a stable working point for the temperature sensor *TS*, which is insensitive to I_{BO} variations. This is because current I_{TS} is kept constant by the *TL431*'s 2.5V internal reference, through the relationship $I_{TS}=V_{ref}/R(T_1)$.

Since, as is well known, each transistor provides a $\Delta V_{be}/\Delta T$ of about –2 mV/°C, *TS* yields a total $\Delta V_{TS}/\Delta T$ of –6 mV/°C. This has been found adequate to compensate for the intrinsic I_Q changes with temperature of power devices.

Bias current I_Q of each mosfet is set at 120mA via trimmer VR_1, after a reasonable

Table 1. Characteristics of Fig. I and Fig. 2 fast audio-power amplifiers. Test conditions are I_Q=120mA, R_s=50, Load=8Ω//0.5µF.

Characteristic	Basic nsa[1]	Fig. 1	Fig. 2
Best input offset voltage[2]	350µV	180µV	170µV
DC gain, open loop	80dB	110dB	111dB
Unity-gain frequency	22.5MHz	19MHz	22MHz
Open-loop gain at 20kHz	64.5dB	67dB	68dB
Open-loop amplifier phase margin[3]	–81°	–127°	–93°
Closed-loop amplifier phase margin[4]	+82°	+79°	+76°
Slew rate, 10V pp square wave input	±160V/µs	± 210V/µs	±185V/µs
Output noise, bandwidth 80kHz	34µV rms	50µV rms	31µV rms

Table 2. THD of amplifiers in Fig 1 and Fig 2 with same test conditions as Table 1.

V_{out} (Vpp)	Basic nsa[1] design		Fig. 1		Fig. 2	
	1kHz	20kHz	1kHz	20kHz	1kHz	20kHz
20	0.0018 %	0.0240%	0.0008 %	0.0140%	0.0006%	0.012 0 %
80	0.0090 %	0.0380%	0.0005%	0.0100%	0.0004%	0.0080 %

Notes
1. Non-slewing amplifier
2. In the simulation phase, devices and components have been considered perfectly matched.
3. Amplifier only, i.e. without the feedback network.
4. Amplifier plus feedback network. Closed loop gain is 30.6dB.

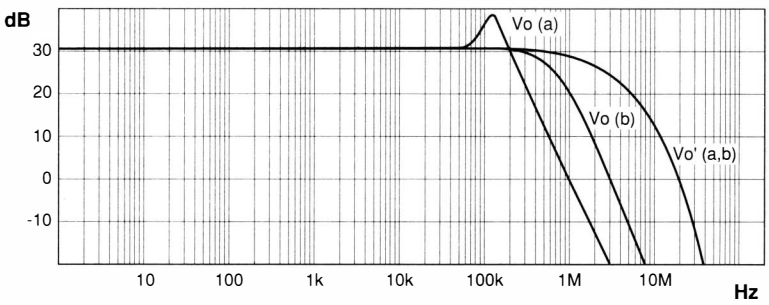

Fig. 5. Simulated frequency response – i.e. magnitude – of the power amplifier in Fig. 3. Test conditions are V_o(a) load=8Ω//0.5µF, V_o(b) load=8Ω//0.05µF, vertical scale is 10dB/div and frequency range is 1Hz to 100MHz.

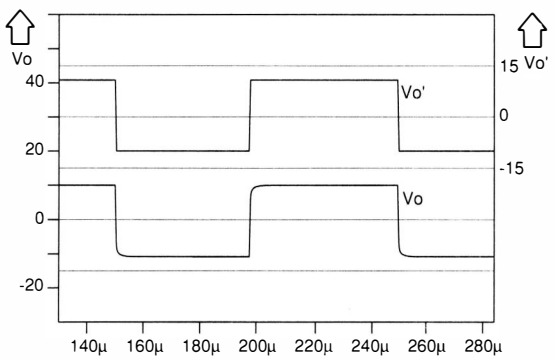

Fig. 6a). Simulated voltage step response of the power amplifier in Fig. 3. Test conditions are V_o'=20V peak-peak, load=8Ω//0.005µF, vertical scale is 15V/div and frequency is 10kHz.

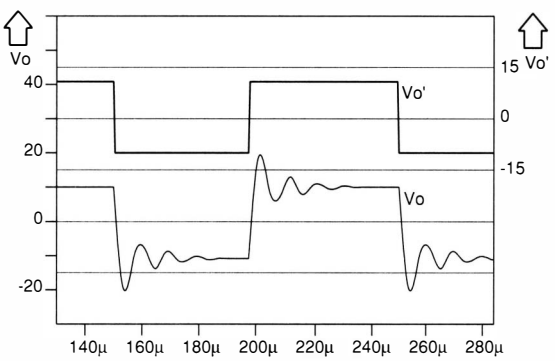

Fig. 6b). Simulated voltage step response of the power amplifier in Fig. 3. Test conditions in this case are the same as for 6a), except for the load, which is 8Ω//0.5µF.

amplifier warm-up time. Make sure to set this trimmer to its highest value before applying power to the amplifier. Measured I_Q variations during operation are less than 20%.

Supplying power

To increase the amplifier's efficiency, separate unregulated ±48V supply rails are used for the output power devices, which are *IRF640* and *IRF9640* types from International Rectifier. The rest of the amplifier is powered by two regulated +55 and –55 V supply rails.

Tables 3 and **4** demonstrate the notable improvement of harmonic distortion figures. At 1kHz, measured thd is mainly limited by the available instrumentation, as illustrated by the fact that it remains virtually unchanged when load impedance reduces to 4Ω.

The maximum rate of change of the output voltage results in excess of 300V/µs, confirming that the new architecture is viable for reliable high-speed power amplification. Measurements of slew-rate were made both in the traditional way, and in accordance with the practical method suggested by Douglas Self,[3] with appropriate adaptations.

The test circuit is shown in Fig. 3b. Assuming $V_O' >> V_{SR}$, the maximum rate of change *SR* is determined by,

$$SR \approx \frac{V_{SR(\max)}}{C_{SR}R_P} = 100 \times V_{SR(\max)} \quad V/\mu s$$

where $R_P = R_{SR} // R_{IN(osc)} = 10\Omega$.

To the best of my knowledge, this speed is the highest ever reported for a high power audio amplifier, which makes use of voltage-feedback.

The theory behind the speed performance of this architecture can be basically explained as follows. The maximum current available at nodes A and B depends on the maximum input voltage, V_{max}, which can be safely applied to the input of the amplifier. This is given by equation 4 of my March '96 article,

$$I_{A(\max)} = \frac{V_{(\max)} - 2V_{be(on)}}{2R_e + R} = \frac{V_{EBO} - V_{be(on)}}{2R_e + R}$$

This current amounts to about 18mA for the component value and active device types used in Fig. 3a.

Since capacitance at nodes A and B in Fig. 3a is about 50pF, the maximum slew rate across C_1 and C_2 is $SR_{A,B}$=360V/µs. Capacitors C_3 and C_4 do not play a major role in this context because the voltage variation across them is limited to a few volts.

On the other hand, the current available at the output of the intermediate stage, nodes C and D, is about 80mA. Total node capacitance, including the reflected capacitance of the output power devices, is less than 230pF. Slew rate at the input of the output stage will therefore exceed $SR_{C,D(min)}$=350V/µs.

Bias current considerations

It is worth pointing out that this high value of slew rate can be sustained by the amplifier only if biasing current I_{BO} is large enough to charge/discharge at the same rate the base-collector capacitances C_{bc} of Tr_{10} and Tr_{11}, which equal 5-8 pF. This means that $I_{BO} \geq SR_{CD(min)} C_{bc}$ has to be set at 2.8mA.

A safety margin is recommended for taking into account parasitics and base drive requirements, which equals,

$I_{B(peak)}/\beta_{(min)}$=80mA/30=2.7 mA.

The minimum output slew rate $SR_{(min)}$ will be slightly less than $SR_{CD(min)}$, due to the gate driving requirements of the output power devices. The above theoretical values are in line with simulation, and with measured results, Table 4.

In this design, a 1nF capacitor has been added across *R* to increase the dynamic transconductance and the available peak current of the input stage corresponding to the maximum expected input signal transients, say 3V peak. In such a case,

$$I_{A(peak)} = \frac{V_{in(peak)} - 2V_{be(on)}}{2R_e} \leq 18\text{mA}$$

This results in a slight increase of speed for input signals within the linear dynamic range of the amplifier and in a further reduction of the already low residue of dynamic intermodulation distortion.

Cross-coupling capacitor *C* needs to be treated very carefully. In fact input transistors Tr_1 to Tr_4, under large signal conditions, behave like a full wave rectifier of the voltage difference V_{IN}–V_F. Current flowing in *C* is thus unidirectional. This results in a dynamic charge build-up across *C*, which is particularly important at high frequencies and during transients, when V_{IN}–V_F is usually larger.

The charge build-up could end by producing undesirable bias and gain modulation of the input stage, and, consequently, increased high frequency thd and intermodulation distortion. This effect is also evident from the fact that while *C* can truly help to boost the linear speed of the amplifier during occasional transients, it does not produce the corresponding improvement of the linear power bandwidth and of the dynamic intermodulation distortion.

Minimising charge build-up

In order to minimise the above side effects, a low value of capacitance should be chosen. Definition of the right value of *C* is not an easy task, since its influence on the circuit performance is both amplitude and frequency dependent. The following rule of thumb has proved effective in many applications,

$$C \leq \frac{1}{10(2\pi R F_M)}$$

where F_M is the maximum input frequency, which is 20kHz for audio applications. This implies that the zero introduced by *R*//*C* in the large signal frequency response of the amplifier has to be located far above the audio frequency range. According to the above empirical inequality, *C* should be lower than 3.9nF. As a matter of fact, the value employed in this design, 1nF, has not produced measurable effects on thd performance. ■

Table 3. Total harmonic distortion of final amplifier in Fig. 3a, with R_s=50Ω, I_Q=120mA and 80kHz bandwidth.

V_{out} (V_{pp})	Spice simulation 8Ω load		Measured 8Ω load*		Measured 4Ω load*	
	1kHz	20kHz	1kHz	20kHz	1kHz	20kHz
5	0.00010%	0.0040%	0.0031%	0.005%	0.0035%	0.007%
10	0.00025%	0.0140%	0.0024%	0.008%	0.0029%	0.010%
20	0.00070%	0.0190%	0.0020%	0.011%	0.0023%	0.013%
40	0.00060%	0.0145%	0.0023%	0.015%	0.0023%	0.018%
80	0.00060%	0.0110%	0.0021%	0.018%	0.0023%	0.026%

*Instrumentation limit, thd+noise): 0.002% at 1kHz; 0.003% at 20kHz.

Table 4. Further characteristics of Fig. 3a amplifier, R_s=50Ω, load=8Ω, I_Q=120mA

Characteristic	Spice simulation	Measurement results
Input offset voltage	....	1.6 mV
Slew rate†, *C*=0pF	+336/–297V/µs	+310/–360V/µs
Slew rate†, *C*=1nF	+360/–304V/µs	+360/–370V/µs
Output noise, bw=80kHz	31µV (rms)	39µV (rms)

† ±6V peak pulse input, as in Fig. 4.

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