SHARP

LM-24003G
LCD GRAPHIC UNIT

■ Description

The Sharp LM-24003G is a graphic display unit of 240 x 128 full dots which combines a dot-matrix LCD panel and driver C-MOS LSI on a single printed wiring board.

It can display graphs, diagrams and characters as bit mapped patterns. It is suitable to various types of equipment, such as, compact OA equipment and measuring instruments which require needs of slim, light weight and low power consumption.

■ Features

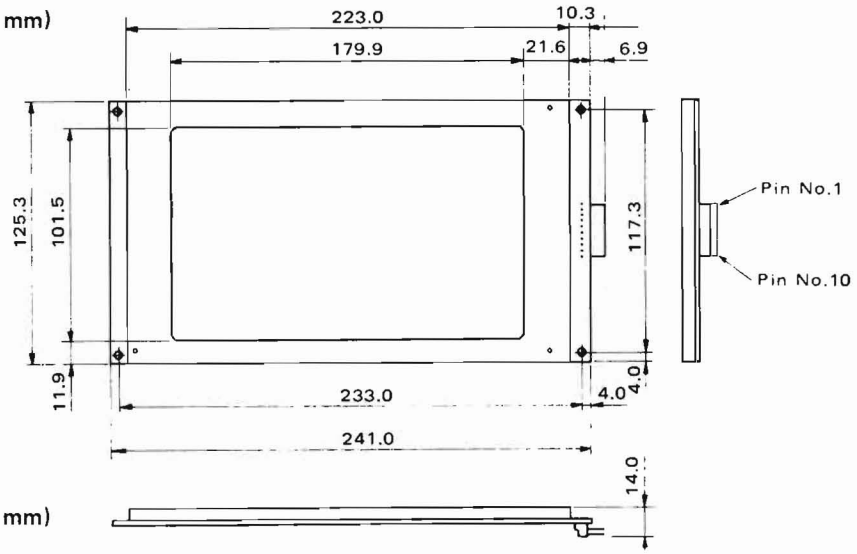
- Displaying graphs and diagrams in addition to characters.
- Very easy to be mounted on other equipment due to compact, slim body and low power consumption.
- Stable display in wide range of temperature due to built-in temperature compensation circuit.
- Easy-to-read display with wide viewing angle and high contrast.
- The unit operates from +5, −12 power supplies.

■ Applications

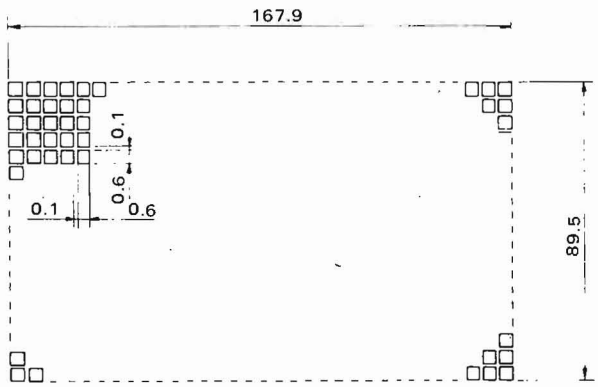
- OA system: Word processor, POS terminal, Computer terminal, etc.
- Measuring instruments: Panel meter, Scaler, Analogue digital tester, etc.

■ Outline Drawing

Outline Dimensions (Units: mm)



Dot Display Details (Units: mm)



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■ Mechanical Specifications

Item	Specifications	Unit
Unit outline dimensions	241 (W) x 125.3 (H) x 14 (D)	mm
Effective viewing area	179.9 (W) x 101.5 (H)	mm
Display format	240 (W) x 128 (H) full dots	–
Dot size	0.6 (W) x 0.6 (H)	mm
Dot spacing	0.1	mm
Dot color	Dark blue	–
Background color	White	–
Weight	Approx. 300	gr

■ Absolute Maximum Ratings

Item	Symbol	Min.	Max.	Unit	Remark
Supply voltage (Logic)	$V_{DD}-V_{SS}$	0	7	V	
Supply voltage (LCD driver)	$V_{DD}-V_{EE}$	0	20	V	
Input voltage	V_{IN}	0	V_{DD}	V	
Storage temperature	T_{stg}	–25	+55	°C	
Operating temperature	T_{opr}	0	+50	°C	

■ *Electro-optical Characteristics

(Ta = 25°C)

Item	Symbol	Min.	Max.	Unit	Conditions
Supply voltage (Logic)	$V_{DD}-V_{SS}$	4.75	5.25	V	
Supply voltage (LCD driver)	$V_{EE}-V_{SS}$	–13	–11	V	
Input signal voltage	V_{IH}	0.7 V_{DD}	V_{DD}	V	"High" level
	V_{IL}	0	0.3 V_{DD}	V	"Low" level
Input leakage current	I_{IL}	–	20	μA	V_{IN}=5V
Power consumption	P_d	–	100	mW	V_{DD}=5V V_{EE}=–12V
Viewing angle	θ_1	40	–	degree	$C_O \geqq 2$
	θ_2	–	15	degree	$C_O \geqq 2$
Contrast ratio	C_o	2.0	**2.5		θ=15°

* Temperature compensation circuit is built-in.

** Typical value

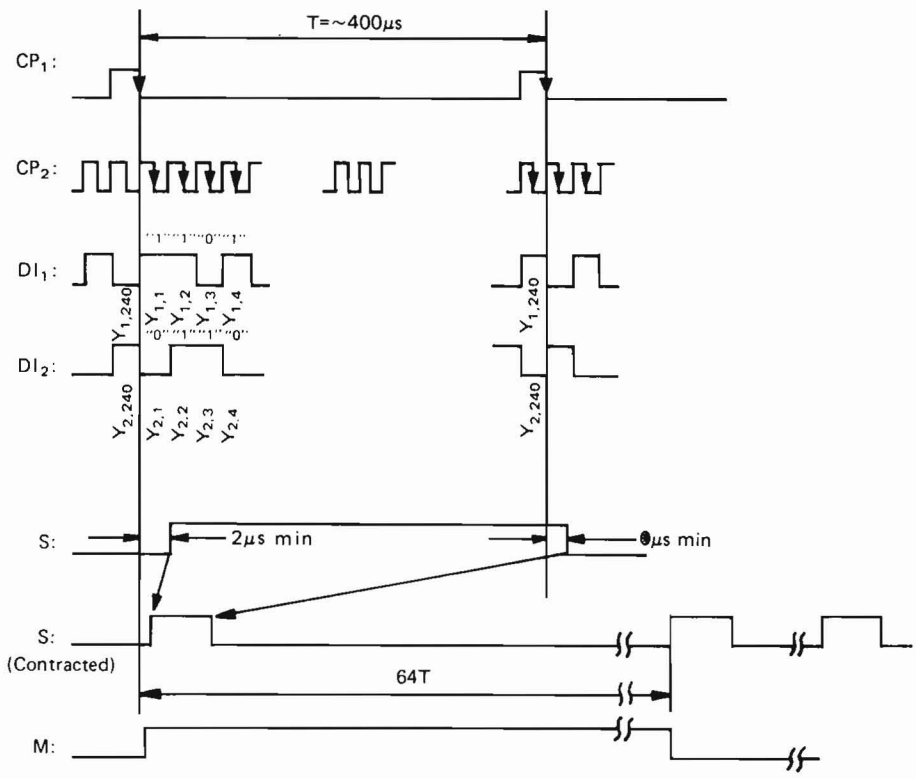
■ Interface Signals

Connector used: MOLEX 5046-10A
Compatible connector: MOLEX 5051-10

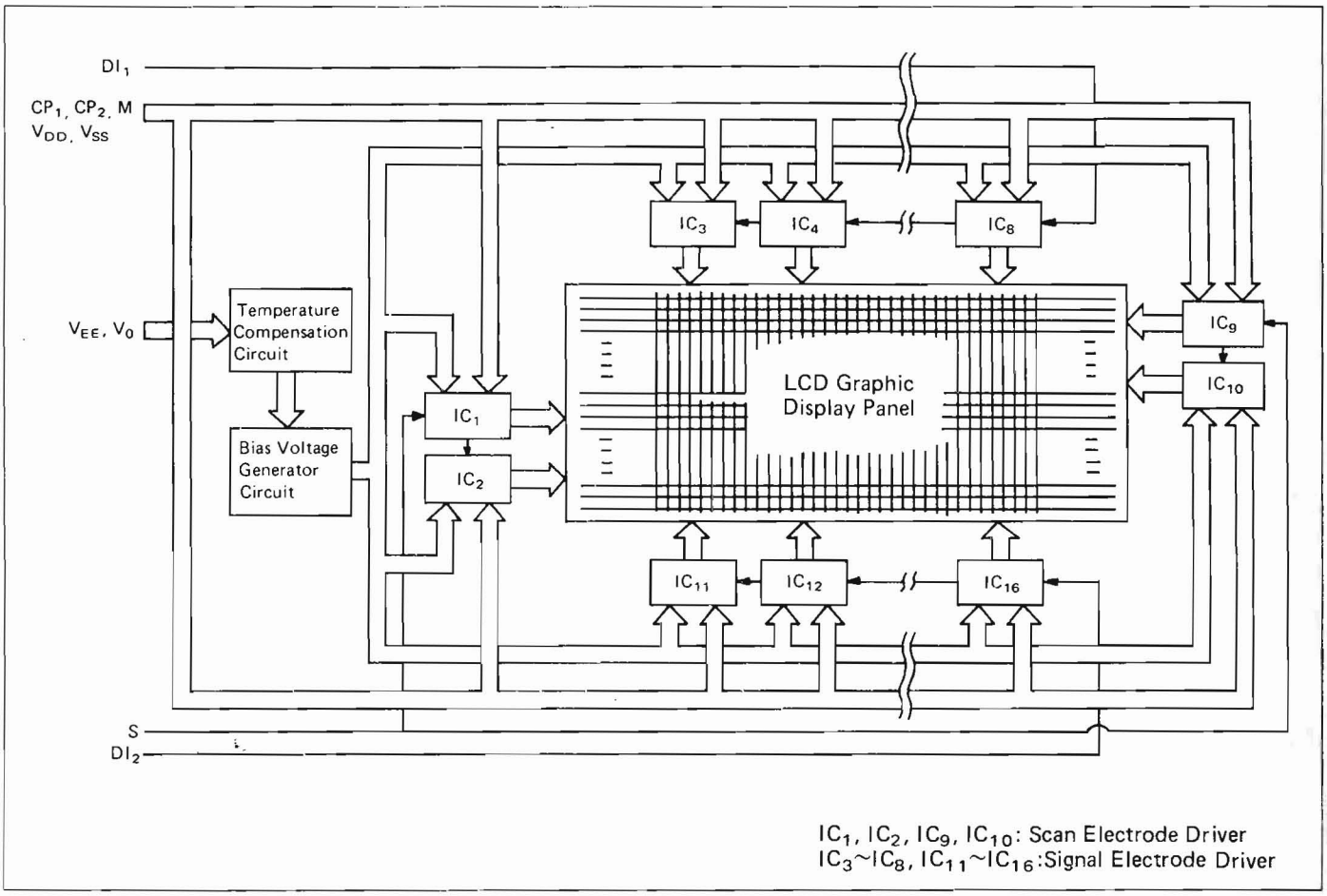
Pin No.*	Symbol	Description	Effective Level
1	S	Scan start-up signal	"H"
2	CP_1	Input data latch signal	H → L
3	CP_2	Data input clock signal	H → L
4	DI_1	Display data signal (Upper half of screen)	H (ON), L (OFF)
5	M	Drive waveform alternating signal	H, L
6	V_O	Power supply for LCD drive(+)	–
7	V_{DD}	Power supply for logic circuit	–
8	V_{SS}	Ground potential	–
9	DI_2	Display data signal (Lower half of screen)	H (ON), L (OFF)
10	V_{EE}	Power supply for LCD drive (–)	–

* For the location of Pin No., refer to outline dimensions.

■ Interface Timing Chart



■ Circuit Block Diagram



(Remarks) This is tentative information and subject to be changed without notice. For detail specifications, contact our sales department.

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3.. Unit Drive Method

3.1 Circuit Configuration

The circuit configuration is shown in Fig. 2.

3.2 Input Data and Control Signals

Input data is entered at DI sequencially row by row with clock pulse CP_2, in the form of 1-bit serial data (high level=ON; Low level=OFF) starting from the top left of the display face. On the falling edge of CP_2 clock, the input data is sequentially transferred via the shift register in the signal electrode driver. After one row of data (480 dots) are entered, they are latched in the form of parallel data corresponding to 480 lines of signal electrodes, then sent to the signal electrodes. At this time, scan start signal S has been transferred from the scan signal driver to the 1st row of scan electrodes, and the contents of data signal on DI are displayed on the 1st row on display face according to the combination of voltages applied to the scan and signal electrodes of the row of LCD.

While the 1st row of data are being displayed, the 2nd row of data are entered to DI pin. When 480 dots of data have been transferred, then latched on the falling edge of CP_1 clock, the display face proceeds to the 2nd row of display. The display input described above is repeated up to the 32nd row to complete the whole area of display. The data input proceeds to the next display face.

The drive waveform alternating signal M is a kind of control signal which provides alternating drive waveform necessary for prolonged operating life of the LCD by alternating the drive waveform according to its high and low levels.

Normally this signal is synchronized at $\pm 1\mu s$ of the rise of scan start signal S and entered at 1/2 duty waveform of 1/2 frequency of repetitive frequency of S.

Since this graphic display unit contains no refresh RAM, it requires data and timing pulse inputs even for static display. The timing chart of input signals is shown in Fig. 1.