SPECIFICATION FOR LCM SAMPLE

Model No. : GDSC-12864WM-64
Sample No. : V1.00

Customer : _____

Prepared By	
Checked By	
Approved By	

XIAMEN OCULAR TECHNOLOGY CO.,LTD

1. General Specification

Interface With **Parallel** MPU

Display Mode:Negative/Transmisstive/STN(Blue) Type

Viewing Angle :**6:00** Clock

Display Duty:**1/65** Driving Bias:**1/9** Driving Voltage:**8.5V**

Lcd Supply Voltage:+3.3V

Mechanical Characteristics(Unit:mm)

Display Dot Matrix :**128*64**

Extenal Dimension: See Drawing

Dots Size:**0.48*0.48**

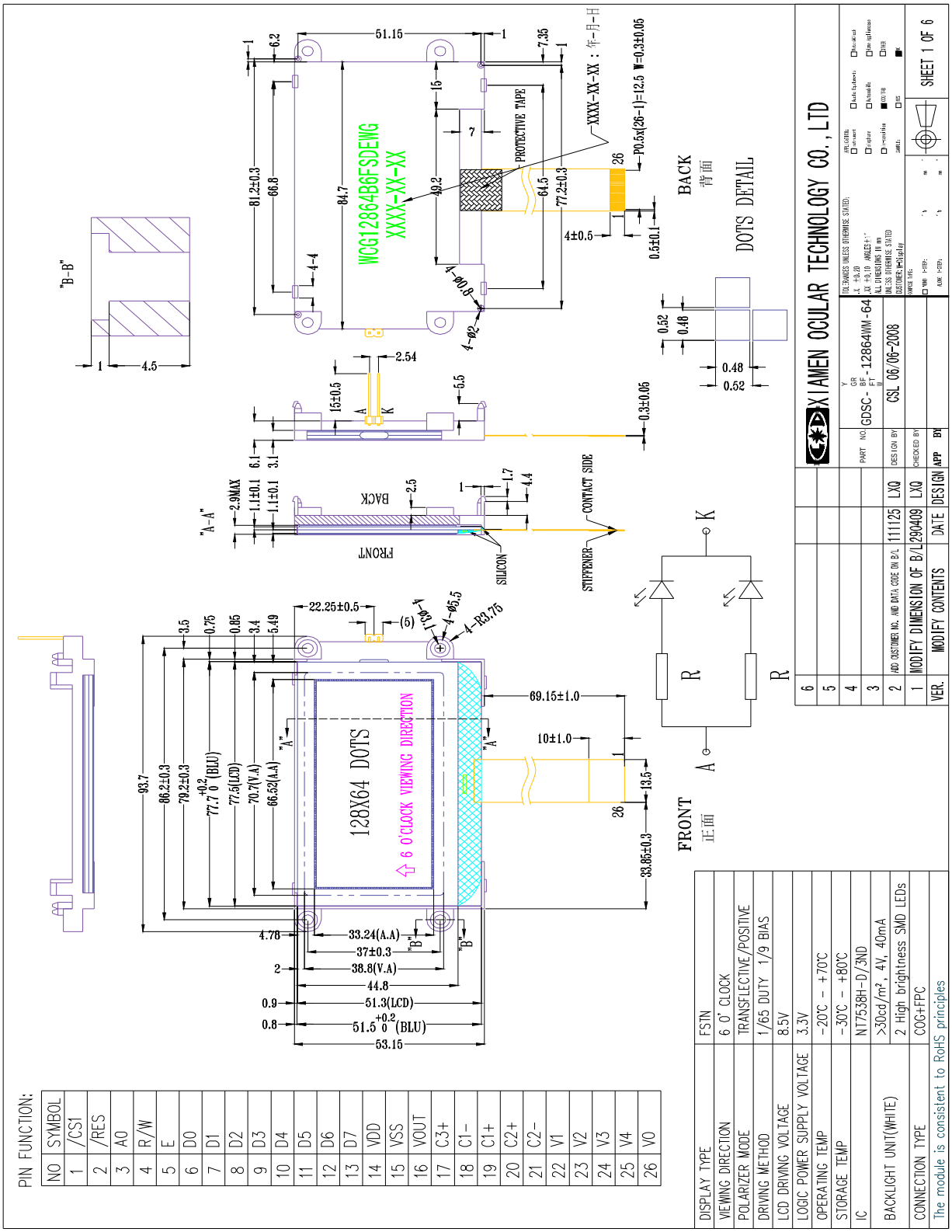
Dots Pitch:**0.50*0.50**

Temperature Specification

Operation Temperature: -20℃～70℃

Storage Temperature:-30℃～80℃

External Dimension



PIN FUNCTION:

NO	SYMBOL
1	/CS1
2	/RES
3	A0
4	R/W
5	E
6	D0
7	D1
8	D2
9	D3
10	D4
11	D5
12	D6
13	D7
14	VDD
15	VSS
16	VOUT
17	C3+
18	C1−
19	C1+
20	C2+
21	C2−
22	V1
23	V2
24	V3
25	V4
26	V0

DISPLAY TYPE	FSTN
VIEWING DIRECTION	6 O' CLOCK
POLARIZER MODE	TRANSFLECTIVE/POSITIVE
DRIVING METHOD	1/65 DUTY 1/9 BIAS
LCD DRIVING VOLTAGE	8.5V
LOGIC POWER SUPPLY VOLTAGE	3.3V
OPERATING TEMP	-20°C ~ +70°C
STORAGE TEMP	-30°C ~ +80°C
IC	NT7538H-D/3ND
BACKLIGHT UNIT(WHITE)	>30cd/m², 4V, 40mA 2 High brightness SMD LEDs
CONNECTION TYPE	COG+FPC

The module is consistent to RoHS principles

PIN Assignment

Pin No	Symbol	I/O	Function
1	CS1B	I	This is the chip select signal .When CS1B= "L" and CS2= "H",then the chip select becomes active,and data/command I/O is enabled
2	RESETB	I	When RESETB is set to "L" ,the setting are initialized The RESETB operation is performed by the RESETB signal level
3	RS	I	Select register. 0:Instruction register (for write) Busy flag &address counter(for read) 1:Data register(for write and read).
4	RW	I	Read/write select signal.
5	E/RD	I	Operation (data read/write) enable signal.
6	DB0	I/O	This is an 8-bit bi-directional data bus that connects to an 8-bit or 16-bit standard MPU data bus. When the serial interface is selected,then D7 serves as the serial data input terminal and D6 serves as the serial clock input terminal.At this time,D0-D5 are set to high impedence. When the chip select is inactive,D0 to D7 are set to high impedance.
7	DB1		
8	DB2		
9	DB3		
10	DB4		
11	DB5		
12	DB6		
13	DB7		
14	VDD	Supply	Power supply for logic
15	VSS	Supply	Ground.
16	VOUT	O	DC/DC voltage converter output
17	C3+	O	Capacitor3+ for internal DC/DC voltage converter
18	C1-	O	Capacitor1- for internal DC/DC voltage converter
19	C1+	O	Capacitor1+ for internal DC/DC voltage converter
20	C2+	O	Capacitor2+ for internal DC/DC voltage converter

<table>
<tr><td>21</td><td>C2-</td><td>O</td><td>Capacitor2- for internal DC/DC voltage converter</td></tr>
<tr><td>22</td><td>V1</td><td rowspan="6">Supply</td><td rowspan="6">LCD driver supply voltages.The voltage determined by LCD cell is impedangce-converted by a resistive driver or an operation amplifier for application .Voltages should be the following relationship:
V0>V1>V2>V3>V4>VSS
When the on-chip operating power circuit is on,the following are given to V1 to V4 by the on-chip power circuit .Voltage selection is performed by the set LCD bias command.
<table>
<tr><th>LCD BIAS</th><th>V1</th><th>V2</th><th>V3</th><th>V4</th></tr>
<tr><td>1/5BIAS</td><td>4/5V0</td><td>3/5V0</td><td>2/5V0</td><td>1/5V0</td></tr>
<tr><td>1/6 BIAS</td><td>5/6V0</td><td>4/6 V0</td><td>2/6 V0</td><td>1/6 V0</td></tr>
<tr><td>1/7 BIAS</td><td>6/7 V0</td><td>5/7 V0</td><td>2/7 V0</td><td>1/7 V0</td></tr>
<tr><td>1/8 BIAS</td><td>7/8 V0</td><td>6/8 V0</td><td>2/8 V0</td><td>1/8 V0</td></tr>
<tr><td>1/9 BIAS</td><td>8/9 V0</td><td>7/9 V0</td><td>2/9 V0</td><td>1/9 V0</td></tr>
</table></td></tr>
<tr><td>23</td><td>V2</td></tr>
<tr><td>24</td><td>V3</td></tr>
<tr><td>25</td><td>V4</td></tr>
<tr><td>26</td><td>V0</td></tr>
</table>

Absolute Maximun Ratings

VDD=3.0V,VSS=0V,Ta=25℃

Item	Symbol	Condition	Min	Max	Unit
Power supply voltage	VDD		0.3	+4.0	V
Input voltage	Vin		-0.3	VDD+0.3	V
DC Supply Voltage	VOUT		0.3	+14.2	V
DC Supply Voltage	V0		0.3	+14.2	V
Operating temperature	Topr		-20	70	℃
Storage temperature	Tstg		-30	80	℃

Electrical Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
Power supply voltage	VDD		1.8	3.0	3.6	V
Current consumption	IDD	Ta=25℃	-	1.0	-	mA

DC Characteristics

Electrical Characteristics

DC Characteristics (VSS = 0V, VDD = 1.8 ~ 3.6V, Ta = -40 ~ +85°C unless otherwise specified)

Symbol Parameter Min. Typ. Max. Unit Condition
VDD
VDD3 Operating Voltage 1.8 - 3.6 V
1.8 - 3.6 2X, 3X boosting
VDD2 Operating Voltage 1.8 - 3.3 4X boosting
1.8 - 2.8
V
5X boosting
VOUT Booster Voltage 6.0 - 14.2 V
V0 Voltage Regulator
Operating Voltage 4.0 - 14.2 V
VREG Reference Voltage **1.36 1.40 1.44** V Ta = 25°C, -0.05%/°C
- 20 35 µA
VDD = 3V, V0 = 11V, built-in boosting
power supply off, display on,
display data = checker and no access,
Ta = 25°C
- **120 160** µA
VDD, VDD2 = 3V, V0 = 11V, 4X built-in
boosting power supply, display on,
display data = checker and no access,
temperature gradient is -0.05%/ °C,
Ta = 25°C, V0 voltage internal resistor is
used, /HPM = 1 (normal power mode).
IDD Current Consumption
- **150 255** µA
VDD, VDD2 = 3V, V0 = 11V, 4X built-in
boosting power supply, display on,
display data = checker and no access,
temperature gradient is -0.05%/ °C,
Ta = 25°C, V0 voltage internal resistor is
used, /HPM = 0 (high power mode).
ISP Sleep Mode Current
Consumption - 0.01 5 µA During sleep, Ta = 25°C
ISB Standby Mode
Current Consumption - 4 8 µA During standby, Ta = 25°C
VIHC High-Level Input
Voltage

0.8 x
VDD - VDD V
VILC Low-Level Input
Voltage VSS - 0.2 x
VDD V
A0, D0 - D7, /RD (E), /WR (R/W), /CS1,
CS2, CLS, CL, FR, M/S, C86, P/S, /DOF,
/RES, IRS and /HPM
VOHC High-Level Output
Voltage
0.8 x
VDD - VDD V IOH = -0.5mA (D0 - D7, FR, FRS, /DOF,
and CL)
VOLC Low -Level Output
Voltage VDD - 0.2 x
VDD V IOL = 0.5mA (D0 - D7, FR, FRS, /DOF,
and CL)
ILI Input Leakage
Current -1.0 - 1.0 μA
Vin = VDD or VSS (A0, /RD (E), /WR
(R/W), /CS1, CS2, CLS, M/S, C86, P/S,
IRS and /RES)
IHZ HZ Leakage Current -3.0 - 3.0 μA When the D0 - D7, FR, CL, and /DOF are
in high impedance
RON1 LCD Driver ON
Resistance - 2.0 3.5 KΩ V0 = 11.0V
RON2 LCD Driver ON
Resistance - 3.2 5.4 KΩ V0 = 8.0V
Ta = 25°C,
These are the resistance
values for when a 0.1V
voltage is applied between
the output terminals SEGn or
COMn and the various power
supply terminal (V0, V1, V2,
V3, V4)
CIN Input Pad Capacity - 5.0 8.0 pF Ta = 25°C, f = 1MHz
78.0 80.5 83.0 Hz fOSC = 31.4 KHz, 1/65duty
fFRM Frame Frequency VDD = 1.8~3.6V
64.9 67.4 69.9 Hz fOSC = 26.3 KHz, 1/65duty
VDD = 1.8~3.6V
Notes: 1. Voltages V0 ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ VSS2 must always be satisfied.

TIMING CHARACTERISTICS

System bus read/write characteristics 1 (8080 Series MPU)

System Bus Read/Write Characteristics 1 (For the 8080 Series MPU)

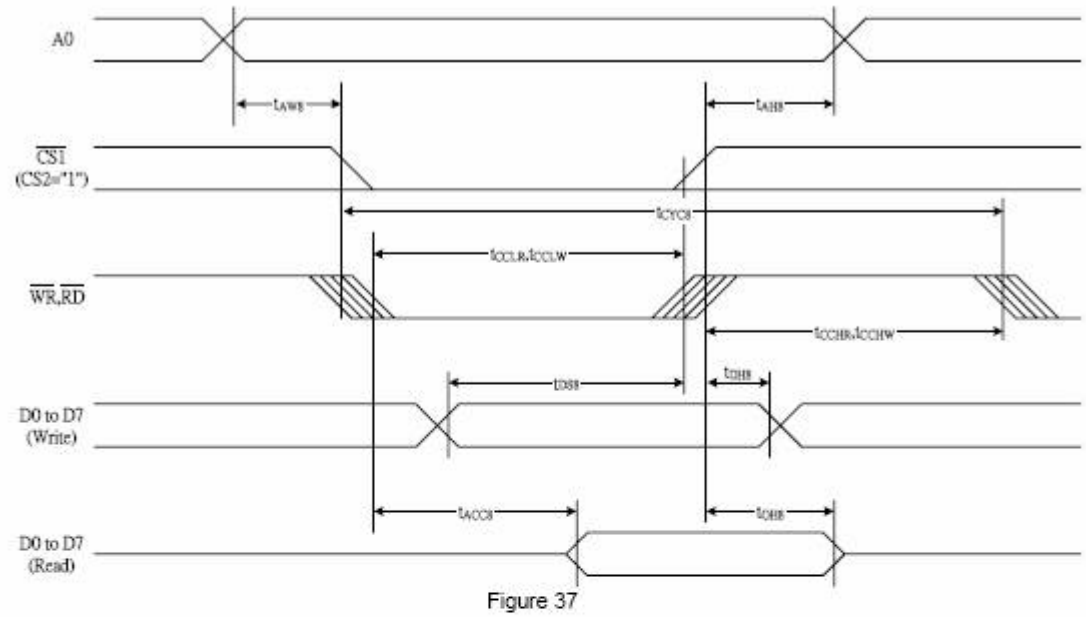


Figure 37

Table 24

(V_{DD} = 3.3V , Ta =25°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	t_{AH8}		0	—	Ns
Address setup time		t_{AW8}		0	—	
System cycle time		t_{CYC8}		240	—	
Enable L pulse width (WRITE)	WR	t_{CCLW}		80	—	
Enable H pulse width (WRITE)		t_{CCHW}		80	—	
Enable L pulse width (READ)	RD	t_{CCLR}		140	—	
Enable H pulse width (READ)		t_{CCHR}		80		
WRITE Data setup time	D0 to D7	t_{DS8}		40	—	
WRITE Address hold time		t_{DH8}		0	—	
READ access time		t_{ACC8}	C_L = 100 pF	—	70	
READ Output disable time		t_{OH8}	C_L = 100 pF	5	50	

(V_{DD} = 2.7 V , Ta = 25°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	t_{AH8}		0	—	ns
Address setup time		t_{AW8}		0	—	
System cycle time		t_{CYC8}		400	—	
Enable L pulse width (WRITE)	WR	t_{CCLW}		220	—	
Enable H pulse width (WRITE)		t_{CCHW}		180	—	
Enable L pulse width (READ)	RD	t_{CCLR}		220	—	
Enable H pulse width (READ)		t_{CCHR}		180	—	
WRITE Data setup time	D0 to D7	t_{DS8}		40	—	
WRITE Address hold time		t_{DH8}		0	—	
READ access time		t_{ACC8}	C_L = 100 pF	—	140	
READ Output disable time		t_{OH8}	C_L = 100 pF	10	100	

Table 26

(V_{DD} = 1.8V , Ta = 25°C)

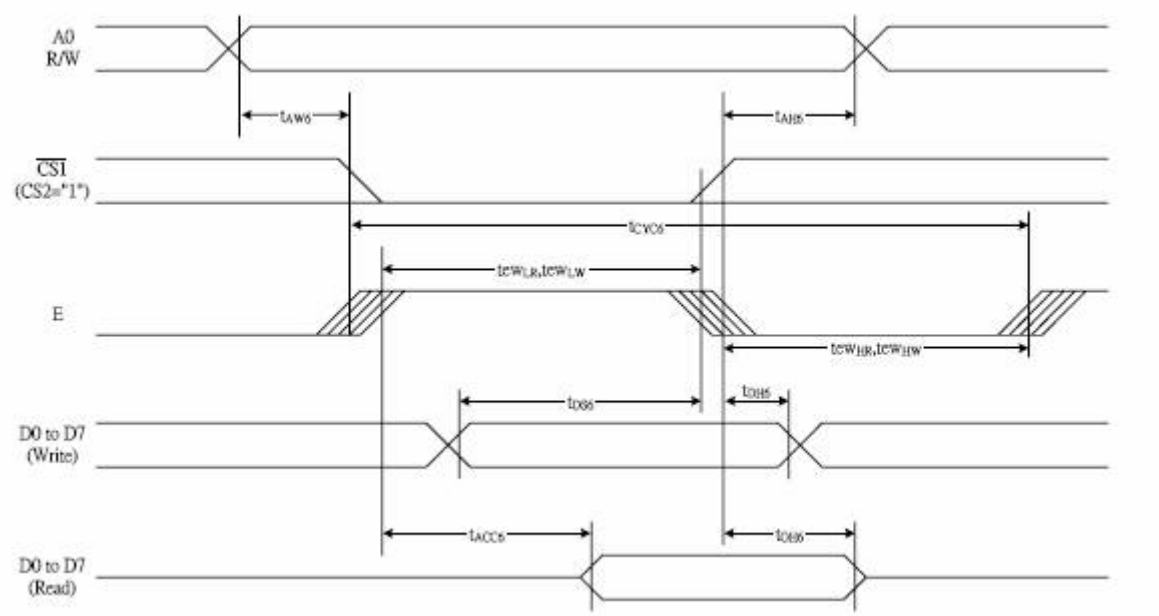
Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	t_{AH8}		0	—	ns
Address setup time		t_{AW8}		0	—	
System cycle time		t_{CYC8}		640	—	
Enable L pulse width (WRITE)	WR	t_{CCLW}		360	—	
Enable H pulse width (WRITE)		t_{CCHW}		280	—	
Enable L pulse width (READ)	RD	t_{CCLR}		360	—	
Enable H pulse width (READ)		t_{CCHR}		280		
WRITE Data setup time	D0 to D7	t_{DS8}		80	—	
WRITE Address hold time		t_{DH8}		0	—	
READ access time		t_{ACC8}	C_L = 100 pF	—	240	
READ Output disable time		t_{OH8}	C_L = 100 pF	10	200	

*1 The input signal rise time and fall time (t_r, t_f) is specified at 15 ns or less. When the system cycle time is extremely fast, ($t_r + t_f$) ≦ ($t_{CYC8} - t_{CCLW} - t_{CCHW}$) for ($t_r + t_f$) ≦ ($t_{CYC8} - t_{CCLR} - t_{CCHR}$) are specified.

*2 All timing is specified using 20% and 80% of V_{DD} as the reference.

*3 t_{CCLW} and t_{CCLR} are specified as the overlap between /CS1 being "L" (CS2 = "H") and /WR and /RD being at the "L" level.

System bus read/write characteristics 2 (6800 Series MPU)



(VDD = 3.3 V , Ta = 25°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	t_{AH6}		0	—	ns
Address setup time		t_{AW6}		0	—	
System cycle time		t_{CYC6}		240	—	
Enable L pulse width (WRITE)	WR	t_{EWLW}		80	—	
Enable H pulse width (WRITE)		t_{EWHW}		80	—	
Enable L pulse width (READ)	RD	t_{EWLR}		80	—	
Enable H pulse width (READ)		t_{EWHR}		140		
WRITE Data setup time	D0 to D7	t_{DS6}		40	—	
WRITE Address hold time		t_{DH6}		0	—	
READ access time		t_{ACC6}	C_L = 100 pF	—	70	
READ Output disable time		t_{OH6}	C_L = 100 pF	5	50	

(V_{DD} = 2.7V , Ta =25°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	t_{AH6}		0	—	ns
Address setup time		t_{AW6}		0	—	
System cycle time		t_{CYC6}		400	—	
Enable L pulse width (WRITE)	WR	t_{EWLW}		220	—	
Enable H pulse width (WRITE)		t_{EWHW}		180	—	
Enable L pulse width (READ)	RD	t_{EWLR}		220	—	
Enable H pulse width (READ)		t_{EWHR}		180	—	
WRITE Data setup time	D0 to D7	t_{DS6}		40	—	
WRITE Address hold time		t_{DH6}		0	—	
READ access time		t_{ACC6}	C_L = 100 pF	—	140	
READ Output disable time		t_{OH6}	C_L = 100 pF	10	100	

Table 29

(V_{DD} =1.8V , Ta =25°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	t_{AH6}		0	—	ns
Address setup time		t_{AW6}		0	—	
System cycle time		t_{CYC6}		640	—	
Enable L pulse width (WRITE)	WR	t_{EWLW}		360	—	
Enable H pulse width (WRITE)		t_{EWHW}		280	—	
Enable L pulse width (READ)	RD	t_{EWLR}		360	—	
Enable H pulse width (READ)		t_{EWHR}		280	—	
WRITE Data setup time	D0 to D7	t_{DS6}		80	—	
WRITE Address hold time		t_{DH6}		0	—	
READ access time		t_{ACC6}	C_L = 100 pF	—	240	
READ Output disable time		t_{OH6}	C_L = 100 pF	10	200	

*1 The input signal rise time and fall time (t_r, t_f) is specified at 15 ns or less. When the system cycle time is extremely fast, ($t_r + t_f$) ≦ ($t_{CYC6} - t_{EWLW} - t_{EWHW}$) for ($t_r + t_f$) ≦ ($t_{CYC6} - t_{EWLR} - t_{EWHR}$) are specified.
*2 All timing is specified using 20% and 80% of V_{DD} as the reference.
*3 t_{EWLW} and t_{EWLR} are specified as the overlap between $\overline{CS1}$ being "L" (CS2 = "H") and E.

IC Specification

The ST7565R identify the data bus signals by a combination of A0, /RD (E), /WR(R/W) signals. Command interpretation and execution does not depend on the external clock, but rather is performed through internal timing only, and thus the processing is fast enough that normally a busy check is not required.

In the 8080 MPU interface, commands are launched by inputting a low pulse to the RD terminal for reading, and inputting a low pulse to the /WR terminal for writing. In the 6800 Series MPU interface, the interface is placed in a read mode when an "H" signal is input to the R/W terminal and placed in a write mode when a "L" signal is input to the R/W terminal and then the command is launched by inputting a high pulse to the E terminal. Consequently, the 6800 Series MPU interface is different than the 80x86 Series MPU interface in that in the

explanation of commands and the display commands the status read and display data read /RD (E) becomes “1(H)”. In the explanations below the commands are explained using the 8080 Series MPU interface as the example.

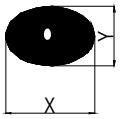
When the serial interface is selected, the data is input in sequence starting with D7.

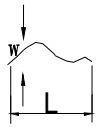
Instruction Table

Command	Command Code										Function
	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	
(1) Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0 1	LCD display ON/OFF 0: OFF, 1: ON
(2) Display start line set	0	1	0	0	1	Display start address						Sets the display RAM display start line address
(3) Page address set	0	1	0	1	0	1	1	Page address				Sets the display RAM page address
(4) Column address set upper bit	0	1	0	0	0	0	1	Most significant column address				Sets the most significant 4 bits of the display RAM column address.
Column address set lower bit	0	1	0	0	0	0	0	Least significant column address				Sets the least significant 4 bits of the display RAM column address.
(5) Status read	0	0	1	Status				0	0	0	0	Reads the status data
(6) Display data write	1	1	0	Write data								Writes to the display RAM
(7) Display data read	1	0	1	Read data								Reads from the display RAM
(8) ADC select	0	1	0	1	0	1	0	0	0	0	0 1	Sets the display RAM address SEG output correspondence 0: normal, 1: reverse
(9) Display normal/ reverse	0	1	0	1	0	1	0	0	1	1	0 1	Sets the LCD display normal/ reverse 0: normal, 1: reverse
(10) Display all points ON/OFF	0	1	0	1	0	1	0	0	1	0	0 1	Display all points 0: normal display 1: all points ON
(11) LCD bias set	0	1	0	1	0	1	0	0	0	1	0 1	Sets the LCD drive voltage bias ratio 0: 1/9 bias, 1: 1/7 bias (ST7565P)
(12) Read/modify/write	0	1	0	1	1	1	0	0	0	0	0	Column address increment At write: +1 At read: 0
(13) End	0	1	0	1	1	1	0	1	1	1	0	Clear read/modify/write
(14) Reset	0	1	0	1	1	1	0	0	0	1	0	Internal reset
(15) Common output mode select	0	1	0	1	1	0	0	0 1	*	*	*	Select COM output scan direction 0: normal direction 1: reverse direction
(16) Power control set	0	1	0	0	0	1	0	1	Operating mode			Select internal power supply operating mode
(17) V_0 voltage regulator internal resistor ratio set	0	1	0	0	0	1	0	0	Resistor ratio			Select internal resistor ratio(Rb/Ra) mode
(18) Electronic volume mode set Electronic volume register set	0	1	0	1 0	0 0	0 Electronic volume value	0	0	0	0	1	Set the V_0 output voltage electronic volume register
(19) Static indicator ON/OFF Static indicator register set	0	1	0	1 0	0 0	1 0	0 0	1 0	1 0	0 0	0 1 Mode	0: OFF, 1: ON Set the flashing mode
(20) Booster ratio set	0	1	0	1 0	1 0	1 0	1 0	1 0	0 0	0 step-up value	0	select booster ratio 00: 2x,3x,4x 01: 5x 11: 6x
(21) Power saver												Display OFF and display all points ON compound command
(22) NOP	0	1	0	1	1	1	0	0	0	1	1	Command for non-operation
(23) Test	0	1	0	1	1	1	1	*	*	*	*	Command for IC test. Do not use this command

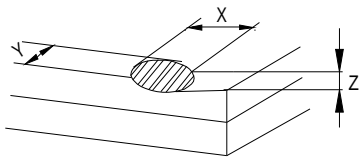
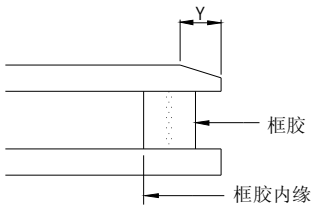
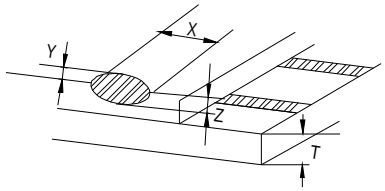
检验标准：

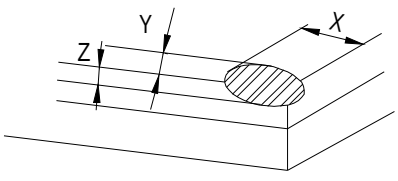
外观检测规格 The Appearance Inspection Criteria (单位 Unit：mm)

<table>
<tr><th>O</th><th>项　目
Item</th><th>规　格
Criteria</th><th>缺陷
定义
Defect
Definition</th></tr>
<tr><td>1</td><td>1.1 点状缺陷(圆形状污物,黑点,漏光点,偏反光片等)
Dot Defect (Round Dirty spot, Black spot, Leak light spot, Polarize upside down)
(V.A 外不计 Outside V.A will be Ignored)</td><td> 

<table>
<tr><th rowspan="2">尺寸Φ
Dimension</th><th>允许个数 Acceptable Number</th></tr>
<tr><th>普通方式 General Mode</th></tr>
<tr><td>Φ≦0.10</td><td>无视 Ignore</td></tr>
<tr><td>0.10<Φ≦0.20</td><td>2</td></tr>
<tr><td>0.20<Φ≦0.25</td><td>1</td></tr>
</table>
Φ=（X+Y）/2
(1) Φ≦0.10 无视,但密集不可(密集定义:直径 5mm 的圆内,黑点个数超过 5 个)两个点状物间距必须大于 10mm。
If Φ≦0.10, it will be ignored, But, concentrate is not acceptable, (Concentrate definition: If the diameter of the round is 5mm, the defect number over 5 Entries) and distance between two dots must≧10mm</td><td>次缺
Minor
Defect</td></tr>
<tr><td></td><td>1.2 线状缺陷(织维、玻璃和偏光片刮伤，黑线，花痕等)
Line Defect (Fiber, Glass and Polarizer scratch, Black line, Crack
(V.A 外不计 Outside V.A will be Ignored)</td><td> 

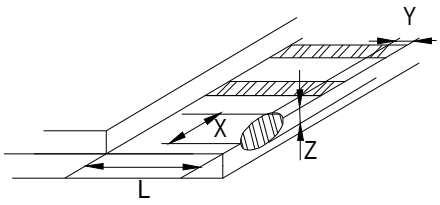
<table>
<tr><th>长(L)
Length</th><th>宽(W)
Width</th><th>允许个数
Acceptable Number</th></tr>
<tr><td>不限
No limit</td><td>W≦0.02</td><td>无视
Ignore</td></tr>
<tr><td>L≦3.0</td><td>0.02≦W≦0.03</td><td rowspan="2">2</td></tr>
<tr><td>L≦2.0</td><td>0.03≦W≦0.05</td></tr>
<tr><td>-</td><td>0.05<W</td><td>依点状规定
According to the Dot Criteria</td></tr>
</table>
(1) L 是指线状缺陷最长处；L is meaning that the longest of the line defect.
(2) 若线状有弯曲来回重复，则 W 计算所有来回线宽总和；
If there is line bending repetition, please use W to calculate the total width of the repetition lines!
(3) 两个线状物间距必须大于 10mm。
The distance between two lines must≧10mm</td><td></td></tr>
</table>

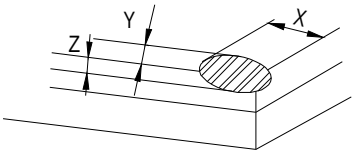
2	2.1 崩缺 Chip out	说明 Explain：(1) 所有崩缺都不可入视野范围； All of the Chip out couldn't in the Viewing Area (2) 崩缺不能触及内部电极线路。 Chip out couldn't in the internal electrode line 代号 Code Name：(X：崩裂长度 Crack Length；Y：崩裂宽度 Crack Width；Z：崩裂厚度 Crack thickness；A：LCD 边长 LCD border length W：电极线宽度 The width electrode line；L：端子长度 End length；T：单层玻璃厚度 The thickness of monolayer glass)	
		2.1.1A 表面崩缺(崩同端面)Chip out in the surface(Crack in one side)：    	次缺 Minor Defect

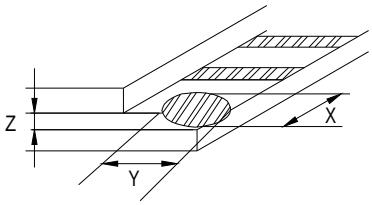
NO	项 目 Item	规 格 Criteria	缺陷定义 Defect Definitio
2	2.1 崩缺 Chip out	 	

X	Y	Z
>1/8A	≦0.3㎜	≦1/2T
≦1/8A	未进入框胶 Not in seal glue	≦T
	未进入框胶内缘 Not inside of seal glue	≦1/2T

2.1.1 B 表面崩缺(崩电脚) Chip out in the surface(Crack in the electrode foot)





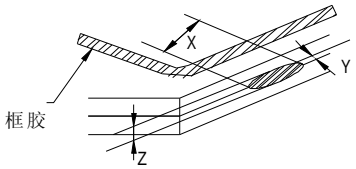


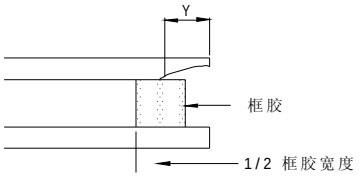
X	Y	Z
>1/8A	≦ 0.3mm	≦1/2T
≦1/8A	≦1/2L	≦T
≦1/8A 且≦2mm	≦L	≦1/2T

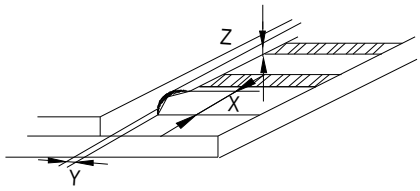
注：崩缺与电极距离必须大于 1 个电极
Note: The distance of chip out and electrode should be larger than one electrode.

次缺 Minor Defect

2.1.2 中间崩缺 Chip out in the middle

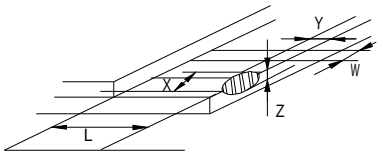


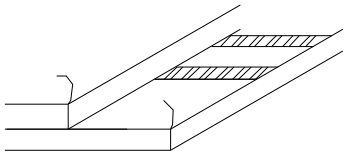
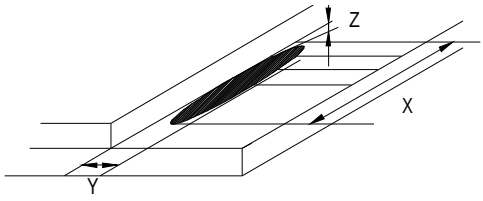




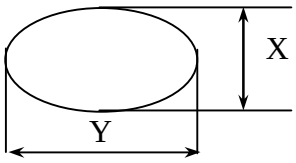
X	Y	Z
≦1/8A	未进入框胶 Not in seal glue	Z≦2T
	未进入 1/2 框胶宽度 Not in 1/2 width of seal glue	Z≦1/2T

次缺 Minor Defect

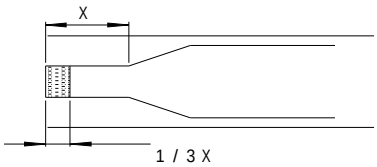
<table>
<tr><th>NO</th><th>项 目
Item</th><th>规 格
Criteria</th><th>缺陷定义
Defect Definition</th></tr>
<tr><td rowspan="4">2</td><td>2.1 崩缺
Chip out</td><td>2.1.4 崩电极(含崩角、崩边)
Crack the electrode (including the electrode corner or side)
 

<table><tr><td>X</td><td>Y</td><td>Z</td></tr><tr><td>>1/8A</td><td>≦1/5L</td><td rowspan="3">≦1/2T</td></tr><tr><td>≦1/8A</td><td>≦1/3L</td></tr><tr><td>≦1/4W</td><td>≦2/3L</td></tr></table></td><td>次缺
Minor Defect</td></tr>
<tr><td>2.2 崩裂 Crack</td><td> 
(1) 框胶周围裂痕拒收；
Around the seal glue is reject
(2) 电极处裂痕长度大于0.5mm 拒收。
The length of crack in the electrode longer than 0.5mm is reject.</td><td>次缺
Minor Defect</td></tr>
<tr><td>2.3 切裂不良
Cutting/ Breaking defect</td><td>2.3.1 多余边 Superabundance side
 

<table><tr><td>X</td><td>Y</td><td>Z</td></tr><tr><td>>1/8A</td><td rowspan="2">≤1/5L</td><td>≦1/2T</td></tr><tr><td>≦1/8A</td><td>1/2T≦Z≦T</td></tr></table></td><td>次缺
Minor Defect</td></tr>
<tr><td>2.3.2 端面不平 The side is not even
超出工程图尺寸公差拒收 Over the tolerance of engineering drawing is reject；</td><td>次缺
Minor Defect</td></tr>
<tr><td>3</td><td>3.1 偏/反光片
Polarizer upside down</td><td>偏光片多贴、少贴、错贴拒收；
Polarizer more, less or wrong stick is reject</td><td>主缺
Major Defect</td></tr>
</table>

	3.2 偏光片气泡 Void in Polarizer (V.A 外不主计 Outside V.A will be Ignored)	 Φ=(X+Y)/ 注 Note：气泡必须无色差影响，否则按 1.1 点状缺陷计，且两点间距必须大于 10mm。Air bubble should be in the same color, or will as 1.1mm dot defect, and the distance between the two dots should be larger than 10mm. 尺寸Φ Dimension / 允许个数 Acceptable number Φ≦0.20 / 无视 Ignore 0.20≦Φ≦0.40 / 2 0.40≦Φ / 0	次缺 Minor Defect
	3.3 偏光片偏位 Polarizer shift from its position	贴片位置超出玻璃边及进入视区拒收。 Polarizer extrudes glass edge and in the viewing area is reject.	次缺 Minor Defect

NO	项 目 Item	规 格 Criteria	缺陷定义 Defect Definition
	3.5 保护膜翘起 Protective layer separated from polarizer	(1) 能贴覆的保护膜翘起可接收；无法贴覆的保护膜翘起，长边须小于 1/3 边长，短边须小于 1/2 边长； If the protective layer could be stick once again, it will be acceptable; but if it isn't, and the long side should less than 1/3 of polarizer length, short side should less than 1/2 of polarizer length. (2) 保护膜翘起导致偏光片有明显划伤、镜脏拒收。 Protective layer separated from polarizer lead to the polarizer is evident crack or dirty is reject.	
4	彩虹 Rainbow of backlight color	有明显有异色拒收或依限度样板。 If it is evident has different color is reject or according to limited sample	次缺 Minor Defect
5	底色 Different background color	同批货品底色有明显差异拒收或依限度样板。 One batch products have the different background color is reject or according to limited sample	次缺 Minor Defect
6	导电点 Contact Dot	导电胶外露拒收。 Contact glue besides is reject	次缺 Minor

			Defect
7	边框胶 End sealing	(1) 密封不良拒收； Pressurize defect is reject (2) 进入视区拒收； End sealing in the viewing area is reject (3) 宽度小于 0.35mm 拒收； Width less than 0.35mm is reject (4) 边框胶夹缝处(电极线区域和其它有 ITO 位置)有液晶残留和脏物拒收； There is liquid crystal and dirt in electrode line area and other ITO position is reject. (5) 边框胶内气泡：需保留 1/2 框胶宽度； There is air bubble in end sealing: need to keep 1/2 end sealing width (6) 边框胶内缘毛边入视区拒收，边框凸起≤1/3 边框宽度，边框变细≤1/2 边框宽度。 End sealing in the viewing area is reject, frame heave no more than 1/3 frame width, frame thin no more than 1/2 frame width	主缺 Major 次缺 Minor 次缺 Minor 次缺 Minor Defect 次缺 Minor 次缺 Minor Defect
8	8.1 密封性 Pressurize quality	密封不良拒收。 Pressurize defect is reject.	主缺 Major Defect
	8.2 封口胶方向 End sealing bearing	封口胶方向需与工程图一致，否则拒收。 End sealing bearing should be the same as engineering drawing, or reject.	次缺 Minor Defect
	8.3 胶污 Glue dirty	拒收； Reject	次缺 Minor Defect
	8.4 胶长、厚、偏 End sealing dimension	超出工程图规格拒收；胶偏未盖住开口拒收。 Over engineering drawing is reject, end sealing deflect and don’t cover the hatch is reject	次缺 Minor Defect
	8.5 透胶 End sealing over permeate	 封口胶透胶进入视区拒收。 Into viewing area is reject X：封口深度 The deepness of the seal	次缺 Minor Defect 次缺 Minor Defect
9	PIN 不良 PIN defect	(1) PIN 组装位置偏移需符合工程图规格；若未注明则 PIN 中心与电极中心偏差必须在 0.25mm 内； The position of install pin should be according to engineering drawing; If it isn’t note, the warp of middle of pin and middle of electrode should in 0.25mm (2) PIN 胶水厚度不可高出偏光片，且涂布范围不得覆盖到偏	次缺 Minor Defect

		光片；The thickness pin glue couldn’t exceeds polarizer, and cover area couldn’t cover polarizer (3) PIN 胶水不得流至 PIN 脚； Pin glue couldn’t flow to PIN (4) PIN 胶水涂布不足：导电端子正背面均需有胶，胶量最少需覆盖背面 PIN 最低点处； Pin glue not enough: conduct electric pins should have glue in just and back sides, the less should cover the lowest of pin in back side. (5) PIN 脚歪斜角度公差须于±5º 范围内(若工程图另有规定则依工程图为依据)；	

NO	项　　目	规　　格	缺陷定义
9	PIN 不良 PIN defect	The tolerance of PIN deflection should less than ±5º(Unless there’s other prescribe, according to engineering drawing) (6) PIN 本体刮伤不可造成铜裸露； Pin crack couldn’t lead to copper bareness (7) PIN 表面不得脏污及生锈； The surface of PIN couldn’t be dirty or rusty (8) 夹 PIN 胶内有汽泡但未造成破洞可允收； There’s air bubble in PIN glue, but won’t lead to break is acceptable (9) PIN 型式、PIN 数、PIN 长、PIN 弯角、尺寸需与工程图不一致拒收；If the mode, number, length, bend angle, dimension of PIN won’t according to engineering drawing is reject. (10) PIN 不能有皱痕及污损。 There couldn’t have crimple or defile at PIN	次缺 Minor Defect

<table>
<tr>
<td>10</td>
<td>油墨印刷
Printing ink print</td>
<td>(1) 图形印刷需与工程图一致，不可错误、漏印、颜色错误或未烘干；
Print figure should according to engineering drawing, couldn’t be wrong, lack, color wrong or not drying;
(2) 油墨色泽有明显偏差拒收或依限度版；
Color of printing ink have evident warp is reject or according to limited sample.
(3) 印刷框线不连续(断线处按线状缺陷计)或粗细不一拒收；
The line of printing frame discontinuity or thickness different is reject
(4) 印刷框线倾斜必须小于±1º；
The incline of line of printing frame should less than ±1º
(5) 印刷位置偏移：依工程图规格判定；若工程图未标识公差时偏位不可超过±0.20㎜且不可碰到显示字体；
Printing position excursion: according to engineering drawing to estimate; If the it isn’t sign tolerance, it couldn’t exceed ±0.20mm, and couldn’t affect the display font.
(6) 印刷线宽判定 Printing line width estimation：
<table>
<tr><th>W：设计宽度
Design width</th><th>P：实际印刷线宽
Actual printing width</th></tr>
<tr><td>W≦0.40</td><td>|W-P|≦1/2W</td></tr>
<tr><td>W>0.40</td><td>|W-P|≦0.20</td></tr>
</table>
注：如工程图上有规定，则依工程图所示。
Note: If the engineering drawing has regulation, please according to it.
(7) 印刷图案凹点、凸点、针孔判定：
Printing pattern concave dot, protruding dot, pin hole estimation:
<table>
<tr><th>尺　寸 Dimension</th><th>允许个数
Acceptable number</th></tr>
<tr><td>Φ<0.10</td><td>无　视 Ignore</td></tr>
<tr><td>0.10<Φ≦0.25</td><td>2</td></tr>
<tr><td>0.25<Φ</td><td>0</td></tr>
</table>
注：两点间距必须大于 5mm。
Note: The distance between the two dots should larger than 5mm.
(8) 印刷图案黑点，刮花参见点状线状缺陷规格；
Printing pattern have black dot, crack, please according to Dot and</td>
<td>主缺
Major Defect
次缺
Minor Defect
次缺
Minor Defect
次缺
Minor Defect
次缺
Minor Defect
次缺
Minor Defect
次缺
Minor Defect
次缺
Minor</td>
</tr>
</table>

		Line Defect Criteria (8) 毛边：起伏幅度须≦0.20㎜。 Burred: Wave range should no more than 0.20mm	Defect