

INA105

Precision Unity Gain DIFFERENTIAL AMPLIFIER

FEATURES

- CMR 86dB min OVER TEMPERATURE
- GAIN ERROR: 0.01% max
- NONLINEARITY: 0.001% max
- NO EXTERNAL ADJUSTMENTS REQUIRED
- EASY TO USE
- COMPLETE SOLUTION
- HIGHLY VERSATILE
- LOW COST
- PLASTIC DIP, TO-99 HERMETIC METAL, AND SO-8 SOIC PACKAGES

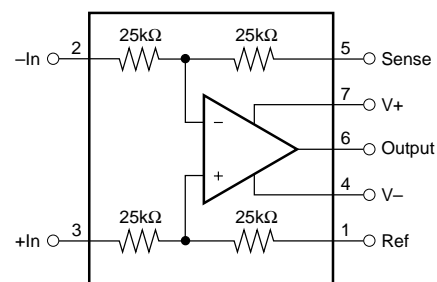
APPLICATIONS

- DIFFERENTIAL AMPLIFIER
- INSTRUMENTATION AMPLIFIER BUILDING BLOCK
- UNITY-GAIN INVERTING AMPLIFIER
- GAIN-OF-1/2 AMPLIFIER
- NONINVERTING GAIN-OF-2 AMPLIFIER
- AVERAGE VALUE AMPLIFIER
- ABSOLUTE VALUE AMPLIFIER
- SUMMING AMPLIFIER
- SYNCHRONOUS DEMODULATOR
- CURRENT RECEIVER WITH COMPLIANCE TO RAILS
- 4mA TO 20mA TRANSMITTER
- VOLTAGE-CONTROLLED CURRENT SOURCE
- ALL-PASS FILTERS

DESCRIPTION

The INA105 is a monolithic Gain = 1 differential amplifier consisting of a precision op amp and on-chip metal film resistors. The resistors are laser trimmed for accurate gain and high common-mode rejection. Excellent TCR tracking of the resistors maintains gain accuracy and common-mode rejection over temperature.

The differential amplifier is the foundation of many commonly used circuits. The INA105 provides this precision circuit function without using an expensive precision resistor network. The INA105 is available in 8-pin plastic DIP, SO-8 surface-mount and TO-99 metal packages.



SPECIFICATIONS

ELECTRICAL

At +25°C, $V_{CC} = \pm 15V$, unless otherwise noted.

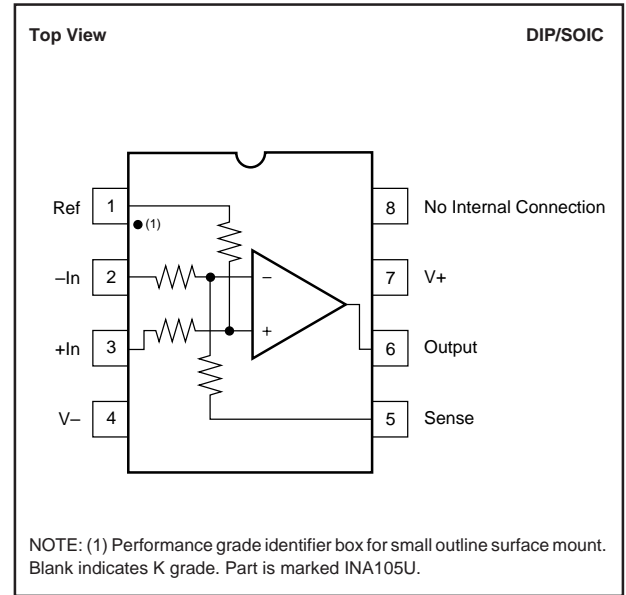
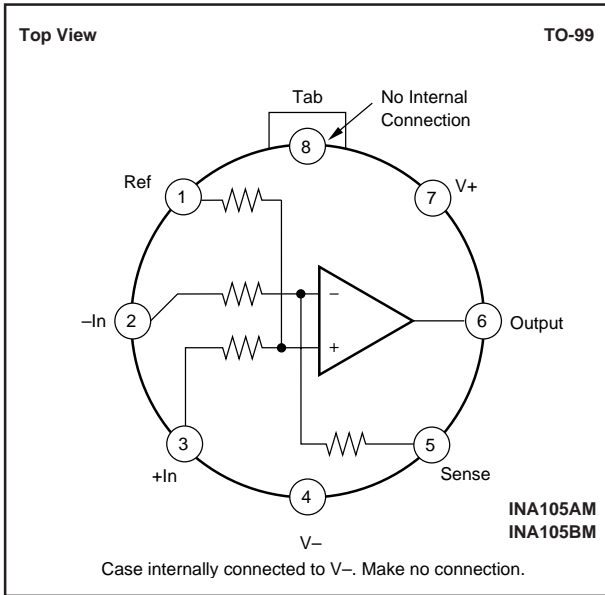
PARAMETER	CONDITIONS	INA105AM			INA105BM			INA105KP, KU			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
GAIN											
Initial ⁽¹⁾			1			*			*		V/V
Error			0.005	0.01		*	*		0.01	0.025	%
vs Temperature			1	5		*	*		*	*	ppm/°C
Nonlinearity ⁽²⁾			0.0002	0.001		*	*		*	*	%
OUTPUT											
Rated Voltage	$I_O = +20mA, -5mA$	10	12		*	*		*	*		V
Rated Current	$V_O = 10V$	+20, -5			*			*			mA
Impedance			0.01			*			*		Ω
Current Limit	To Common		+40/-10			*			*		mA
Capacitive Load	Stable Operation		1000			*			*		pF
INPUT											
Impedance ⁽³⁾	Differential		50			*			*		k Ω
	Common-Mode		50			*			*		k Ω
Voltage Range ⁽⁴⁾	Differential	± 10			*			*			V
	Common-Mode	± 20			*			*			V
Common-Mode Rejection ⁽⁵⁾	$T_A = T_{MIN}$ to T_{MAX}	80	90		86	100		72	*		dB
OFFSET VOLTAGE											
Initial	RTO ^{(6), (7)}		50	250		*	*		*	500	μV
vs Temperature			5	20		5	10		*	*	$\mu V/°C$
vs Supply	$\pm V_S = 6V$ to $18V$		1	25		*	15		*	*	$\mu V/V$
vs Time			20			*			*		$\mu V/mo$
OUTPUT NOISE VOLTAGE											
$f_B = 0.01Hz$ to $10Hz$	RTO ^{(6), (8)}		2.4			*			*		$\mu Vp-p$
$f_O = 10kHz$			60			*			*		nV/\sqrt{Hz}
DYNAMIC RESPONSE											
Small Signal Bandwidth	-3dB		1			*			*		MHz
Full Power Bandwidth	$V_O = 20Vp-p$	30	50		*	*		*	*		kHz
Slew Rate		2	3		*	*		*	*		V/ μs
Settling Time: 0.1%	$V_O = 10V$ Step		4			*			*		μs
0.01%	$V_O = 10V$ Step		5			*			*		μs
0.01%	$V_{CM} = 10V$ Step, $V_{DIFF} = 0V$		1.5			*			*		μs
POWER SUPPLY											
Rated			± 15			*			*		V
Voltage Range	Derated Performance	± 5		± 18	*	*	*	*	*	*	V
Quiescent Current	$V_O = 0V$		± 1.5	± 2		*	*		*	*	mA
TEMPERATURE RANGE											
Specification		-40		+85	*		*	*		*	°C
Operation		-55		+125	*		*	-40		+85	°C
Storage		-65		+150	*		*	-40		+125	°C

* Specification same as for INA105AM.

NOTES: (1) Connected as difference amplifier (see Figure 4). (2) Nonlinearity is the maximum peak deviation from the best-fit straight line as a percent of full-scale peak-to-peak output. (3) 25k Ω resistors are ratio matched but have $\pm 20\%$ absolute value. (4) Maximum input voltage without protection is 10V more than either $\pm 15V$ supply ($\pm 25V$). Limit I_{IN} to 1mA. (5) With zero source impedance (see "Maintaining CMR" section). (6) Referred to output in unity-gain difference configuration. Note that this circuit has a gain of 2 for the operational amplifier's offset voltage and noise voltage. (7) Includes effects of amplifier's input bias and offset currents. (8) Includes effects of amplifier's input current noise and thermal noise contribution of resistor network.

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PIN CONFIGURATIONS



ABSOLUTE MAXIMUM RATINGS

Supply	±18V
Input Voltage Range	±V _S
Operating Temperature Range: M	-55°C to +125°C
P, U	-40°C to +85°C
Storage Temperature Range: M	-65°C to +150°C
P, U	-40°C to +125°C
Lead Temperature (soldering, 10s) M, P	+300°C
Wave Soldering (3s, max) U	+260°C
Output Short Circuit to Common	Continuous

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER ⁽¹⁾	TEMPERATURE RANGE
INA105AM	TO-99 Metal	001	-40°C to +85°C
INA105BM	TO-99 Metal	001	-40°C to +85°C
INA105KP	8-Pin Plastic DIP	006	-40°C to +85°C
INA105KU	8-Pin SOIC	182	-40°C to +85°C

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

TYPICAL PERFORMANCE CURVES

At $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$, unless otherwise noted.

STEP RESPONSE



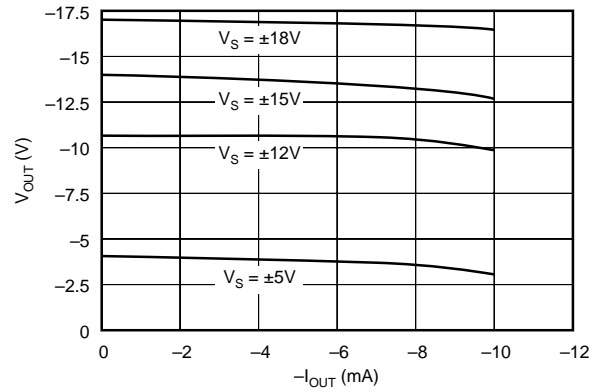
SMALL SIGNAL RESPONSE (No Load)



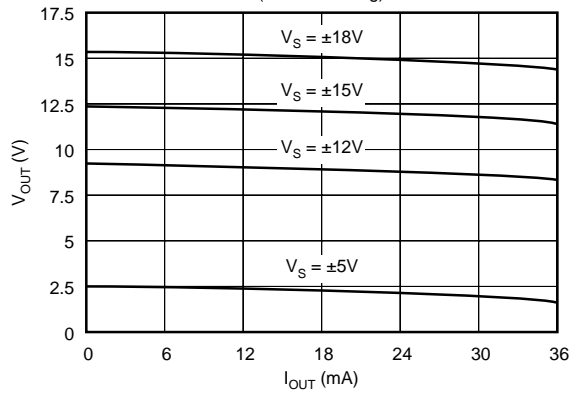
SMALL SIGNAL RESPONSE ($R_{\text{LOAD}} = \infty\Omega$, $C_{\text{LOAD}} = 1000\text{pF}$)



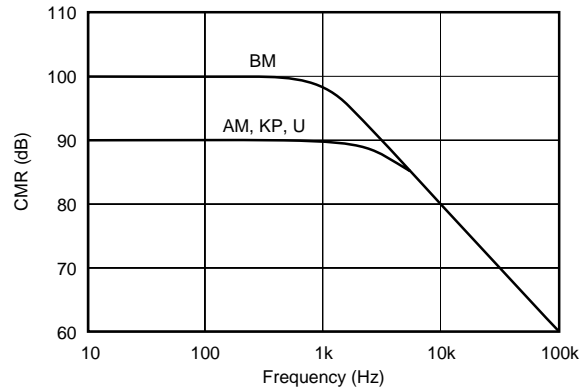
MAXIMUM V_{OUT} vs I_{OUT} (Negative Swing)



MAXIMUM V_{OUT} vs I_{OUT} (Positive Swing)



CMR vs FREQUENCY



TYPICAL PERFORMANCE CURVES (CONT)

At $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$, unless otherwise noted.



APPLICATION INFORMATION

Figure 1 shows the basic connections required for operation of the INA105. Power supply bypass capacitors should be connected close to the device pins.

The differential input signal is connected to pins 2 and 3 as shown. The source impedances connected to the inputs must be nearly equal to assure good common-mode rejection. A 5Ω mismatch in source impedance will degrade the common-mode rejection of a typical device to approximately 80dB. If the source has a known mismatch in source impedance, an additional resistor in series with one input can be used to preserve good common-mode rejection.

The output is referred to the output reference terminal (pin 1) which is normally grounded. A voltage applied to the Ref terminal will be summed with the output signal. This can be used to null offset voltage as shown in Figure 2. The source impedance of a signal applied to the Ref terminal should be less than 10Ω to maintain good common-mode rejection.

Do not interchange pins 1 and 3 or pins 2 and 5, even though nominal resistor values are equal. These resistors are laser trimmed for precise resistor ratios to achieve accurate gain and highest CMR. Interchanging these pins would not provide specified performance.



FIGURE 1. Basic Power Supply and Signal Connections.



FIGURE 2. Offset Adjustment.



FIGURE 3. Precision Difference Amplifier.



FIGURE 4. Precision Instrumentation Amplifier.

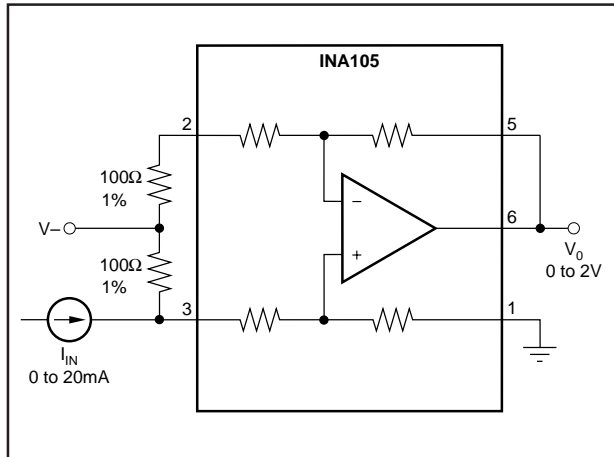


FIGURE 5. Current Receiver with Compliance to Rails.



FIGURE 6. Precision Unity-Gain Inverting Amplifier.

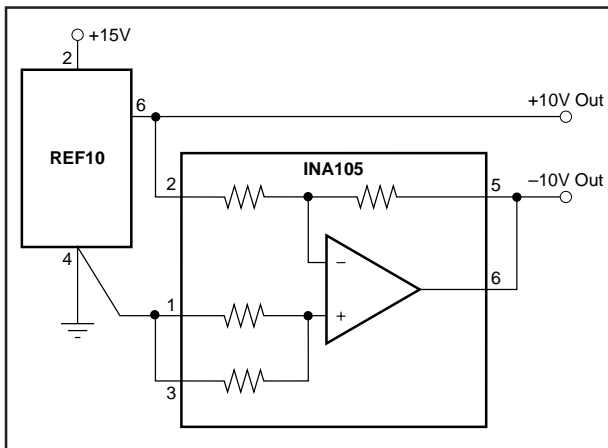


FIGURE 7. ±10V Precision Voltage Reference.

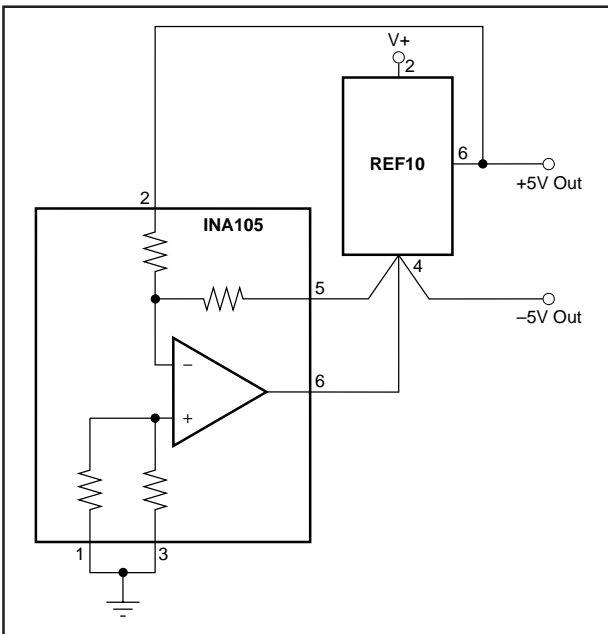


FIGURE 8. ±5V Precision Voltage Reference.

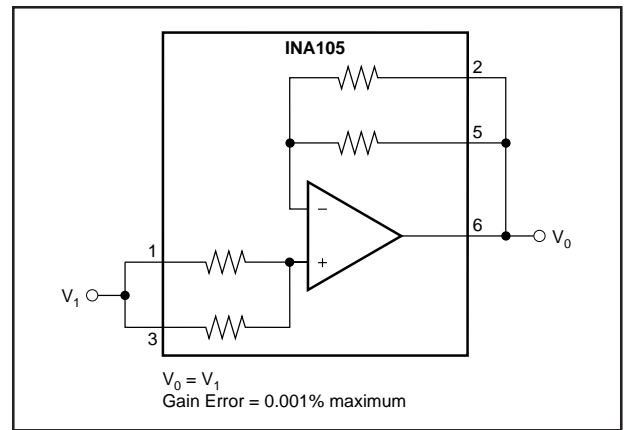


FIGURE 9. Precision Unity-Gain Buffer.

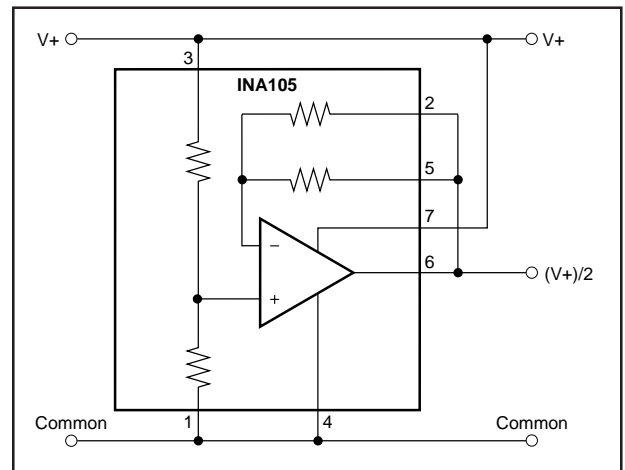


FIGURE 10. Pseudoground Generator.

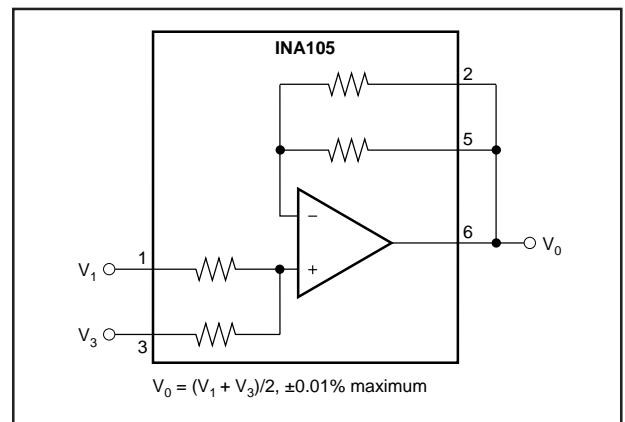


FIGURE 11. Precision Average Value Amplifier.



FIGURE 12. Precision (G = 2) Amplifier.



FIGURE 13. Precision Summing Amplifier.



FIGURE 14. Precision Gain = 1/2 Amplifier.



FIGURE 15. Precision Bipolar Offsetting.

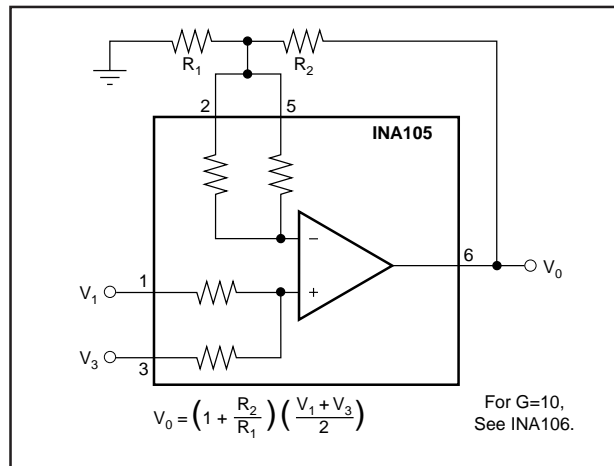


FIGURE 16. Precision Summing Amplifier with Gain.



FIGURE 17. Instrumentation Amplifier Guard Drive Generator.



FIGURE 18. Precision Summing Instrumentation Amplifier.

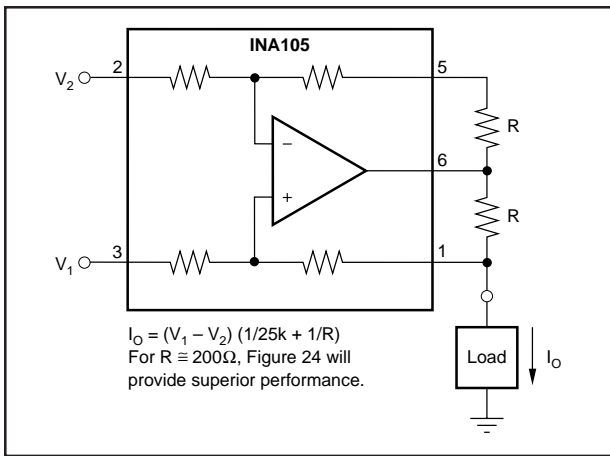


FIGURE 19. Precision Voltage-to-Current Converter with Differential Inputs.

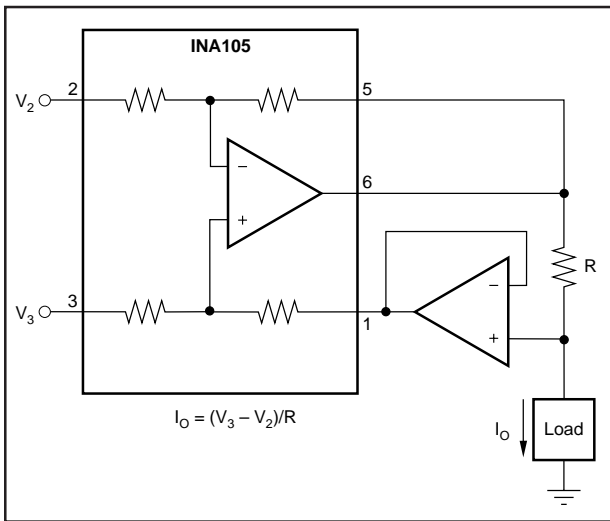


FIGURE 20. Differential Input Voltage-to-Current Converter for Low I_{OUT} .

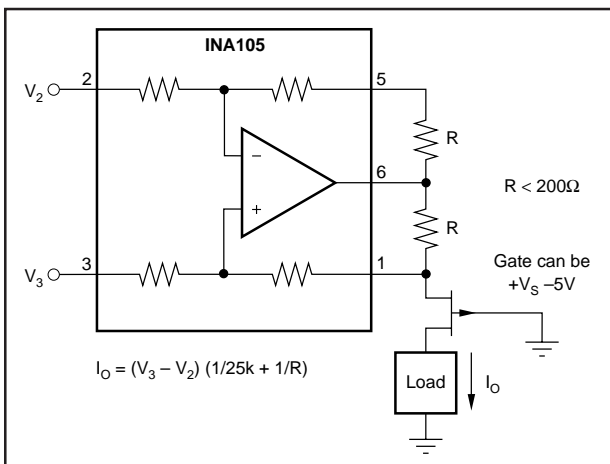


FIGURE 21. Isolating Current Source.



FIGURE 22. Differential Output Difference Amplifier.



FIGURE 23. Isolating Current Source with Buffering Amplifier for Greater Accuracy.



FIGURE 24. Window Comparator with Window Span and Window Center Inputs.



FIGURE 25. Precision Voltage-Controlled Current Source with Buffered Differential Inputs and Gain.



FIGURE 26. Digitally Controlled Gain of ±1 Amplifier.



FIGURE 27. Boosting Instrumentation Amplifier Common-Mode Range From ± 5 to ± 7.5 V with 10V Full-Scale Output.



FIGURE 28. Precision Absolute Value Buffer.

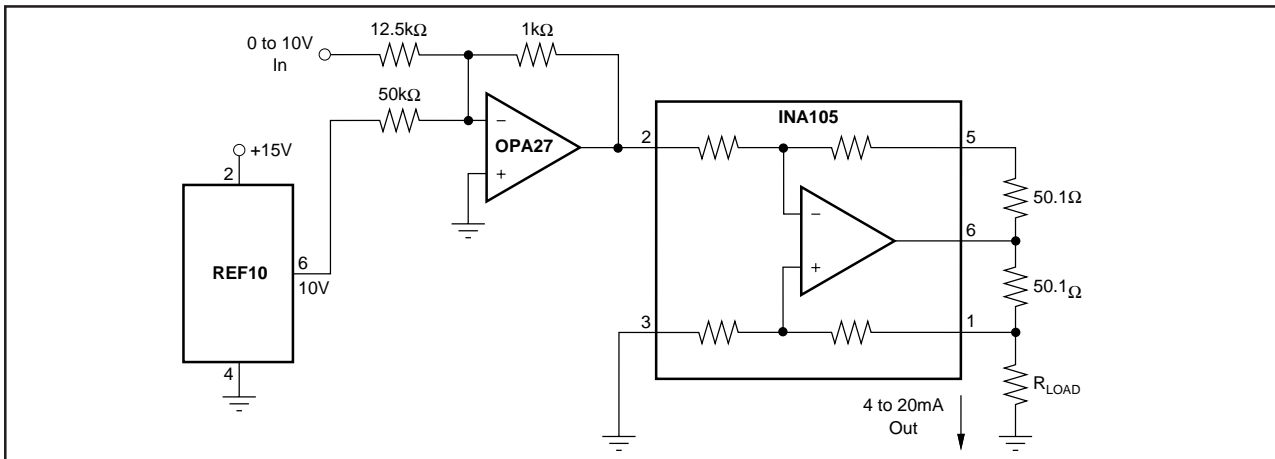


FIGURE 29. Precision 4-20mA Current Transmitter.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA105AM	NRND	TO-99	LMC	8	1	Green (RoHS & no Sb/Br)	AU	N / A for Pkg Type		INA105AM	
INA105BM	NRND	TO-99	LMC	8	1	Green (RoHS & no Sb/Br)	AU	N / A for Pkg Type		INA105BM	
INA105KP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		INA105KP	Samples
INA105KPG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		INA105KP	Samples
INA105KU	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	INA 105U	Samples
INA105KU/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	INA 105U	Samples
INA105KU/2K5E4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	INA 105U	Samples
INA105KUE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	INA 105U	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA105KU/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA105KU/2K5	SOIC	D	8	2500	367.0	367.0	35.0

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