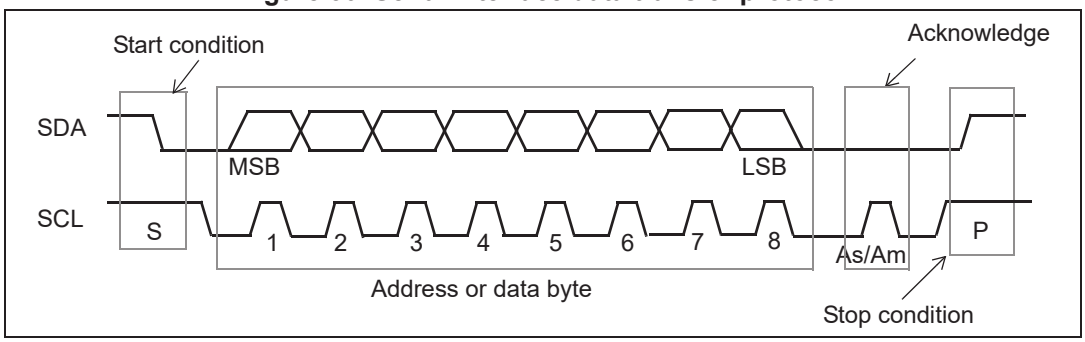
4 I²C control interface

The VL6180X is controlled over an I²C interface. The default I²C address is 0x29 (7-bit). This section describes the I²C protocol.

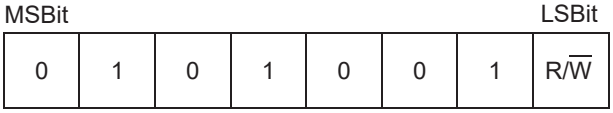
Figure 30. Serial interface data transfer protocol



Information is packed in 8-bit packets (bytes) always followed by an acknowledge bit, As for sensor acknowledge and Am for master acknowledge. The internal data is produced by sampling SDA at a rising edge of SCL. The external data must be stable during the high period of SCL. The exceptions to this are start (S) or stop (P) conditions when SDA falls or rises respectively, while SCL is high.

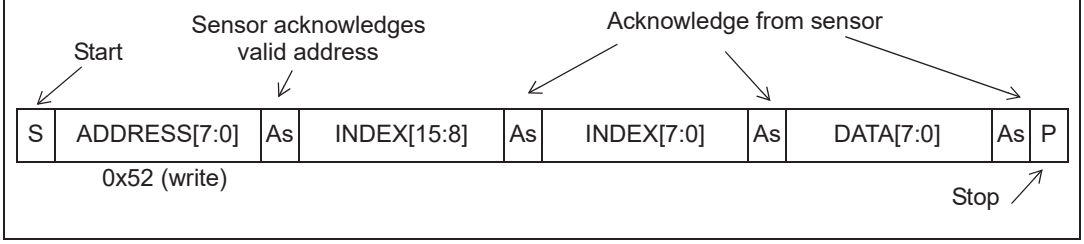
A message contains a series of bytes preceded by a start condition and followed by either a stop or repeated start (another start condition but without a preceding stop condition) followed by another message. The first byte contains the device address (0x52) and also specifies the data direction. If the least significant bit is low (0x52) the message is a master write to the slave. If the lsb is set (0x53) then the message is a master read from the slave.

Figure 31. I²C device address



All serial interface communications with the sensor must begin with a start condition. The sensor acknowledges the receipt of a valid address by driving the SDA wire low. The state of the read/write bit (lsb of the address byte) is stored and the next byte of data, sampled from SDA, can be interpreted. During a write sequence the second and third bytes received provide a 16-bit index which points to one of the internal 8-bit registers.

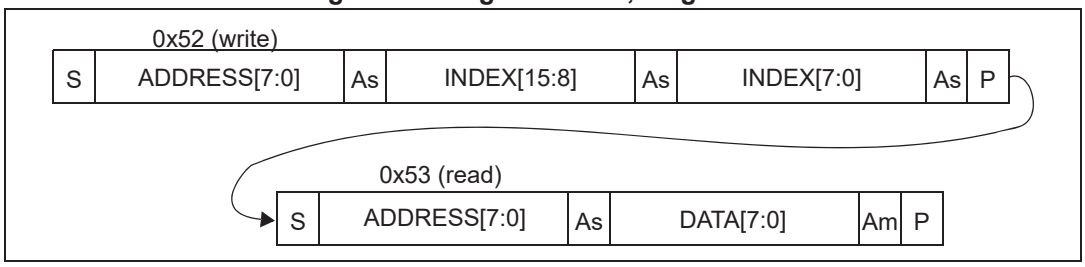
Figure 32. Single location, single write)



As data is received by the slave it is written bit by bit to a serial/parallel register. After each data byte has been received by the slave, an acknowledge is generated, the data is then stored in the internal register addressed by the current index.

During a read message, the contents of the register addressed by the current index is read out in the byte following the device address byte. The contents of this register are parallel loaded into the serial/parallel register and clocked out of the device by the falling edge of SCL.

Figure 33. Single location, single read



At the end of each byte, in both read and write message sequences, an acknowledge is issued by the receiving device (that is, the sensor for a write and the master for a read).

A message can only be terminated by the bus master, either by issuing a stop condition or by a negative acknowledge (that is, **not** pulling the SDA line low) after reading a complete byte during a read operation.

The interface also supports auto-increment indexing. After the first data byte has been transferred, the index is automatically incremented by 1. The master can therefore send data bytes continuously to the slave until the slave fails to provide an acknowledge or the master terminates the write communication with a stop condition. If the auto-increment feature is used the master does **not** have to send address indexes to accompany the data bytes.

Figure 34. Multiple location write

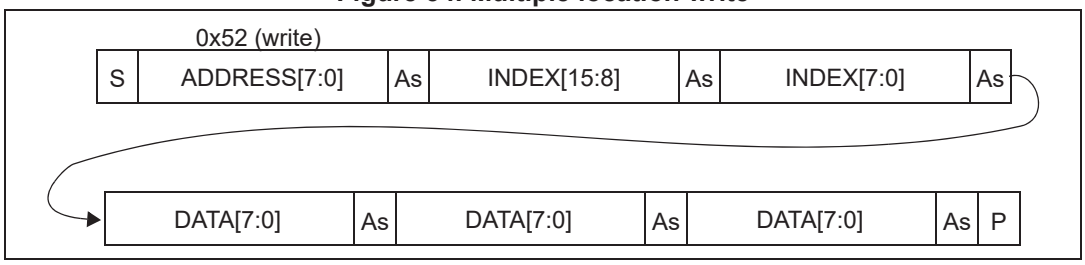
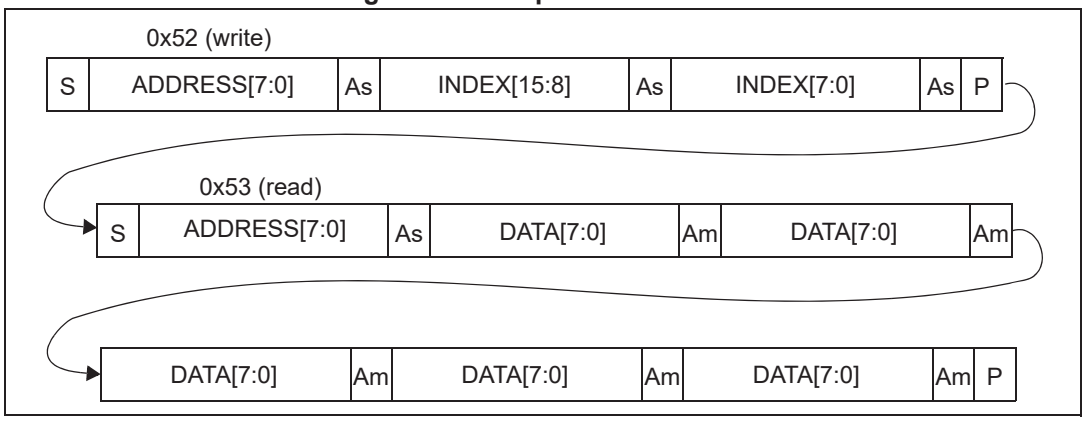


Figure 35. Multiple location read



4.1 I²C interface - timing characteristics

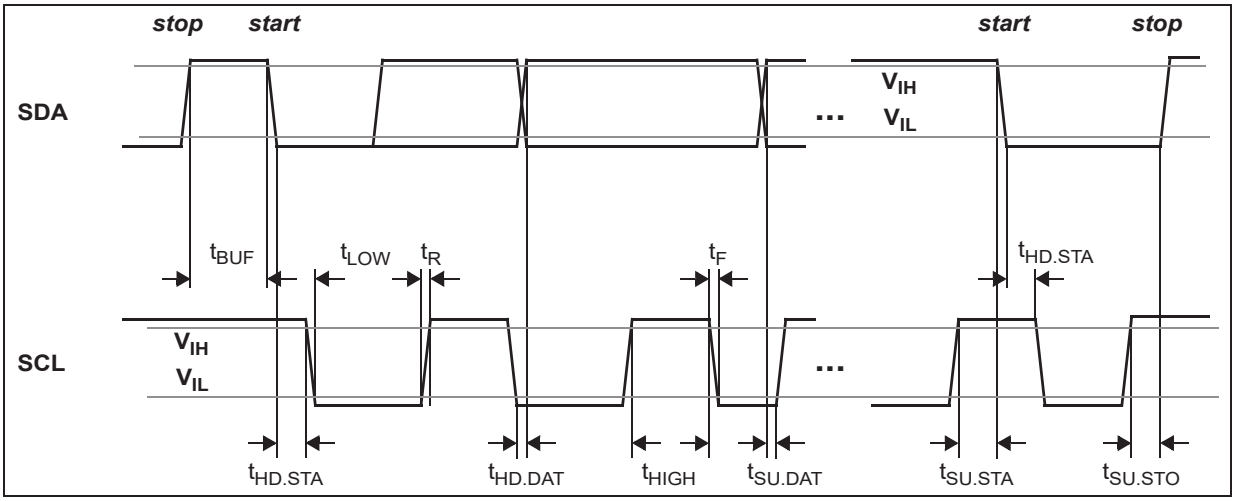
Timing characteristics are shown in *Table 21*. Please refer to *Figure 36* for an explanation of the parameters used.

Table 21. I²C interface - timing characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Unit
F_{I2C}	Operating frequency	0	-	400(1)	kHz
t_{LOW}	Clock pulse width low	0.5	-	-	µs
t_{HIGH}	Clock pulse width high	0.26	-	-	µs
t_{SP}	Pulse width of spikes which are suppressed by the input filter	-	-	50	ns
t_{BUF}	Bus free time between transmissions	0.5	-	-	µs
$t_{HD.STA}$	Start hold time	0.26	-	-	µs
$t_{SU.STA}$	Start set-up time	0.26	-	-	µs
$t_{HD.DAT}$	Data in hold time	0	-	-	µs
$t_{SU.DAT}$	Data in set-up time	50	-	-	ns
t_R	SCL/SDA rise time	-	-	120	ns
t_F	SCL/SDA fall time	-	-	120	ns
$t_{SU.STO}$	Stop set-up time	0.26	-	-	µs
Ci/o	Input/output capacitance (SDA)	-	-	4	pF
Cin	Input capacitance (SCL)	-	-	4	pF
C_L	Load capacitance	-	125	-	pF

1. The maximum bus speed may also be limited by the combination of load capacitance and pull-up resistor. Please refer to the I²C specification for further information.

Figure 36. I²C timing characteristics



All timing characteristics are measured with respect to V_{IL_MAX} or V_{IH_MIN}.