Description	2” TFT LCD Module with resistive Touch Panel
Model Name	KD020QVTMA008-RT
Product Revision	First revision
Doc. Revision	1.0
Date	2017.03.18

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1. Summary

This is a color active matrix TFT (Thin Film Transistor) LCD (liquid crystal display) that uses amorphous silicon TFT as a switching device. This model is composed of a transmissive type TFT-LCD Panel, driver circuit, and back-light unit. The resolution of this 2.0" TFT-LCD contains 240x320 pixels, and it can display up to 65K/262K colors.

2. Features

a. Low input voltage: 3.3V (typ)
b. Display colors of TFT LCD: 65K/262K colors
c. Interface: 8/9/16/18bit MCU interface
3/4 SPI + 16/18bit RGB interface
3-line/4-line serial interface

3. General Specifications

Parameter		Specifications	Unit
Display area (AA)		30.60(H)*40.80(V)	mm
Driver element		TFT active matrix	-
Display colors		65K/262K	colors
Number of pixels		240(RGB)*320	dots
Pixel pitch		0.1275(H)*0.1275(V)	mm
View angle direction		6:00	O'Clock
Controller IC		ST7789V	-
Temperature	Operation	-20 - +70	°C
	Storage	-30 - +80	°C

4. Mechanical Information

Item	Min	Typ	Max	Unit	Remark
Horizontal(H)		35.8		mm	-
Vertical(V)		52.1		mm	-
Depth(D)		3.70		mm	-
Weight		TBD		g	-

5. Input terminal pin assignment

Pin	Symbol	Description	Remark
1	GND	Ground	P
2	VCI	Supply voltage(3.3V)	P
3	IOVCC	Supply voltage (1.65V - 3.3V)	P
4	IM2	MPU parallel interface bus and serial interface select. Fix this pin at VCI or GND.	I
5	IM1		I
6	IM0		I
7	RESET	This signal resets the device and must be applied to properly initialize the chip.	I
8	CS	Chip select input pin ("Low" enable). Fix to pin to VCI or GND when not in use.	I
9	DC(SPI-SCL)	-Display data/command selection pin in parallel interface. DC="1": display data or parameter DC="0": command -Serial interface clock. If not in use please fix this pin to VCI or GND.	I
10	WR(SPI-RS)	-Write enable in parallel interface. -Display data/command selection pin in 4-line serial interface mode. If not in use please fix this pin to VCI or GND.	I
11	RD	Serves as a read signal and MCU read data at the rising edge. If not in use please fix this pin to VCI or GND.	I
12	VSYNC	Frame synchronizing signal for RGB interface operation. If not in use please fix this pin to VCI or GND.	I
13	HSYNC	Line synchronizing signal for RGB interface operation. If not in use please fix this pin to VCI or GND.	I
14	ENABLE	Data enable signal for RGB interface operation. fix this pin at VCI or GND when not in use.	
15	DOTCLK	Dot clock signal for RGB interface operation. Fix this pin at VCI or GND when not in use.	
16	SDA	Serial input signal. The data is latched on the rising edge of the SCL signal. fix this pin at VCI or GND when not in use.	
17-34	DB0-DB17	18-bit parallel bi-directional data bus for MCU system and RGB interface mode . Fix to GND level when not in use	I/O
35	SDO	SPI interface output pin. -The data is output on the falling edge of the SCL signal. -If not used, let this pin open.	O
36	LEDA	Anode pin of backlight	P
37	LEDK1	Cathode pin of backlight	P
38	LEDK2	Cathode pin of backlight	P
39	LEDK3	Cathode pin of backlight	P
40	LEDK4	Cathode pin of backlight	P
41	XR	Touch panel Right Glass Terminal.	A/D
42	YU	Touch panel Top Film Terminal.	A/D
43	XL	Touch panel LIFT Glass Terminal.	A/D
44	YD	Touch panel Bottom Film Terminal.	A/D
45	GND	Ground.	P

6. LCD Optical Characteristics

6.1 Optical specification

Item		Symbol	Condition	Min.	Typ.	Max.	Unit.	Note
Contrast Ratio		CR	Θ=0 Normal viewing angle	250	350			
Response time	Rising	T_R		--	20	30	msec	
	Falling	T_F						
Color gamut		S(%)		--	60	--	%	
Color Filter Chromacicity	White	W_X		0.276	0.316	0.356		
		W_Y		0.316	0.356	0.406		
	Red	R_X		0.597	0.617	0.637		
		R_Y		0.342	0.362	0.382		
	Green	G_X		0.331	0.351	0.371		
		G_Y		0.588	0.608	0.628		
	Blue	B_X		0.131	0.151	0.171		
		B_Y		0.095	0.115	0.135		
Viewing angle	Hor.	Θ_L	CR>10	35	45	--		
		Θ_R		35	45	--		
	Ver.	Θ_U		35	45	--		
		Θ_D		20	30	--		
Option View Direction			6：00					

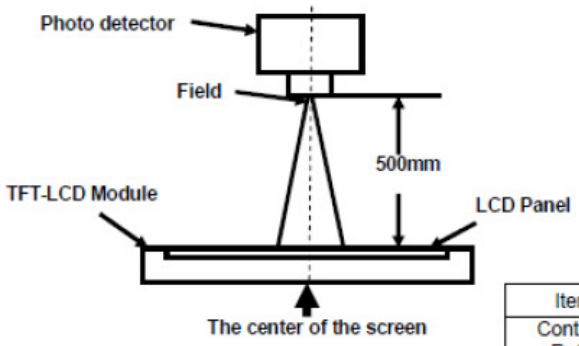
6.2 Measuring Condition

- Measuring surrounding : dark room
- Ambient temperature: 25 ±2˚C
- 15min. warm-up time

6.3 Measuring Equipment

Note 1: Definition of optical measurement system.

The optical characteristics should be measured in dark room. After 5 minutes operation, the optical properties are measured at the center point of the LCD screen. All input terminals LCD panel must be ground when measuring the center area of the panel.



Item	Photo detector	Field
Contrast Ratio	SR-3A	1°
Chromaticity		
Response Time	BM-7A	2°

Note 2: Definition of viewing angle range and measurement system.

viewing angle is measured at the center point of the LCD by CONOSCOPE(ergo-80)。

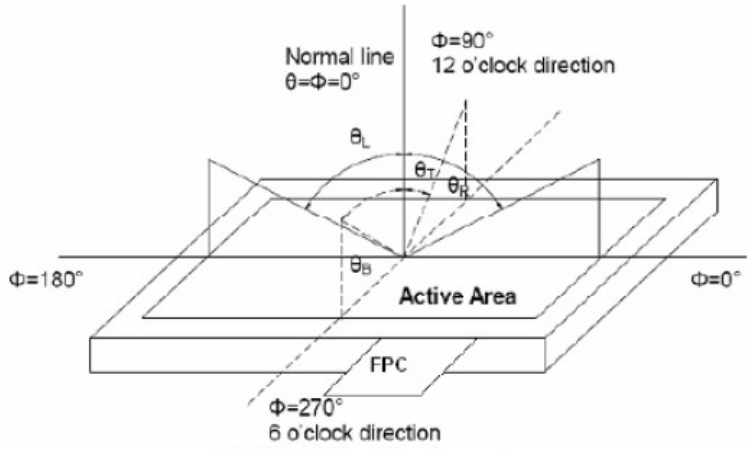


Fig. 1 Definition of viewing angle

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD is on the "White" state}}{\text{Luminance measured when LCD is on the "Black" state}}$$

Note 3: Definition of contrast ratio

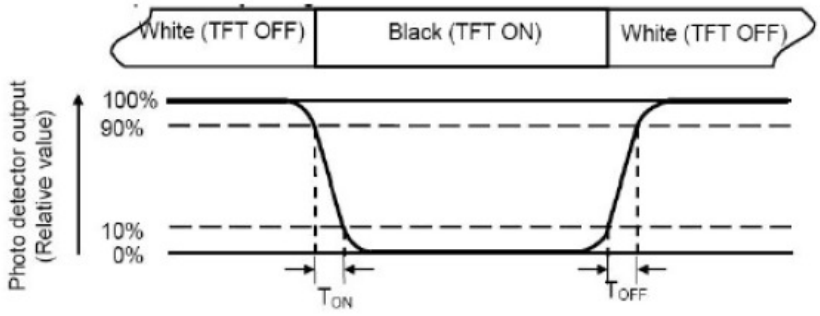
"White state ":The state is that the LCD should driven by Vwhite.

"Black state": The state is that the LCD should driven by Vblack.

Vwhite: To be determined Vblack: To be determined.

Note 4: Definition of Response time

The response time is defined as the LCD optical switching time interval between "White" state and "Black" state. Rise time (TON) is the time between photo detector output intensity changed from 90% to 10%. And fall time (TOFF) is the time between photo detector output intensity changed from 10% to 90%.



Note 5: Definition of color chromaticity (CIE1931)

Color coordinates measured at center point of LCD.

7. Electrical Characteristics

7.1 Absolute operation rating (Ta=25˚C VSS=0V)

Item	Symbol	RATING	Unit
Supply Voltage	VCI	-0.3~4.6	V
Digital interface supply Voltage	IOVCC	-0.3~4.6	V
Operating temperature	T_{OP}	-20~+70	℃
Storage temperature	T_{ST}	-30~+80	℃

7.2 DC Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply Voltage	VCI	2.4	2.8	3.3	V	
Digital interface supply Voltage	IOVCC	1.65	1.8	3.3	V	
Normal mode Current consumption	IDD	--	7	--	mA	
Level input voltage	V_{IH}	0.7 IOVCC		IOVCC	V	
	V_{IL}	GND		0.3 IOVCC	V	
Level output voltage	V_{OH}	0.8 IOVCC		IOVCC	V	
	V_{OL}	GND		0.2 IOVCC	V	

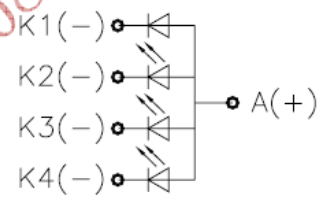
7.3 LED Backlight Characteristics

The back-light system is edge-lighting type with 4 chips White LED

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Forward Current	I_F	60	80	--	mA	
Forward Voltage	V_F	--	3.2	--	V	
LCM Luminance	L_V	350	400	--	cd/m2	Note3
LED life time	Hr	50000	--	--	Hour	Note1,2
Uniformity	AVg	80	--	--	%	Note3

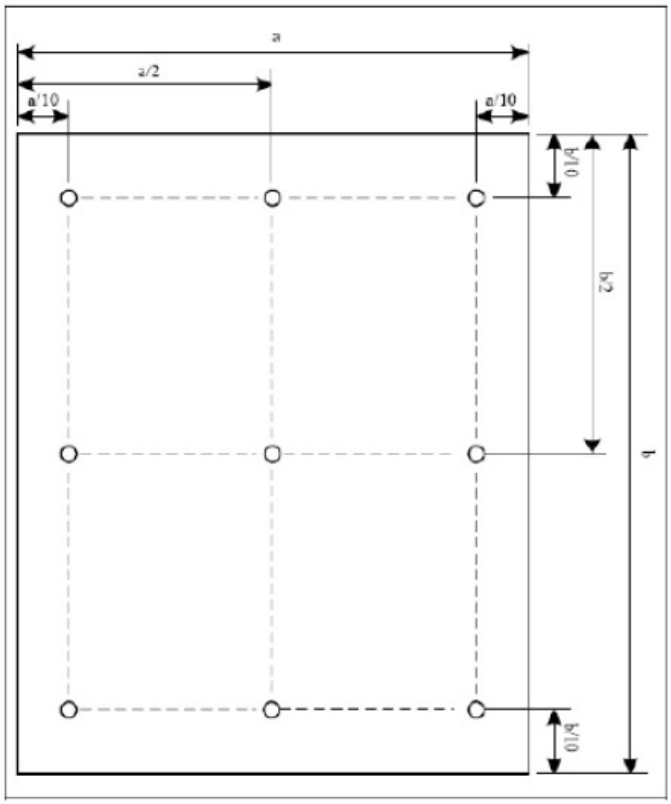
Note (1) LED life time (Hr) can be defined as the time in which it continues to operate under the condition: Ta=25±3 ℃, typical IL value indicated in the above table until the brightness becomes less than 50%.

Note (2) The "LED life time" is defined as the module brightness decrease to 50% original brightness at Ta=25℃ and IL=80mA. The LED lifetime could be decreased if operating IL is larger than 80mA. The constant current driving method is suggested.



BLU CIRCUIT DIAGRAM

NOTE 3: Luminance Uniformity of these 9 points is defined as below:



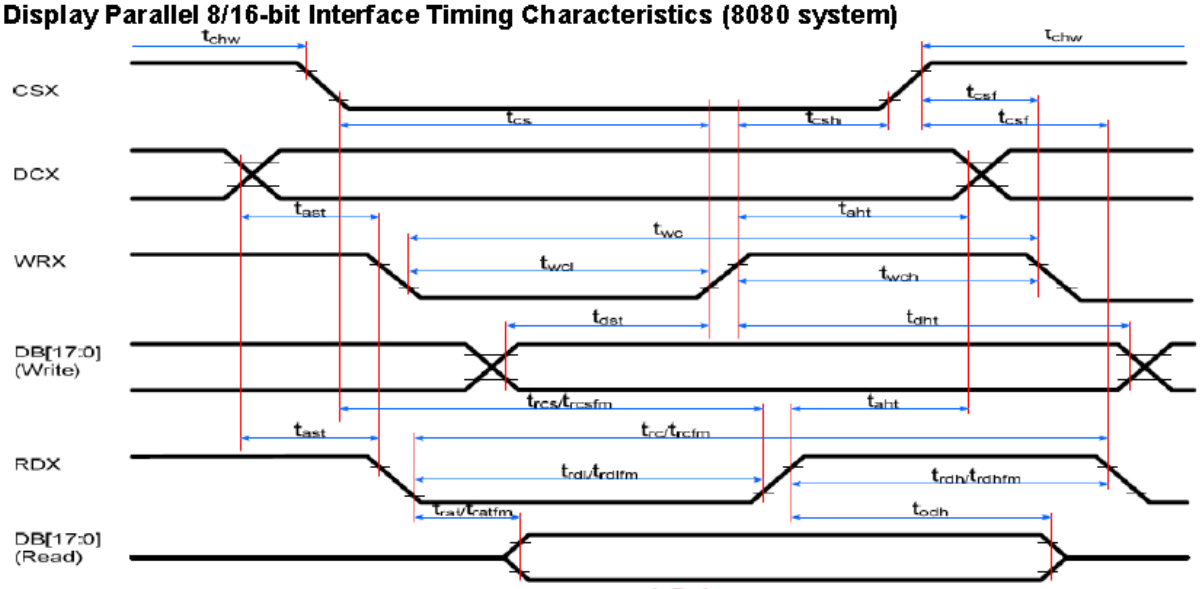
$$\text{Uniformity} = \frac{\text{minimum luminance in 9 points (1-9)}}{\text{maximum luminance in 9 points (1-9)}}$$

$$\text{Luminance} = \frac{\text{Total Luminance of 9 points}}{9}$$

8. AC Characteristic

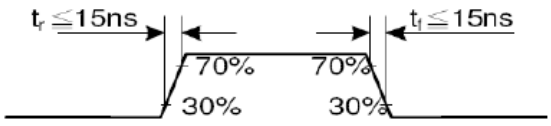
8.1 Display Parallel 8/16-bit Interface Timing Characteristics (8080 system)

Display Parallel 8/16-bit Interface Timing Characteristics (8080 system)

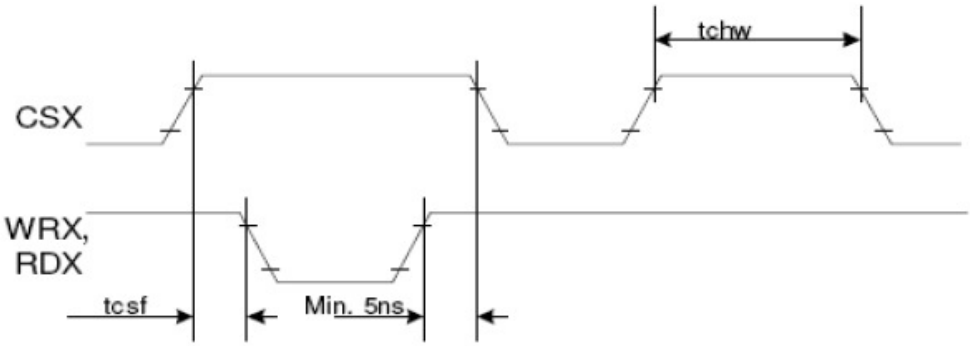


Signal	Symbol	Parameter	min	max	Unit	Description
DCX	tast	Address setup time	0	-	ns	
	taht	Address hold time (Write/Read)	10	-	ns	
CSX	tchw	CSX "H" pulse width	0	-	ns	
	tcs	Chip Select setup time (Write)	15	-	ns	
	trcs	Chip Select setup time (Read ID)	45	-	ns	
	trcsfm	Chip Select setup time (Read FM)	355	-	ns	
	tcsf	Chip Select Wait time (Write/Read)	10	-	ns	
WRX	twc	Write cycle	66	-	ns	
	twrh	Write Control pulse H duration	15	-	ns	
	twrl	Write Control pulse L duration	15	-	ns	
RDX (FM)	trcfm	Read Cycle (FM)	450	-	ns	
	trdhfm	Read Control H duration (FM)	90	-	ns	
	trdlfm	Read Control L duration (FM)	355	-	ns	
RDX (ID)	trc	Read cycle (ID)	160	-	ns	
	trdh	Read Control pulse H duration	90	-	ns	
	trdl	Read Control pulse L duration	45	-	ns	
D[17:0], D[15:0], D[8:0], D[7:0]	tdst	Write data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	tdht	Write data hold time	10	-	ns	
	trat	Read access time	-	40	ns	
	tratfm	Read access time	-	340	ns	
	trod	Read output disable time	20	80	ns	

Note: Ta = -30 to 70 °C, IOVCC=1.65V to 2.8V, VCI=2.6V to 3.3V, GND=0V

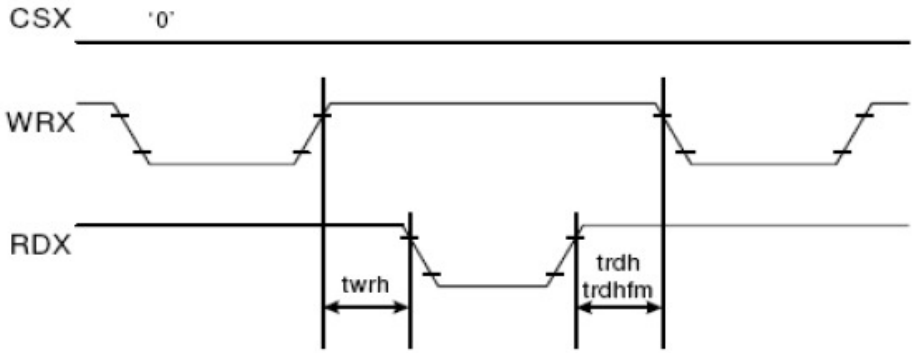


CSX timings :



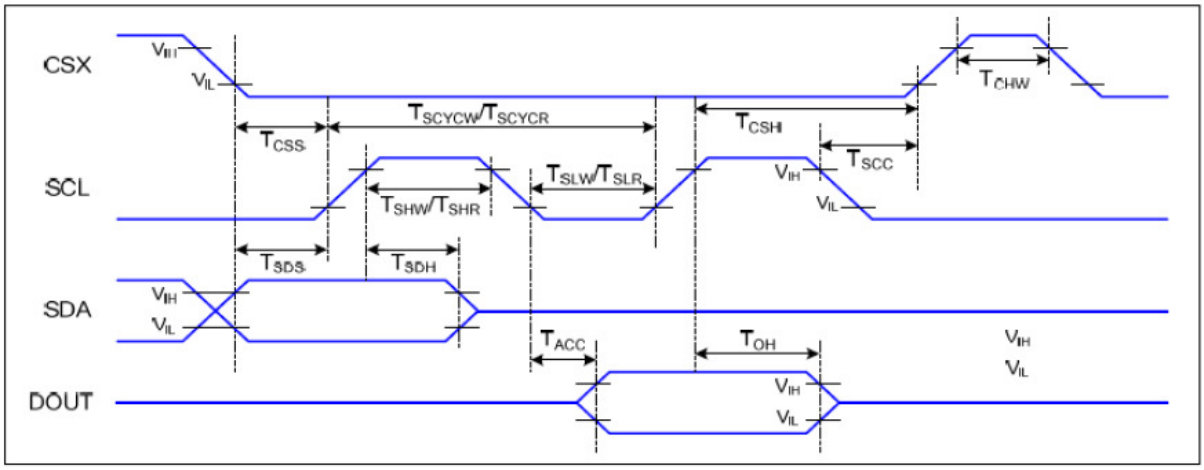
Note: Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

Write to read or read to write timings:



Note: Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

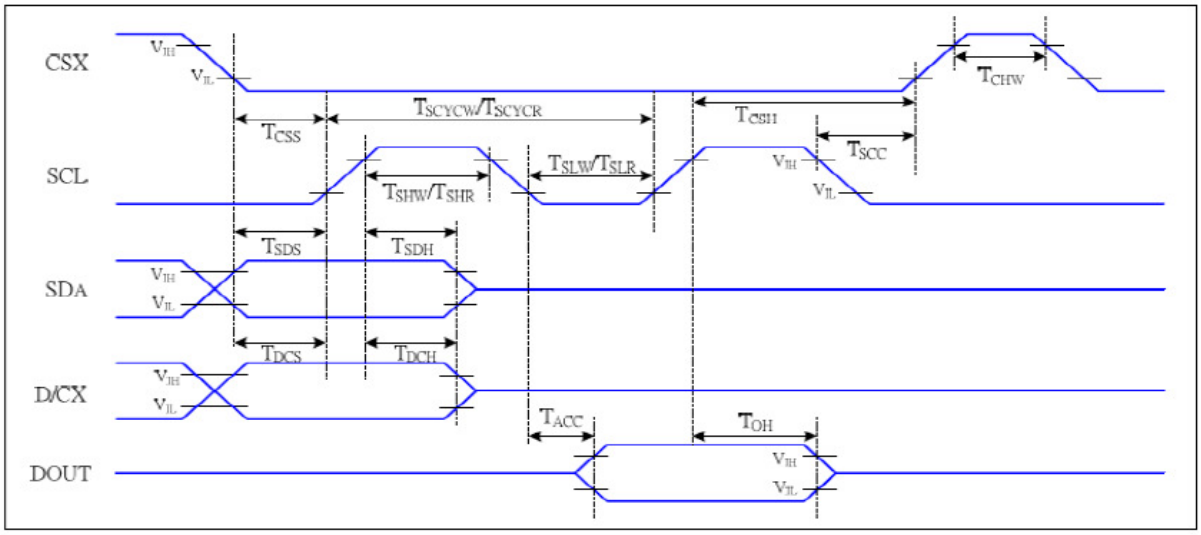
8.2 Display Serial Interface Timing Characteristics (3-line SPI system)



VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=-30 to 70 ℃

Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select "H" pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	66		ns	
	T_{SHW}	SCL "H" pulse width (Write)	15		ns	
	T_{SLW}	SCL "L" pulse width (Write)	15		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	
	T_{SHR}	SCL "H" pulse width (Read)	60		ns	
	T_{SLR}	SCL "L" pulse width (Read)	60		ns	
SDA (DIN)	T_{SDS}	Data setup time	10		ns	
	T_{SDH}	Data hold time	10		ns	
DOUT	T_{ACC}	Access time	10	50	ns	For maximum CL=30pF
	T_{OH}	Output disable time	15	50	ns	For minimum CL=8pF

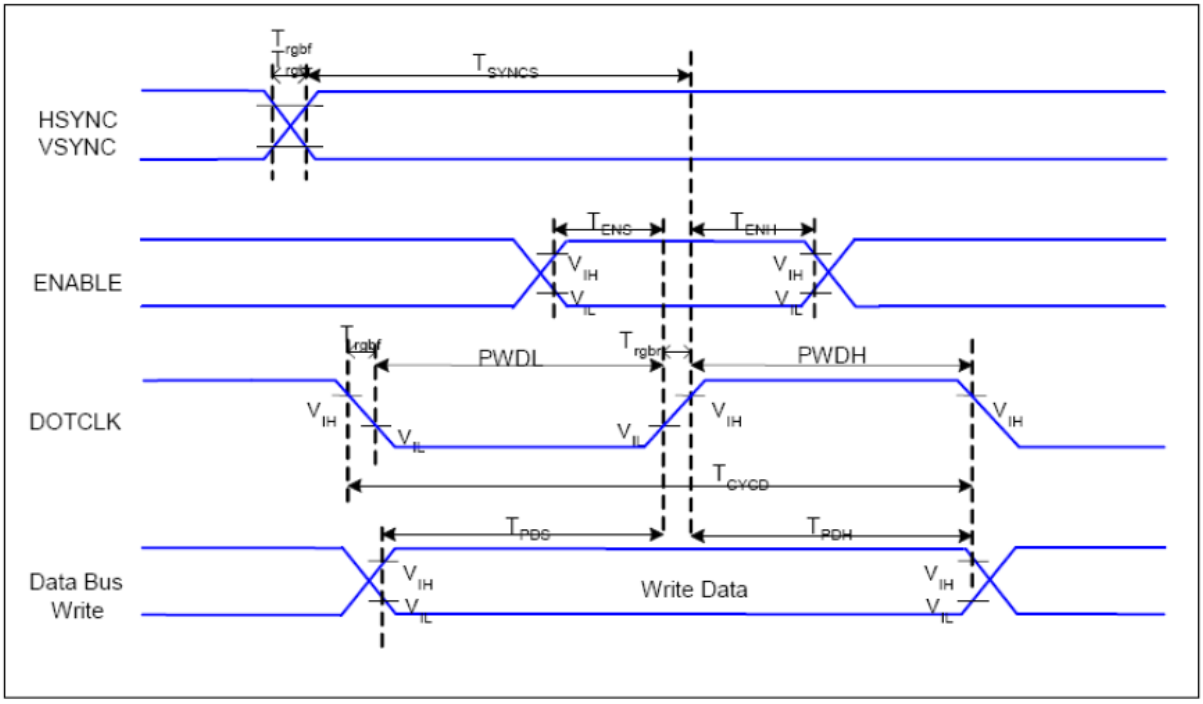
8.3 Display Serial Interface Timing Characteristics (4-line SPI system)



VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=-30 to 70 ℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select "H" pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	66		ns	-write command & data ram
	T_{SHW}	SCL "H" pulse width (Write)	15		ns	
	T_{SLW}	SCL "L" pulse width (Write)	15		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	-read command & data ram
	T_{SHR}	SCL "H" pulse width (Read)	60		ns	
	T_{SLR}	SCL "L" pulse width (Read)	60		ns	
D/CX	T_{DCS}	D/CX setup time	10		ns	
	T_{DCH}	D/CX hold time	10		ns	
SDA (DIN)	T_{SDS}	Data setup time	10		ns	
	T_{SDH}	Data hold time	10		ns	
DOUT	T_{ACC}	Access time	10	50	ns	For maximum CL=30pF For minimum CL=8pF
	T_{OH}	Output disable time	15	50	ns	

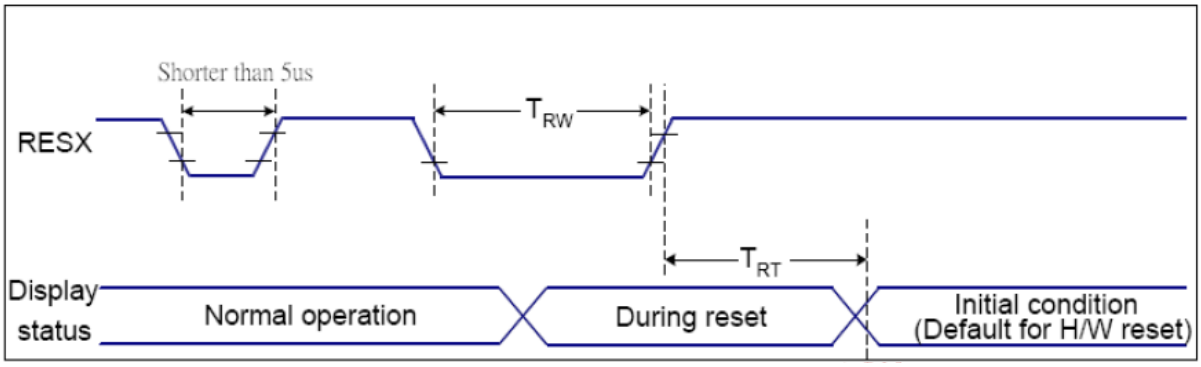
8.4 Parallel RGB Interface Timing Characteristics



VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=-30 ~ 70 ℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
HSYNC, VSYNC	T_{SYNCS}	VSYNC, HSYNC Setup Time	30	-	ns	
ENABLE	T_{ENS}	Enable Setup Time	25	-	ns	
	T_{ENH}	Enable Hold Time	25	-	ns	
DOTCLK	PWDH	DOTCLK High-level Pulse Width	60	-	ns	
	PWDL	DOTCLK Low-level Pulse Width	60	-	ns	
	T_{CYCD}	DOTCLK Cycle Time	120	-	ns	
	Trghr, Trghf	DOTCLK Rise/Fall time	-	20	ns	
DB	T_{PDS}	PD Data Setup Time	50	-	ns	
	T_{PDH}	PD Data Hold Time	50	-	ns	

8.5 Reset Timing Characteristics



VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=-30 ~ 70 ℃

Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1, 5)	ms
				120 (Note 1, 6, 7)	ms

Notes:

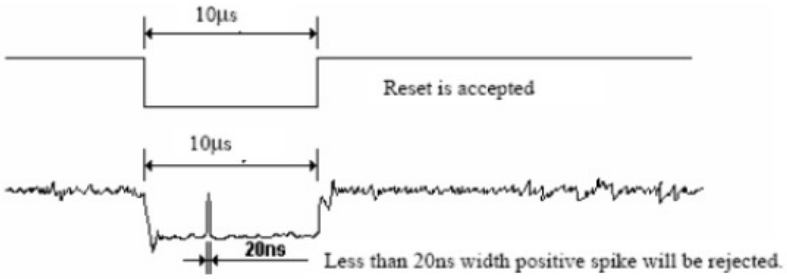
1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:

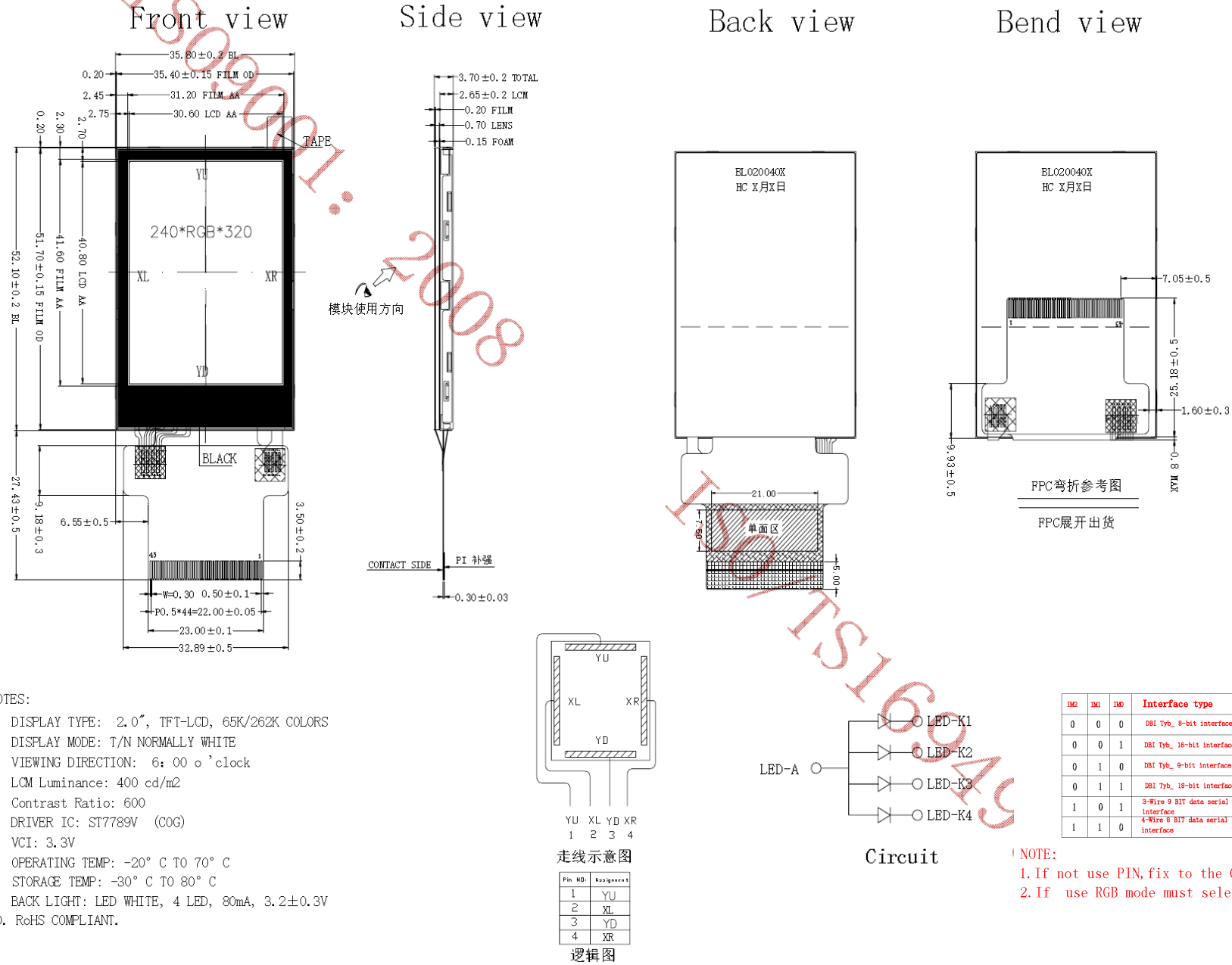


5. When Reset applied during Sleep In Mode.

6. When Reset applied during Sleep Out Mode.

7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

9. **Outline dimension**



Pin NO:	Assignment
1	YU
2	XL
3	YD
4	XR

逻辑图

NOTES:

1. DISPLAY TYPE: 2.0″, TFT-LCD, 65K/262K COLORS
2. DISPLAY MODE: T/N NORMALLY WHITE
3. VIEWING DIRECTION: 6: 00 o 'clock
4. LCM Luminance: 400 cd/m2
5. Contrast Ratio: 600
6. DRIVER IC: ST7789V (COG)
7. VCI: 3.3V
8. OPERATING TEMP: -20° C TO 70° C
   STORAGE TEMP: -30° C TO 80° C
9. BACK LIGHT: LED WHITE, 4 LED, 80mA, 3.2±0.3V
10. RoHS COMPLIANT.

IM2	IM1	IM0	Interface type	DB Pin in use
0	0	0	DBI Typ_ 8-bit interface	DB7-DB0
0	0	1	DBI Typ_ 16-bit interface	DB15-DB0
0	1	0	DBI Typ_ 9-bit interface	DB8-DB0
0	1	1	DBI Typ_ 18-bit interface	DB17-DB0
1	0	1	3-Wire 9 BIT data serial interface	SDA SCL CS
1	1	0	4-Wire 8 BIT data serial interface	SDA SCL CS RS

NOTE:
1. If not use PIN, fix to the GND , IOVCC or NC.
2. If use RGB mode must select serial interface

NO.	Pin Name
1	GND
2	VCI
3	IOVCC
4	IM2
5	IM1
6	IM0
7	RESET
8	CS
9	DC(SPI-SCL)
10	WR(SPI-RS)
11	RD
12	VSYNC
13	HSYNC
14	ENABLE
15	DOTCLK
16	SDA
17	DB0
18	DB01
19	DB02
20	DB03
21	DB04
22	DB05
23	DB06
24	DB07
25	DB08
26	DB09
27	DB10
28	DB11
29	DB12
30	DB13
31	DB14
32	DB15
33	DB16
34	DB17
35	SDO
36	LEDA
37	LEDK1
38	LEDK2
39	LEDK3
40	LEDK4
41	XR(NC)
42	YU(NC)
43	XL(NC)
44	YD(NC)
45	GND