

2.1 Einstellungen

IFSEL1	IFSEL0	RGB_EN	Register Data	Display Data
0	0	0	Command-parameter interface	Command-parameter interface
0	1	0	Register-content interface	Register-content interface
0	1	1	Register-content interface	RGB interface
1	X	1	Register-content interface (with Hardware control interface)	RGB interface

X means don't care

Table 5. 1 Interface Mode Selection

P68	Input signal format selection
0	Format for I80 series MPU
1	Format for M68 series MPU

Table 5. 2 MPU selection in Register-content Interface Circuit

BS2	BS1	BS0	Interface	Transferring Method of RAM data	Transferring Method of Command
0	0	0	16-bit system interface	16-bit collective	8-bit collective
0	0	1		16-bit + 2 bit	
0	1	0	18-bit system interface	18-bit collective	
0	1	1	8-bit system interface	8-bit + 8-bit + 8-bit	
1	1	x	Serial bus transfer interface	16 or 24-bit serial	8-bit serial

Table 5. 3 Interface Selection in Register-content Interface Mode

2.2 Operation

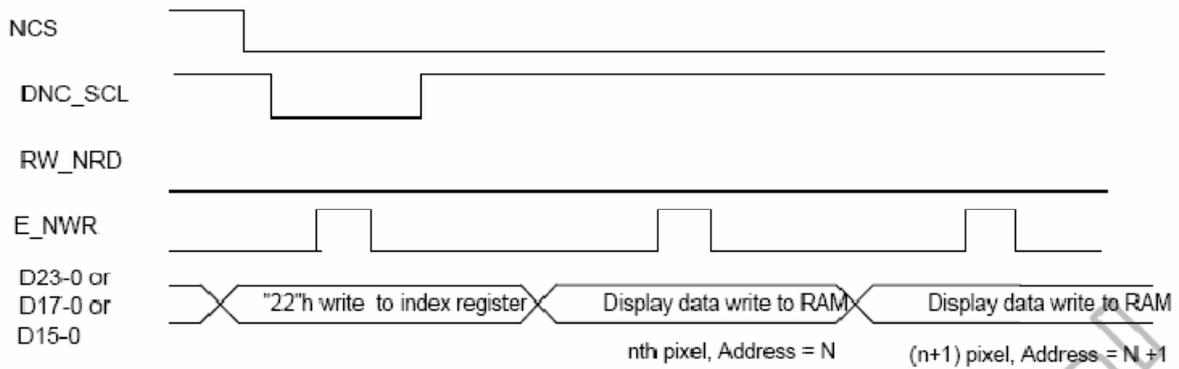
Operations	E_NWR	RW_NRD	DNC_SCL
Writes Indexes into IR	0	1	0
Reads Internal status	1	0	0
Writes command into register or data into GRAM	0	1	1
Reads command from register or data from GRAM	1	0	1

Table 5. 4 Data Pin Function for I80 Series CPU

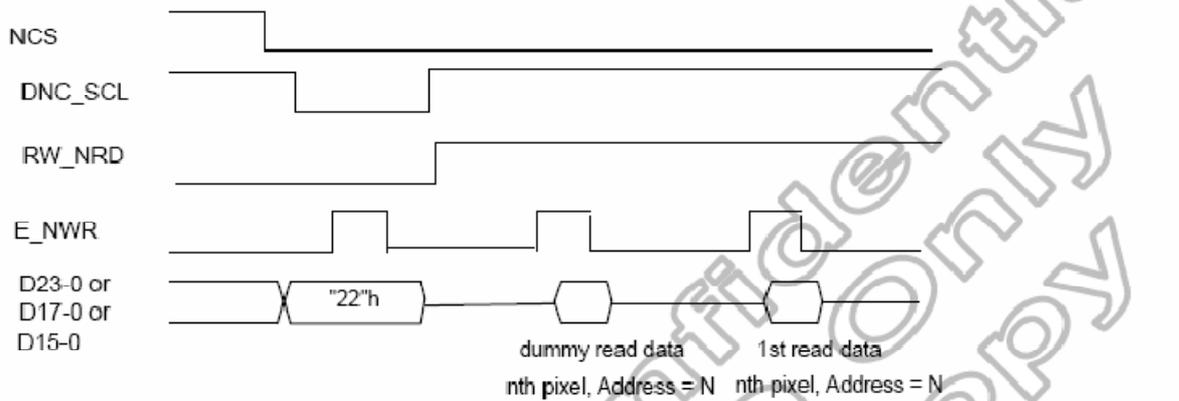
Operations	E_NWR	RW_NRD	DNC_SCL
Writes Indexes into IR	1	0	0
Reads Internal status	1	1	0
Writes command into register or data into GRAM	1	0	1
Reads command from register or data from GRAM	1	1	1

Table 5. 5 Data Pin Function for M68 Series CPU

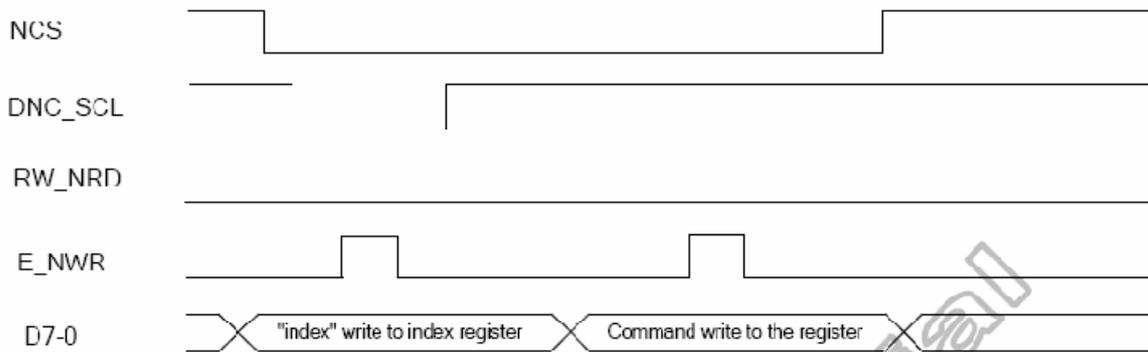
Write to the graphic RAM (18-bit or 16-bit collective)



Read the graphic RAM (18-bit or 16-bit collective)



Write to the register

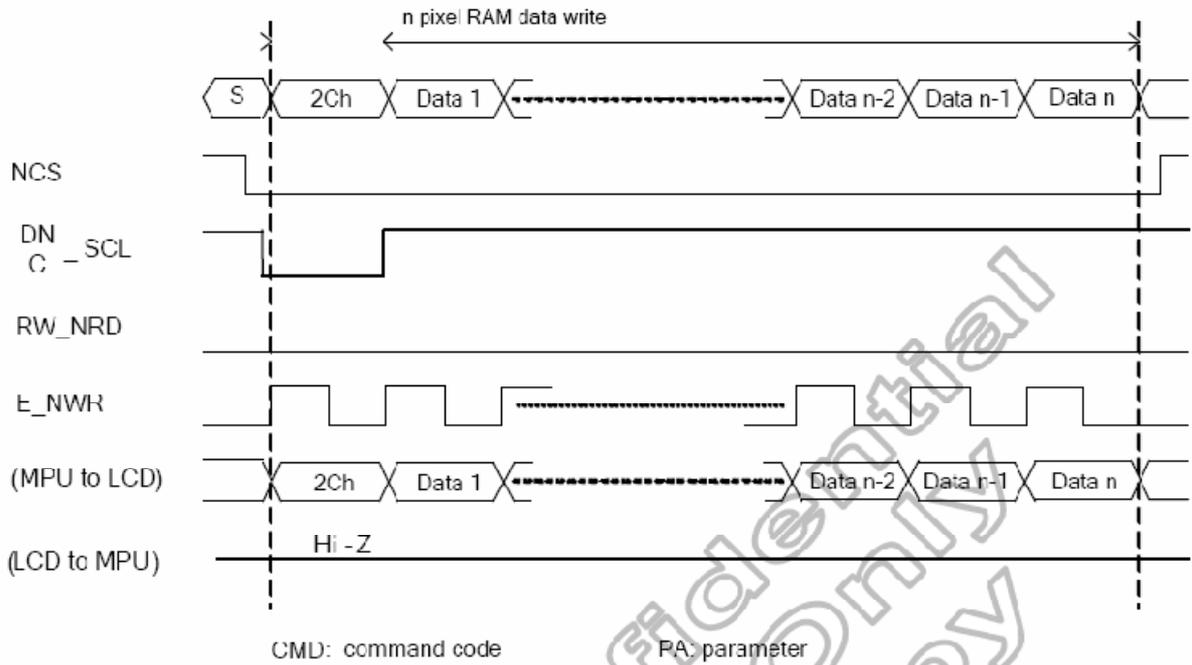


Read the register



Figure 5. 4 Register read/write Timing in Parallel Bus System Interface (for M68 series MPU)

Write to GRAM



Read from GRAM

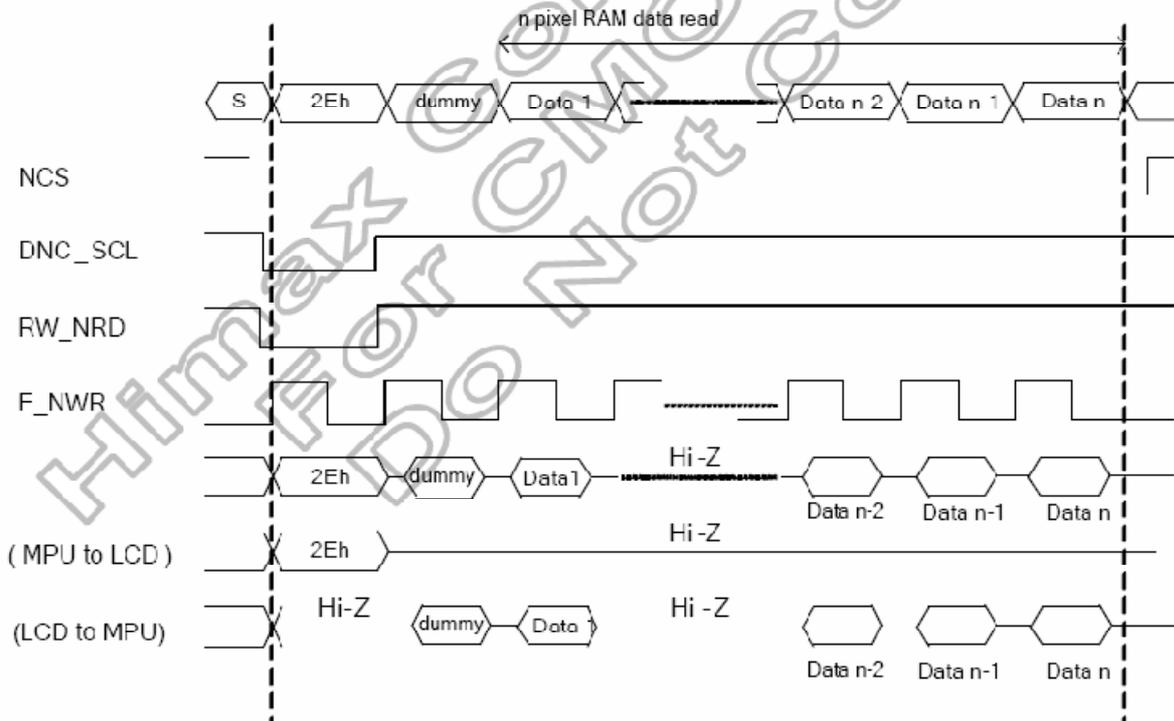


Figure 5. 19 GRAM Read/Write Timing In Parallel Bus System Interface (for M68 series MPU)