SILICON LABORATORIES

AN230

Si4700/01 Programming Guide

1. Introduction

1.1. Scope

This document applies to Si4700/01 firmware revision 7 and greater and example code version 1 and greater.

1.2. Purpose

The purpose of this programming guide is to describe the following:

- Device initialization sequence and busmode selection
- 2-wire and 3-wire busmodes
- Step-by-step procedures for
  - setting default configuration
  - channel selection
  - seek up/seek down
  - RDS/RBDS

This document references the Si4700/01 data sheet.

1.3. Terminology

SENB or $\overline{\text{SEN}}$—serial enable pin, active low, used only for 3-wire operation

SDIO—serial data in/data out pin.

SCLK—serial clock pin.

RSTB or $\overline{\text{RST}}$—reset pin, active low

Device—refers to the Si4700/01

2. Functional Description

2.1. Powerup, Powerdown, and Reset

Setting the $\overline{\text{RST}}$ pin low will disable analog and digital circuitry, reset the registers to their default settings, and disable the bus. Setting the $\overline{\text{RST}}$ pin high will bring the device out of reset and place the device in powerdown mode. Setting $\overline{\text{SEN}}$ high on the rising edge of $\overline{\text{RST}}$ will select 2-wire operation and setting $\overline{\text{SEN}}$ low will select 3-wire operation. SDIO must always be set low on the rising edge of $\overline{\text{RST}}$. Refer to "Table 4. Reset Timing Characteristics" and "Figure 1. Reset Timing Diagram" of the Si4700/01 data sheet for more information.

Setting the ENABLE bit high and the DISABLE bit low will powerup the device. A powerdown mode is available to reduce power consumption when the part is idle. Setting the ENABLE bit high and the DISABLE bit high will disable analog and digital circuitry while maintaining register configuration and keeping the bus active. Note that the device automatically sets the ENABLE bit low after the internal powerdown sequence completes. Setting the ENABLE bit low directly will cause the device to partially powerdown. Setting the ENABLE bit high and the DISABLE bit low will bring the device out of powerdown mode and resume normal operation. Refer to Figure 1 on page 2.

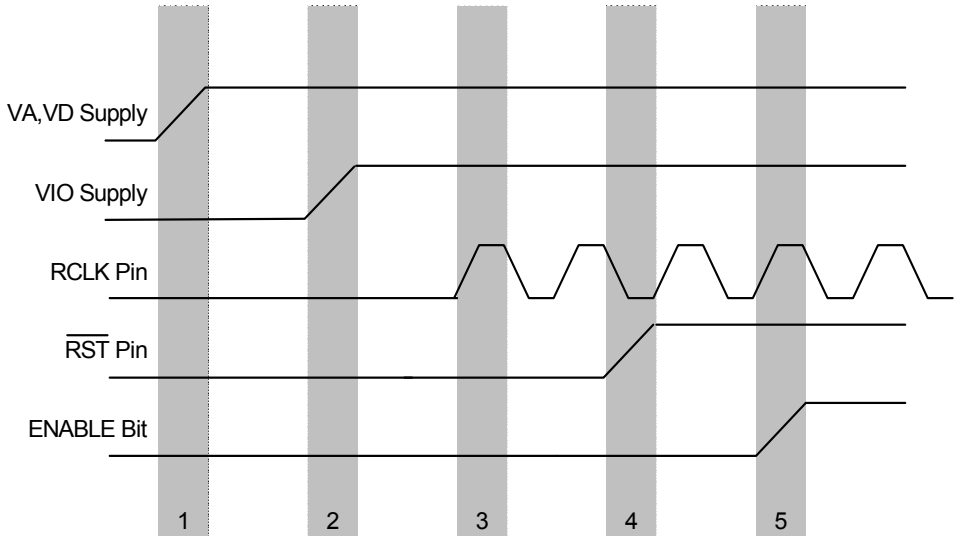

Figure 1. Initialization Sequence

2.2. Initialization Sequence and Busmode Selection

Refer to Figure 1.

To initialize the device:

1. Supply VA and VD.
2. Supply VIO while keeping the $\overline{\text{RST}}$ pin low. Note that power supplies may be sequenced in any order (steps 1 and 2 may be reversed).
3. Provide RCLK.
4. Set the $\overline{\text{RST}}$ pin high. Setting the $\overline{\text{SEN}}$ pin high on the rising edge of $\overline{\text{RST}}$ will select 2-wire operation and setting the $\overline{\text{SEN}}$ pin low will select 3-wire operation. SDIO must always be set low on the rising edge of $\overline{\text{RST}}$. The device registers may now be read and written.
5. Set the ENABLE bit high and the DISABLE bit low to powerup the device.

To power down the device:

1. Set the ENABLE bit high and the DISABLE bit high to place the device in powerdown mode. Note that all register states are maintained so long as VIO is supplied and the $\overline{\text{RST}}$ pin is high.
2. Remove VA and VD supplies as needed.

To power up the device (after power down):

1. Note that VIO is still supplied in this scenario. If VIO is not supplied, refer to device initialization procedure above.
2. Supply VA and VD.
3. Set the ENABLE bit high and the DISABLE bit low to powerup the device.

2.3. 3-Wire Control Interface

For three-wire operation, a transfer begins when the $\overline{SEN}$ pin is set low on a rising SCLK edge. The control word is latched internally on rising SCLK edges and is nine bits in length, comprised of a four bit chip address A7:A4 = 0110b, a read/write bit (read = 1 and write = 0), and a four bit register address, A3:A0. The ordering of the control word is A7:A5, R/$\overline{W}$, A4:A0, as shown in Figure 2.

For write operations, the serial control word is followed by a 16-bit data word and is latched internally on rising SCLK edges.

Refer to "Table 5. 3-Wire Control Interface Characteristics" and "Figure 2. 3-Wire Control Interface Write Timing Parameters" of the Si4700/01 Data Sheet for more information.

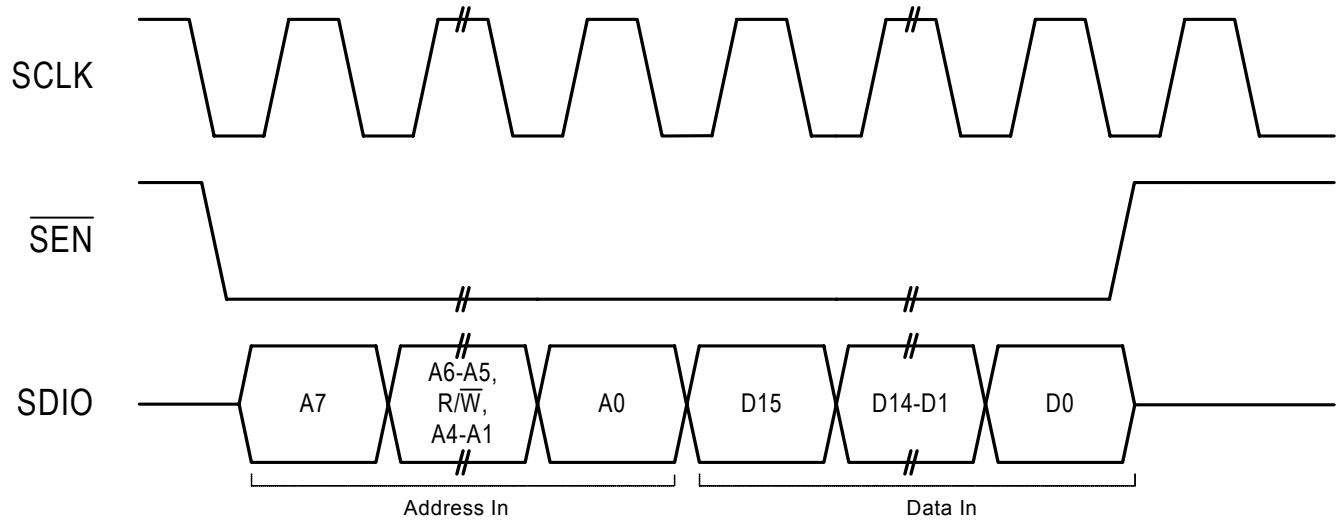

Figure 2. 3-Wire Control Interface Write Timing Diagram

For read operations, a bus turn-around of half a cycle is followed by a 16-bit data word shifted out on rising SCLK edges. The transfer ends on the rising SCLK edge after $\overline{SEN}$ is set high. Note that 26 SCLK cycles are required for a transfer; however, SCLK may run continuously.

Refer to "Table 5. 3-Wire Control Interface Characteristics" and "Figure 3. 3-Wire Control Interface Read Timing Parameters" of the Si4700/01 Data Sheet for more information.

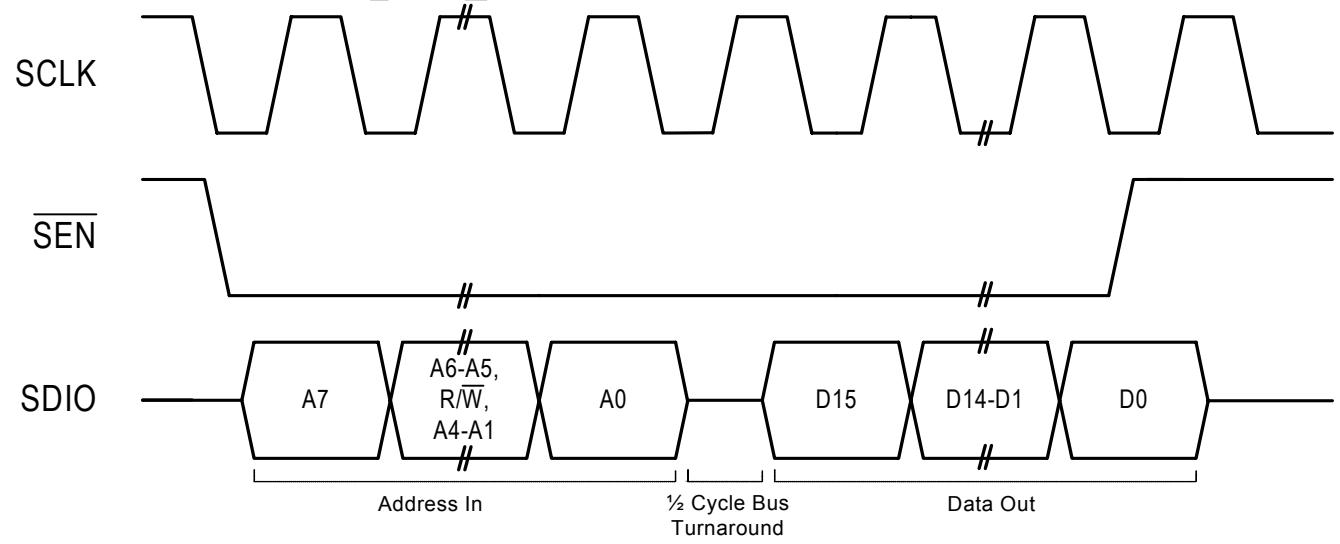

Figure 3. 3-Wire Control Interface Read Timing Diagram

2.4. 2-Wire Control Interface

For two-wire operation, a transfer begins with the START condition. The control word is latched internally on rising SCLK edges and is eight bits in length, comprised of a seven bit device address equal to 0010000b and a read/write bit (read = 1 and write = 0). The ordering of the control word is A7:A0, R/$\overline{W}$ as shown below.

The device acknowledges the control word by setting SDIO low on the next falling SCLK edge.

For write operations, the control word and device acknowledge is followed by an eight bit data word latched internally on rising edges of SCLK. The device always acknowledges the data by setting SDIO low on the next falling SCLK edge. Any number of data bytes may be written and register addresses are incremented by an internal address counter, starting with the upper byte of register 02h, followed by the lower byte of register 02h, and wrapping back to 00h at the end of the register file.

For read operations, the control word and device acknowledge is followed by an eight bit data word shifted out on falling SCLK edges. The controller IC returns an acknowledge if additional data will be transferred. Any number of data bytes can be read and register addresses are incremented by an internal address counter, starting at the upper byte of register 0Ah, followed by the lower byte of register 0Ah, and wrapping back to 00h at the end of the register file. The transfer ends with the STOP conditions regardless of the state of the acknowledge.

Refer to “Table 6. 2-Wire Control Interface Characteristics” and “Figure 4. 2-Wire Control Interface Read and Write Timing Parameters” of the Si4700/01 Data Sheet.

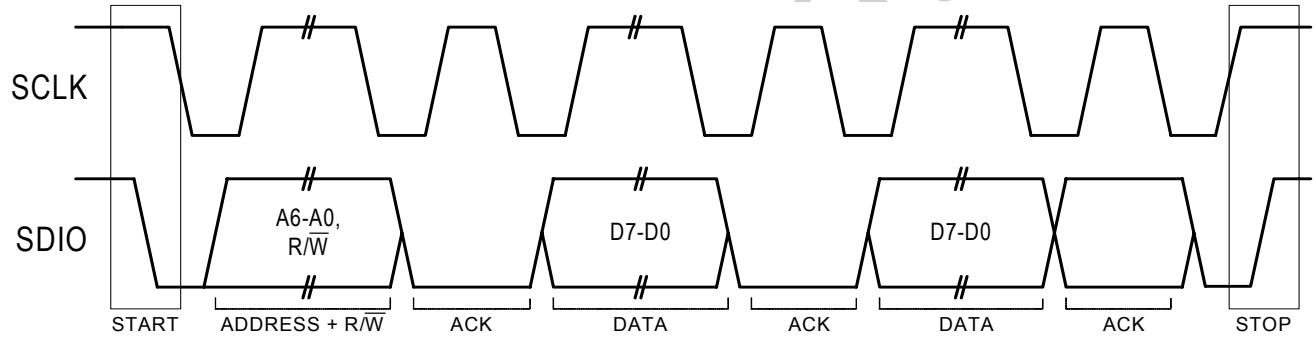

Figure 4. 2-Wire Control Interface Read and Write Timing Diagram

2.5. Powerup Configuration

Table 1 shows the sequence of commands required to configure the device prior to channel selection, seek or RDS. Note that address 03h may be written during powerup configuration.

Table 1. Powerup Configuration Sequence

Write address 02h (required). ■ Set the DMUTE bit to disable mute. ■ Set the ENABLE bit high to set the powerup state. ■ Set the DISABLE bit low to set the powerup state. **Example:** Write data 4001h.
Write address 04h (required). ■ Set the STCIEN bit high to enable a low interrupt on GPIO2 when tuning completes. ■ Set the RDSIEN bit high to enable a low interrupt on GPIO2 when RDS data are ready. ■ Set the DE bit to the desired de-emphasis setting. ■ Set GPIO2[1:0] = 01 to enable STC and RDSR interrupts on GPIO2. **Example:** To configure for operation in the United States, set DE = 0 to set de-emphasis to 75 µs, and set GPIO2[1:0] = 01 to enable interrupts. Write data C004h.
Write address 05h (required). ■ Set bits SEEKTH[7:0] to the desired seek threshold RSSI level. ■ Set bits VOLUME[3:0] to select the desired volume. ■ Set the BAND bit for US/European or Japanese operation. ■ Set the SPACE[1:0] bits for 50, 100, or 200 kHz channel spacing. **Example:** To set the volume to maximum, select the United States band, set 200 kHz channel spacing, and the seek threshold level to 25% of range, write data 3F0Fh. Note that the output is muted during the seek operation regardless of the state of bits DMUTE and VOLUME.
Wait for device powerup (required). ■ Refer to the Powerup Time specification in Table 7 "FM Characterstics" of the data sheet.
Read addresses 00h–01h (optional). ■ The bits PN[3:0] = 1 indicate the part number Si4700/01. ■ The bits MFGID[11:0] = 242h indicate Silicon Laboratories as the manufacturer. ■ The bits REV[5:0] = 1 indicate silicon revision A. ■ The bit DEV = 0 indicates the Si4700 and DEV = 1 indicates the Si4701 after powerup. ■ The bits FIRMWARE[8:0] indicate the firmware revision after powerup.

2.6. Powerdown

Table 2 shows the sequence of commands required to powerdown the device.

Table 2. Powerdown Sequence

Write address 02h (required).

- Clear the DMUTE bit to enable mute.
- Set the ENABLE bit high and DISABLE bit high to set the powerdown state.
- After the DISABLE bit is set high, the device performs an internal powerdown sequence and then sets ENABLE low. Setting the ENABLE bit directly will cause the device to partially powerdown.

Example: Write data 0041h.

2.7. Channel Selection

Table 3 shows the sequence of commands required for channel selection and assumes that the Powerup Configuration, detailed in section 2.5, has completed.

Table 3. Channel Selection Sequence

Write address 03h (required). ■ Set the TUNE bit high to begin a tuning operation. ■ Set CHAN[9:0] bits to select the desired channel. **Example:** To tune to 103.5 MHz in the United States, with BAND = 0 and SPACE[1:0] = 00 as described in the powerup sequence, set CHAN[9:0] = 80d = 50h such that frequency = 103.5 MHz = 200 kHz x 80 + 87.5 MHz). Write data 8050h.
Wait for GPIO2 = 0 (required). ■ This indicates that a seek/tune operation has completed.
Read address 0Ah (optional). ■ The STC bit being set indicates tuning has completed. ■ The ST bit being set indicates stereo operation. ■ The bits RSSI[7:0] indicate RSSI level for the current channel.
Read address 0Bh (optional). ■ The bits READCHAN[9:0] indicate the current channel.
Write address 03h (required). ■ Set the TUNE bit low to end the tuning operation and to set the STC bit low. **Example:** Write data to 0050h.
Read address 0Ah (optional). ■ The STC bit being cleared indicates that the TUNE or SEEK bits may be set again to start another tune or seek operation. Do not set the TUNE or SEEK bits until the Si470x clears the STC bit.

2.8. Seek Up/Seek Down

Table 4 shows the sequence of commands required for seek and assumes that the Powerup Configuration, detailed in section 2.5, has completed.

Table 4. Seek Up/Seek Down Sequence

Write address 02h (required). ■ Set the DMUTE bit to disable mute. ■ Set the SEEKUP bit high to seek up and low to seek down. ■ Set the SEEK bit high to begin the seek operation. ■ Set the ENABLE bit high to maintain the powerup state. ■ Set the DISABLE bit low to maintain the powerup state. **Example:** Write data 4301h to seek up or 4101h to seek down.
Wait for GPIO2 = 0 (required). ■ This indicates that a seek/tune operation has completed.
Read address 0Ah (optional). ■ The STC bit being set indicates tuning has completed. ■ The SF bit being set indicates the seek operation searched the band without finding a channel with an RSSI greater than or equal to SEEKTH[7:0]. ■ The ST bit being set indicates stereo operation. ■ The bits RSS[7:0] indicate RSSI level for the current channel.
Read address 0Bh (optional). ■ The bits READCHAN[9:0] indicate the current channel.
Write address 02h (required). ■ Set the SEEK bit low to end the tuning operation and to set the STC bit low. **Example:** Write data to 4001h.
Read address 0Ah (optional). ■ The STC bit being cleared indicates that the TUNE or SEEK bits may be set again to start another tune or seek operation. Do not set the TUNE or SEEK bits until the Si470x clears the STC bit.

2.9. RDS/RBDS (Si4701 only)

Table 5 shows the sequence of commands required for RDS and assumes that the Powerup Configuration, detailed in section 2.5, has completed.

Table 5. RDS/RBDS Sequence

Write address 04h (required). ■ Set the RDSIEN bit high to enable a low interrupt on GPIO2 when RDS data are ready. ■ Set GPIO2[1:0] = 01 to enable STC and RDSR interrupts on GPIO2. **Example:** To enable RDS operation with RDS interrupts and seek/tune interrupts enabled, write data D004h.
Wait for GPIO2 = 0 (required). ■ This indicates that RDS data are ready.
Read address 0Ah (optional). ■ The RDSR bit being set indicates RDS data are ready (Si4701 only). ■ The three RDSE bits count the number of errors in the four RDS words RDSA, RDSB, RDSC, and RDSD. Zero indicates no errors exist.
Read addresses 0Ch–0Fh (required). ■ The bits RDSA[15:0], RDSB[15:0], RDSC[15:0], and RDSD[15:0] contain error-corrected RDS group data.

DOCUMENT CHANGE LIST

Revision 0.2 to Revision 0.3

- "1.1. Scope" on page 1 updated.
- "1.2. Purpose" on page 1 updated.
- "2.5. Powerup Configuration" on page 5 updated.
  - Second paragraph removed.
  - Second column removed.
- "2.6. Powerdown" on page 6 updated.
  - Second paragraph removed.
  - Second column removed.
  - Changed “Set the DMUTE bit” to “Clear the DMUTE bit.”
- "2.7. Channel Selection" on page 7 updated.
  - Second paragraph removed.
  - Second column removed.
  - Removed the text “The RDSR bit indicates RDS data are ready (Si4701 only).”
  - Added “Read Address 0Ah (optional).”
- "2.8. Seek Up/Seek Down" on page 8 updated.
  - Second paragraph removed.
  - Second column removed.
  - Removed the text “The RDSR bit indicates RDS data are ready (Si4701 only).”
  - Added “Read Address 0Ah (optional).”
- "2.9. RDS/RBDS (Si4701 only)" on page 9 updated.
  - Second paragraph removed.
  - Second column removed.
  - Removed the text “...or a seek/tune operation has completed.”
  - Updated “Read Address 0Ah.”
  - Removed “Read Address 0Bh.”
- “3. Example Microcontroller Pseudo-Code” section removed.

NOTES:

CONTACT INFORMATION

Silicon Laboratories Inc.
4635 Boston Lane
Austin, TX 78735
Tel: 1+(512) 416-8500
Fax: 1+(512) 416-9669
Toll Free: 1+(877) 444-3032

Email: FMinfo@silabs.com
Internet: www.silabs.com