7 EPL 24 V LIN devices with RX and TX access

This clause addresses class A and class B devices.

7.1 Test specification overview

7.1.1 Test case organization

The intention of each test case is described at first, with a short textual explanation. Before tests are executed, the test system shall be set to its initial state as described in 7.2.

The test procedure and the expected results are described in the form of a chart for each test case. The table below is a typical test description.

Table 94 defines the test case organization.

Table 94 — Test case organization

IUT node as	Class A/B/C device as master or slave or both	Corresponding test number TC x, TC y, where x, y are the test case number
Initial state	**Parameters:**	
	Number of nodes	number of node in the test implementation
	Bus loads	in order to simulate a LIN network
	Operational conditions:	
	IUT mode	Operation mode for the IUT (e.g. normal mode, low power mode, ...).
	TX signal	State of TX pin at the beginning of the test.
	RX signal	Logical output voltages of the Rx pin corresponding to recessive/dominant level at the LIN pin are taken from the datasheet of the IUT.
	V_{BAT}, V_{SUP}, V_{IUT}, V_{CC}, $V_{PS1/2}$, V_{BUS}	Value in Volt
	Failure	In order to set failure at
	GND Shift	Value in Volt
Test steps	Describe the test stages.	
Response	Describe the result expected in order to decide if the test passed or failed.	
Reference	Corresponding number in ISO 17987-4.	

IUT may be a master or slave ECU or an individual transceiver chip. The RX, TX and V_{SUP} signals shall be accessible for proper test execution. It is recommended to test with RX/TX access, if not possible testing according the specification without RX/TX access (see Clause 6) is accepted. Depending on the type of IUT, the supply voltage is V_{BAT} for ECU or V_{SUP} for a chip called V_{IUT} in this description.

7.1.2 Measurement and signal generation — Requirements

Table 95 defines the measurement and signal generation — Requirements.

Table 95 — Measurement and signal generation — Requirements

Signal generation:	Rise/Fall time		40ns
	Frequency		20 ppm
	Jitter		<30 ns
Signal measurement:	Dynamic signals:		Oscilloscope 100 MHz Rise time ≤3,5ns
	Static signals:	DC voltage	0,5 %
		DC current	0,6 %
		Resistance	0,5 %
Power Supply (V_{BAT}, V_{SUP}, V_{IUT}, V_{CC}, $V_{PS1/2}$, V_{BUS})	Resolution		10 mV/1 mA
	Accuracy		0,2 % of value

7.2 Operational conditions — Calibration

7.2.1 Electrical input/output, LIN protocol

The initial configuration for each test case is defined here. Any requirements for individual tests are specified with the test case.

Table 96 defines the initial state of electrical input/output.

Table 96 — Initial state of electrical input/output

Initial state	**Parameters:**	
	Number of nodes	1
	Bus loads	
	Operational conditions:	
	IUT mode	Set to normal/active mode
	TX signal	Recessive
	V_{BAT}, V_{SUP}, V_{IUT}, V_{CC}, $V_{PS1/2}$, V_{BUS}	Specified for each test
	Failure	No failure
	GND shift	0 V

7.2.2 [EPL–CT 51] Operating voltage range

This test shall ensure the correct operation in the valid supply voltage ranges, by correct reception of dominant bits. The IUT is therefore supplied with an increasing/decreasing voltage ramp.

Figure 43 shows the test configuration of the test system "Operating voltage range with RX and TX access for 24 V LIN systems".

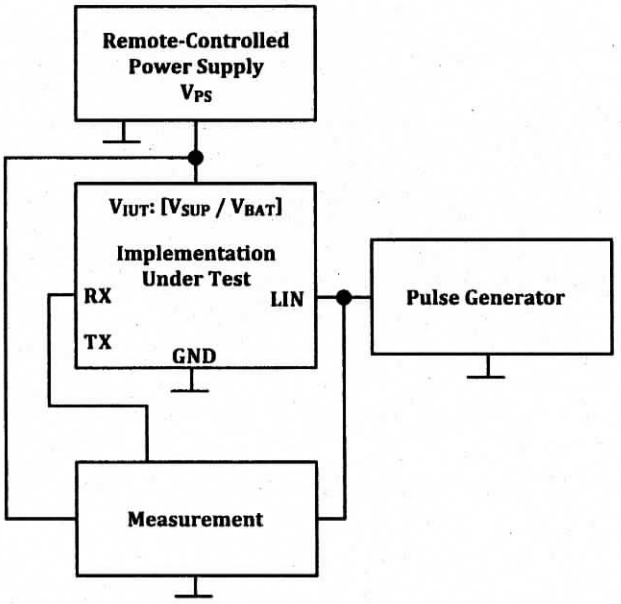

Figure 43 — Test system: Operating voltage range with RX and TX access

Table 97 defines the test system "Operating voltage range with RX and TX access".

Table 97 — Test system: Operating voltage range with RX and TX access

IUT node as	Class B device as master or slave Class A device	[EPL–CT 51].1, [EPL–CT 51].2
Initial state	**Operational conditions:**	
	V_{IUT}: [V_{SUP}/V_{BAT}]	Table 98
Test steps	A voltage ramp is set on the V_{SUP}/V_{BAT} as defined on Table 98. For BR_Range_20K 24 V LIN system the LIN signal is driven with a 10 kHz rectangular signal with a duty cycle of 50 %, a voltage swing of 36 V and a rise/fall time of 40 ns. For BR_Range_10K 24 V LIN system the LIN signal is driven with a 5,2 kHz rectangular signal with a duty cycle of 50 % and a voltage swing of 36V and a rise/fall time of 40 ns. The IUT shall be in operational/active mode	
Response	For BR_Range_20K 24 V LIN system the RX pin of the IUT shall show the 10 kHz signal and for BR_Range_10K 24 V LIN system the RX pin of the IUT shall show a 5,2 kHz signal. A maximum deviation of 10 % (time, voltage) is allowed (see Figure 2).	
Reference	ISO 17987–4:2016, Table 15, Param 7, Param 8, Param 52, Param 53	

Figure 44 shows the RX response of the test system "Operating voltage range".

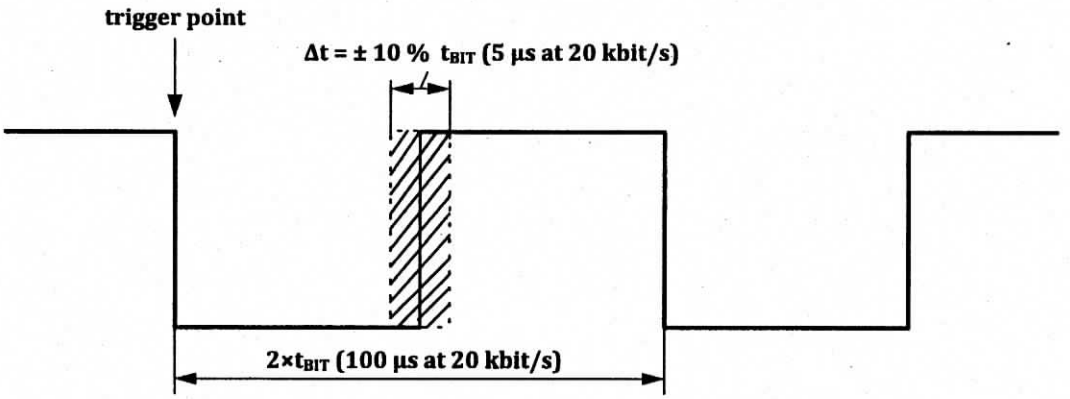

Figure 44 — RX response of test system: Operating voltage range

Table 98 defines the test cases for "Operating voltage ramp".

Table 98 — Test cases: Operating voltage ramp

EPL-CT-TC	V_{IUT} range: [V_{SUP} range/V_{BAT} range]	Signal ramp	Test
[EPL-CT 51].1	[15,0 V to 36 V]/[16,0 V to 36 V]	0,1 V/s	BR_Range_20K test
[EPL-CT 51].2	[36 V to 15,0 V]/[36 V to 16,0 V]	0,1 V/s	BR_Range_20K test
[EPL-CT 51].3	[7,0 V to 36 V]/[8,0 V to 36 V]	0,1 V/s	BR_Range_10K test
[EPL-CT 51].4	[36 V to 7,0 V]/[36 V to 8,0 V]	0,1 V/s	BR_Range_10K test

7.2.3 Threshold voltages

7.2.3.1 General

This group of tests checks whether the receiver threshold voltages of the IUT are implemented correctly within the entire specified operating supply voltage range. The LIN bus voltage is driven with a voltage ramp, checking the entire dominant and recessive signal area with respect to the applied supply voltage. In 7.2.3.2 and 7.2.3.3, the signal shall stay continuously on recessive or dominant level depending on the test case. In 7.2.3.4, the RX output transition is detected. Figure 45 shows the triangle signal on the LIN bus.

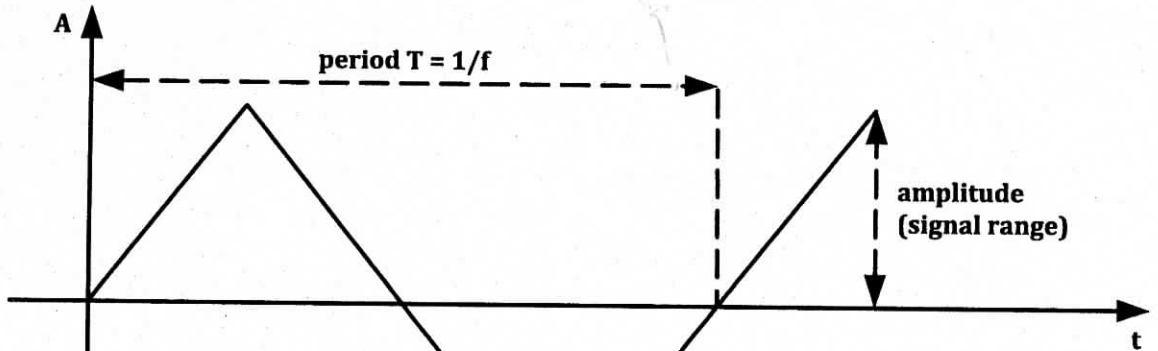

Figure 45 — Triangle signal on the LIN bus

7.2.3.2 [EPL-CT 52] IUT as receiver: V_{SUP} at V_{BUS_dom} (down)

Figure 46 shows the test configuration of the test system "IUT as receiver V_{SUP} at V_{BUS_dom} (down)".

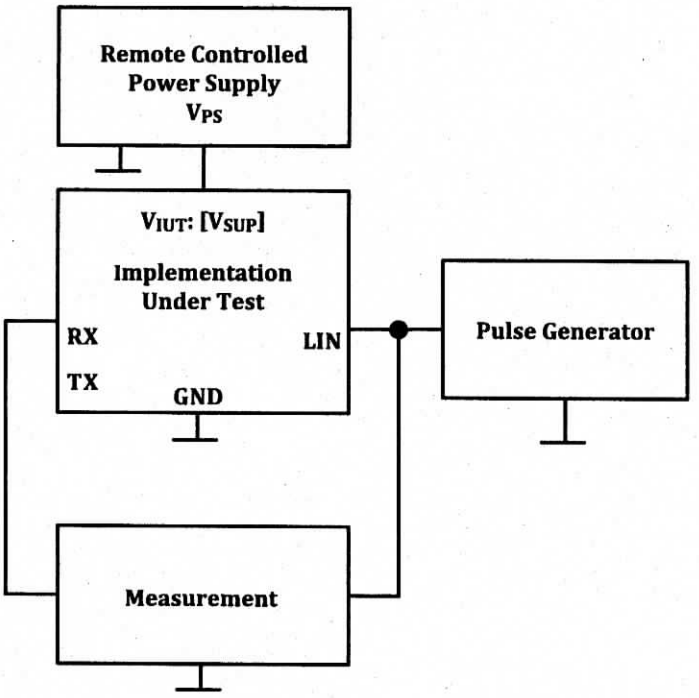

Figure 46 — Test system: IUT as receiver V_{SUP} at V_{BUS_dom} (down)

Table 99 defines the test system "IUT as receiver V_{SUP} at V_{BUS_dom} (down)".

Table 99 — Test system: IUT as receiver V_{SUP} at V_{BUS_dom} (down)

IUT node as	Class A device	[EPL–CT 52].1, [EPL–CT 52].2, [EPL–CT 52].3
Initial state	**Operational conditions:**	
	V_{IUT}: [V_{SUP}]	Table 100
Test steps	A triangle signal with f = 20 Hz and symmetry of 50 % is set on the LIN Bus (see Figure 45).	
Response	The IUT shall generate a dominant or recessive value on RX as defined on Table 100 during the falling slope of the triangle signal.	
Reference	ISO 17987–4:2016, Table 15, Param 62, Param 63 ISO 17987–4:2016, Figure 4	

Table 100 defines the test cases for the falling slope of the triangle signal on the LIN bus.

Table 100 — Test cases: Falling slope of the triangle signal on the LIN bus

EPL–CT–TC	V_{IUT}: [V_{SUP}]	Signal range	Expected RX signal	Test
[EPL–CT 52].1	7 V	[36 V to 4,2 V]	recessive	BR_Range_10K test
		[2,8 V to –1,05 V]	dominant	BR_Range_10K test
[EPL–CT 52].2	15 V	[36 V to 9,0 V]	recessive	BR_Range_20K, BR_Range_10K test
		[6,0 V to –2,25 V]	dominant	BR_Range_20K, BR_Range_10K test
[EPL–CT 52].3	36 V	[41,4 V to 21,6 V]	recessive	BR_Range_20K, BR_Range_10K test
		14,4 V to –5,4 V]	dominant	BR_Range_20K, BR_Range_10K test

7.2.3.3 [EPL–CT 53] IUT as receiver: V_{SUP} at V_{BUS_rec} (up)

Figure 47 shows the test configuration of the test system "IUT as receiver V_{SUP} at V_{BUS_rec} (up)".

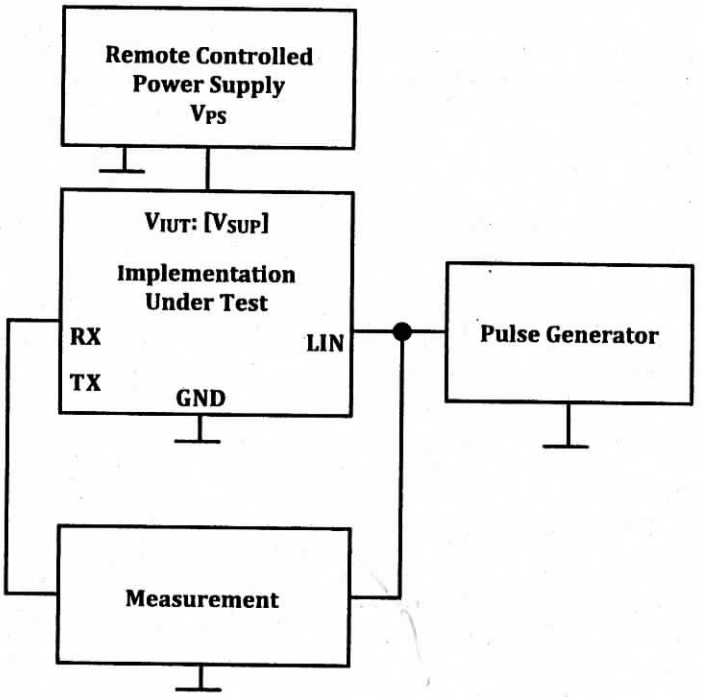

Figure 47 — Test system: IUT as receiver V_{SUP} at V_{BUS_rec} (up)

Table 101 defines the test system "IUT as receiver V_{SUP} at V_{BUS_rec} (up)".

Table 101 — Test system: IUT as receiver V_{SUP} at V_{BUS_rec} (up)

IUT node as	Class A device	[EPL–CT 53].1, [EPL–CT 53].2, [EPL–CT 53].3
Initial state	**Operational conditions:**	
	V_{IUT}: [V_{SUP}]	Table 102
Test steps	A triangle signal with f = 20 Hz and symmetry of 50 % is set on the LIN Bus (see Figure 45).	
Response	The IUT shall generate a dominant or recessive value on RX as defined on Table 102 during the rising slope of the triangle signal.	
Reference	ISO 17987–4:2016, Table 15, Param 62, Param 63 ISO 17987–4:2016, Figure 4	

Table 102 defines the test cases for the rising slope of the triangle signal on the LIN bus.

Table 102 — Test cases: Rising slope of the triangle signal on the LIN bus

EPL–CT–TC	V_{IUT}: [V_{SUP}]	Signal range	Expected RX signal	Test
[EPL–CT 53].1	7 V	[–1,05 V to 2,8 V]	dominant	BR_Range_10K test
		[4,2 V to 36 V]	recessive	BR_Range_10K test
[EPL–CT 53].2	15 V	[–2,25 V to 6,0 V]	dominant	BR_Range_20K, BR_Range_10K test
		[9,0 V to 36 V]	recessive	BR_Range_20K, BR_Range_10K test
[EPL–CT 53].3	36 V	[–5,4 V to 14,4 V]	dominant	BR_Range_20K, BR_Range_10K test
		[21,6 V to 41,4 V]	recessive	BR_Range_20K, BR_Range_10K test

7.2.3.4 [EPL-CT 54] IUT as receiver: V_{SUP} at V_{BUS}

This test shall verify the symmetry of the receiver thresholds. For this purpose, a voltage ramp on V_{BUS} shows the required threshold values.

Figure 48 shows the test configuration of the test system "IUT as receiver V_{SUP} at V_{BUS}".

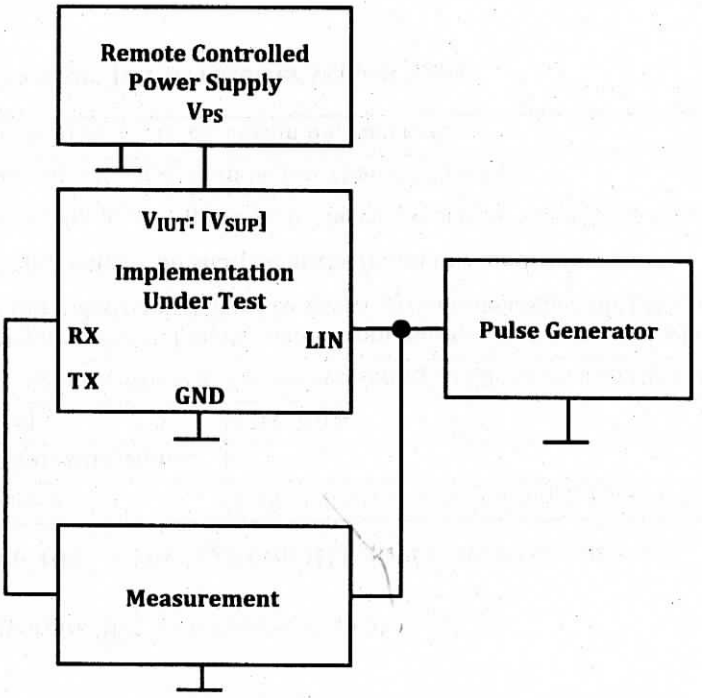

Figure 48 — Test system: IUT as receiver V_{SUP} at V_{BUS}

Table 103 defines the test system "IUT as receiver V_{SUP} at V_{BUS}".

Table 103 — Test system: IUT as receiver V_{SUP} at V_{BUS}

IUT node as	Class A device	[EPL-CT 54].1, [EPL-CT 54].2, [EPL-CT 54].3
Initial state	**Operational conditions:**	
	V_{IUT}: [V_{SUP}]	Table 104
Test steps	A triangle signal with f = 20 Hz and symmetry of 50 % is set on the LIN Bus (see Figure 45).	
Response	The RX output of the IUT shall switch from dominant to recessive when the LIN bus voltage ramps up and it shall switch from recessive to dominant when the LIN bus voltage ramps down. The RX output transition shall meet the following conditions: $V_{BUS\_CNT} = (V_{th\_dom} + V_{th\_rec})/2$ in the range of (0,475 to 0,525) × V_{SUP} $V_{HYS} = V_{th\_rec} - V_{th\_dom}$ shall be less than 0,175 × V_{SUP}	
Reference	ISO 17987-4:2016, Table 15, Param 64, Param 65	

Table 104 defines the test cases for "IUT as receiver V_{SUP} at V_{BUS}".

Table 104 — Test cases: IUT as receiver V_{SUP} at V_{BUS}

EPL-CT-TC	V_{IUT}: [V_{SUP}]	Signal range	Test
[EPL-CT 54].1	7 V	[-1,05 V to 8,05 V] up [8,05 V to -1,05 V] down	BR_Range_10K test
[EPL-CT 54].2	15 V	[-2,25 V to 17,25 V] up [17,25 V to -2,25 V] down	BR_Range_20K, BR_Range_10K test
[EPL-CT 54].3	36 V	[-5,4 V to 41,4 V] up [41,4 V to -5,4 V] down	BR_Range_20K, BR_Range_10K test

7.2.4 [EPL-CT 55] Variation of $V_{SUP\_NON\_OP}$

The variation of $V_{SUP\_NON\_OP}$ shall be checked within this test, whether the IUT influences the bus during under voltage and over voltage conditions.

Figure 49 shows the test configuration of the test system "Variation of $V_{SUP\_NON\_OP}$".

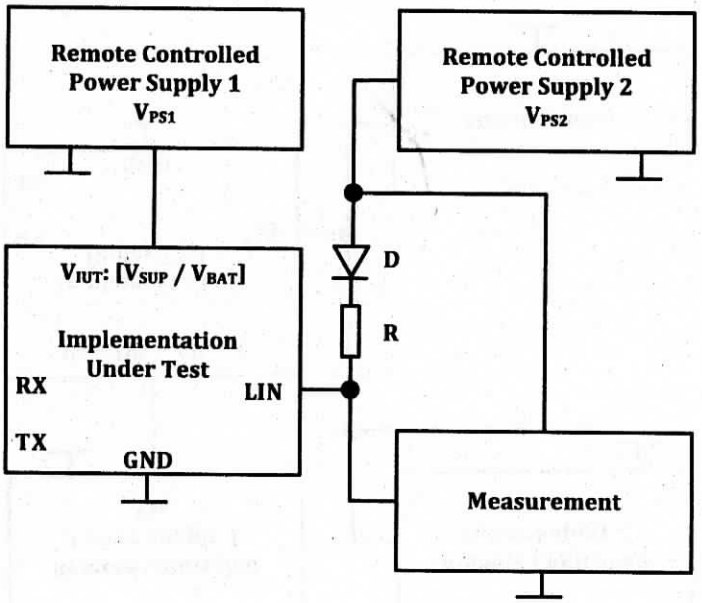

Figure 49 — Test system: Variation of $V_{SUP\_NON\_OP}$

Table 105 defines the test system "Variation of $V_{SUP\_NON\_OP}$".

Table 105 — Test system: Variation of $V_{SUP\_NON\_OP}$

IUT node as	Class B device as master	[EPL-CT 55].1 (BR_Range_20K)/ [EPL-CT 55].4 (BR_Range_10K)
	Class B device as slave	[EPL-CT 55].2 (BR_Range_20K)/ [EPL-CT 55].5 (BR_Range_10K)
	Class A device	[EPL-CT 55].3 (BR_Range_20K)/ [EPL-CT 55].6 (BR_Range_10K)
Initial state	**Operational conditions:**	
	V_{IUT}: [V_{SUP}/V_{BAT}]	V_{IUT} Signal with a 1 V/s ramp in the range
	V_{IUT}; V_{PS2}	See Table 106
	Bus load	See Table 106

Table 105 *(continued)*

Test steps	A voltage ramp (up and down) is set on V_{IUT1}. The stimulus stays for t = 30 s at V_{IUT1} = 58 V. The TX signal shall be left open, if an internal pull-up is provided or applied with a recessive level.
Response	No dominant state on LIN shall occur. The IUT shall not be destroyed during the test. The afterward recessive voltage shall have a maximum deviation of ±5 % from the before recessive voltage.
Reference	ISO 17987-4:2016, Table 15, Param 56

Table 106 defines the test cases "Variation of $V_{SUP\_NON\_OP}$".

Table 106 — Test cases: Variation of $V_{SUP\_NON\_OP}$

EPL-CT-TC	V_{IUT} range: [V_{SUP} range/V_{BAT} range]	V_{PS2}	Bus load	Test
[EPL-CT 55].1	[-0,3 V to 16 V], [36 V to 58 V]	36 V	60 k + diode (1N4148)	BR_Range_20K test
[EPL-CT 55].2	[-0,3 V to 16 V], [36 V to 58 V]	36 V	1,1 k + diode (1N4148)	BR_Range_20K test
[EPL-CT 55].3	[-0,3 V to 15 V], [36 V to 58 V]	36 V	1,1 k + diode (1N4148)	BR_Range_20K test
[EPL-CT 55].4	[-0,3 V to 8 V], [36 V to 58 V]	36 V	60 k + diode (1N4148)	BR_Range_10K test
[EPL-CT 55].5	[-0,3 V to 8 V], [36 V to 58 V]	36 V	1,1 k + diode (1N4148)	BR_Range_10K test
[EPL-CT 55].6	[-0,3 V to 7 V], [36 V to 58 V]	36 V	1,1 k + diode (1N4148)	BR_Range_10K test

7.2.5 I_{BUS} under several conditions

7.2.5.1 [EPL-CT 56] I_{BUS_LIM} at dominant state (driver on)

This test checks the drive capability of the output stage. A LIN driver shall pull the LIN bus below a certain voltage according to the LIN standard. The current limitation is measured indirectly.

Figure 50 shows the test configuration of the test system "I_{BUS_LIM} at dominant state (driver on)".

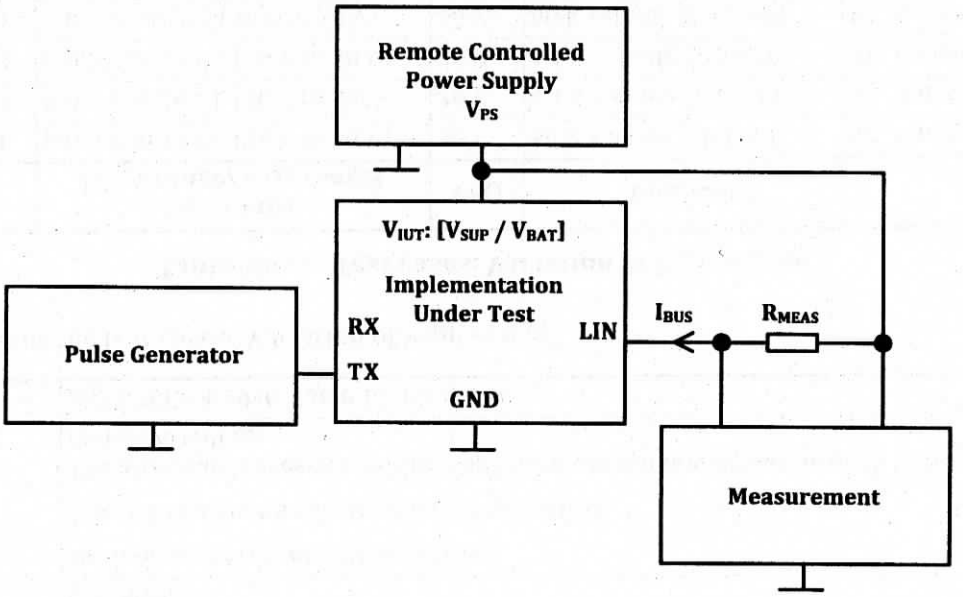

Figure 50 — Test system: I_{BUS_LIM} at dominant state (driver on)

Table 107 defines the test system "I_{BUS_LIM} at dominant state (driver on)".

Table 107 — Test system: I_{BUS_LIM} at dominant state (driver on)

IUT node as	Class B device as master Class B device as slave Class A device	[EPL-CT 56].1
Initial state	**Operational conditions:**	
	V_{IUT}: [V_{SUP}/V_{BAT}] R_{MEAS}	See Table 108
Test steps	The LIN pin is connected via R_{MEAS} to V_{IUT}. The TX signal is driven with a rectangular signal (T = 10 ms) with a duty cycle of 50 %.	
Response	LIN shall show the rectangular Signal. The dominant state bus level shall be lower than TH_DOM = 0,284 × V_{IUT} = 10,224 V for transceiver. The dominant state bus level shall be lower than TH_DOM = 0,284 × (V_{IUT} – 1 V) = 9,94 V for ECU's.	
Reference	ISO 17987-4:2016, Table 15, Param 57	

Table 108 defines the test cases "I_{BUS_LIM} at dominant state (driver on)".

Table 108 — Test cases: I_{BUS_LIM} at dominant state (driver on)

EPL-CT-TC	V_{IUT}: [V_{SUP}/V_{BAT}]	R_{MEAS}
[EPL-CT 56].1	36 V	480 Ω (0,1 %)

7.2.5.2 [EPL-CT 57] $I_{BUS\_PAS\_dom}$: IUT in recessive state: V_{BUS} = 0 V

This test case is intended to test the input leakage current $I_{BUS\_PAS\_dom}$ into a node during dominant state of the LIN bus.

Figure 51 shows the test configuration of the test system "$I_{BUS\_PAS\_dom}$ IUT in recessive state V_{BUS} = 0 V".

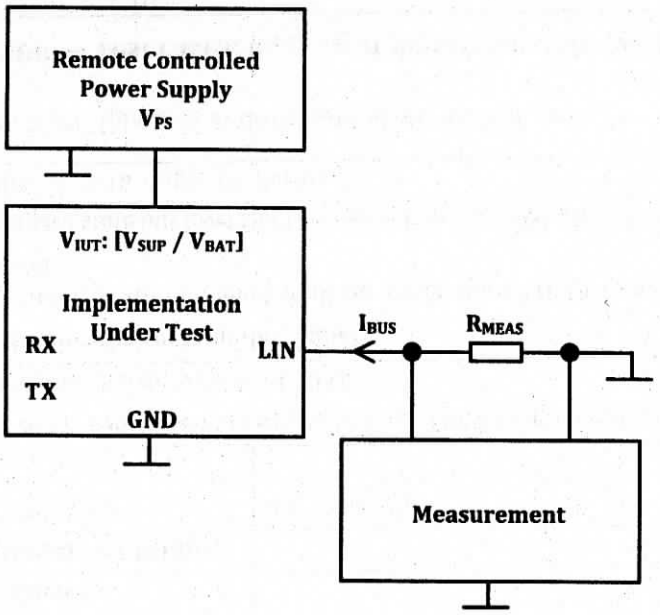

Figure 51 — Test system: $I_{BUS\_PAS\_dom}$ IUT in recessive state V_{BUS} = 0 V

Table 109 defines the test system "$I_{BUS\_PAS\_dom}$ IUT in recessive state V_{BUS} = 0 V".

Table 109 — Test system: $I_{BUS\_PAS\_dom}$ IUT in recessive state V_{BUS} = 0 V

IUT node as	Class B device as slave Class A device	[EPL-CT 57].1
Initial state	**Operational conditions:**	
	V_{IUT}: [V_{SUP}/V_{BAT}] R_{MEAS}	See Table 110
Test steps	The TX signal is set recessive.	
Response	The maximum value of voltage drop shall be higher than -1 000 mV.	
Reference	ISO 17987-4:2016, Table 15, Param 58	

Table 110 defines the test cases "$I_{BUS\_PAS\_dom}$ IUT in recessive state V_{BUS} = 0 V".

Table 110 — Test cases: $I_{BUS\_PAS\_dom}$ IUT in recessive state V_{BUS} = 0 V

EPL-CT-TC	V_{IUT}: [V_{SUP}/V_{BAT}]	R_{MEAS}
[EPL-CT 57].1	24 V	499 Ω (0,1 %)

7.2.5.3 [EPL-CT 58] $I_{BUS\_PAS\_rec}$: IUT in recessive state: V_{SUP} = 7,0 V with variation of V_{BUS} ∈ [8,0 V to 36 V]

This test checks whether there is a diode implementation within the termination path of the IUT. The reverse current should be limited to $I_{BUS\_PAS\_rec(max)}$ from the LIN wire into the IUT even if V_{BUS} is higher than the IUTs supply voltage V_{IUT}.

Figure 52 shows the test configuration of the test system "$I_{BUS\_PAS\_rec}$ IUT in recessive state".

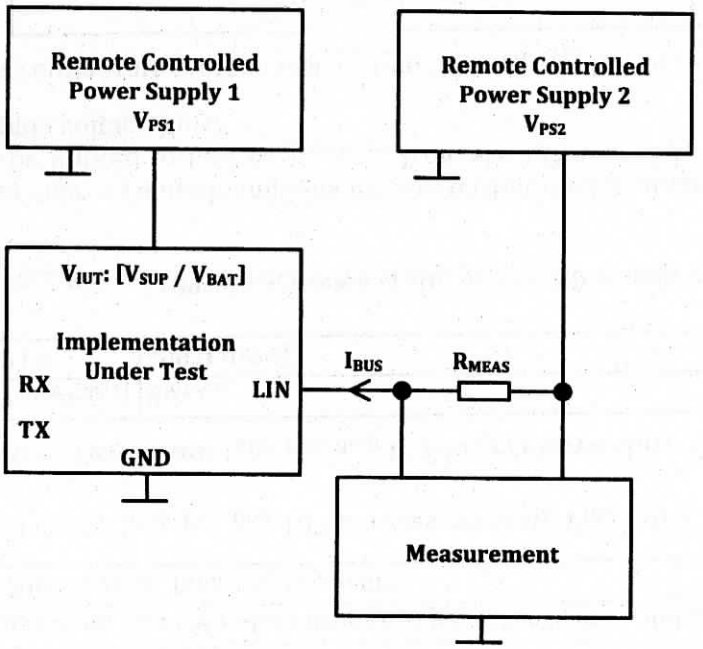

Figure 52 — Test system: $I_{BUS\_PAS\_rec}$ IUT in recessive state

Table 111 defines the test system "$I_{BUS\_PAS\_rec}$ IUT in recessive state".

Table 111 — Test system: $I_{BUS\_PAS\_rec}$ IUT in recessive state

IUT node as	Class B device as master Class B device as slave Class A device	[EPL–CT 58].1
Initial state	**Operational conditions:**	
	V_{IUT}: [V_{SUP}/V_{BAT}]	See Table 112
	R_{MEAS}	
Test steps	V_{PS2} = Signal with a 2 V/s ramp in the range [8 V to 36 V] up and down. The TX signal is set recessive.	
Response	The maximum value of voltage drop shall be less than or equal to 20 mV.	
Reference	ISO 17987–4:2016, Table 15, Param 59	

Table 112 defines the test case "$I_{BUS\_PAS\_rec}$ IUT in recessive state".

Table 112 — Test cases: $I_{BUS\_PAS\_rec}$ IUT in recessive state

EPL–CT–TC	V_{IUT}: [V_{SUP}/V_{BAT}]	R_{MEAS}
[EPL–CT 58].1	7,0 V/8,0 V	1 000 Ω (0,1 %)

7.2.6 Slope control

7.2.6.1 Purpose

The purpose of this test is to check the duty cycle of the driver stage.

7.2.6.2 [EPL–CT 59] Measuring the duty cycle at 10,417 kbit/s — IUT as transmitter

Figure 53 shows the test configuration of the test system "Slope control".

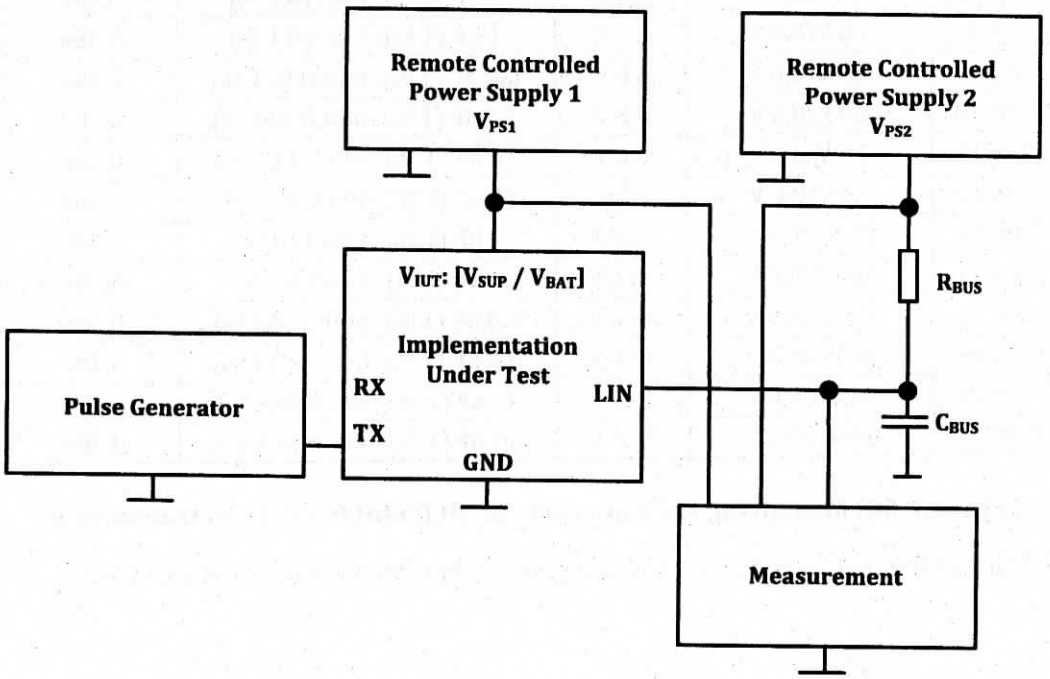

Figure 53 — Test system: Slope control

Table 113 defines the test system "Slope control".

Table 113 — Test system: Slope control (BR_Range_10K)

IUT node as	Class B device as master or slave Class A device	[EPL-CT 59].1 to [EPL-CT 59].18
Initial state	**Operational conditions:**	
	Bus loads	See Table 114
	V_{IUT}: [V_{SUP}/V_{BAT}]	See Table 114
	V_{PS2}	See Table 114
Test steps	TXD is driven with a rectangular signal (T = 192 µs) with a duty cycle of 50 %. TXD slope time <500 ns, 100 % voltage swing.	
Response	The measured duty cycle D3 shall be greater or equal than 0,386 for V_{SUP} = [7,0 V to 36 V], the measured duty cycle D4 shall be less than or equal to 0,591 for V_{SUP} = [7,6 V to 36 V]. If V_{SUP} is not accessible, then V_{BAT} – 0,7 V shall be used for calculation of the duty cycle.	
Reference	ISO 17987-4:2016, Table 18, Param 74, Param 75 ISO 17987-4:2016, Figure 5	

Table 114 defines the test cases "Slope control".

Table 114 — Test cases: Slope control

EPL-CT-TC	V_{IUT}: [V_{SUP}/V_{BAT}] (PS 1)	V_{PS2} (PS 2)	Bus loads (C_{BUS}; R_{BUS})	Duty cycle	
				D3 min.	D4 max.
[EPL-CT 59].1	7,0 V/8,0 V	6,0 V	1 nF (1 %); 1 kΩ (0,1 %)	0,386	—
[EPL-CT 59].2	7,0 V/8,0 V	6,6 V	1 nF (1 %); 1 kΩ (0,1 %)	0,386	—
[EPL-CT 59].3	7,0 V/8,0 V	6,0 V	6,8 nF (1 %); 660 Ω (0,1 %)	0,386	—
[EPL-CT 59].4	7,0 V/8,0 V	6,6 V	6,8 nF (1 %); 660 Ω (0,1 %)	0,386	-
[EPL-CT 59].5	7,0 V/8,0 V	6,0 V	10 nF (1 %); 500 Ω (0,1 %)	0,386	—
[EPL-CT 59].6	7,0 V/8,0 V	6,6 V	10 nF (1 %); 500 Ω (0,1 %)	0,386	—
[EPL-CT 59].7	7,6 V/8,6 V	6,6 V	1 nF (1 %); 1 kΩ (0,1 %)	0,386	0,591
[EPL-CT 59].8	7,6 V/8,6 V	7,2 V	1 nF (1 %); 1 kΩ (0,1 %)	0,386	0,591
[EPL-CT 59].9	7,6 V/8,6 V	6,6 V	6,8 nF (1 %); 660 Ω (0,1 %)	0,386	0,591
[EPL-CT 59].10	7,6 V/8,6 V	7,2 V	6,8 nF (1 %); 660 Ω (0,1 %)	0,386	0,591
[EPL-CT 59].11	7,6 V/8,6 V	6,6 V	10 nF (1 %); 500 Ω (0,1 %)	0,386	0,591
[EPL-CT 59].12	7,6 V/8,6 V	7,2 V	10 nF (1 %); 500 Ω (0,1 %)	0,386	0,591
[EPL-CT 59].13	36 V/36,6 V	35,0 V	1 nF (1 %); 1 kΩ (0,1 %)	0,386	0,591
[EPL-CT 59].14	36 V/36,6 V	35,6 V	1 nF (1 %); 1 kΩ (0,1 %)	0,386	0,591
[EPL-CT 59].15	36 V/36,6 V	35,0 V	6,8 nF (1 %); 660 Ω (0,1 %)	0,386	0,591
[EPL-CT 59].16	36 V/36,6 V	35,6 V	6,8 nF (1 %); 660 Ω (0,1 %)	0,386	0,591
[EPL-CT 59].17	36 V/36,6 V	35,0 V	10 nF (1 %); 500 Ω (0,1 %)	0,386	0,591
[EPL-CT 59].18	36 V/36,6 V	35,6 V	10 nF (1 %); 500 Ω (0,1 %)	0,386	0,591

7.2.6.3 [EPL-CT 60] Measuring the duty cycle at 20,0 kbit/s— IUT as transmitter

Figure 54 shows the test configuration of the test system "Measuring the duty cycle".

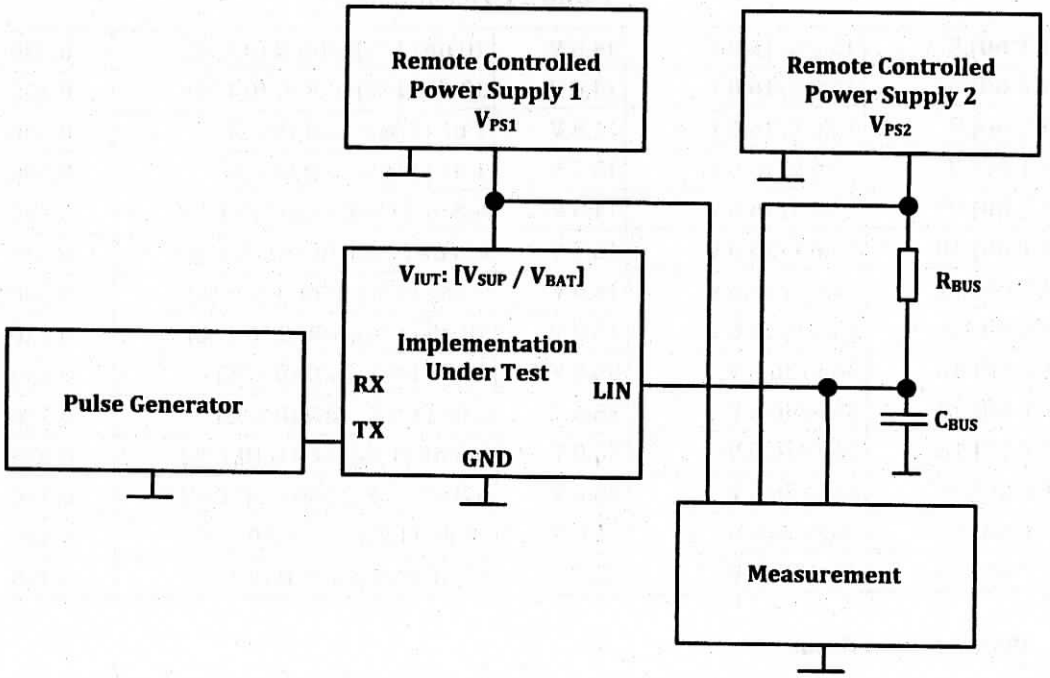

Figure 54 — Test system: Measuring the duty cycle

Table 115 defines the test system "Measuring the duty cycle".

Table 115 — Test system: Measuring the duty cycle (BR_Range_20K)

IUT node as	Class B device as master or slave Class A device	[EPL-CT 60].1 to [EPL-CT 60].18
Initial state	**Operational conditions:**	
	Bus loads	See Table 116
	V_{IUT}: [V_{SUP}/V_{BAT}]	See Table 116
	V_{PS2}	See Table 116
Test steps	TXD is driven with a rectangular signal (T = 100 µs) with a duty cycle of 50 %. TXD slope time <500 ns, 100 % voltage swing.	
Response	The measured duty cycle D1 shall be greater or equal than 0,330 for V_{SUP} = [15,0 V to 36 V], the measured duty cycle D2 shall be less than or equal to 0,642 for V_{SUP} = [15,6 V to 36 V]. If V_{SUP} is not accessible, then V_{BAT} – 0,7 V shall be used for calculation of the duty cycle.	
Reference	ISO 17987-4:2016, Table 17, Param 72, Param 73 ISO 17987-4:2016, Figure 5	

Table 116 defines the test cases "Measuring the duty cycle".

Table 116 — Test cases: Measuring the duty cycle

EPL-CT-TC	V_{IUT}: [V_{SUP}/V_{BAT}] (PS 1)	V_{PS2} (PS 2)	Bus loads (C_{BUS}; R_{BUS})	Duty cycle	
				D1 min.	D2 max.
[EPL-CT 60].1	15,0 V/16,0 V	14,0 V	1 nF (1 %); 1 kΩ (0,1 %)	0,330	—
[EPL-CT 60].2	15,0 V/16,0 V	14,6 V	1 nF (1 %); 1 kΩ (0,1 %)	0,330	—
[EPL-CT 60].3	15,0 V/16,0 V	14,0 V	6,8 nF (1 %); 660 Ω (0,1 %)	0,330	—
[EPL-CT 60].4	15,0 V/16,0 V	14,6 V	6,8 nF (1 %); 660 Ω (0,1 %)	0,330	—

Table 116 *(continued)*

[EPL-CT 60].5	15,0 V/16,0 V	14,0 V	10 nF (1 %); 500 Ω (0,1 %)	0,330	—
[EPL-CT 60].6	15,0 V/16,0 V	14,6 V	10 nF (1 %); 500 Ω (0,1 %)	0,330	—
[EPL-CT 60].7	15,6 V/16,6 V	14,6 V	1 nF (1 %); 1 kΩ (0,1 %)	0,330	0,642
[EPL-CT 60].8	15,6 V/16,6 V	15,2 V	1 nF (1 %); 1 kΩ (0,1 %)	0,330	0,642
[EPL-CT 60].9	15,6 V/16,6 V	14,6 V	6,8 nF (1 %); 660 Ω (0,1 %)	0,330	0,642
[EPL-CT 60].10	15,6 V/16,6 V	15,2 V	6,8 nF (1 %); 660 Ω (0,1 %)	0,330	0,642
[EPL-CT 60].11	15,6 V/16,6 V	14,6 V	10 nF (1 %); 500 Ω (0,1 %)	0,330	0,642
[EPL-CT 60.12	15,6 V/16,6 V	15,2 V	10 nF (1 %); 500 Ω (0,1 %)	0,330	0,642
[EPL-CT 60].13	36 V/36,6 V	35,0 V	1 nF (1 %); 1 kΩ (0,1 %)	0,330	0,642
[EPL-CT 60].14	36 V/36,6 V	35,6 V	1 nF (1 %); 1 kΩ (0,1 %)	0,330	0,642
[EPL-CT 60].15	36 V/36,6 V	35,0 V	6,8 nF (1 %); 660 Ω (0,1 %)	0,330	0,642
[EPL-CT 60].16	36 V/36,6 V	35,6 V	6,8 nF (1 %); 660 Ω (0,1 %)	0,330	0,642
[EPL-CT 60].17	36 V/36,6 V	35,0 V	10 nF (1 %); 500 Ω (0,1 %)	0,330	0,642
[EPL-CT 60].18	36 V/36,6 V	35,6 V	10 nF (1 %); 500 Ω (0,1 %)	0,330	0,642

7.2.7 Propagation delay

7.2.7.1 Overview

The following test checks the receiver's internal delay and its symmetry. The method for measuring the values is shown in ISO 17987-4:2016, Figure 5.

7.2.7.2 [EPL-CT 61] Propagation delay of the receiver

Figure 55 shows the test configuration of the test system "Propagation delay".

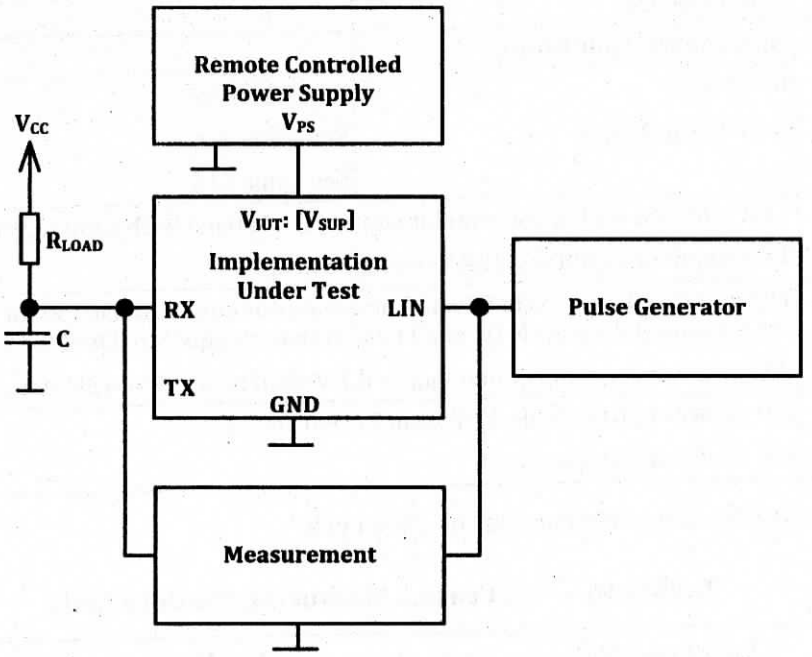

Figure 55 — Test system: Propagation delay

Table 117 defines the test system "Propagation delay".

Table 117 — Test system: Propagation delay

IUT node as	Class A device	[EPL-CT 61].1, [EPL-CT 61].2, [EPL-CT 61].3
Initial state	**Operational conditions:**	
	RXD	C = 20 pF (5 %)
	V_{IUT}: [V_{SUP}]	R_{LOAD} = 2,4 kΩ (0,1 %): pull-up resistor for "open drain" transceiver only; see Table 118
	V_{CC}	Depends on device under test (5 V or 3,3 V)
Test steps	LIN bus is driven with a 5 kHz rectangular signal with a duty cycle of 50 %, V_{BUS} starts at V_{SUP} and ramps down to 0 V within 40 ns and vice versa.	
Response	The measured time t_{rx_pd} shall be less than 6 µs. $t_{rx\_sym} = t_{rx\_pdf} - t_{rx\_pdr}$ shall be in the range -2 to +2 µs.	
Reference	ISO 17987-4:2016, Table 19, Param 76, Param 77 ISO 17987-4:2016, Figure 5	

Table 118 defines the test cases "Propagation delay".

Table 118 — Test cases: Propagation delay

EPL-CT-TC	V_{IUT}: [V_{SUP}]	Test
[EPL-CT 61].1	7,0 V	BR_Range_10K test
[EPL-CT 61].2	15 V	BR_Range_20K, BR_Range_10K test
[EPL-CT 61].3	36 V	BR_Range_20K, BR_Range_10K test

7.2.8 Supply voltage offset

7.2.8.1 Purpose

The purpose of this test is to check the robustness in case of V_{BAT} and ground shift.

7.2.8.2 GND/V_{BAT} shift test — Dynamic

Figure 56 shows the test configuration of the test system "GND — V_{BAT} shift test — Dynamic".

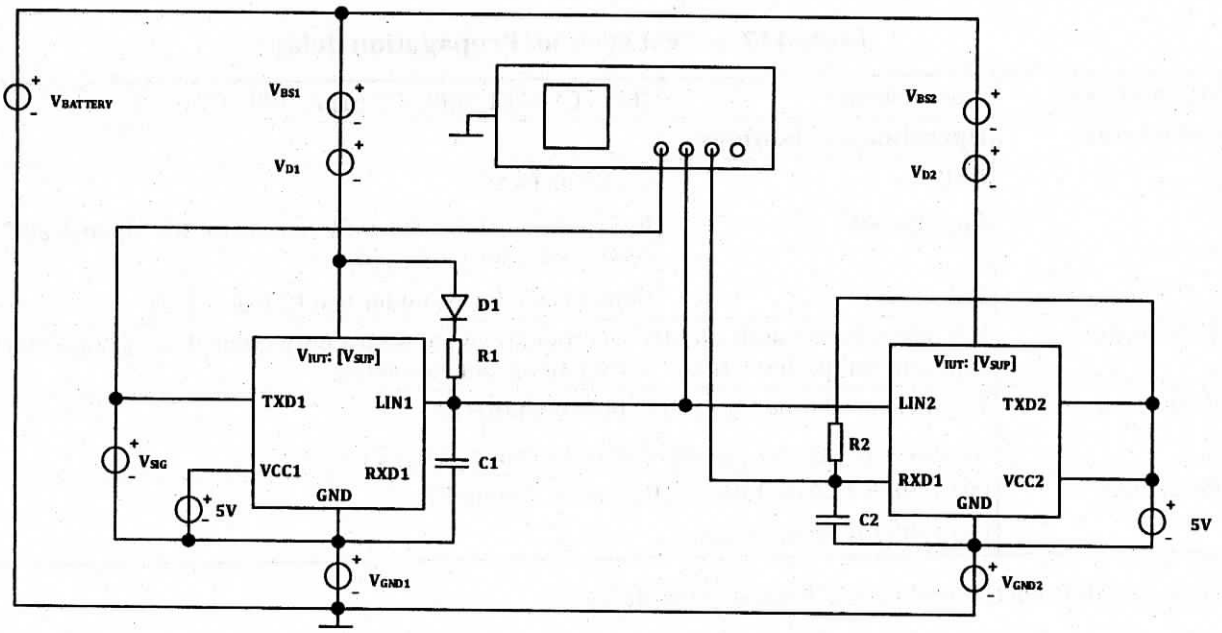

Figure 56 — Test system: GND — V_{BAT} shift test — Dynamic

Concept: The two operating voltages (V_{CC} and V_{SUP}) are ground-free and completely decoupled from each other and with that, a superposition with each of these voltages with low frequency and high frequency can be realized independently.

The operating voltages V_{CC} depends on the specific part (3,3 V or 5 V). However, they may be varied indirectly through suitable triggering. The two voltages need independent, ground-free direct current supplies, in order to exclude interconnections.

7.2.8.3 [EPL-CT 62] GND shift test — Dynamic — IUT as a class A device

Table 119 defines the test system "IUT as BR_Range_20K 24 V class A device".

Table 119 — Test system: Dynamic — IUT for a BR_Range_20K 24 V LIN Class A device

IUT node as	Class A device	[EPL-CT 62].1
Initial state	**Operational conditions:**	
	$V_{BATTERY}$	18,4 V
	V_{BS1}	0,1 × $V_{BATTERY}$
	V_{D1}	1 V
	V_{GND1}	0,03 × $V_{BATTERY}$
	V_{BS2}	0,03 × $V_{BATTERY}$
	V_{D2}	0,4 V
	V_{GND2}	[0,5 × sin(2 × π × 5 × t) + 0,5] × 0,1 × $V_{BATTERY}$ 5 Hz sinus signal with offset
	C2	20 pF (including input capacitance of oscilloscope)
	R2	2,4 kΩ (0,1 %): Only for open drain transceiver assembled
Test steps	A signal at 10 kHz is set on TXD1. The test shall be done with R1 = 1 kΩ (0,1 %) and C1 = 1 nF (1 %). The test shall be repeated with R1 = 500 Ω (0,1 %) and C1 = 10 nF (1 %).	
Response	The duty cycle measured at RXD2 shall be in the range of 0,310, 0,662 (D1 – 2 µs to D2 + 2 µs).	
Reference	ISO 17987-4:2016, Table 15, Param 68 ISO 17987-4:2016, Table 17, Param 72, 73	

7.2.8.4 [EPL-CT 63] GND shift test — Dynamic — IUT as a class A device

Table 120 defines the test system "IUT as BR_Range_10K 24 V class A device".

Table 120 — Test system: Dynamic — IUT for as a BR_Range_10K class A device

IUT node as	Class A device	[EPL-CT 63].1
Initial state	**Operational conditions:**	
	$V_{BATTERY}$	9,2 V
	V_{BS1}	0,1 × $V_{BATTERY}$
	V_{D1}	1 V
	V_{GND1}	0,03 × $V_{BATTERY}$
	V_{BS2}	0,03 × $V_{BATTERY}$
	V_{D2}	0,4 V
	V_{GND2}	[0,5 × sin(2 × π × 5 × t) + 0,5] × 0,1 × $V_{BATTERY}$ 5 Hz sinus signal with offset
	C2	20 pF (including input capacitance of oscilloscope)
	R2	2,4 kΩ (0,1 %): Only for open drain transceiver assembled
Test steps	A signal at 5,208 kHz is set on TXD1. The test shall be done with R1 = 1 kΩ (0,1 %) and C1 = 1 nF (1 %). The test shall be repeated with R1 = 500 Ω (0,1 %) and C1 = 10 nF (1 %).	
Response	The duty cycle measured at RXD2 shall be in the range of 0,366 to 0,611 (D3 – 2 µs to D4 + 2 µs).	
Reference	ISO 17987-4:2016, Table 15, Param 68 ISO 17987-4:2016, Table 18, Param 74, 75	

7.2.8.5 [EPL-CT 64] GND shift test — Dynamic — IUT as a class A device

Table 121 defines the test system "Dynamic — IUT as BR_Range_20K 24 V class A device".

Table 121 — Test system: Dynamic — IUT as a BR_Range_20K class A device

IUT node as	Class A device	[EPL-CT 64].1
Initial state	**Operational conditions:**	
	$V_{BATTERY}$	18,4 V
	V_{BS1}	0,03 × $V_{BATTERY}$
	V_{D1}	0,4 V
	V_{GND1}	[0,5 × sin(2 × π × 5 × t) + 0,5] × 0,1 × $V_{BATTERY}$ 5 Hz sinus signal with offset
	V_{BS2}	0,1 × $V_{BATTERY}$
	V_{D2}	1 V
	V_{GND2}	0,03 × $V_{BATTERY}$
	C2	20 pF (including input capacitance of oscilloscope)
	R2	2,4 kΩ (0,1 %): Only for open drain transceiver assembled
Test steps	A signal at 10 kHz is set on TXD1. The test shall be done with R1 = 1 kΩ (0,1 %) and C1 = 1 nF (1 %). The test shall be repeated with R1 = 500 Ω (0,1 %) and C1 = 10 nF (1 %).	
Response	The duty cycle measured at RXD2 shall be in the range of 0,310 to 0,662 (D1 – 2 µs to D2 + 2 µs).	
Reference	ISO 17987-4:2016, Table 15, Param 68 ISO 17987-4:2016, Table 17, Param 72, 73	

7.2.8.6 [EPL-CT 65] GND shift test — Dynamic — IUT as a class A device

Table 122 defines the test system "Dynamic — IUT as BR_Range_10K 24 V class A device".

Table 122 — Test system: Dynamic — IUT as a BR_Range_10K class A device

IUT node as	Class A device	[EPL-CT 65].1
Initial state	**Operational conditions:**	
	$V_{BATTERY}$	9,2 V
	V_{BS1}	0,03 × $V_{BATTERY}$
	V_{D1}	0,4 V
	V_{GND1}	[0,5 × sin(2 × π × 5 × t) + 0,5] × 0,1 × $V_{BATTERY}$ 5 Hz sinus signal with offset
	V_{BS2}	0,1 × $V_{BATTERY}$
	V_{D2}	1 V
	V_{GND2}	0,03 × $V_{BATTERY}$
	C2	20 pF (including input capacitance of oscilloscope)
	R2	2,4 kΩ (0,1 %): Only for open drain transceiver assembled
Test steps	A signal at 5,208 kHz is set on TXD1. The test shall be done with R1 = 1 kΩ (0,1 %) and C1 = 1 nF (1 %). The test shall be repeated with R1 = 500 Ω (0,1 %) and C1 = 10 nF (1 %).	
Response	The duty cycle measured at RXD2 shall be in the range of 0,375 to 0,601 (D3 – 2 µs to D4 + 2 µs).	
Reference	ISO 17987-4:2016, Table 15, Param 68 ISO 17987-4:2016, Table 17, Param 72, 73	

7.2.8.7 [EPL-CT 66] V_{BAT} shift test — Dynamic — IUT as a class A device

Table 123 defines the test system "Dynamic — IUT as a BR_Range_20K 24 V LIN Class A device".

Table 123 — Test system: Dynamic — IUT as a BR_Range_20K 24 V LIN Class A device

IUT node as	Class A device	[EPL-CT 66].1
Initial state	**Operational conditions:**	
	$V_{BATTERY}$	18,4 V
	V_{BS1}	[0,5 × sin(2 × π × 5 × t) + 0,5] × 0,1 × $V_{BATTERY}$ 5 Hz sinus signal with offset
	V_{D1}	1 V
	V_{GND1}	0,03 × $V_{BATTERY}$
	V_{BS2}	0,03 × $V_{BATTERY}$
	V_{D2}	0,4 V
	V_{GND2}	0,1 × $V_{BATTERY}$
	C2	20 pF (including input capacitance of oscilloscope)
	R2	2,4 kΩ (0,1 %): Only for open drain transceiver assembled
Test steps	A signal at 10 kHz is set on TXD1. The test shall be done with R1 = 1 kΩ (0,1 %) and C1 = 1 nF (1 %). The test shall be repeated with R1 = 500 Ω (0,1 %) and C1 = 10 nF (1 %).	
Response	The duty cycle measured at RXD2 shall be in the range of 0,310 to 0,662 (D1 – 2 µs to D2 + 2 µs).	
Reference	ISO 17987-4:2016, Table 15, Param 67 ISO 17987-4:2016, Table 17, Param 72, 73	

7.2.8.8 [EPL-CT 67] V_{BAT} shift test — Dynamic — IUT as a class A device

Table 124 defines the test system "Dynamic — IUT as a BR_Range_10K 24 V class A device".

Table 124 — Test system: Dynamic — IUT as a BR_Range_10K class A device

IUT node as	Class A device	[EPL-CT 67].1
Initial state	**Operational conditions:**	
	$V_{BATTERY}$	9,2 V
	V_{BS1}	[0,5 × sin(2 × π × 5 × t) + 0,5] × 0,1 × $V_{BATTERY}$ 5 Hz sinus signal with offset
	V_{D1}	1 V
	V_{GND1}	0,03 × $V_{BATTERY}$
	V_{BS2}	0,03 × $V_{BATTERY}$
	V_{D2}	0,4 V
	V_{GND2}	0,1 × $V_{BATTERY}$
	C2	20 pF (including input capacitance of oscilloscope)
	R2	2,4 kΩ (0,1 %): Only for open drain transceiver assembled
Test steps	A signal at 5,208 kHz is set on TXD1. The test shall be done with R1 = 1 kΩ (0,1 %) and C1 = 1 nF (1 %). The test shall be repeated with R1 = 500 Ω (0,1 %) and C1 = 10 nF (1 %).	
Response	The duty cycle measured at RXD2 shall be in the range of 0,375 to 0,601 (D3 – 2 µs to D4 + 2 µs).	
Reference	ISO 17987-4:2016, Table 15, Param 67 ISO 17987-4:2016, Table 18, Param 74, 75	

7.2.8.9 [EPL-CT 68] V_{BAT} shift test — Dynamic — IUT as a class A device

Table 125 defines the test system "Dynamic — IUT as a BR_Range_20K 24 V class A device.

Table 125 — Test system: Dynamic — IUT as BR_Range_20K class A device

IUT node as	Class A device	[EPL-CT 68].1
Initial state	**Operational conditions:**	
	$V_{BATTERY}$	18,4 V
	V_{BS1}	0,03 × $V_{BATTERY}$
	V_{D1}	0,4 V
	V_{GND1}	0,1 × $V_{BATTERY}$
	V_{BS2}	[0,5 × sin(2 × π × 5 × t) + 0,5] × 0,1 × $V_{BATTERY}$ 5 Hz sinus signal with offset
	V_{D2}	1 V
	V_{GND2}	0,03 × $V_{BATTERY}$
	C2	20 pF (including input capacitance of oscilloscope)
	R2	2,4 kΩ (0,1 %): Only for open drain transceiver assembled
Test steps	A signal at 10 kHz is set on TXD1. The test shall be done with R1 = 1 kΩ (0,1 %) and C1 = 1 nF (1 %). The test shall be repeated with R1 = 500 Ω (0,1 %) and C1 = 10 nF (1 %).	
Response	The duty cycle measured at RXD2 shall be in the range of 0,310 to 0,662 (D1 – 2 µs to D2 + 2 µs).	
Reference	ISO 17987-4:2016, Table 15, Param 67 ISO 17987-4:2016, Table 17, Param 72, 73	

7.2.8.10 [EPL-CT 69] V_{BAT} shift test — Dynamic — IUT as a class A device

Table 126 defines the test system "Dynamic — IUT as a BR_Range_10K 24 V class A device.

Table 126 — Test system: Dynamic — IUT as BR_Range_10K class A device

IUT node as	Class A device	[EPL-CT 69].1
Initial state	**Operational conditions:**	
	$V_{BATTERY}$	9,2 V
	V_{BS1}	0,03 × $V_{BATTERY}$
	V_{D1}	0,4 V
	V_{GND1}	0,1 × $V_{BATTERY}$
	V_{BS2}	[0,5 × sin(2 × π × 5 × t) + 0,5] × 0,1 × $V_{BATTERY}$ 5 Hz sinus signal with offset
	V_{D2}	1 V
	V_{GND2}	0,03 × $V_{BATTERY}$
	C2	20 pF (including input capacitance of oscilloscope)
	R2	2,4 kΩ (0,1 %): Only for open drain transceiver assembled
Test steps	A signal at 5,208 kHz is set on TXD1. The test shall be done with R1 = 1 kΩ (0,1 %) and C1 = 1 nF (1 %). The test shall be repeated with R1 = 500 Ω (0,1 %) and C1 = 10 nF (1 %).	
Response	The duty cycle measured at RXD2 shall be in the range of 0,375 to 0,601 (D3 – 2 µs to D4 + 2 µs).	
Reference	ISO 17987-4:2016, Table 15, Param 67 ISO 17987-4:2016, Table 18, Param 74, 75	

7.2.8.11 [EPL-CT 70] GND shift test — Dynamic — IUT as a class B ECU

Table 127 defines the test system "IUT as a BR_Range_20K 24 V class B device ECU".

Table 127 — Test system: Dynamic — IUT for a BR_Range_20K 24 V LIN ECU

IUT node as	Class B device as master or slave	[EPL-CT 70].1
Initial state	**Operational conditions:**	
	$V_{BATTERY}$	18,4 V
	V_{BS1}	0,1 × $V_{BATTERY}$
	V_{GND1}	0,03 × $V_{BATTERY}$
	V_{BS2}	0,03 × $V_{BATTERY}$
	V_{D1}	1 V (use 0 V if D_{Rev_Batt} is implemented)
	V_{D2}	0,4 V (use 0 V if D_{Rev_Batt} is implemented)
	V_{GND2}	[0,5 × sin(2 × π × 5 × t) + 0,5] × 0,1 × $V_{BATTERY}$ 5 Hz sinus signal with offset
	C2	20 pF (including input capacitance of oscilloscope)
	R2	2,4 kΩ (0,1 %): Only for open drain transceiver assembled
Test steps	A signal at 10 kHz is set on TXD1. The test shall be done with R1 = 1 kΩ (0,1 %) and C1 = 1 nF (1 %). The test shall be repeated with R1 = 500 Ω (0,1 %) and C1 = 10 nF (1 %).	
Response	The duty cycle measured at RXD2 shall be in the range of 0,310 to 0,662 (D1 – 2 µs to D2 + 2 µs).	
Reference	ISO 17987-4:2016, Table 15, Param 68 ISO 17987-4:2016, Table 17, Param 72, 73	

7.2.8.12 [EPL-CT 71] GND shift test — Dynamic — IUT as a class B ECU

Table 128 defines the test system "IUT as BR_Range_10K 24 V class B device ECU".

Table 128 — Test system: Dynamic — IUT for as a BR_Range_10K class B ECU

IUT node as	Class B device as master or slave	[EPL-CT 71].1
Initial state	**Operational conditions:**	
	$V_{BATTERY}$	9,2 V
	V_{BS1}	0,1 × $V_{BATTERY}$
	V_{GND1}	0,03 × $V_{BATTERY}$
	V_{BS2}	0,03 × $V_{BATTERY}$
	V_{D1}	1 V (use 0 V if D_{Rev_Batt} is implemented)
	V_{D2}	0,4 V (use 0 V if D_{Rev_Batt} is implemented)
	V_{GND2}	[0,5 × sin(2 × π × 5 × t) + 0,5] × 0,1 × $V_{BATTERY}$ 5 Hz sinus signal with offset
	C2	20 pF (including input capacitance of oscilloscope)
	R2	2,4 kΩ (0,1 %): Only for open drain transceiver assembled
Test steps	A signal at 5,208 kHz is set on TXD1. The test shall be done with R1 = 1 kΩ (0,1 %) and C1 = 1 nF (1 %). The test shall be repeated with R1 = 500 Ω (0,1 %) and C1 = 10 nF (1 %).	
Response	The duty cycle measured at RXD2 shall be in the range of 0,375 to 0,601 (D3 – 2 µs to D4 + 2 µs).	
Reference	ISO 17987-4:2016, Table 15, Param 68 ISO 17987-4:2016, Table 18, Param 74, 75	

7.2.8.13 [EPL-CT 72] GND shift test — Dynamic — IUT as a class B ECU

Table 129 defines the test system "Dynamic — IUT as BR_Range_20K 24 V class B device ECU".

Table 129 — Test system: Dynamic — IUT as a BR_Range_20K ECU

IUT node as	Class B device as master or slave	[EPL–CT 72].1
Initial state	**Operational conditions:**	
	$V_{BATTERY}$	18,4 V
	V_{BS1}	0,03 × $V_{BATTERY}$
	V_{D1}	0,4 V (use 0 V if D_{Rev_Batt} is implemented)
	V_{D2}	1 V (use 0 V if D_{Rev_Batt} is implemented)
	V_{GND1}	[0,5 × sin(2 × π × 5 × t) + 0,5] × 0,1 × $V_{BATTERY}$ 5 Hz sinus signal with offset
	V_{BS2}	0,1 × $V_{BATTERY}$
	V_{GND2}	0,03 × $V_{BATTERY}$
	C2	20 pF (including input capacitance of oscilloscope)
	R2	2,4 kΩ (0,1 %): Only for open drain transceiver assembled
Test steps	A signal at 10 kHz is set on TXD1. The test shall be done with R1 = 1 kΩ (0,1 %) and C1 = 1 nF (1 %). The test shall be repeated with R1 = 500 Ω (0,1 %) and C1 = 10 nF (1 %).	
Response	The duty cycle measured at RXD2 shall be in the range of 0,310 to 0,662 (D1 – 2 µs to D2 + 2 µs).	
Reference	ISO 17987-4:2016, Table 15, Param 68 ISO 17987-4:2016, Table 17, Param 72, 73	

7.2.8.14 [EPL–CT 73] GND shift test — Dynamic — IUT as a class B ECU

Table 130 defines the test system "Dynamic — IUT as BR_Range_10K 24 V class B device ECU".

Table 130 — Test system: Dynamic — IUT as a BR_Range_10K ECU

IUT node as	Class B device as master or slave	[EPL-CT 73].1
Initial state	**Operational conditions:**	
	$V_{BATTERY}$	9,2 V
	V_{BS1}	0,03 × $V_{BATTERY}$
	V_{D1}	0,4 V (use 0 V if D_{Rev_Batt} is implemented)
	V_{D2}	1 V (use 0 V if D_{Rev_Batt} is implemented)
	V_{GND1}	[0,5 × sin(2 × π × 5 × t) + 0,5] × 0,1 × $V_{BATTERY}$ 5 Hz sinus signal with offset
	V_{BS2}	0,1 × $V_{BATTERY}$
	V_{GND2}	0,03 × $V_{BATTERY}$
	C2	20 pF (including input capacitance of oscilloscope)
	R2	2,4 kΩ (0,1 %): Only for open drain transceiver assembled
Test steps	A signal at 5,208 kHz is set on TXD1. The test shall be done with R1 = 1 kΩ (0,1 %) and C1 = 1 nF (1 %). The test shall be repeated with R1 = 500 Ω (0,1 %) and C1 = 10 nF (1 %).	
Response	The duty cycle measured at RXD2 shall be in the range of 0,375 to 0,601 (D3 - 2 µs to D4 + 2 µs).	
Reference	ISO 17987-4:2016, Table 15, Param 68 ISO 17987-4:2016, Table 17, Param 72, 73	

7.2.8.15 [EPL-CT 74] V_{BAT} shift test — Dynamic — IUT as a class B ECU

Table 131 defines the test system "Dynamic — IUT as a BR_Range_20K 24 V class B LIN ECU".

Table 131 — Test system: Dynamic — IUT as a BR_Range_20K 24 V LIN ECU

IUT node as	Class B device as master or slave	[EPL–CT 74].1
Initial state	**Operational conditions:**	
	$V_{BATTERY}$	18,4 V
	V_{BS1}	$[0,5 \times \sin(2 \times \pi \times 5 \times t) + 0,5] \times 0,1 \times V_{BATTERY}$ 5 Hz sinus signal with offset
	V_{D1}	1 V (use 0 V if D_{Rev_Batt} is implemented)
	V_{D2}	0,4 V (use 0 V if D_{Rev_Batt} is implemented)
	V_{GND1}	$0,03 \times V_{BATTERY}$
	V_{BS2}	$0,03 \times V_{BATTERY}$
	V_{GND2}	$0,1 \times V_{BATTERY}$
	C2	20 pF (including input capacitance of oscilloscope)
	R2	2,4 kΩ (0,1 %): Only for open drain transceiver assembled
Test steps	A signal at 10 kHz is set on TXD1. The test shall be done with R1 = 1 kΩ (0,1 %) and C1 = 1 nF (1 %). The test shall be repeated with R1 = 500 Ω (0,1 %) and C1 = 10 nF (1 %).	
Response	The duty cycle measured at RXD2 shall be in the range of 0,310 to 0,662 (D1 – 2 µs to D2 + 2 µs).	
Reference	ISO 17987–4:2016, Table 15, Param 67 ISO 17987–4:2016, Table 17, Param 72, 73	

7.2.8.16 [EPL–CT 75] V_{BAT} shift test — Dynamic — IUT as a class B ECU

Table 132 defines the test system "Dynamic — IUT as a BR_Range_10K 24 V class B LIN ECU".

Table 132 — Test system: Dynamic — IUT as a BR_Range_10K ECU

IUT node as	Class B device as master or slave	[EPL–CT 75].1
Initial state	**Operational conditions:**	
	$V_{BATTERY}$	9,2 V
	V_{BS1}	$[0,5 \times \sin(2 \times \pi \times 5 \times t) + 0,5] \times 0,1 \times V_{BATTERY}$ 5 Hz sinus signal with offset
	V_{D1}	1 V (use 0 V if D_{Rev_Batt} is implemented)
	V_{D2}	0,4 V (use 0 V if D_{Rev_Batt} is implemented)
	V_{GND1}	$0,03 \times V_{BATTERY}$
	V_{BS2}	$0,03 \times V_{BATTERY}$
	V_{GND2}	$0,1 \times V_{BATTERY}$
	C2	20 pF (including input capacitance of oscilloscope)
	R2	2,4 kΩ (0,1 %): Only for open drain transceiver assembled
Test steps	A signal at 5,208 kHz is set on TXD1. The test shall be done with R1 = 1 kΩ (0,1 %) and C1 = 1 nF (1 %). The test shall be repeated with R1 = 500 Ω (0,1 %) and C1 = 10 nF (1 %).	
Response	The duty cycle measured at RXD2 shall be in the range of 0,375 to 0,601 (D3 – 2 µs to D4 + 2 µs).	
Reference	ISO 17987–4:2016, Table 15, Param 67 ISO 17987–4:2016, Table 18, Param 74, 75	

7.2.8.17 [EPL–CT 76] V_{BAT} shift test — Dynamic — IUT as a class B ECU

Table 133 defines the test system "Dynamic — IUT as a BR_Range_20K 24 V class B LIN ECU".

Table 133 — Test system: Dynamic — IUT as BR_Range_20K ECU

IUT node as	Class B device as master or slave	[EPL-CT 76].1
Initial state	**Operational conditions:**	
	$V_{BATTERY}$	18,4 V
	V_{BS1}	0,03 × $V_{BATTERY}$
	V_{D1}	0,4 V (use 0 V if D_{Rev_Batt} is implemented)
	V_{D2}	1 V (use 0 V if D_{Rev_Batt} is implemented)
	V_{GND1}	0,1 × $V_{BATTERY}$
	V_{BS2}	[0,5 × sin(2 × π × 5 × t) + 0,5] × 0,1 × $V_{BATTERY}$ 5 Hz sinus signal with offset
	V_{GND2}	0,03 × $V_{BATTERY}$
	C2	20 pF (including input capacitance of oscilloscope)
	R2	2,4 kΩ (0,1 %): Only for open drain transceiver assembled
Test steps	A signal at 10 kHz is set on TXD1. The test shall be done with R1 = 1 kΩ (0,1 %) and C1 = 1 nF (1 %). The test shall be repeated with R1 = 500 Ω (0,1 %) and C1 = 10 nF (1 %).	
Response	The duty cycle measured at RXD2 shall be in the range of 0,310 to 0,662 (D1 – 2 µs to D2 + 2 µs).	
Reference	ISO 17987-4:2016, Table 15, Param 67 ISO 17987-4:2016, Table 17, Param 72, 73	

7.2.8.18 [EPL-CT 77] V_{BAT} shift test — Dynamic — IUT as a class B ECU

Table 134 defines the test system "Dynamic — IUT as a BR_Range_10K 24 V class B LIN ECU".

Table 134 — Test system: Dynamic — IUT as BR_Range_10K ECU

IUT node as	Class B device as master or slave	[EPL–CT 77].1
Initial state	**Operational conditions:**	
	$V_{BATTERY}$	9,2 V
	V_{BS1}	0,03 × $V_{BATTERY}$
	V_{D1}	0,4 V (use 0 V if D_{Rev_Batt} is implemented)
	V_{D2}	1 V (use 0 V if D_{Rev_Batt} is implemented)
	V_{GND1}	0,1 × $V_{BATTERY}$
	V_{BS2}	[0,5 × sin(2 × π × 5 × t) + 0,5] × 0,1 × $V_{BATTERY}$ 5 Hz sinus signal with offset;
	V_{GND2}	0,03 × $V_{BATTERY}$
	C2	20 pF (including input capacitance of oscilloscope)
	R2	2,4 kΩ (0,1 %): Only for open drain transceiver assembled
Test steps	A signal at 5,208 kHz is set on TXD1. The test shall be done with R1 = 1 kΩ (0,1 %) and C1 = 1 nF (1 %). The test shall be repeated with R1 = 500 Ω (0,1 %) and C1 = 10 nF (1 %).	
Response	The duty cycle measured at RXD2 shall be in the range of 0,375 to 0,601 (D3 – 2 µs to D4 + 2 µs).	
Reference	ISO 17987–4:2016, Table 15, Param 67 ISO 17987–4:2016, Table 18, Param 74, 75	

7.2.9 Failure

7.2.9.1 Purpose

The purpose of the test is to check whether some parasitic reverse currents are flowing into the IUT.

7.2.9.2 [EPL–CT 78] Loss of battery

Figure 57 shows the test configuration of the test system "Loss of battery".

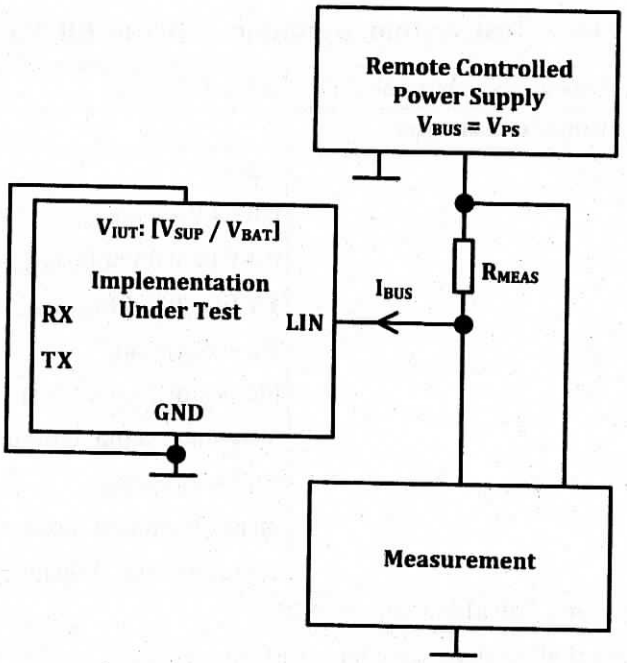

Figure 57 — Test system: Loss of battery

Table 135 defines the test system "Loss of battery.

Table 135 — Test system: Loss of battery

IUT node as	Class B device as master or slave Class A device	[EPL–CT 78].1
Initial state	**Operational conditions:**	
	V_{IUT} = GND Failure 0 < V_{BUS} < 36 V R_{MEAS}	V_{IUT}: [V_{SUP}/V_{BAT}] Loss of Battery 10 kΩ (0,1 %)
Test steps	The power supply is disconnected from the IUT V_{IUT} PIN. V_{BUS} = Signal with a 2 V/s ramp in the range (0 V to 36 V) up and down.	
Response	During all test, no parasitic current paths shall be formed between the bus line and the IUT. I_{BUS} shall be less than 100 µA, means 1 V voltage drop over R = 10 kΩ. After reconnecting battery line, the IUT shall restart after failure recovery.	
Reference	ISO 17987–4:2016, Table 15, Param 61	

7.2.9.3 [EPL–CT 79] Loss of GND

Figure 58 shows the test configuration of the test system "Loss of GND".

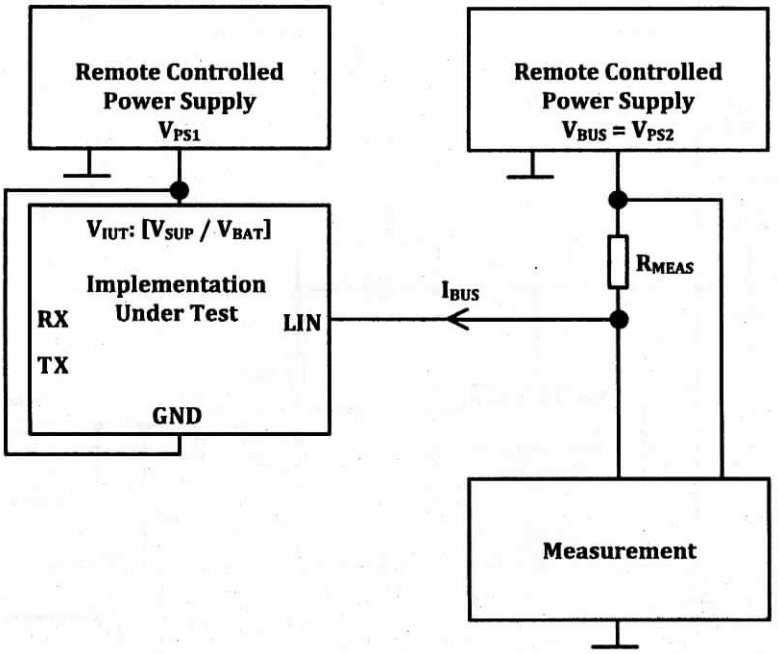

Figure 58 — Test system: Loss of GND

Table 136 defines the test system "Loss of GND".

Table 136 — Test system: Loss of GND

IUT node as	Class B device as slave Class A device	[EPL-CT 79].1
Initial state	**Operational conditions:**	
	V_{IUT}: [V_{SUP}/V_{BAT}]	$V_{IUT} = V_{PS1} = 24$ V
	$GND_{SUP}/GND_{BAT} = V_{IUT}$	Local GND shorted to V_{IUT}
	Failure	Loss of ground
	R_{MEAS}	1 kΩ (0,1 %)
Test steps	The ground is disconnected from the IUT. V_{BUS} = Signal with a 2 V/s ramp in the range (0 V to 36 V) up and down.	
Response	During all test, no parasitic current paths shall be formed between the bus line and the IUT. I_{BUS} shall be included in ±2 mA, means 2 V voltage drop over R = 1 kΩ. After reconnecting ground line, the IUT shall restart after failure recovery.	
Reference	ISO 17987-4:2016, Table 15 , Param 60	

7.2.10 [EPL-CT 80] Verifying internal capacitance and dynamic interference — IUT as slave

The purpose of this test is to check the internal capacitance of the IUT under normal and fault conditions.

The IUT shall not interfere dynamically with bus signals when it is in passive (non-transmitting) or unpowered state.

In case of a switchable internal pull-up resistor, the internal pull-up resistor shall be active.

Figure 59 shows the test configuration of the test system "Verifying internal capacitance and dynamic interference — IUT as slave".

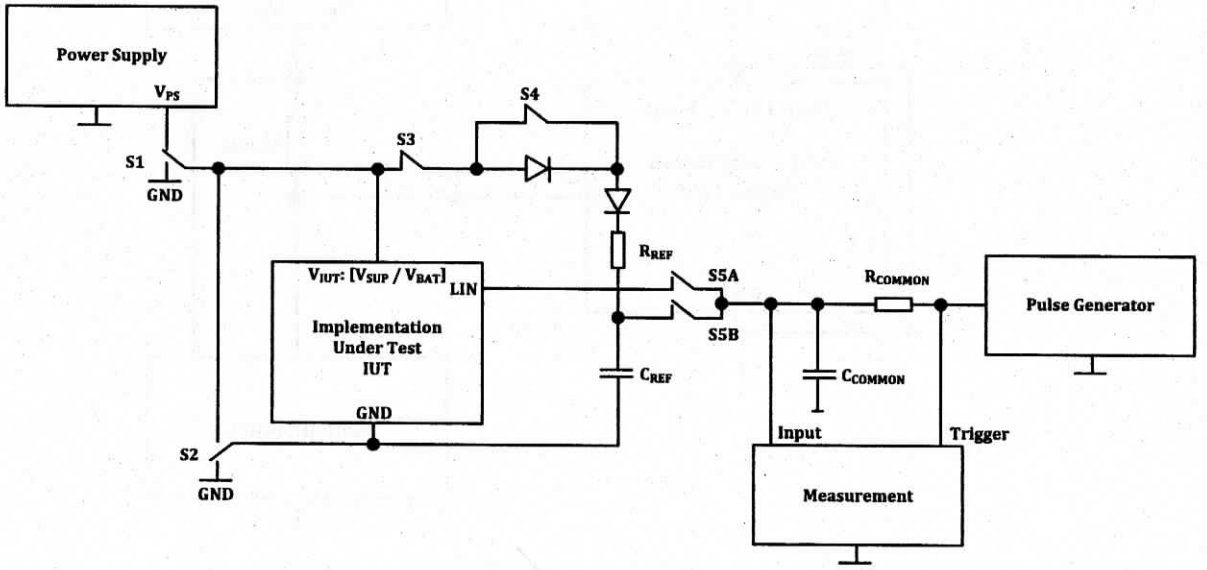

Figure 59 — Test system: Verifying internal capacitance and dynamic interference — IUT as slave

Table 137 defines the test system "Switch settings depending on IUT configuration".

Table 137 — Test system: Switch settings depending on IUT configuration

Switch	Setting
S3	Normally closed. In case where IUT has switchable and deactivated internal pull-up (e.g. in power loss conditions), open S3.
S4	Normally closed. In case where IUT is a 3-pin node or ECU, where reverse polarity protection is included in IUT, open S4.
S5A/S5B	In case where IUT is connected by a wire harness: During reference measurement, close both S5A and S5B and disconnect IUT from harness. So the harness capacitance is accounted for in the reference.

Table 138 defines the test system "Verifying internal capacitance and dynamic interference — IUT as slave".

Table 138 — Test system: Verifying internal capacitance and dynamic interference — IUT as slave

IUT node as	Class B device as slave Class A device	[EPL-CT 80].1, [EPL-CT 80].2, [EPL-CT 80].3
Initial state	**Operational conditions:**	
	V_{IUT}: [V_{SUP}/V_{BAT}]	24 V
	R_{COMMON}	1 kΩ (0,1 %)
	C_{COMMON}	750 pF (1,5 nF + 1,5 nF in series) (1 %)
	R_{REF}	30 kΩ (0,1 %)
	C_{REF}	250 pF (100 pF || 150 pF parallel) (1 %)
Test steps	The LIN Bus is driven with a 10 kHz rectangular signal with a duty cycle of 50 %. Rise time ≤40 ns. Slope time measurements are done at 10 %, 90 % of slope voltage. S5B closed: Measuring rise time T_{REF} on a known capacitance of 250 pF + 750 pF. S5A closed: Measuring rise time T_{int} with the IUT internal capacitance + 750 pF.	
Response	C_{SLAVE} shall be less than or equal to 250 pF: $T_{int} \leq T_{REF}$. The IUT shall not interfere with the dynamic stimulus.	
Reference	ISO 17987-4:2016, Table 20, Param 37 and ISO 17987-4:2016, 5.3.9.2.	

Table 139 defines the test cases "Verifying internal capacitance and dynamic interference — IUT as slave".

Table 139 — Test cases: Verifying internal capacitance and dynamic interference — IUT as slave

EPL-CT-TC	Condition	S1	S2
[EPL-CT 80].1	Normal power supply IUT shall be in normal mode.	V_{PS}	GND
[EPL-CT 80].2	IUT loss of GND (IUT GND shorted to power supply).	V_{PS}	V_{PS}
[EPL-CT 80].3	IUT loss of V_{PS} (IUT V_{IUT}: [V_{SUP}/V_{BAT}] shorted to GND).	GND	GND

7.3 Operation mode termination

7.3.1 General

An external resistor R_{meas} is switched to the LIN pin. To get the value of the internal resistor, current and voltage shall be measured. These values are gathered for two different settings, and the internal resistance is calculated using Formulae (1), (2), (3) and (4).

Figure 60 shows the test configuration of the test system "Operation mode".

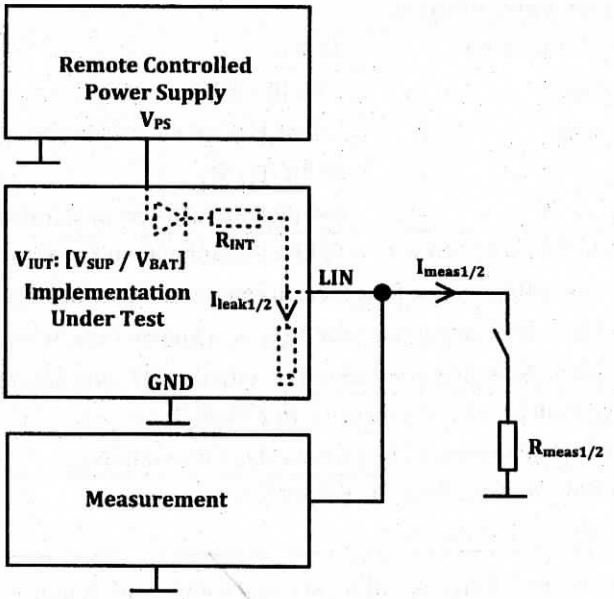

Figure 60 — Test system: Operation mode

7.3.2 [EPL-CT 81] Measuring internal resistor — IUT as slave

Table 140 defines the test system "Measuring internal resistor — IUT as slave".

Table 140 — Test system: Measuring internal resistor — IUT as slave

IUT node as	Class A device Class B device as slave	
Initial state	**Parameters:**	
	R_{meas1}	10 kΩ (0,1 %)
	R_{meas2}	20 kΩ (0,1 %)
	Operational conditions:	
	V_{IUT}: [V_{SUP}/V_{BAT}]	24 V
Test steps	The IUT shall be in operational/active mode. There is no communication on the LIN bus. If the IUT incorporates a bus dominant state timeout detection, which disables the IUT's pull-up resistor, the measurement shall take place before a timeout is detected.	
Response	R_{int} value shall be included in the range [20 kΩ; 60 kΩ]; see Formula (4).	
Reference	ISO 17987-4:2016, Table 11 , Param 26	

7.3.3 [EPL-CT 82] Measuring internal resistor — IUT as master

Table 141 defines the test system "Measuring internal resistor — IUT as master".

Table 141 — Test system: Measuring internal resistor — IUT as master

IUT node as	Class B device as master	
Initial state	**Parameters:**	
	R_{meas1}	1 kΩ (0,1 %)
	R_{meas2}	2 kΩ (0,1 %)
	Operational conditions:	
	V_{IUT}: [V_{SUP}/V_{BAT}]	24 V
Test steps	The IUT shall be in operational/active mode. There is no communication on the LIN bus. If the IUT incorporates a bus dominant state timeout detection, which disables the IUT's pull-up resistor, the measurement shall take place before a timeout is detected.	
Response	R_{int} value shall be included in the range [900 Ω; 1 100 kΩ]; see Formula (4). R_{meas1} = 1 kΩ (0,1 %); R_{meas2} = 2 kΩ (0,1 %).	
Reference	ISO 17987-4, Table 11 , Param 25	

7.4 Static test cases

Static test cases aim to check the availability and the boundaries in the datasheet of the IUT. For all integrated circuits, every related parameter in Table 142 shall be part of the datasheet and fulfil the specified boundaries in terms of physical worst-case condition. Datasheet parameter names may deviate from the names in Table 142, but in this case, a cross-reference list (datasheet versus Table 142) shall be provided for this test. Parameter conditions may deviate from the conditions in Table 142, if the datasheet conditions are according to the physical worst case context in Table 142 at least.

If one parameter does not pass this test, the result of the whole conformance test is "Failed". See ISO 17987-4:—, 5.3.6, 5.3.5.1 and 5.3.5.2.

Table 142 defines the test system "LIN static test parameters for datasheets of integrated circuits".

Table 142 — Test system: LIN static test parameters for datasheets of integrated circuits

No	Reference	Parameter	Min.	Max.	Unit	Comment/ condition	Valid for	Conformance test is passed if value is	
								≤	≥
1.	Param 52	$V_{BAT\_BR\_Range\_20K}$[a]	16,0	36,0	V	ECU operating voltage range	All devices with integrated reverse polarity diode	Min.	Max.
2.	Param 53	$V_{SUP\_BR\_Range\_20K}$[b]	15,0	36,0	V	Supply voltage range	All devices without integrated reverse polarity diode	Min.	Max.
3.	Param 54	$V_{BAT\_BR\_Range\_10K}$[a]	8,0	36,0	V	ECU operating voltage range	All devices with integrated reverse polarity diode	Min.	Max.
4.	Param 55	$V_{SUP\_BR\_Range\_10K}$[b]	7,0	36,0	V	Supply voltage range	All devices without integrated reverse polarity diode	Min.	Max.

Table 142 *(continued)*

No	Reference	Parameter	Min.	Max.	Unit	Comment/ condition	Valid for	Conformance test is passed if value is	
								≤	≥
5.	Param 56	$V_{SUP\_NON\_OP}$	−0,3	58,0	V	Voltage range within which the device is not destroyed. An optional time limit for the maximum value shall be at least 350 ms. No guarantee of correct operation.	All devices	Min.	Max.
6.	Param 57	I_{BUS_LIM}[c]	75	300	mA	Current Limitation for Driver dominant state driver on $V_{BUS} = V_{BAT\_max}$[d]	All devices with integrated LIN transmitter	Min.	Max.
5.	Param 58	$I_{BUS\_PAS\_dom}$	−1	—	mA	Input leakage current at the receiver incl. slave pull-up resistor as specified in Param 71 driver off $V_{BUS} = 0$ V $V_{BAT} = 24$ V	all devices with integrated slave pull-up resistor	—	Min.
6.	Param 59	$I_{BUS\_PAS\_rec}$	—	20	µA	Driver off 8 V < V_{BAT} < 36 V 8 V < V_{BUS} < 36 V $V_{BUS} > V_{BAT}$	All devices	Max.	—
7.	Param 60	$I_{BUS\_NO\_GND}$	−2	2	mA	Control unit disconnected from ground $GND_{Device} = V_{SUP}$ 0 V < V_{BUS} < 36 V $V_{BAT} = 24$ V Loss of local ground shall not affect communication in the residual network.	All devices	Max.	Min.
8.	Param 61	$I_{BUS\_NO\_BAT}$	—	100	µA	V_{BAT} disconnected V_{SUP} = GND 0 V < V_{BUS} < 36 V Node shall sustain the current that can flow under this condition. Bus shall remain operational under this condition.	All devices	Max.	—
9.	Param 62	V_{BUS_dom}	—	0,4	V_{SUP}	Receiver dominant state	All devices with integrated LIN receiver	—	Max.
10.	Param 63	V_{BUS_rec}	0,6	—	V_{SUP}	Receiver recessive state	All devices with integrated LIN receiver	Min.	—
11.	Param 64	V_{BUS_CNT}	0,475	0,525	V_{SUP}	$V_{BUS\_CNT} = (V_{th\_dom} + V_{th\_rec})/2$[e]	All devices with integrated LIN receiver	Max.	Min.

Table 142 *(continued)*

No	Reference	Parameter	Min.	Max.	Unit	Comment/ condition	Valid for	Conformance test is passed if value is	
								≤	≥
12.	Param 65	V_{HYS}	—	0,175	V_{SUP}	$V_{HYS} = V_{th\_rec} - V_{th\_dom}$	All devices with integrated LIN receiver	Max.	—
13.	Param 72	D1 (Duty Cycle 1)	0,330	—	—	$TH_{Rec(max)} = 0{,}710 \times V_{SUP}$; $TH_{Dom(max)} = 0{,}554 \times V_{SUP}$; V_{SUP} = 15,0 V to 36 V; t_{BIT} = 50 µs; $D1 = t_{Bus\_rec(min)}/(2 \times t_{BIT})$	All devices with integrated LIN transmitter D1 valid for 20 kbit/s	—	Min.
14.	Param 73	D2 (Duty Cycle 2)	—	0,642	—	$TH_{Rec(min)} = 0{,}446 \times V_{SUP}$; $TH_{Dom(min)} = 0{,}302 \times V_{SUP}$; V_{SUP} = 15,6 V to 36 V; t_{BIT} = 50 µs; $D2 = t_{Bus\_rec(max)}/(2 \times t_{BIT})$	All devices with integrated LIN transmitter D2 valid for 20 kbit/s	Max.	—
15.	Param 74	D3 (Duty Cycle 3)	0,386	—	—	$TH_{Rec(max)} = 0{,}744 \times V_{SUP}$; $TH_{Dom(max)} = 0{,}581 \times V_{SUP}$; V_{SUP} = 7,0 V to 36 V; t_{BIT} = 96 µs; $D3 = t_{Bus\_rec(min)}/(2 \times t_{BIT})$	All devices with integrated LIN transmitter D3 valid for 10,417 kbit/s	—	Min.
16.	Param 75	D4 (Duty Cycle 4)	—	0,591	—	$TH_{Rec(min)} = 0{,}422 \times V_{SUP}$; $TH_{Dom(min)} = 0{,}284 \times V_{SUP}$; V_{SUP} = 7,6 V to 36 V; t_{BIT} = 96 µs; $D4 = t_{Bus\_rec(max)}/(2 \times t_{BIT})$	All devices with integrated LIN transmitter D4 valid for 10,417 kbit/s	Max.	—
17.	Param 76	t_{rx_pd}	—	6	µs	Propagation delay of receiver	All devices with integrated LIN receiver	Max.	—
18.	Param 77	t_{rx_sym}	−2	2	µs	Symmetry of receiver propagation delay rising edge with respect to falling edge	All devices with integrated LIN receiver	Max.	Min.
19.	Param 71	R_{SLAVE}	20	60	kΩ	—	All devices with integrated slave pull-up resistor	Max.	Min.
20.	Param 70	R_{MASTER}	900	1 100	Ω	The serial diode is mandatory. Only valid for transceiver with integrated master pull-up resistor	All devices with integrated master pull-up resistor	Max.	Min.

Table 142 *(continued)*

No	Reference	Parameter	Min.	Max.	Unit	Comment/ condition	Valid for	Conformance test is passed if value is	
								≤	≥
21.	Param 37	C_{SLAVE}	—	250	pF	Capacitance of slave node	All LIN slave devices	Max.	—
22.	6.3.7.1	LIN device states changes	—	—	—	All LIN device state changes on conditional events (e.g. temperature shutdown) shall be specified in the LIN device datasheet.	All devices	—	—
23.	—	LIN transceiver input capacitance	—	—	—	A maximum LIN transceiver input capacitance shall be specified in the LIN device datasheet. Please consider the datasheet limits (e.g. voltage, temperature). The value should be as low as possible.	All devices	—	—

[a] V_{BAT} denotes the supply voltage at the connector of the control unit and may be different from the internal supply V_{SUP} for electronic components (see ISO 17987-4:2016, 5.3.2).

[b] V_{SUP} denotes the supply voltage at the transceiver inside the control unit and may be different from the external supply V_{BAT} for control units (see ISO 17987-4:2016, 5.3.2).

[c] I_{BUS}: Current flowing into the node.

[d] A transceiver shall be capable to sink at least 40 mA. The maximum current flowing into the node shall not exceed 200 mA under DC conditions to avoid possible damage.

[e] V_{th_dom}: Receiver threshold of the recessive to dominant LIN bus edge. V_{th_rec}: receiver threshold of the dominant to recessive LIN bus edge.

8 EPL 24 V LIN devices without RX and TX access

This clause addresses class C devices.

8.1 Test specification overview

This test specification is intended for LIN conformance tests of the electrical physical layer of ECUs (see ISO 17987-4) with inaccessible TX and RX pin. This may be the case for integrated devices.

Lacking access to the TX pin, the IUT is stimulated to transmit LIN frames to the bus to test the transmit functions of the device. The LIN frames transmitted by the IUT can then be evaluated by the test system.

Lacking access to the RX pin, the reception of the IUT is tested by establishing a communication between the test system and the IUT.

8.2 Communication scheme

8.2.1 Overview

Depending on the IUT type (class C as master/slave), several different communication schemes are used for conformance testing; see 8.2.2 to 8.2.4.

8.2.2 IUT as slave

The following (mandatory) test frames named in concordance with ISO 17987-3 are used for slave tests.

Table 143 defines the test frames used for slave tests.

Table 143 — Test frames used for slave tests

Test Frame	Requirements for the test frame
TST_FRM_RDBI_0	ReadByIdentifier (Identifier = 0). All other parameters shall be filled with default values according to the IUT specification and according to the test case specification.
TST_HDR_SR_3D	Slave response header, Identifier = $3D_{16}$.

The test system as master, cyclically transmits a TST_FRM_RDBI_0 followed by TST_HDR_SR_3D with a maximum supported bit rate unless defined otherwise by the test case.

One TST_FRM_RDBI_0 followed by a TST_HDR_SR_3D is referred to as one communication cycle. A communication cycle is considered successful if the IUT as slave responds correctly to TST_HDR_SR_3D (with positive or negative response, depending on TST_FRM_RDBI_0).

8.2.3 IUT as master

If possible, a test application is installed on the IUT as master. The test application shall support the following test scheme:

— Bit rate: Maximum bit rate supported by master application, unless specified otherwise by test case;

— Checksum model: Enhanced checksum.

The communication between the test system and the IUT shall be implemented as follows:

1) Counter = 0;
2) IUT as master: Transmit a frame header (ID 01_{16}), followed by response of one data byte (counter [00]) and checksum;
3) Test system as slave: If frame is received without errors, store received counter and set transmit flag;
4) IUT as master: Transmit frame header (ID 02_{16});
5) Test system as slave: If transmit flag is set, respond with one data byte (stored counter [00]) and check sum, and clear transmit flag;
6) IUT as master: If test system has answered without errors and received counter value == transmitted counter value, increment counter by 1;
7) Goto step 2);

One sequence of steps 2) to 7) is referred to as one communication cycle. A communication cycle is considered successful, if the counter is incremented in step 6), verified by test system in consecutive communication cycle.

There shall be a possibility to deactivate transmission of LIN headers by the IUT (e.g. by setting an input pin), so that the LIN bus remains recessive.

If bit rates of both higher than10,417 kbit/s and lower than or equal to 10,417 kbit/s are supported by the application, there shall be a possibility to select between maximum bit rate and 10,417 kbit/s or lower (e.g. by setting an input pin).

If no test software may be installed on the IUT as master (e.g. integrated device), a device-specific communication scheme is used which allows verification if the IUT as master correctly receives responses from the test system.

8.2.4 IUT Class C device

8.2.4.1 General

For class C devices (e.g. microcontrollers with integrated transceiver or SBCs with integrated UART and transceiver), a test application is required.

The type of test application depends on the type of integrated device.

8.2.4.2 IUT Class C device as slave

This device type only supports slave applications.

For conformance testing, the IUT class C device as slave is supplied with a test application which shall support the following test scheme:

— Application can adapt to all bit rates supported by the device;

— Checksum model: Enhanced checksum.

The communication between the test system and the IUT shall be implemented as follows:

1) Counter = 0;

2) Test System as master: Transmit a frame header (ID 01_{16}), followed by response of one data byte (counter [00]) and checksum;

3) IUT as slave: If frame is received without errors, store received counter and set transmit flag;

4) Test System as master: Transmit frame header (ID 02_{16});

5) IUT as slave: If transmit flag is set, respond with one data byte (stored counter [00]) and check sum, and clear transmit flag;

6) Test System as master: If IUT as slave has answered without errors and received counter value == transmitted counter value, increment counter by 1;

7) Goto step 2);

One sequence of steps 2) to 7) is referred to as one communication cycle. A communication cycle is considered successful, if the counter is incremented in step 6).

8.2.4.3 IUT class C device as master

This device type only supports master applications.

If the IUT does not have an integrated master pull-up resistor, it shall be equipped with an external pull-up circuitry as specified in the IUT's datasheet. If the IUT's datasheet does not specify a pull-up circuitry, the circuitry as described in Figure 61 is used.

Figure 61 shows the default master pull-up circuitry.

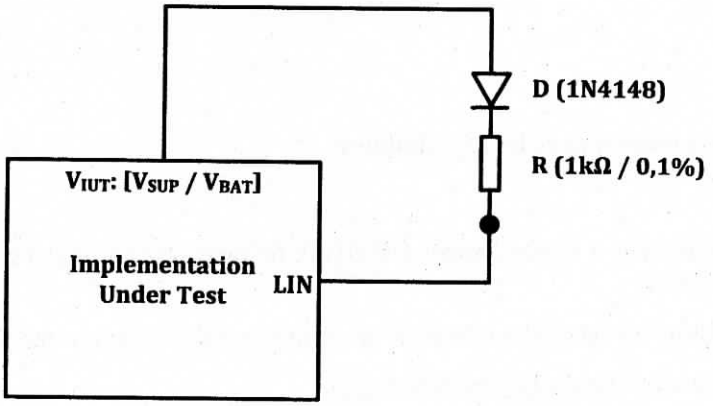

Figure 61 — Default master pull-up circuitry

For conformance testing, the IUT class C device as master is supplied with a test application which shall support the following test scheme:

— Bit rate: maximum supported bit rate, unless specified otherwise by test case;

— Checksum model: Enhanced checksum.

The communication between the test system and the IUT shall be implemented as follows:

1) Counter = 0;

2) IUT as master: Transmit a frame header (ID 01_{16}), followed by response of one data byte (counter [00]) and checksum;

3) Test System as slave: If frame is received without errors, store received counter and set transmit flag;

4) IUT as master: Transmit frame header (ID 02_{16});

5) Test System as slave: If transmit flag is set, respond with one data byte (stored counter [00]) and check sum, and clear transmit flag;

6) IUT as master: If test system as slave has answered without errors and received counter value == transmitted counter value, increment counter by 1;

7) Goto step 2);

One sequence of steps 2) to 7) is referred to as one communication cycle. A communication cycle is considered successful, if the counter is incremented in step 6), verified by the test system in consecutive communication cycle.

There shall be a possibility to deactivate transmission of LIN headers by the IUT (e.g. by setting a port pin) so that the LIN bus remains recessive.

If bit rates of both higher than10,417 kbit/s and lower than or equal to 10,417 kbit/s are supported by the device, there shall be a possibility to select between maximum bit rate and 10,417 kbit/s or lower (e.g. by setting a port pin).

8.2.4.4 IUT class C device as master or slave for devices supporting both master and slave applications (two IUTs are needed)

One IUT is provided with a slave application as described in 8.2.4.2, one IUT is provided with a master application and, if required, external master pull-up circuitry as described in 8.2.4.3. During GND shift and V_{BAT} shift tests, communication is established between these two IUTs.

The communication scheme then looks as follows:

1) Counter = 0;
2) Master IUT: Transmit a frame header (ID 01_{16}), followed by response of one data byte (counter [00]) and checksum;
3) Slave IUT: If frame is received without errors, store received counter and set transmit flag;
4) Master IUT: Transmit frame header (ID 02_{16});
5) Slave IUT: If transmit flag is set, respond with one data byte (stored counter [00]) and check sum, and clear transmit flag;
6) Master IUT: If slave IUT has answered without errors and received counter value == transmitted counter value, increment counter by 1;
7) Goto step 2);

One sequence of steps 2) to 7) is referred to as one communication cycle. A communication cycle is considered successful, if the counter is incremented in step 6), verified by the test system in consecutive communication cycle.

If the selection of master/slave application does not affect the physical layer of the device (e.g. switch internal pull-up resistor), the IUT provided with the slave application is used for all remaining test cases and is regarded as IUT class C device as slave.

If the selection of master/slave application does affect the physical layer of the device, the IUTs shall be tested both as IUT class C device as slave and IUT class C device as master for test cases where test parameters differ for master and slave.

8.3 Test case organization

The intention of each test case is described at first, with a short textual explanation.

Before tests are executed, the test system shall be set to its initial state as described in 8.5.

The test procedure and the expected results are described in the form of a chart for each test case. Table 144 defines a typical test description.

Table 144 — Typical test description

IUT node as	Class A/B/C device as master or slave or both	Corresponding test number TC x, TC y, where x, y are the test case number.
Initial state	**Parameters:**	
	Number of nodes	Number of node in the test implementation
	Bus loads	In order to simulate a LIN network
	Operational conditions:	
	IUT Mode	Operation Mode for the IUT (e.g. normal mode, low power mode, ...)
	V_{BAT},V_{SUP},V_{IUT}	Value in volt
	Failure	In order to set failure at
	GND Shift	Value in volt
Test steps	Describe the test stages.	
Response	Describe the result expected in order to decide if the test passed or failed.	
Reference	Corresponding number in ISO 17987-4.	

NOTE IUT may be a class C device as master or slave ECU.

Depending on the type of IUT, the supply voltage is V_{BAT} for class C device or V_{SUP} for class A, called V_{IUT} in this description.

8.4 Measurement and signal generation — Requirements

8.4.1 Data generation

The test system shall be able to transmit LIN frames with adjustable recessive/dominant levels. For example, with the test system acting as master and the IUT as slave responding to LIN headers sent by the test system.

Figure 62 shows the LIN header sent by test system as master with dominant voltage (V_{Dom_TS}) adjusted and IUT as slave answering with nominal dominant voltage (V_{Dom_IUT}).

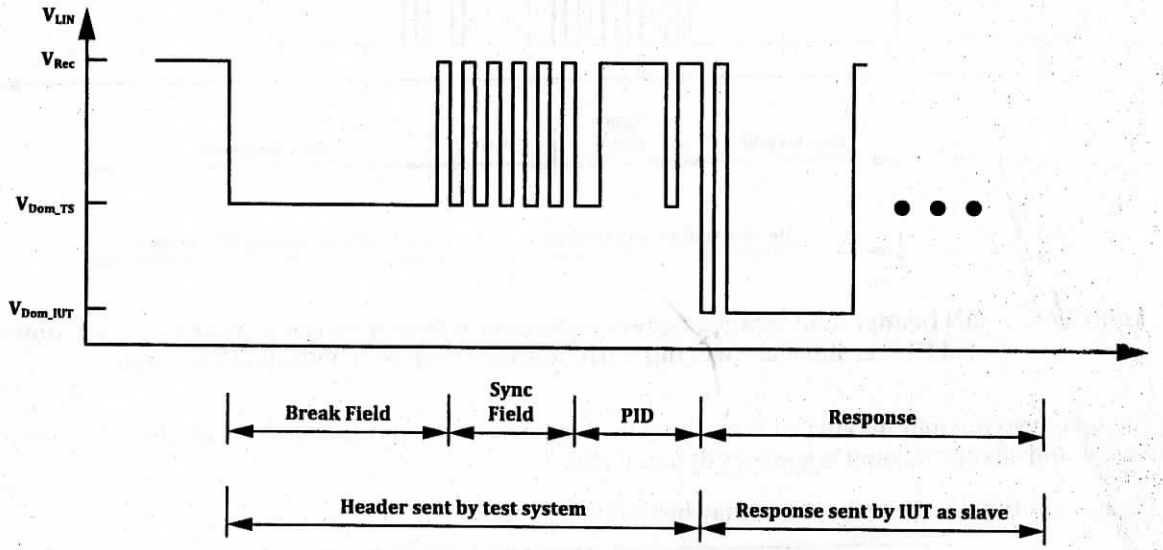

Figure 62 — LIN header sent by test system as master with dominant voltage (V_{Dom_TS}) adjusted and IUT as slave answering with nominal dominant voltage (V_{Dom_IUT})

Figure 63 shows the LIN header sent by test system as master with recessive voltage (V_{Rec_TS}) adjusted and IUT as slave answering with nominal recessive voltage (V_{Rec_IUT}).

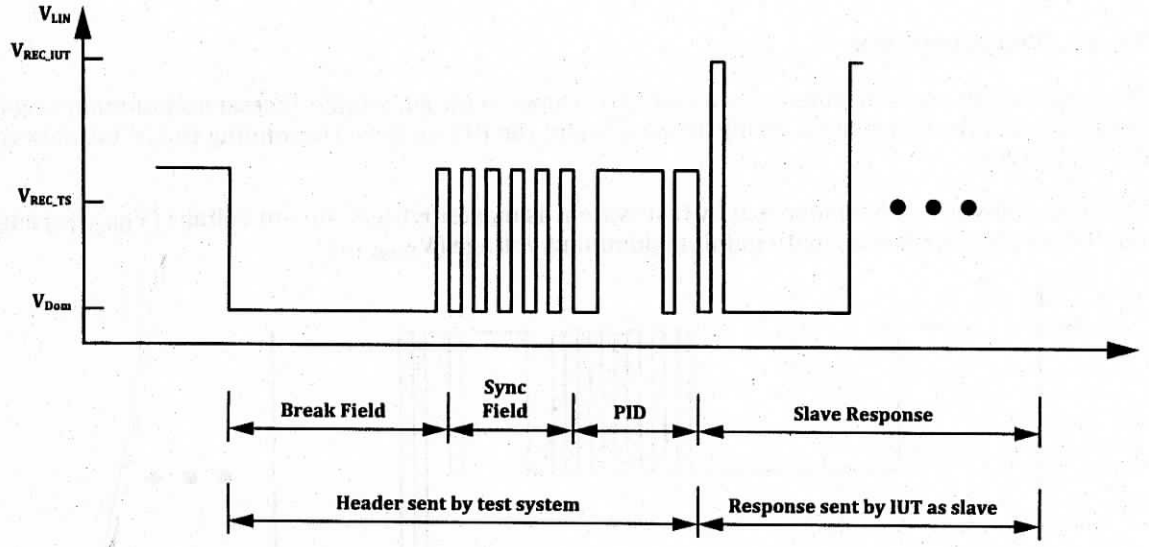

Figure 63 — LIN header sent by test system as master with recessive voltage (V_{Rec_TS}) adjusted and IUT as slave answering with nominal recessive voltage (V_{Rec_IUT})

The test system shall be able to transmit LIN headers and responses. It shall be able to receive LIN frames and change its own responses dynamically.

Data generation by the test system may be realized as shown in Figure 64

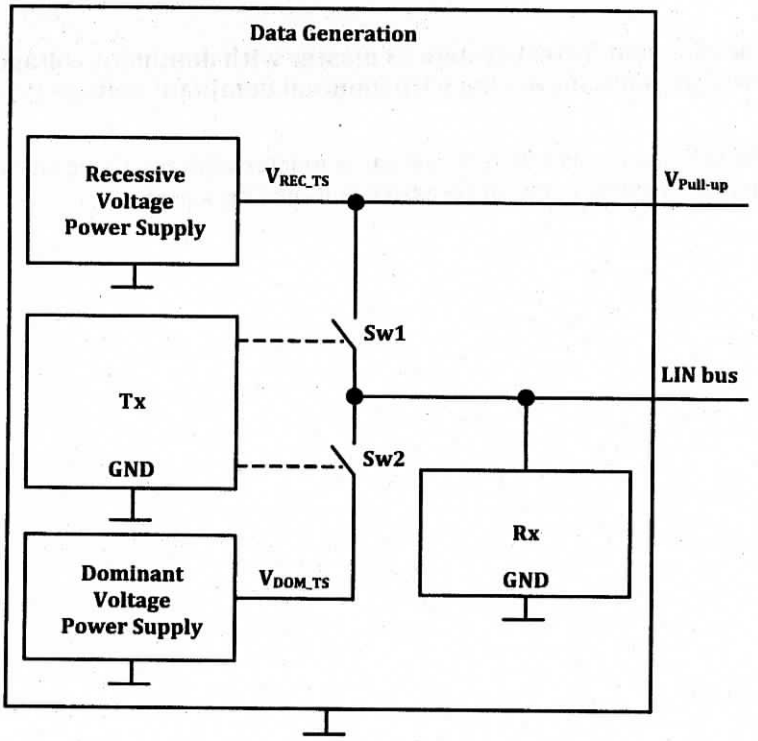

Figure 64 — Data generation

Data generation includes two power supplies that provide the recessive and dominant voltage (V_{Rec_TS} and V_{Dom_TS}) for LIN frames transmitted by data generation. Data generation shall be able to transmit recessive bits by connecting the LIN bus to its recessive voltage power supply using a low-impedance

path (Sw1) so the transmitted recessive level will not get corrupted by the IUT's internal pull-up resistor if $V_{IUT} > V_{LIN\_bus}$. The internal recessive voltage V_{Rec_TS} is provided to the test setup as $V_{Pull\text{-}up}$ to supply a pull-up resistor if necessary.

V_{Dom_TS} and $V_{Rec\_TS}/V_{Pull\text{-}up}$ is specified in the test cases where data generation is used.

8.4.2 Various requirements

Table 145 defines the data generation, signal measurement and power supply requirements.

Table 145 — Data generation, signal measurement and power supply requirements

Data generation	**Resolution**		**10 mV**
	Accuracy		0,2 % of value
	Rise/Fall Time		<40 ns
	Bit timing precision		20 ppm
	Internal resistance		<1 Ω
	Bit timing for BR_ Range_20K 24 V LIN systems		20 kbit/s t_{Bit} = 50 µs
	Bit timing for BR_ Range_10K 24 V LIN systems		10,417 kbit/s t_{Bit} = 96 µs
Signal measurement	**Dynamic signals**		**Oscilloscope 100 MHz**
			Rise time ≤3,5 ns
	Static signals:	DC voltage	0,5 %
		DC current	0,6 %
		Resistance	0,5 %
Power supply	**Resolution**		**10 mV/1 mA**
(V_{CC}, V_{IUT}, V_{LIN})	Accuracy		0,2 % of value

8.5 Operational conditions — Calibration

8.5.1 Electrical input/output, LIN protocol

The initial configuration for each test case is defined in Table 146. Any requirements for individual tests are specified in each test case.

Table 146 — Initial state of electrical input/output

Parameters	—
Number of nodes	1
Bus loads	—
Operational conditions	—
IUT mode	Set to normal/active mode
V_{BAT}, V_{SUP}, V_{IUT}, V_{PS}	Specified for each test
Failure	No failure
GND shift	0 V

8.5.2 [EPL–CT 83] Operating voltage range

This test shall ensure the correct operation in the valid supply voltage ranges, by correct reception of dominant bits. The IUT is therefore supplied with an increasing/decreasing voltage ramp.

Figure 65 shows the test configuration of the test system "Operating voltage range without RX and TX access".

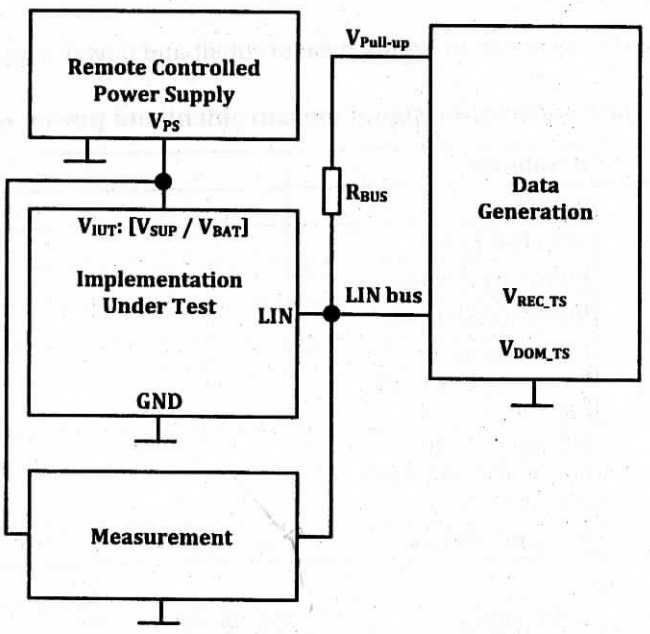

Figure 65 — Test system: Operating voltage range without RX and TX access

Table 147 defines the test system "Operating voltage range without RX and TX access".

Table 147 — Test system: Operating voltage range without RX and TX access

IUT node as	Class C device as master	[EPL-CT 83].1, [EPL-CT 83].2 [EPL-CT 83].5, [EPL-CT 83].6
	Class C device as slave	[EPL-CT 83].3, [EPL-CT 83].4 [EPL-CT 83].7, [EPL-CT 83].8
Initial state	**Operational conditions:**	
	V_{IUT}: [V_{SUP}/V_{BAT}]	Table 148 (BR_Range_20K) / Table 149 (BR_Range_10K)
	V_{Dom_TS}	0 V
	V_{Rec_TS}/$V_{Pull-up}$	36 V
Test steps	A voltage ramp is set on the V_{BAT}/V_{SUP} as defined in Tables 148/149. LIN communication is established between test system and IUT.	
Response	All IUT communication cycles sent during signal ramp shall be successful.	
Reference	ISO 17987-4:2016, Table 15, Param 52, Param 53	

Table 148 defines the test cases "Operating voltage ramp without RX and TX access for BR_Range_20K 24 V LIN systems".

Table 148 — Test cases: Operating voltage ramp without RX and TX access for BR_Range_20K 24 V LIN systems

EPL-CT-TC	V_{IUT} range: [V_{SUP} range/V_{BAT} range]	Signal ramp	R_{BUS}
[EPL-CT 83].1	[15,0 V to 36 V]/[16,0 V to 36 V]	0,1 V/s	30 kΩ (0,1 %)
[EPL-CT 83].2	[36 V to 15,0 V]/[36 V to 16,0 V]	0,1 V/s	30 kΩ (0,1 %)
[EPL-CT 83].3	[15,0 V to 36 V]/[16,0 V to 36 V]	0,1 V/s	1 kΩ (0,1 %)
[EPL-CT 83].4	[36 V to 15,0 V]/[36 V to 16,0 V]	0,1 V/s	1 kΩ (0,1 %)

Table 149 defines the test cases "Operating voltage ramp without RX and TX access for BR_Range_10K 24 V LIN systems".

Table 149 — Test cases: Operating voltage ramp without RX and TX access for BR_Range_10K 24 V LIN systems

EPL-CT-TC	V_{IUT} range: [V_{SUP} range/V_{BAT} range]	Signal ramp	R_{BUS}
[EPL-CT 83].5	[7,0 V to 36 V]/[8,0 V to 36 V]	0,1 V/s	30 kΩ (0,1 %)
[EPL-CT 83].6	[36 V to 7,0 V]/[36 V to 8,0 V]	0,1 V/s	30 kΩ (0,1 %)
[EPL-CT 83].7	[7,0 V to 36 V]/[8,0 V to 36 V]	0,1 V/s	1 kΩ (0,1 %)
[EPL-CT 83].8	[36 V to 7,0 V]/[36 V to 8,0 V]	0,1 V/s	1 kΩ (0,1 %)

8.5.3 Threshold voltages

8.5.3.1 General

This group of tests checks whether the receiver threshold voltages of the IUT are implemented correctly within the entire specified operating supply voltage range. Communication is established between the test system and the IUT, during which the dominant or recessive levels of the LIN frames transmitted by the test system are varied with respect to the applied supply voltage. The communication shall be either successful or unsuccessful dependent on the recessive/dominant levels.

8.5.3.2 [EPL-CT 84] IUT as receiver: V_{SUP} at V_{BUS_dom} (down)

Figure 66 shows the test configuration of the test system "IUT as receiver V_{SUP} at V_{BUS_dom} (down)".

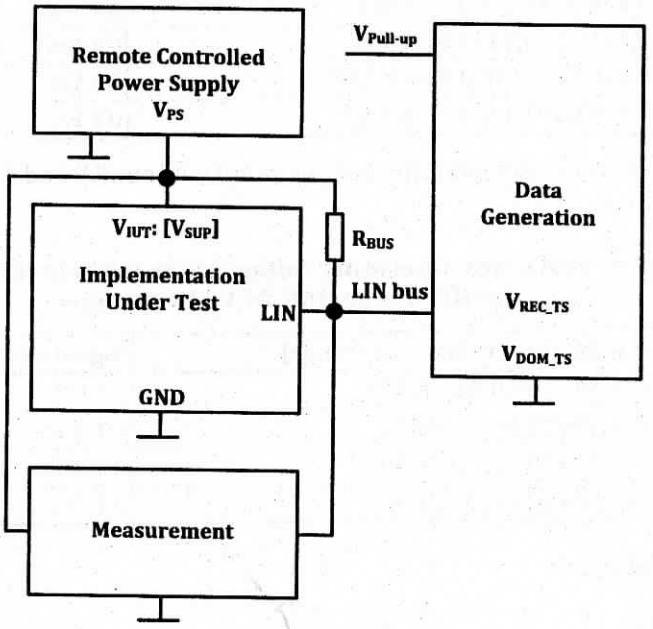

Figure 66 — Test system: IUT as receiver V_{SUP} at V_{BUS_dom} (down)

Table 150 defines the test system "IUT as receiver V_{SUP} at V_{BUS_dom} (down)".

Table 150 — Test system: IUT as receiver V_{SUP} at V_{BUS_dom} (down)

IUT node as	Class C device as slave	[EPL-CT 84].1, [EPL-CT 84].2, [EPL-CT 84].3, [EPL-CT 84].7, [EPL-CT 84].8, [EPL-CT 84].9
	Class C device as master	[EPL-CT 84].4, [EPL-CT 84].5, [EPL-CT 84].6, [EPL-CT 84].10, [EPL-CT 84].11, [EPL-CT 84].12
Initial state	**Operational conditions**	
	V_{IUT}: [V_{SUP}] V_{DOM_TS} V_{REC_TS}/$V_{Pull-up}$ R_{BUS}	Table 151 (BR_Range_20K), Table 152 (BR_Range_10K)
Test steps	Communication is established between the test system and the IUT. The initial dominant level transmitted by the test system is the lowest voltage as defined in Table 151 and Table 152 for each test case. The dominant level transmitted by the test system is increased by 20 mV after each IUT communication cycle until the highest level as defined in Table 151 and Table 152 for each test case is reached. The last V_{Dom} at which communication is successful is recorded as V_{th_dom}. See Figure 62 for an example of the communication between test system as master and slave IUT. See 8.4.1 for requirements on the data generation unit. The rise and fall time of the LIN signal shall be less than 500 ns.	
Response	Communication shall be successful or unsuccessful as defined in Table 151 and Table 152.	
Reference	ISO 17987-4:2016, Table 15, Param 62, Param 63 ISO 17987-4:2016, Figure 4	

Table 151 defines the test cases "IUT as receiver V_{SUP} at V_{BUS_dom} (down)".

Table 151 — Test cases: IUT as receiver V_{SUP} at V_{BUS_dom} (down) for BR_Range_20K 24 V LIN systems

EPL-CT-TC	V_{IUT}: [V_{SUP}]	V_{DOM_TS}	V_{REC_TS}	Expected communication result	R_{BUS}
[EPL-CT 84].1	15 V	[-2,25 V to 6,0 V]	36 V	Successful	1 kΩ (0,1 %)
		[9,0 V to 36 V]		Unsuccessful	
[EPL-CT 84].2	24 V	[-3,6 V to 9,6 V]	36 V	Successful	
		[14,4 V to 36 V]		Unsuccessful	
[EPL-CT 84].3	36 V	[-5,4 V to 14,4 V]	41,4 V	Successful	
		[21,6 V to 41,4 V]		Unsuccessful	
[EPL-CT 84].4	15 V	[-2,25 V to 6,0 V]	36 V	Successful	30 kΩ (0,1 %)
		[9,0 V to 36 V]		Unsuccessful	
[EPL-CT 84].5	24 V	[-3,6 V to 9,6 V]	36 V	Successful	
		[14,4 V to 36 V]		Unsuccessful	
[EPL-CT 84].6	36 V	[-5,4 V to 14,4 V]	41,4 V	Successful	
		[21,6 V to 41,4 V]		Unsuccessful	

Table 152 defines the test cases "IUT as receiver V_{SUP} at V_{BUS_dom} (down)"for BR_Range_10K 24 V LIN systems.

Table 152 — Test cases: IUT as receiver V_{SUP} at V_{BUS_dom} (down) for BR_Range_10K 24 V LIN systems

EPL-CT-TC	V_{IUT}: [V_{SUP}]	V_{DOM_TS}	V_{REC_TS}	Expected communication result	R_{BUS}
[EPL-CT 84].7	7 V	[-1,05 V to 2,8 V]	36 V	Successful	1 kΩ (0,1 %)
		[4,2 V to 36 V]		Unsuccessful	
[EPL-CT 84].8	24 V	[-3,6 V to 9,6 V]	36 V	Successful	
		[14,4 V to 36 V]		Unsuccessful	
[EPL-CT 84].9	36 V	[-5,4 V to 14,4 V]	41,4 V	Successful	
		[21,6 V to 41,4 V]		Unsuccessful	
[EPL-CT 84].10	7 V	[-1,05 V to 2,8 V]	36 V	Successful	30 kΩ (0,1 %)
		[4,2 V to 36 V]		Unsuccessful	
[EPL-CT 84].11	24 V	[-3,6 V to 9,6 V]	36 V	Successful	
		[14,4 V to 36 V]		Unsuccessful	
[EPL-CT 84].12	36 V	[-5,4 V to 14,4 V]	41,4 V	Successful	
		[21,6 V to 41,4 V]		Unsuccessful	

8.5.3.3 [EPL-CT 85] IUT as receiver: V_{SUP} at V_{BUS_rec} (up)

Figure 67 shows the test system "IUT as receiver V_{SUP} at V_{BUS_rec} (up)".

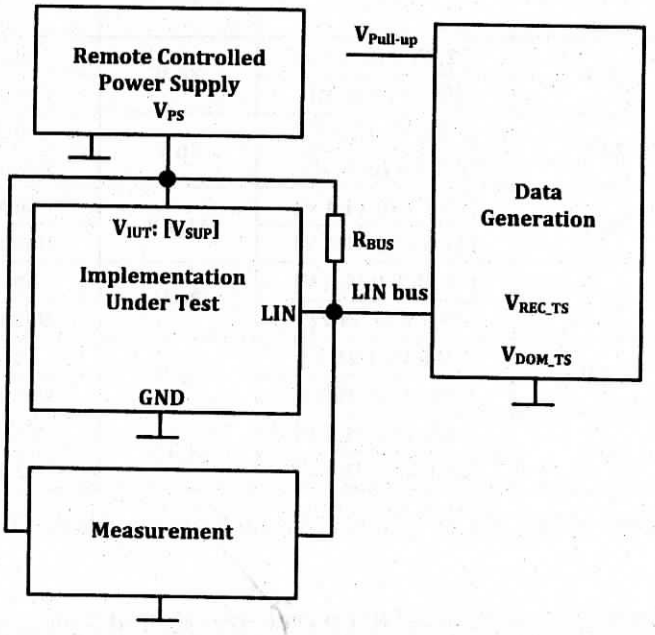

Figure 67 — Test system: IUT as receiver V_{SUP} at V_{BUS_rec} (up)

Table 153 defines the test system "IUT as receiver V_{SUP} at V_{BUS_rec} (up)".

Table 153 — Test system: IUT as receiver V_{SUP} at V_{BUS_rec} (up)

IUT node as	Class C device as slave	[EPL-CT 85].1, [EPL-CT 85].2, [EPL-CT 85].3, [EPL-CT 85].7, [EPL-CT 85].8, [EPL-CT 85].9
	Class C device as master	[EPL-CT 85].4, [EPL-CT 85].5, [EPL-CT 85].6, [EPL-CT 85].10, [EPL-CT 85].11, [EPL-CT 85].12
Initial state	**Operational conditions:**	
	V_{IUT}: [V_{SUP}] V_{DOM_TS} $V_{REC\_TS}/V_{Pull-up}$ R_{BUS}	Table 154 (BR_Range_20K), Table 155 (BR_Range_10K)
Test steps	Communication is established between the test system and the IUT. The initial recessive level transmitted by the test system is the highest voltage as defined in Table 154 and Table 155 for each test case. The recessive level transmitted by the test system is decreased by 20 mV after each IUT communication cycle until the lowest level as defined in Table 154 and Table 155 for each test case is reached. The last V_{Rec} at which communication is successful is recorded as V_{th_rec}. See Figure 62 for an example of the communication between test system as master and slave IUT. See 8.4.1 for requirements on the data generation unit. The rise and fall time of the LIN signal shall be less than 500 ns.	
Response	The Communication shall be successful or unsuccessful as defined in Table 154 and Table 155.	
Reference	ISO 17987-4:2016, Table 15, Param 62, Param 63 ISO 17987-4:2016, Figure 4	

Table 154 defines the test cases "IUT as receiver V_{SUP} at V_{BUS_rec} (up)".

Table 154 — Test cases: IUT as receiver V_{SUP} at V_{BUS_rec} (up) for BR_Range_20K 24 V LIN systems

EPL-CT-TC	V_{IUT}: [V_{SUP}]	V_{DOM_TS}	V_{REC_TS}	Expected communication result	R_{BUS}
[EPL-CT 85].1	15 V	-2,25 V	[36 V to 9,0 V]	Successful	1 kΩ (0,1 %)
			[6,0 V to -2,25 V]	Unsuccessful	
[EPL-CT 85].2	24 V	-3,6 V	[36 V to 14,4 V]	Successful	
			[9,6 V to -3,6 V]	Unsuccessful	
[EPL-CT 85].3	36 V	-5,4 V	[41,4 V to 21,6 V]	Successful	
			[14,4 V to -5,4 V]	Unsuccessful	
[EPL-CT 85].4	15 V	-2,25 V	[36 V to 9,0 V]	Successful	30 kΩ (0,1 %)
			[6,0 V to -2,25 V]	Unsuccessful	
[EPL-CT 85].5	24 V	-3,6 V	[36 V to 14,4 V]	Successful	
			[9,6 V to -3,6 V]	Unsuccessful	
[EPL-CT 85].6	36 V	-5,4 V	[41,4 V to 21,6 V]	Successful	
			[14,4 V to -5,4 V]	Unsuccessful	

Table 155 defines the test cases "IUT as receiver V_{SUP} at V_{BUS_rec} (up)" for BR_Range_10K 24 V Lin systems.

Table 155 — Test cases: IUT as receiver V_{SUP} at V_{BUS_rec} (up) for BR_Range_10K 24 V LIN systems

EPL-CT-TC	V_{IUT}: [V_{SUP}]	V_{DOM_TS}	V_{REC_TS}	Expected communication result	R_{BUS}
[EPL-CT 85].7	7 V	-1,05 V	[36 V to 4,2 V]	Successful	1 kΩ (0,1 %)
			[2,8 V to -1,05 V]	Unsuccessful	
[EPL-CT 85].8	24 V	-3,6 V	[36 V to 14,4 V]	Successful	
			[9,6 V to -3,6 V]	Unsuccessful	
[EPL-CT 85].9	36 V	-5,4 V	[41,4 V to 21,6 V]	Successful	
			[14,4 V to -5,4 V]	Unsuccessful	
[EPL-CT 85].10	7 V	-1,05 V	[36 V to 4,2 V]	Successful	30 kΩ (0,1 %)
			[2,8 V to -1,05 V]	Unsuccessful	
[EPL-CT 85].11	24 V	-3,6 V	[36 V to 14,4 V]	Successful	
			[9,6 V to -3,6 V]	Unsuccessful	
[EPL-CT 85].12	36 V	-5,4 V	[41,4 V to 21,6 V]	Successful	
			[14,4 V to -5,4 V]	Unsuccessful	

8.5.3.4 [EPL-CT 86] IUT as receiver: V_{SUP} at V_{BUS}

This test shall verify the symmetry of the receiver thresholds. It evaluates V_{th_dom} (3 values) measured in 8.5.3.2 and V_{th_rec} (3 values) measured in 8.5.3.3.

Table 156 defines the test system "IUT as Receiver: V_{SUP} at V_{BUS}".

Table 156 — Test system: IUT as receiver: V_{SUP} at V_{BUS}

IUT node as	Class C device as slave	[EPL–CT 86].1, [EPL–CT 86].2, [EPL–CT 86].3, [EPL–CT 86].7, [EPL–CT 86].8, [EPL–CT 86].9
	Class C device as master	[EPL–CT 86].4, [EPL–CT 86].5, [EPL–CT 86].6, [EPL–CT 86].10, [EPL–CT 86].11, [EPL–CT 86].12
Initial state	**Operational conditions:**	
	V_{IUT}: [V_{SUP}] V_{th_dom} V_{th_rec}	Table 157 (BR_Range_20K), Table 158 (BR_Range_10K)
Test steps	Calculate $V_{BUS\_CNT} = (V_{th\_dom} + V_{th\_rec})/2$ and $V_{HYS} = V_{th\_rec} - V_{th\_dom}$	
Response	V_{BUS_CNT} shall be in the range of [0,475 to 0,525] × V_{SUP} V_{HYS} shall be less than 0,175 × V_{SUP}.	
Reference	ISO 17987–4:2016, Table 15, Param 64, Param 65 ISO 17987–4:2016, Figure 4	

Table 157 defines the test cases "IUT as receiver for BR_Range_20K 24 V LIN systems: V_{SUP} at V_{BUS}".

Table 157 — Test cases: IUT as receiver for BR_Range_20K 24 V LIN systems: V_{SUP} at V_{BUS}

EPL–CT	V_{th_dom} as measured in test case	V_{th_rec} as measured in test case	V_{IUT}: [V_{SUP}]
[EPL–CT 86].1	[EPL–CT 84].1	[EPL–CT 85].1	15 V
[EPL–CT 86].2	[EPL–CT 84].2	[EPL–CT 85].2	24 V
[EPL–CT 86].3	[EPL–CT 84].3	[EPL–CT 85].3	36 V
[EPL–CT 86].4	[EPL–CT 84].4	[EPL–CT 85].4	15 V
[EPL–CT 86].5	[EPL–CT 84].5	[EPL–CT 85].5	24 V
[EPL–CT 86].6	[EPL–CT 84].6	[EPL–CT 85].6	36 V

Table 158 defines the test cases "IUT as receiver for BR_Range_10K 24 V LIN systems: V_{SUP} at V_{BUS}".

Table 158 — Test cases: IUT as receiver for BR_Range_10K 24 V LIN systems: V_{SUP} at V_{BUS}

EPL–CT	V_{th_dom} as measured in test case	V_{th_rec} as measured in test case	V_{IUT}: [V_{SUP}]
[EPL–CT 86].7	[EPL–CT 84].7	[EPL–CT 85].7	7 V
[EPL–CT 86].8	[EPL–CT 84].8	[EPL–CT 85].8	24 V
[EPL–CT 86].9	[EPL–CT 84].9	[EPL–CT 85].9	36 V
[EPL–CT 86].10	[EPL–CT 84].10	[EPL–CT 85].10	7 V
[EPL–CT 86].11	[EPL–CT 84].11	[EPL–CT 85].11	24 V
[EPL–CT 86].12	[EPL–CT 84].12	[EPL–CT 85].12	36 V

8.5.4 [EPL–CT 87] Variation of $V_{SUP\_NON\_OP}$ ∈ [–0,3 V to 7,0 V], [18 V to 58 V]

This test checks whether the IUT influences the bus during under voltage and over voltage conditions.

Table 68 shows the test configuration of the test system "Variation of $V_{SUP\_NON\_OP}$.

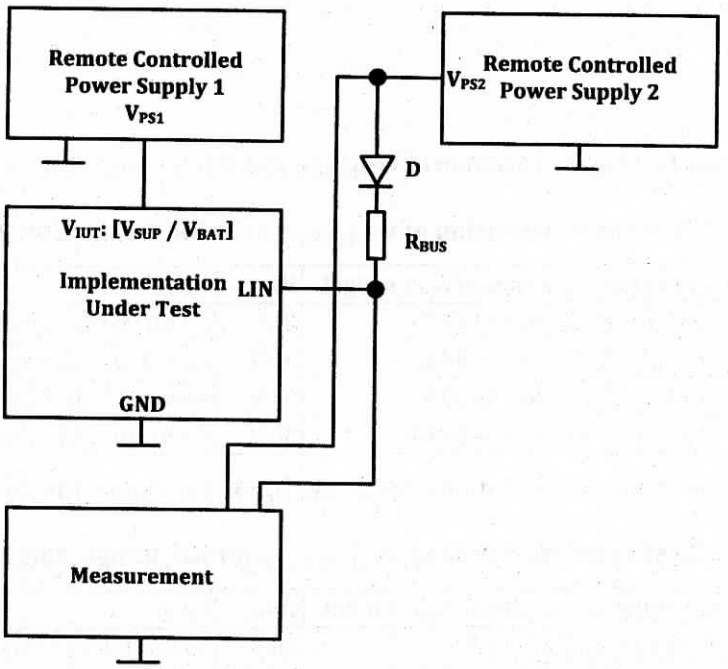

Figure 68 — Test system: Variation of $V_{SUP\_NON\_OP}$

Table 159 defines the test system "Variation of $V_{SUP\_NON\_OP}$".

Table 159 — Test system: Variation of $V_{SUP\_NON\_OP}$

IUT node as	Class C device as master	[EPL–CT 87].1, [EPL–CT 87].3, [EPL–CT 87].5, [EPL–CT 87].7
	Class C device as slave	[EPL–CT 87].2, [EPL–CT 87].4, [EPL–CT 87].6, [EPL–CT 87].8
Initial state	**Operational conditions:**	
	V_{IUT}: [V_{SUP}/V_{BAT}]	Signal with a 1 V/s ramp as defined in Table 160, Table 161.
	V_{PS2}	See Table 160, Table 161.
	R_{BUS}	See Table 160, Table 161.
Test steps	There is no communication on the LIN bus. A voltage ramp (up and down) is set on V_{IUT}: [V_{SUP}/V_{BAT}]. The stimulus stays for t = 30 s at V_{BAT} = 58 V.	
Response	No dominant state on LIN shall occur. The IUT shall not be destroyed during the test. The afterward recessive voltage shall have a maximum deviation of ±5 % from the before recessive voltage.	
Reference	ISO 17987–4:2016, Table 15, Param 56	

Table 160 defines the test cases "Variation of $V_{SUP\_NON\_OP}$ for BR_Range_20K 24 V LIN systems".

Table 160 — Test cases: Variation of $V_{SUP\_NON\_OP}$ for BR_Range_20K 24 V LIN systems

EPL-CT-TC	V_{IUT} range: [V_{SUP} range/V_{BAT} range]	V_{PS2}	R_{BUS}
[EPL-CT 87].1	[-0,3 V to 16 V], [36 V to 58 V]	36 V	60 kΩ (0,1 %) + diode (1N4148)
[EPL-CT 87].2	[-0,3 V to 16 V], [36 V to 58 V]	36 V	1,1 kΩ (0,1 %) + diode (1N4148)
[EPL-CT 87].3	[-0,3 V to 15 V], [36 V to 58 V]	36 V	60 kΩ (0,1 %) + diode (1N4148)
[EPL-CT 87].4	[-0,3 V to 15 V], [36 V to 58 V]	36 V	1,1 kΩ (0,1 %) + diode (1N4148)

Table 161 defines the test cases "Variation of $V_{SUP\_NON\_OP}$ for BR_Range_10K 24 V LIN systems".

Table 161 — Test cases: Variation of $V_{SUP\_NON\_OP}$ for BR_Range_10K 24 V LIN systems

EPL-CT-TC	V_{IUT} range: [V_{SUP} range/V_{BAT} range]	V_{PS2}	R_{BUS}
[EPL-CT 87].5	[-0,3 V to 8 V], [36 V to 58 V]	36 V	60 kΩ (0,1 %) + diode (1N4148)
[EPL-CT 87].6	[-0,3 V to 8 V], [36 V to 58 V]	36 V	1,1 kΩ (0,1 %) + diode (1N4148)
[EPL-CT 87].7	[-0,3 V to 7 V], [36 V to 58 V]	36 V	60 kΩ (0,1 %) + diode (1N4148)
[EPL-CT 87].8	[-0,3 V to 7 V], [36 V to 58 V]	36 V	1,1 kΩ (0,1 %) + diode (1N4148)

8.5.5 I_{BUS} under several conditions

8.5.5.1 [EPL-CT 88] I_{BUS_LIM} at dominant state (driver on)

This test checks the drive capability of the output stage. A LIN driver shall pull the LIN bus below a certain voltage according to the LIN standard. The current limitation is measured indirectly.

Figure 69 shows the test configuration of the test system "I_{BUS_LIM} at dominant state (driver on)".

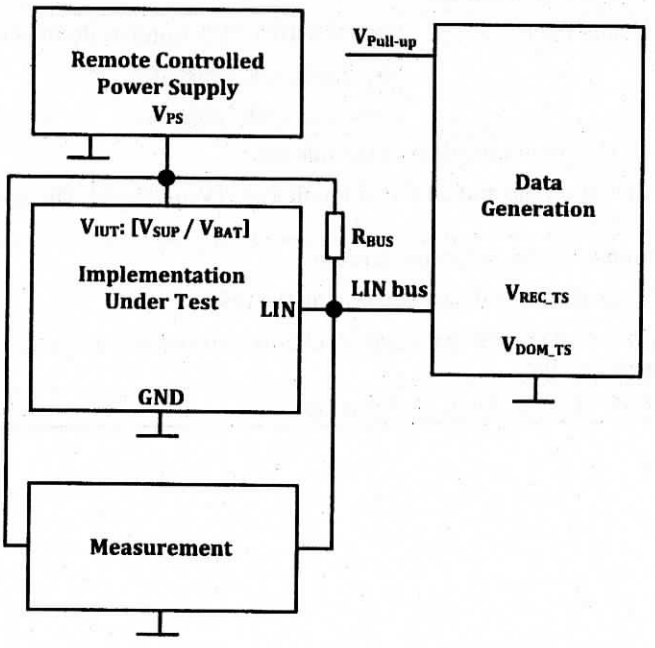

Figure 69 — Test system: I_{BUS_LIM} at dominant state (driver on)

Table 162 defines the test system "I_{BUS_LIM} at dominant state (driver on)".

Table 162 — Test system: I_{BUS_LIM} at dominant state (driver on)

IUT node as	Class C device as master Class C device as slave	[EPL-CT 88].1
Initial state	**Operational conditions:**	
	V_{IUT}: [V_{SUP}/V_{BAT}] V_{Dom_TS} V_{Rec_TS} R_{BUS}	See Table 163
Test steps	The LIN pin is connected via R_{BUS} to V_{IUT}: [V_{SUP}/V_{BAT}]. A LIN communication is established between the test system and the IUT.	
Response	One communication cycle shall be successful. For BR_Range_20K 24 V LIN systems: The dominant state bus level shall be lower than TH_DOM = 0,302 × V_{IUT} = 10,872 V for integrated devices. The dominant state bus level shall be lower than TH_DOM = 0,302 × (V_{IUT} – 1 V) = 10,52 V for ECUs. For BR_Range_10K 24 V LIN systems: The dominant state bus level shall be lower than TH_DOM = 0,284 × V_{IUT} = 10,224 V for integrated devices. The dominant state bus level shall be lower than TH_DOM = 0,302 × (V_{IUT} – 1 V) = 9,94 V for ECUs.	
Reference	ISO 17987-4:2016, Table 15, Param 57	

Table 163 defines the test cases "I_{BUS_LIM} at dominant state (driver on)".

Table 163 — Test cases: I_{BUS_LIM} at dominant state (driver on)

EPL-CT-TC	V_{IUT}: [V_{SUP}/V_{BAT}]	V_{DOM_TS}	V_{Rec_TS}	R_{BUS}
[EPL-CT 88].1	36 V	0 V	36 V	480 Ω (0,1 %)

8.5.5.2 [EPL-CT 89] $I_{BUS\_PAS\_dom}$: IUT in recessive state: V_{BUS} = 0 V

This test case is intended to test the input leakage current $I_{BUS\_PAS\_dom}$ into a node during dominant state of the LIN bus.

Table 70 shows the test configuration of the test system "$I_{BUS\_PAS\_dom}$ IUT in recessive state V_{BUS} = 0 V".

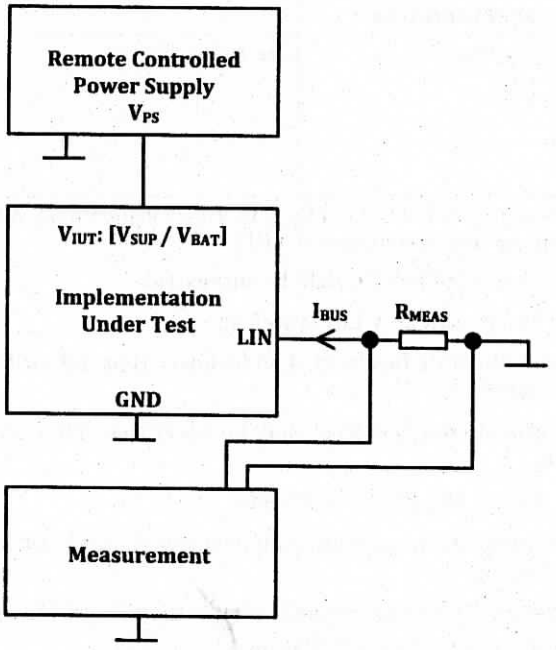

Figure 70 — Test case: $I_{BUS\_PAS\_dom}$ IUT in recessive state V_{BUS} = 0 V

Table 164 defines the test system "$I_{BUS\_PAS\_dom}$ IUT in recessive state V_{BUS} = 0 V".

Table 164 — Test system: $I_{BUS\_PAS\_dom}$ IUT in recessive state V_{BUS} = 0 V

IUT node as	Class C device as slave	[EPL–CT 89].1
Initial state	**Operational conditions:**	
	V_{IUT}: [V_{SUP}/V_{BAT}] R_{MEAS}	See Table 165
Test steps	There is no communication on the LIN bus.	
Response	The maximum value of voltage drop shall be higher than –1 000 mV.	
Reference	ISO 17987-4:2016, Table 15, Param 58	

Table 165 defines the test cases "$I_{BUS\_PAS\_dom}$ IUT in recessive state V_{BUS} = 0 V".

Table 165 — Test cases: $I_{BUS\_PAS\_dom}$ IUT in recessive state V_{BUS} = 0 V

EPL–CT–TC	V_{IUT}: [V_{SUP}/V_{BAT}]	R_{MEAS}
[EPL–CT 89].1	24 V	499 Ω (0,1 %)

8.5.5.3 [EPL–CT 90] $I_{BUS\_PAS\_rec}$: IUT in Recessive State: V_{BAT} = 8,0 V with Variation of $V_{BUS} \in$ [8,0 V to 36 V]

This test checks whether there is a diode implementation within the termination path of the IUT. The reverse current should be limited to $I_{BUS\_PAS\_rec(max)}$ from the LIN wire into the IUT even if V_{BUS} is higher than the IUTs supply voltage V_{BAT}.

Figure 71 shows the test configuration of the test system "$I_{BUS\_PAS\_rec}$ IUT in recessive state: V_{BAT} = 8,0 V with Variation of $V_{BUS} \in$ [8,0 V to 36 V]".

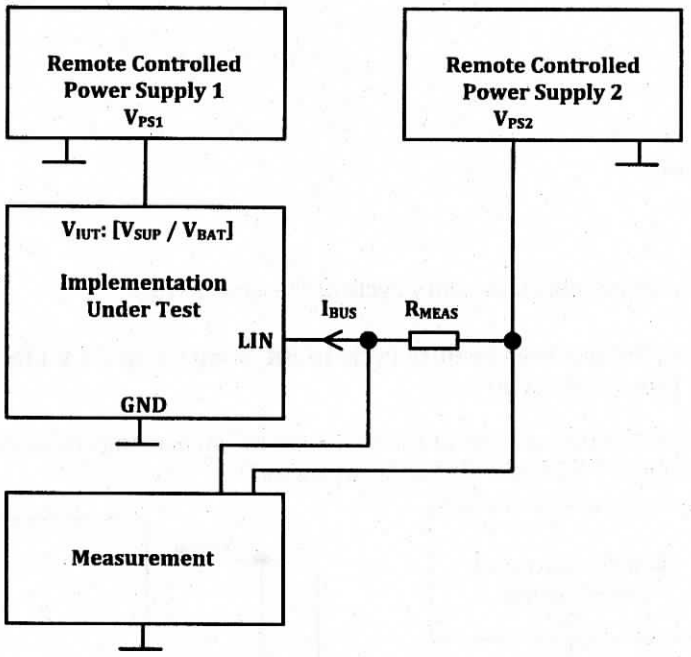

Figure 71 — Test system: $I_{BUS\_PAS\_rec}$ IUT in recessive state: V_{BAT} = 8,0 V with variation of V_{BUS} ∈ [8,0 V to 36 V]

Table 166 defines the test system "$I_{BUS\_PAS\_rec}$ IUT in recessive state: V_{BAT} = 8,0 V with variation of V_{BUS} [8,0 V to 36 V]".

Table 166 — Test system: $I_{BUS\_PAS\_rec}$ IUT in recessive state: V_{BAT} = 8,0 V with variation of V_{BUS} [8,0 V to 36 V]

IUT node as	Class C device as master Class C device as slave	[EPL-CT 90].1
Initial state	**Operational conditions:**	
	V_{IUT}: [V_{SUP}/V_{BAT}] R_{MEAS}	See Table 167
Test steps	V_{PS2} = Signal with a 2 V/s ramp in the range [8 V to 36 V] up and down. There is no communication on the LIN bus.	
Response	The maximum value of voltage drop shall be less than or equal to 20 mV.	
Reference	ISO 17987-4:2016, Table 15, Param 59	

Table 167 defines the test cases "$I_{BUS\_PAS\_rec}$ IUT in recessive state: V_{BAT} = 8,0 V with variation of V_{BUS} [8,0 V to 36 V]".

Table 167 — Test cases: $I_{BUS\_PAS\_rec}$ IUT in recessive state: V_{BAT} = 8,0 V with variation of V_{BUS} [8,0 V to 36 V]

EPL-CT-TC	V_{IUT}: [V_{SUP}/V_{BAT}]	R_{MEAS}
[EPL-CT 90].1	7,0 V/8,0 V	1 000 Ω (0,1 %)

8.5.6 Slope control

8.5.6.1 Purpose

The purpose of this test is to check the duty cycle of the driver stage.

8.5.6.2 [EPL–CT 91] Measuring the duty cycle of BR_Range_10K 24 V LIN networks at 10,417 kbit/s — IUT as transmitter

Figure 72 shows the test configuration of the test system "Measuring the duty cycle of BR_Range_10K 24 V LIN networks at 10,417 kbit/s — IUT as transmitter".

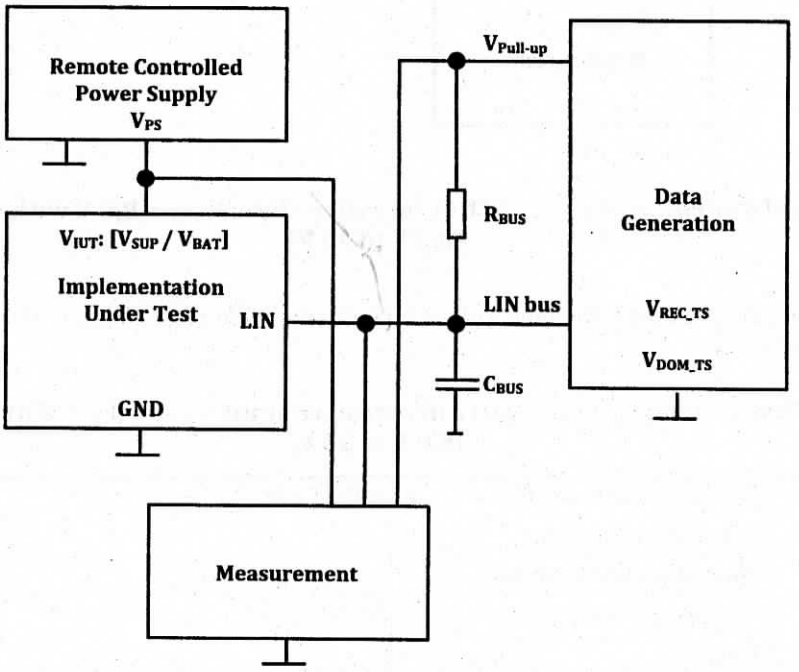

Figure 72 — Test case: Measuring the duty cycle of BR_Range_10K 24 V LIN networks at 10,417 kbit/s — IUT as transmitter

Table 168 defines the test system "Measuring the duty cycle of BR_Range_10K 24 V LIN networks at 10,417 kbit/s — IUT as transmitter".

Table 168 — Test system: Measuring the duty cycle of BR_Range_10K 24 V LIN networks at 10,417 kbit/s — IUT as transmitter

IUT node as	Class C device as master Class C device as slave	[EPL-CT 91].1 - [EPL-CT 91].18
Initial state	**Parameters:**	
	Bus loads	See Table 169
	Operational conditions:	
	V_{IUT}: [V_{SUP}/V_{BAT}]	See Table 169
	V_{Dom_TS}	0 V
	V_{Rec_TS}/$V_{Pull\text{-}up}$	See Table 169
Test steps	A LIN communication is established between the test system and the IUT. The highest bit rate supported by the IUT (but a maximum of 10,417 kbit/s) is used. Rising and falling edges shall be less than 500 ns. Master IUT: The test system records one LIN frame transmitted by the IUT. The exact bit rate of the IUT is identified by measuring the time between the falling edges of the start bit and bit 7 of the synch byte field in the recorded frame. $t_{Bus\_rec(max)}$ and $t_{Bus\_rec(min)}$ are measured at bit 0 of the synch byte field in the recorded frame. Slave IUT: TST_FRM_RDBI_0 followed by TST_HDR_SR_3D is transmitted by the test system. TST_HDR_SR_3D is recorded by the test system. The exact slave bit rate is identified by measuring the time between the falling edges of the start bit and bit 2 of DB3 (RSID = $F2_{16}$) of the slave answer. $t_{Bus\_rec(max)}$ and $t_{Bus\_rec(min)}$ are measured at bit 1 of DB3 (RSID = $F2_{16}$) of the slave answer.	
Response	The measured duty cycle D3 shall be greater than or equal to 0,386 for V_{SUP} = [7,0 V to 36 V], the measured duty cycle D4 shall be less than or equal to 0,591 for V_{SUP} = [7,6 V to 36 V]. If V_{SUP} is not accessible, then V_{BAT} - 0,7 V shall be used for threshold calculation of the duty cycle.	
Reference	ISO 17987-4:2016, Table 18, Param 74, Param 75 ISO 17987-4:2016, Figure 5	

Table 169 defines the test cases "Measuring the duty cycle of BR_Range_10K 24 V LIN networks at 10,417 kbit/s — IUT as transmitter".

Table 169 — Test cases: Measuring the duty cycle of BR_Range_10K 24 V LIN networks at 10,417 kbit/s — IUT as transmitter

EPL-CT-TC	V_{IUT}: [V_{SUP}/V_{BAT}]	V_{Rec_TS}/ $V_{Pull\text{-}up}$	Bus loads (C_{BUS}; R_{BUS})	Duty cycle	
				D3 min.	D4 max.
[EPL-CT 91].1	7,0 V/8,0 V	6,0 V	1 nF (1 %); 1 kΩ (0,1 %)	0,386	—
[EPL-CT 91].2	7,0 V/8,0 V	6,6 V	1 nF (1 %); 1 kΩ (0,1 %)	0,386	—
[EPL-CT 91].3	7,0 V/8,0 V	6,0 V	6,8 nF (1 %); 660 Ω (0,1 %)	0,386	—
[EPL-CT 91].4	7,0 V/8,0 V	6,6 V	6,8 nF (1 %); 660 Ω (0,1 %)	0,386	—
[EPL-CT 91].5	7,0 V/8,0 V	6,0 V	10 nF (1 %); 500 Ω (0,1 %)	0,386	—
[EPL-CT 91].6	7,0 V/8,0 V	6,6 V	10 nF (1 %); 500 Ω (0,1 %)	0,386	—
[EPL-CT 91].7	7,6 V/8,6 V	6,6 V	1 nF (1 %); 1 kΩ (0,1 %)	0,386	0,591
[EPL-CT 91].8	7,6 V/8,6 V	7,2 V	1 nF (1 %); 1 kΩ (0,1 %)	0,386	0,591
[EPL-CT 91].9	7,6 V/8,6 V	6,6 V	6,8 nF (1 %); 660 Ω (0,1 %)	0,386	0,591
[EPL-CT 91].10	7,6 V/8,6 V	7,2 V	6,8 nF (1 %); 660 Ω (0,1 %)	0,386	0,591
[EPL-CT 91].11	7,6 V/8,6 V	6,6 V	10 nF (1 %); 500 Ω (0,1 %)	0,386	0,591
[EPL-CT 91].12	7,6 V/8,6 V	7,2 V	10 nF (1 %); 500 Ω (0,1 %)	0,386	0,591
[EPL-CT 91].13	36 V/36,6 V	35,0 V	1 nF (1 %); 1 kΩ (0,1 %)	0,386	0,591
[EPL-CT 91].14	36 V/36,6 V	35,6 V	1 nF (1 %); 1 kΩ (0,1 %)	0,386	0,591
[EPL-CT 91].15	36 V/36,6 V	35,0 V	6,8 nF (1 %); 660 Ω (0,1 %)	0,386	0,591
[EPL-CT 91].16	36 V/36,6 V	35,6 V	6,8 nF (1 %); 660 Ω (0,1 %)	0,386	0,591
[EPL-CT 91].17	36 V/36,6 V	35,0 V	10 nF (1 %); 500 Ω (0,1 %)	0,386	0,591
[EPL-CT 91].18	36 V/36,6 V	35,6 V	10 nF (1 %); 500 Ω (0,1 %)	0,386	0,591

8.5.6.3 [EPL-CT 92] Measuring the duty cycle of BR_Range_20K 24 V LIN network at 20,0 kbit/s — IUT as transmitter

Figure 73 shows the test configuration of the test system "Measuring the duty cycle of BR_Range_20K 24 V LIN networks at 20,0 kbit/s — IUT as transmitter".

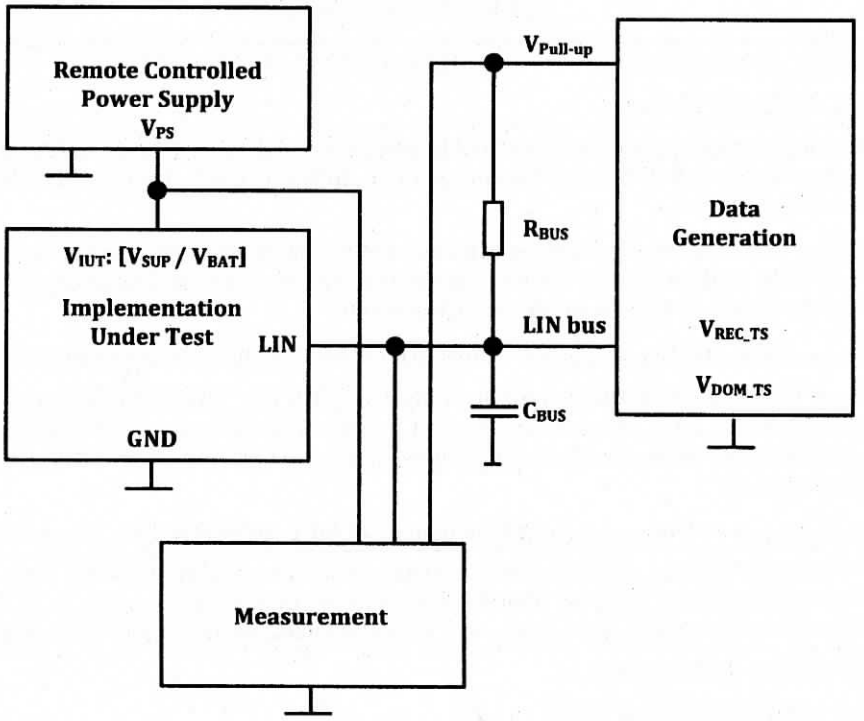

Figure 73 — Test system: Measuring the duty cycle of BR_Range_20K 24 V LIN networks at 20,0 kbit/s — IUT as transmitter

Table 170 defines the test system "Measuring the duty cycle of BR_Range_20K 24 V LIN networks at 20,0 kbit/s — IUT as transmitter".

Table 170 — Test system: Measuring the duty cycle of BR_Range_20K 24 V LIN networks at 20,0 kbit/s — IUT as transmitter

IUT node as	Class C device as master Class C device as slave	[EPL-CT 92].1 - [EPL-CT 92].18
Initial state	**Parameters:**	
	Bus loads	See Table 171
	Operational conditions:	
	V_{IUT}: [V_{SUP}/V_{BAT}]	See Table 171
	V_{Dom_TS}	0 V
	V_{Rec_TS}/$V_{Pull\text{-}up}$	See Table 171

Table 170 *(continued)*

IUT node as	Class C device as master Class C device as slave	[EPL-CT 92].1 – [EPL-CT 92].18
Test steps	A LIN communication is established between the test system and the IUT. The highest bit rate supported by the IUT (but a maximum of 20 kbit/s) is used. Rising and falling edges shall be less than 500 ns. Master IUT: The test system records one LIN frame transmitted by the IUT. The exact bit rate of the IUT is identified by measuring the time between the falling edges of the start bit and bit 7 of the synch byte field in the recorded frame. $t_{Bus\_rec(max)}$ and $t_{Bus\_rec(min)}$ are measured at bit 0 of the synch byte field in the recorded frame. Slave IUT: TST_FRM_RDBI_0 followed by TST_HDR_SR_3D is transmitted by the test system. TST_HDR_SR_3D is recorded by the test system. The exact slave bit rate is identified by measuring the time between the falling edges of the start bit and bit 2 of DB3 (RSID = $F2_{16}$) of the slave answer. $t_{Bus\_rec(max)}$ and $t_{Bus\_rec(min)}$ are measured at bit 1 of DB3 (RSID = $F2_{16}$) of the slave answer.	
Response	The measured duty cycle D1 shall be greater than or equal to 0,330 for V_{SUP} = [15,0 V to 36 V], the measured duty cycle D2 shall be less than or equal to 0,642 for V_{SUP} = [15,6 V to 36 V]. If V_{SUP} is not accessible, then V_{BAT} – 0,7 V shall be used for threshold calculation of the duty cycle.	
Reference	ISO 17987-4:2016, Table 17 ISO 17987-4:2016, Figure 5	

Table 171 defines the test cases "Measuring the duty cycle of BR_Range_20K 24 V LIN networks at 20,0 kbit/s — IUT as transmitter".

Table 171 — Test cases: Measuring the duty cycle of BR_Range_20K 24 V LIN networks at 20,0 kbit/s — IUT as transmitter

EPL-CT-TC	V_{IUT}: [V_{SUP}/V_{BAT}]	V_{Rec_TS}/$V_{Pull\text{-}up}$	Bus loads (C_{BUS}; R_{BUS})	Duty cycle	
				D1 min.	D2 max.
[EPL-CT 92].1	15,0 V/16,0 V	14,0 V	1 nF (1 %); 1 kΩ (0,1 %)	0,330	—
[EPL-CT 92].2	15,0 V/16,0 V	14,6 V	1 nF (1 %); 1 kΩ (0,1 %)	0,330	—
[EPL-CT 92].3	15,0 V/16,0 V	14,0 V	6,8 nF (1 %); 660 Ω (0,1 %)	0,330	—
[EPL-CT 92].4	15,0 V/16,0 V	14,6 V	6,8 nF (1 %); 660 Ω (0,1 %)	0,330	—
[EPL-CT 92].5	15,0 V/16,0 V	14,0 V	10 nF (1 %); 500 Ω (0,1 %)	0,330	—
[EPL-CT 92].6	15,0 V/16,0 V	14,6 V	10 nF (1 %); 500 Ω (0,1 %)	0,330	—
[EPL-CT 92].7	15,6 V/16,6 V	14,6 V	1 nF (1 %); 1 kΩ (0,1 %)	0,330	0,642
[EPL-CT 92].8	15,6 V/16,6 V	15,2 V	1 nF (1 %); 1 kΩ (0,1 %)	0,330	0,642
[EPL-CT 92].9	15,6 V/16,6 V	14,6 V	6,8 nF (1 %); 660 Ω (0,1 %)	0,330	0,642
[EPL-CT 92].10	15,6 V/16,6 V	15,2 V	6,8 nF (1 %); 660 Ω (0,1 %)	0,330	0,642
[EPL-CT 92].11	15,6 V/16,6 V	14,6 V	10 nF (1 %); 500 Ω (0,1 %)	0,330	0,642
[EPL-CT 92].12	15,6 V/16,6 V	15,2 V	10 nF (1 %); 500 Ω (0,1 %)	0,330	0,642
[EPL-CT 92].13	36 V/36,6 V	35,0 V	1 nF (1 %); 1 kΩ (0,1 %)	0,330	0,642
[EPL-CT 92].14	36 V/36,6 V	35,6 V	1 nF (1 %); 1 kΩ (0,1 %)	0,330	0,642
[EPL-CT 92].15	36 V/36,6 V	35,0 V	6,8 nF (1 %); 660 Ω (0,1 %)	0,330	0,642
[EPL-CT 92].16	36 V/36,6 V	35,6 V	6,8 nF (1 %); 660 Ω (0,1 %)	0,330	0,642
[EPL-CT 92].17	36 V/36,6 V	35,0 V	10 nF (1 %); 500 Ω (0,1 %)	0,330	0,642
[EPL-CT 92].18	36 V/36,6 V	35,6 V	10 nF (1 %); 500 Ω (0,1 %)	0,330	0,642

8.5.7 [EPL–CT 93] Propagation delay

8.5.7.1 Propagation delay with minimum/maximum duty cycles

The following test checks the receiver's internal delay and its symmetry. The test is done indirectly by setting the duty cycles of the responses transmitted by the test system to the maximum/minimum values. Furthermore, the test system bit rate is adjustet to achieve a worst case deviation from the IUT.

Bytes sent by the test system would then look as shown in Figure 74 and Figure 75. To reduce testing effort, only the rising edges are transmitted delayed or in advance, as shown in Figure 76 and Figure 77, which does not affect the test result.

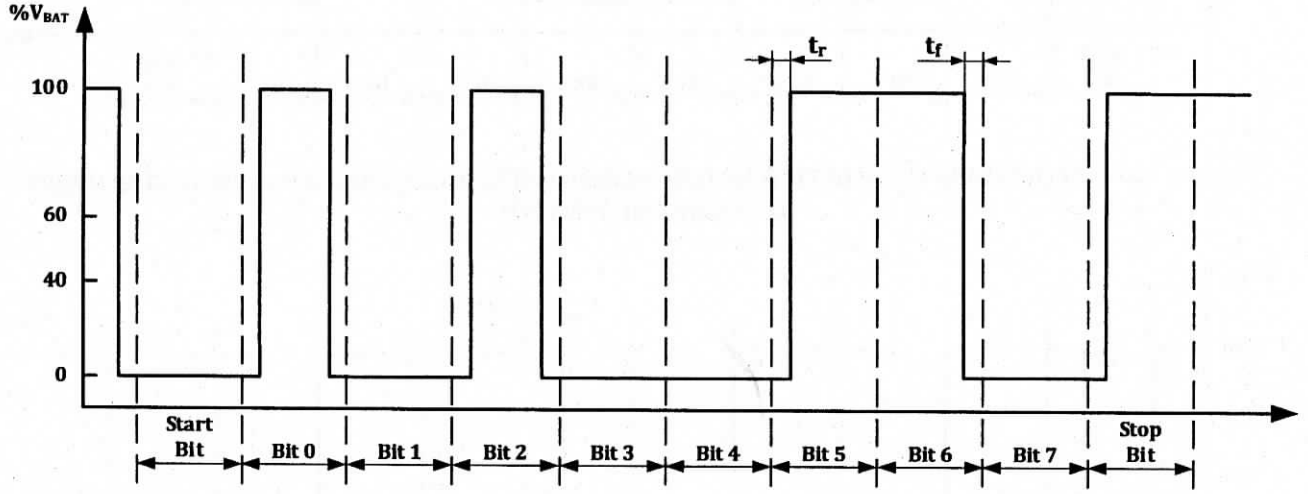

Figure 74 — Byte with minimum duty cycle (falling edges transmitted in advance, rising edges transmitted delayed)

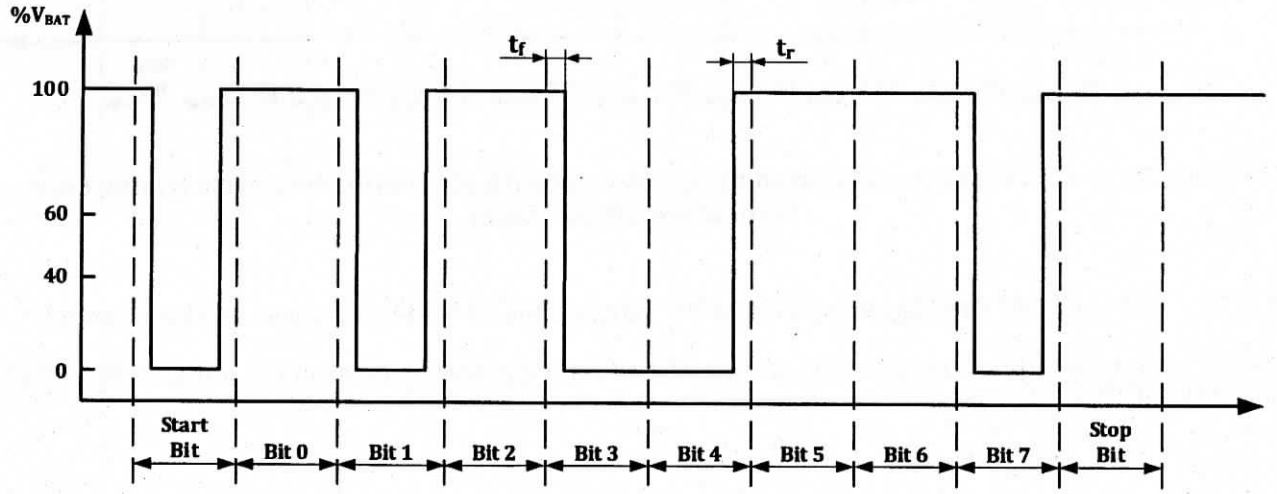

Figure 75 — Byte with maximum duty cycle (falling edges transmitted delayed, rising edges transmitted in advance)

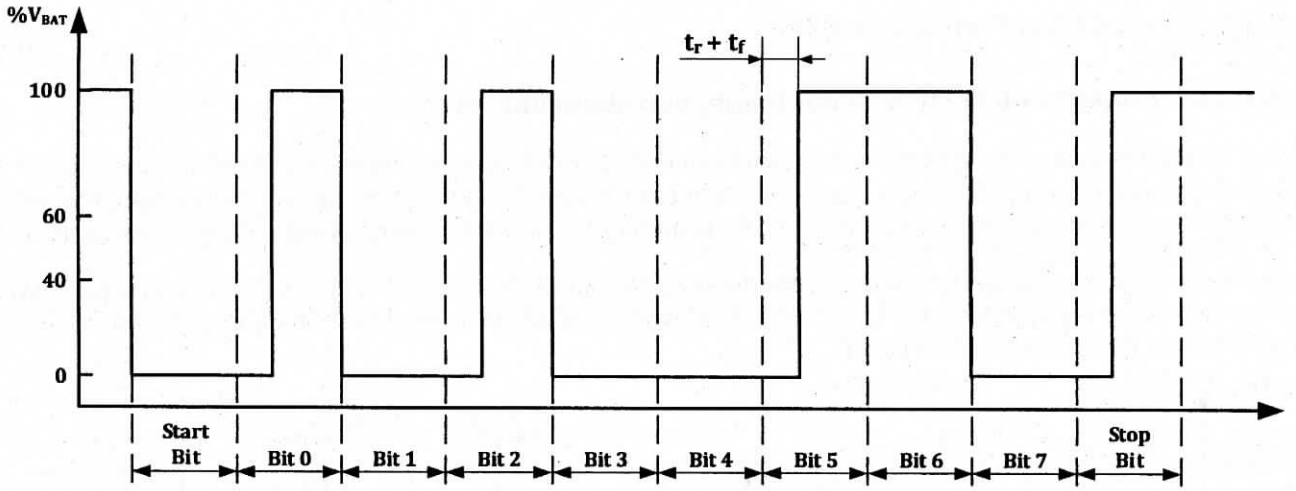

Figure 76 — Actual byte transmitted by test system with minimum duty cycle (rising edges transmitted delayed)

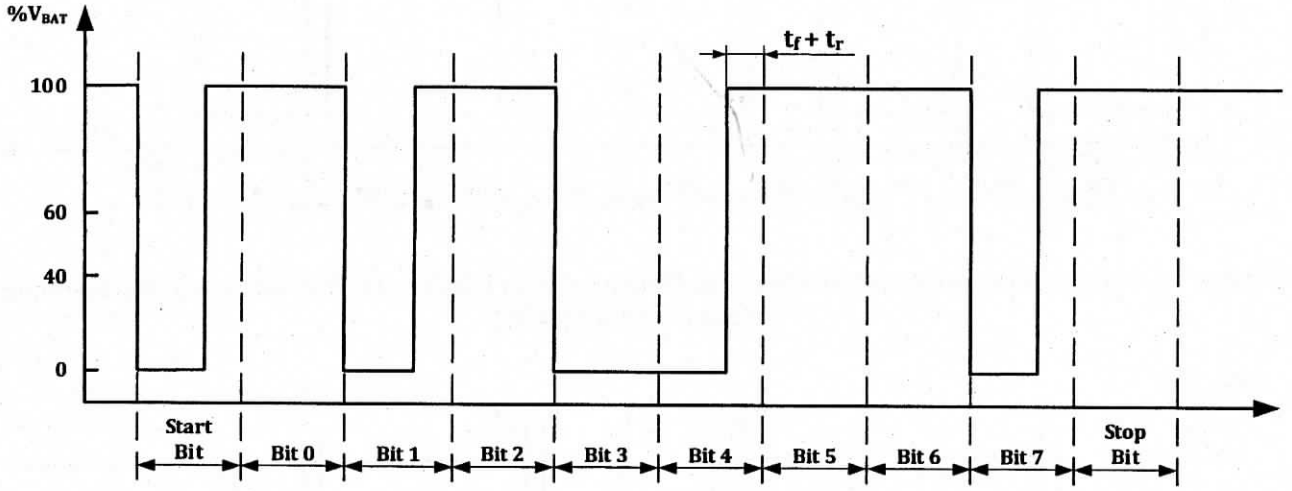

Figure 77 — Actual byte transmitted by test system with maximum duty cycle (rising edges transmitted in advance)

8.5.7.2 [EPL-CT 94] Propagation delay of BR_Range_10K 24 V LIN networks at 10,417 kbit/s

Figure 78 shows the test configuration of the test system "Propagation delay of BR_Range_10K 24 V LIN networks at 10,417 kbit/s".

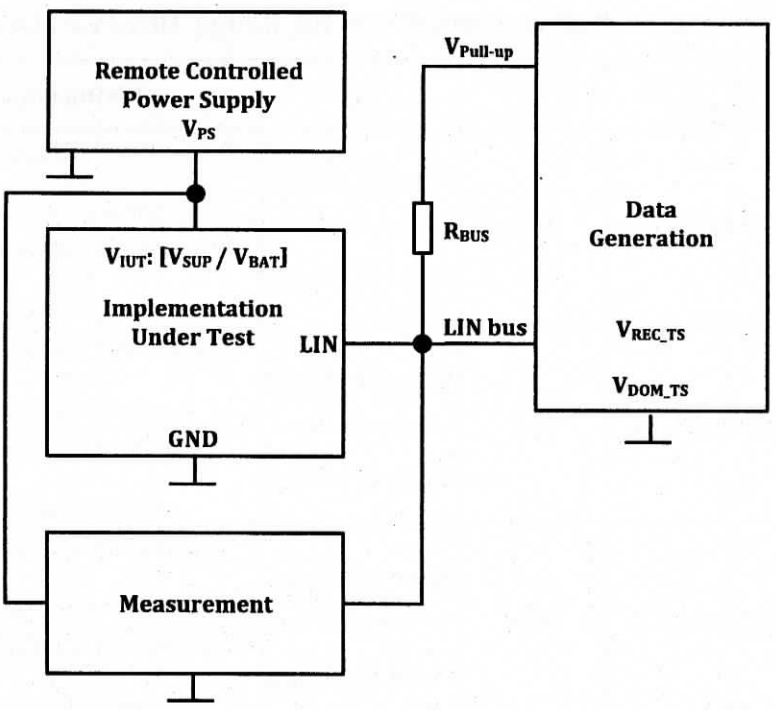

Figure 78 — Test system: Propagation delay of BR_Range_10K 24 V LIN networks at 10,417 kbit/s

Table 172 defines the test system "Propagation delay of BR_Range_10K 24 V LIN networks at 10,417 kbit/s".

Table 172 — Test system: Propagation delay of BR_Range_10K 24 V LIN networks at 10,417 kbit/s

IUT node as	Class C device as master	[EPL-CT 94].1 – [EPL-CT 94].6
	Class C device as slave	[EPL-CT 94].7 – [EPL-CT 94].12
Initial state	**Operational conditions:**	
	V_{IUT}: [V_{SUP}/V_{BAT}]	See Table 173
	V_{Dom_TS}	0 V
	V_{Rec_TS}/$V_{Pull-up}$	See Table 173
Test steps	For master IUTs and slave IUTs without making use of synchronization, a LIN communication is established between the test system and the IUT. The highest bit rate supported by the IUT (but a maximum of 10,417 kbit/s) is used. The IUT bit rate F_{IUT} is measured (master bit rate in synch field, between falling edge of start bit and bit 7; slave bit rate in data byte 1,between falling edge of start bit and bit 7, possible for values 40_{16} to $7F_{16}$). For slave IUTs with making use of synchronization, F_{IUT} is set to the nominal bit rate (e.g. 10,417 kbit/s). The test system bit rate is adjusted to F_{TS} as defined in Table 173. F_{TOL} is 2 % for master IUTs and slave IUTs without making use of synchronization, and 0,5 % for slave IUTs with making use of synchronization. The rising and falling edges of the test system data are sent delayed or in advance as defined in Table 173.	
Response	256 consecutive IUT communication cycles are successful.	
Reference	ISO 17987-4:2016, Table 19, Param 76, Param 77 ISO 17987-4:2016, Figure 5	

Table 173 defines the test cases "Propagation delay of BR_Range_10K 24 V LIN systems at 10,417 kbit/s"

Table 173 — Test cases: Propagation delay of BR_Range_10K 24 V LIN at 10,417 kbit/s

EPL-CT-TC	V_{IUT}: [V_{SUP}/ V_{BAT}]	V_{Rec_TS}/ $V_{Pull\text{-}up}$	F_{TS}	Rising edge	R_{BUS}
[EPL-CT 94].1	7,0 V/8,0 V	7,0 V	$F_{IUT} \times (1 - F_{TOL})$	Transmitted delayed by $t_{r3} + t_{f3}$; see Formula (9)	30 kΩ (0,1 %)
[EPL-CT 94].2			$F_{IUT} \times (1 + F_{TOL})$	Transmitted delayed by $t_{r4} + t_{f4}$; see Formula (10)	
[EPL-CT 94].3	24,0 V/24,6 V	24 V	$F_{IUT} \times (1 - F_{TOL})$	Transmitted delayed by $t_{r3} + t_{f3}$; see Formula (9)	
[EPL-CT 94].4			$F_{IUT} \times (1 + F_{TOL})$	Transmitted delayed by $t_{r4} + t_{f4}$; see Formula (10)	
[EPL-CT 94].5	36,0 V/36,6 V	36 V	$F_{IUT} \times (1 - F_{TOL})$	Transmitted delayed by $t_{r3} + t_{f3}$; see Formula (9)	
[EPL-CT 94].6			$F_{IUT} \times (1 + F_{TOL})$	Transmitted delayed by $t_{r4} + t_{f4}$; see Formula (10)	
[EPL-CT 94].7	7,0 V/8,0 V	7,0 V	$F_{IUT} \times (1 - F_{TOL})$	Transmitted delayed by $t_{r3} + t_{f3}$; see Formula (9)	1 kΩ (0,1 %)
[EPL-CT 94].8			$F_{IUT} \times (1 + F_{TOL})$	Transmitted delayed by $t_{r4} + t_{f4}$; see Formula (10)	
[EPL-CT 94].9	24,0 V/24,6 V	24 V	$F_{IUT} \times (1 - F_{TOL})$	Transmitted delayed by $t_{r3} + t_{f3}$; see Formula (9)	
[EPL-CT 94].10			$F_{IUT} \times (1 + F_{TOL})$	Transmitted delayed by $t_{r4} + t_{f4}$; see Formula (10)	
[EPL-CT 94].11	24,0 V/24,6 V	36 V	$F_{IUT} \times (1 - F_{TOL})$	Transmitted delayed by $t_{r3} + t_{f3}$; see Formula (9)	
[EPL-CT 94].12			$F_{IUT} \times (1 + F_{TOL})$	Transmitted delayed by $t_{r4} + t_{f4}$; see Formula (10)	

BIT 3 falling/rising edges transmitted delay:

$$t_{r3} = t_{f3} = \left| \frac{t_{BUS\_rec(min)} - t_{BIT}}{2} \right| = \left| \frac{(D_{3\_min} \times 2 \times t_{BIT}) - t_{BIT}}{2} \right| = \left| \frac{(0{,}386 \times 2 \times \frac{1}{F_{TS}}) - \frac{1}{F_{TS}}}{2} \right| \quad (9)$$

BIT 3 falling/rising edges transmitted delay:

$$t_{r4} = t_{f4} = \left| \frac{t_{BUS\_rec(min)} - t_{BIT}}{2} \right| = \left| \frac{(D_{4\_min} \times 2 \times t_{BIT}) - t_{BIT}}{2} \right| = \left| \frac{(0{,}591 \times 2 \times \frac{1}{F_{TS}}) - \frac{1}{F_{TS}}}{2} \right| \quad (10)$$

8.5.7.3 [EPL-CT 95] Propagation delay of BR_Range_20K 24 V LIN networks at 20,0 kbit/s

Figure 79 shows the test configuration of the test system "Propagation delay of a BR_Range_20K 24 V LIN Networks at 20,0 kbit/s".

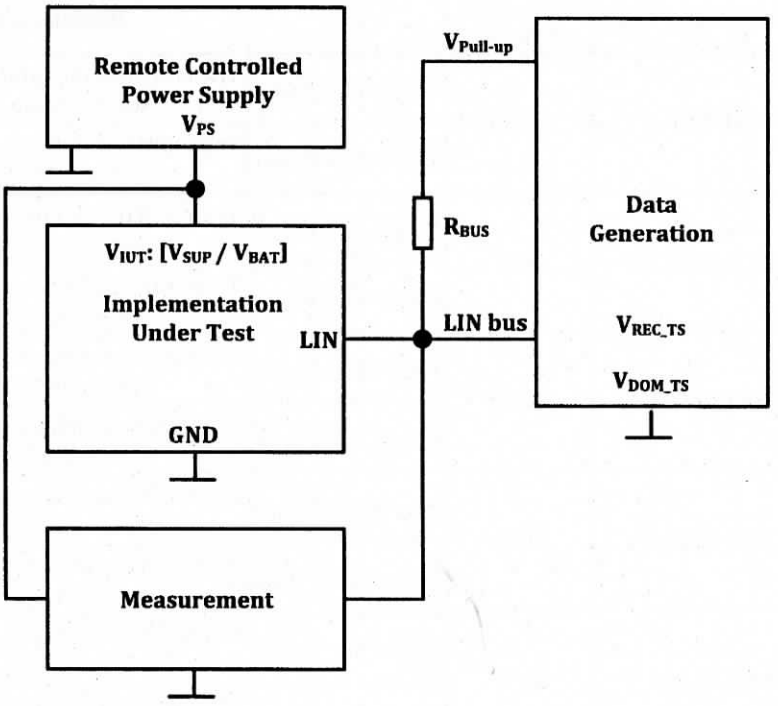

Figure 79 — Test system: Propagation delay of a BR_Range_20K 24 V LIN networks at 20,0 kbit/s

Table 174 defines the test system "Propagation delay of BR_Range_20K 24 V LIN networks at 20,0 kbit/s".

Table 174 — Test system: Propagation delay of BR_Range_20K 24 V LIN systems at 20,0kbit/s

IUT node as	Class C device as master	[EPL-CT 95].1 - [EPL-CT 95].6
	Class C device as slave	[EPL-CT 95].7 - [EPL-CT 95].12
Initial state	**Operational conditions:**	
	V_{IUT}: [V_{SUP}/V_{BAT}]	See Table 175
	V_{Dom_TS}	0 V
	V_{Rec_TS}/$V_{Pull-up}$	See Table 175
Test steps	For master IUTs and slave IUTs without making use of synchronization, a LIN communication is established between the test system and the IUT. The IUT bit rate F_{IUT} is measured (master bit rate in synch field, between falling edge of start bit and bit 7; slave bit rate in data byte 1, between falling edge of start bit and bit 7, possible for values 40_{16} to $7F_{16}$). For slave IUTs with making use of synchronization, F_{IUT} is set to the nominal bit rate (i.e. 19,2 kbit/s). The test system bit rate is adjusted to F_{TS} as defined in Table 175. F_{TOL} is 2 % for master IUTs and slave IUTs without making use of synchronization, and 0,5 % for slave IUTs with making use of synchronization. The rising and falling edges of the test system data are sent delayed or in advance as defined in Table 175.	
Response	256 consecutive communication cycles are successful.	
Reference	ISO 17987-4:2016, Table 19, Param 76, Param 77 ISO 17987-4:2016, Figure 5	

Table 175 defines the test cases "Propagation delay of BR_Range_20K 24 V LIN networks at 20,0 kbit/s".

Table 175 — Test cases: Propagation delay of BR_Range_20K 24 V LIN networks at 20,0 kbit/s

EPL-CT-TC	V_{IUT}: [V_{SUP}/V_{BAT}]	V_{Rec_TS}/ $V_{Pull\text{-}up}$	F_{TS}	Rising edge	R_{BUS}
[EPL-CT 95].1	15,0 V/16,0 V	15,0 V	$F_{IUT} \times (1 - F_{TOL})$	Transmitted delayed by $t_{r1} + t_{f1}$; see Formula (11)	30 kΩ (0,1 %)
[EPL-CT 95].2			$F_{IUT} \times (1 + F_{TOL})$	Transmitted delayed by $t_{r2} + t_{f2}$; see Formula (12)	
[EPL-CT 95].3	24,0 V/24,6 V	24 V	$F_{IUT} \times (1 - F_{TOL})$	Transmitted delayed by $t_{r1} + t_{f1}$; see Formula (11)	
[EPL-CT 95].4			$F_{IUT} \times (1 + F_{TOL})$	Transmitted delayed by $t_{r2} + t_{f2}$; see Formula (12)	
[EPL-CT 95].5	36,0 V/36,6 V	36 V	$F_{IUT} \times (1 - F_{TOL})$	Transmitted delayed by $t_{r1} + t_{f1}$; see Formula (11)	
[EPL-CT 95].6			$F_{IUT} \times (1 + F_{TOL})$	Transmitted delayed by $t_{r2} + t_{f2}$; see Formula (12)	
[EPL-CT 95].7	15,0 V/16,0 V	15,0 V	$F_{IUT} \times (1 - F_{TOL})$	Transmitted delayed by $t_{r1} + t_{f1}$; see Formula (11)	1 kΩ (0,1 %)
[EPL-CT 95].8			$F_{IUT} \times (1 + F_{TOL})$	Transmitted delayed by $t_{r2} + t_{f2}$; see Formula (12)	
[EPL-CT 95].9	24,0 V/24,6 V	24 V	$F_{IUT} \times (1 - F_{TOL})$	Transmitted delayed by $t_{r1} + t_{f1}$; see Formula (11)	
[EPL-CT 95].10			$F_{IUT} \times (1 + F_{TOL})$	Transmitted delayed by $t_{r2} + t_{f2}$; see Formula (12)	
[EPL-CT 95].11	36,0 V/36,6 V	36 V	$F_{IUT} \times (1 - F_{TOL})$	Transmitted delayed by $t_{r1} + t_{f1}$; see Formula (11)	
[EPL-CT 95].12			$F_{IUT} \times (1 + F_{TOL})$	Transmitted delayed by $t_{r2} + t_{f2}$ see Formula (12)	

BIT 1 falling/rising edges transmitted delay:

$$t_{r1} = t_{f1} = \left| \frac{t_{BUS\_rec(min)} - t_{BIT}}{2} \right| = \left| \frac{(D_{1\_min} \times 2 \times t_{BIT}) - t_{BIT}}{2} \right| = \left| \frac{(0,330 \times 2 \times \frac{1}{F_{TS}}) - \frac{1}{F_{TS}}}{2} \right| \quad (11)$$

BIT 2 falling/rising edges transmitted delay:

$$t_{r2} = t_{f2} = \left| \frac{t_{BUS\_rec(min)} - t_{BIT}}{2} \right| = \left| \frac{(D_{2\_min} \times 2 \times t_{BIT}) - t_{BIT}}{2} \right| = \left| \frac{(0,642 \times 2 \times \frac{1}{F_{TS}}) - \frac{1}{F_{TS}}}{2} \right| \quad (12)$$

8.5.8 Supply voltage offset

8.5.8.1 Purpose

The purpose of this test is to check the robustness in case of V_{BAT} and Ground shift.

8.5.8.2 GND/V_{BAT} shift test — Dynamic

Figure 80 shows the test configuration of the test system "GND/V_{BAT} shift test — Dynamic".

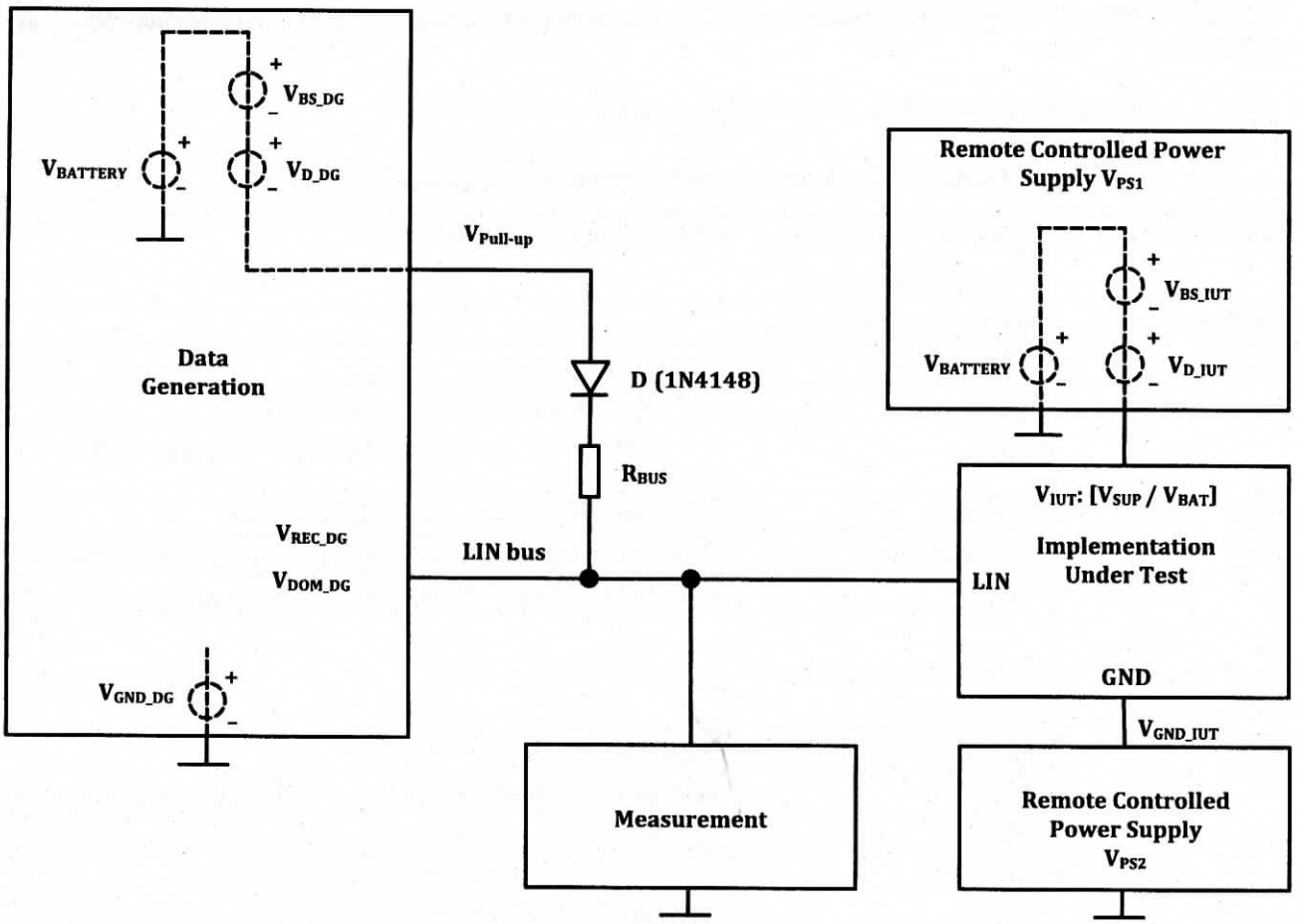

Figure 80 — Test system: GND/V_{BAT} shift test — Dynamic

8.5.8.3 [EPL-CT 96] IUT GND shift test — Dynamic for BR_Range_20K 24 V LIN networks — at 20kbit/s

Table 176 defines the test system of "GND shift is applied to the IUT".

Table 176 — Test system: GND shift is applied to the IUT"

IUT node as	Class C device as master Class C device as slave	[EPL-CT 96].1 – [EPL-CT 96].4
Initial state	**Operational conditions:**	
	$V_{BATTERY}$	See Table 177
	V_{BS_DG}	0,1 × $V_{BATTERY}$ [part of $V_{REC\_DG}/V_{Pull\text{-}up}$]
	V_{D_DG}	1 V [part of $V_{REC\_DG}/V_{Pull\text{-}up}$] (use 0 V if D_{Rev_Batt} is implemented)
	V_{GND_DG}	0,03 × $V_{BATTERY}$ [part of $V_{REC\_DG}/V_{Pull\text{-}up}$]
	$V_{REC\_DG}/V_{Pull\text{-}up}$	0,710 × ($V_{BATTERY}$ – V_{D_DG} – V_{BS_DG} – V_{GND_DG}); see Figure 80
	V_{DOM_DG}	0,302 × ($V_{BATTERY}$ – V_{D_DG} – V_{BS_DG} – V_{GND_DG}); see Figure 80
	Test system slew rate	$1,67 \times \frac{V_{REC\_DG}}{t_{BIT}}$
	V_{BS_IUT}	0,03 × $V_{BATTERY}$ [part of V_{IUT}]
	V_{D_IUT}	See Table 177 [part of V_{IUT}] (use 0 V if D_{Rev_Batt} is implemented)
	V_{IUT}	$V_{BATTERY}$ – V_{BS_IUT} – V_{D_IUT} – V_{GND_IUT}; see Figure 80]
	V_{GND_IUT}	[0,5 × sin(2 × π × 5 × t) + 0,5] × 0,1 × $V_{BATTERY}$ 5 Hz sinus signal with offset, [part of V_{IUT}] see Figure 80
Test steps	For master IUTs and slave IUTs without making use of synchronization, a LIN communication is established between the test system and the IUT. The IUT bit rate F_{IUT} is measured (master bit rate in synch field, between falling edge of start bit and bit 7; slave bit rate in data byte 1, between falling edge of start bit and bit 7, possible for values 40_{16} to $7F_{16}$). For slave IUTs with making use of synchronization, F_{IUT} is set to the nominal bit rate (i.e. 19,2 kbit/s). The test system bit rate is adjusted to F_{TS} as defined in Table 177. F_{TOL} is 2 % for master IUTs and slave IUTs without making use of synchronization, and 0,5 % for slave IUTs with making use of synchronization.	
Response	256 consecutive IUT communication cycles shall be successful.	
Reference	ISO 17987-4:2016, Table 15, Param 67, Param 68 ISO 17987-4:2016, Figure 5	

Table 177 defines the test cases of "GND shift is applied to the IUT".

Table 177 — Test cases: GND shift is applied to the IUT

EPL-CT-TC	F_{TS}	$V_{BATTERY}$	IUT node as	V_{D_IUT}	R_{BUS}
[EPL-CT 96].1	$F_{IUT} \times (1 - F_{TOL})$	18,4 V	Class C device as master	0,4 V	30 kΩ
			Class C device as slave		1 kΩ
[EPL-CT 96].2	$F_{IUT} \times (1 + F_{TOL})$		Class C device as master		30 kΩ
			Class C device as slave		1 kΩ
[EPL-CT 96].3	$F_{IUT} \times (1 - F_{TOL})$	41,4 V	Class C device as master		30 kΩ
			Class C device as slave		1 kΩ
[EPL-CT 96].4	$F_{IUT} \times (1 + F_{TOL})$		Class C device as master		30 kΩ
			Class C device as slave		1 kΩ

8.5.8.4 [EPL-CT 97] Test System GND shift test for BR_Range_20K 24 V LIN networks — Dynamic — at 20 kbit/s

Table 178 defines the test system of "GND shift is applied to the test system".

Table 178 — Test system: GND shift is applied to the test system

IUT node as	Class C device as master Class C device as slave	[EPL-CT 97].1 – [EPL-CT 97].4
Initial state	**Operational conditions:**	
	$V_{BATTERY}$	See Table 179
	V_{BS_DG}	$0,03 \times V_{BATTERY}$ [part of $V_{REC\_DG}/V_{Pull\text{-}up}$]
	V_{D_DG}	0,4 V [part of $V_{REC\_DG}/V_{Pull\text{-}up}$] (use 0 V if D_{Rev_Batt} is implemented)
	V_{GND_DG}	$[0,5 \times \sin(2 \times \pi \times 5 \times t) + 0,5] \times 0,1 \times V_{BAT}$ [part of $V_{REC\_DG}/V_{Pull\text{-}up}$]
	$V_{REC\_DG}/V_{Pull\text{-}up}$	$0,710 \times (V_{BATTERY} - V_{D\_DG} - V_{BS\_DG} - V_{GND\_DG})$; see Figure 80
	V_{DOM_DG}	$0,302 \times (V_{BATTERY} - V_{D\_DG} - V_{BS\_DG} - V_{GND\_DG})$; see Figure 80
	Test system slew rate	$1,67 \times \frac{V_{REC\_DG}}{t_{BIT}}$
	V_{BS_IUT}	$0,1 \times V_{BATTERY}$ [part of V_{IUT}]
	V_{D_IUT}	See Table 179 [part of V_{IUT}] (use 0 V if D_{Rev_Batt} is implemented)
	V_{IUT}	$V_{BATTERY} - V_{BS\_IUT} - V_{D\_IUT}$; see Figure 80
	V_{Gnd_IUT}	$0,03 \times V_{BATTERY}$; see Figure 80

Table 178 *(continued)*

Test steps	For master IUTs and slave IUTs without making use of synchronization, a LIN communication is established between the test system and the IUT. The IUT bit rate F_{IUT} is measured (master bit rate in synch field, between falling edge of start bit and bit 7; slave bit rate in data byte 1, between falling edge of start bit and bit 7, possible for values 40_{16} to $7F_{16}$). For slave IUTs with making use of synchronization, F_{IUT} is set to the nominal bit rate (i.e. 19,2 kbit/s). The test system bit rate is adjusted to F_{TS} as defined in Table 179. F_{TOL} is 2 % for master IUTs and slave IUTs without making use of synchronization, and 0,5 % for slave IUTs with making use of synchronization.
Response	256 consecutive IUT communication cycles shall be successful.
Reference	ISO 17987-4:2016, Table 15, Param 67, Param 68 ISO 17987-4:2016, Figure 5

Table 179 defines the test cases of "GND shift is applied to the test system".

Table 179 — Test cases: GND shift is applied to the test system

EPL-CT-TC	F_{TS}	$V_{BATTERY}$	IUT node as	V_{D_IUT}	R_{BUS}
[EPL-CT 97].1	$F_{IUT} \times (1 - F_{TOL})$	18,4 V	Class C device as master	1 V	30 kΩ
			Class C device as slave		1 kΩ
[EPL-CT 97].2	$F_{IUT} \times (1 + F_{TOL})$		Class C device as master		30 kΩ
			Class C device as slave		1 kΩ
[EPL-CT 97].3	$F_{IUT} \times (1 - F_{TOL})$	41,4 V	Class C device as master		30 kΩ
			Class C device as slave		1 kΩ
[EPL-CT 97].4	$F_{IUT} \times (1 + F_{TOL})$		Class C device as master		30 kΩ
			Class C device as slave		1 kΩ

8.5.8.5 [EPL-CT 98] IUT V_{BAT} shift test for BR_Range_20K 24 V LIN networks — Dynamic — at 20 kbit/s

Table 180 defines the test system of "V_{BAT} shift is applied the IUT".

Table 180 — Test system: V_{BAT} shift is applied the IUT

IUT node as	Class C device as master Class C device as slave	[EPL-CT 98].1, [EPL-CT 98].2, [EPL-CT 98].3, [EPL-CT 98].4
Initial state	**Operational conditions:**	
	$V_{BATTERY}$	See Table 181
	V_{BS_DG}	$[0,5 \times \sin(2 \times \pi \times 5 \times t) + 0,5] \times 0,1 \times V_{BATTERY}$ (5 Hz sinus signal with offset [part of $V_{REC\_DG}/V_{Pull\text{-}up}$]
	V_{D_DG}	1 V [part of $V_{REC\_DG}/V_{Pull\text{-}up}$] (use 0 V if D_{Rev_Batt} is implemented)
	V_{GND_DG}	$0,03 \times V_{BATTERY}$ [part of $V_{REC\_DG}/V_{Pull\text{-}up}$]
	$V_{REC\_DG}/V_{Pull\text{-}up}$	$0,710 \times (V_{BATTERY} - V_{D\_DG} - V_{BS\_DG} - V_{GND\_DG})$; see Figure 80
	V_{DOM_DG}	$0,302 \times (V_{BATTERY} - V_{D\_DG} - V_{BS\_DG} - V_{GND\_DG})$; see Figure 80
	Test system slew rate	$1,67 \times \frac{V_{REC\_DG}}{t_{BIT}}$
	V_{BS_IUT}	$0,03 \times V_{BATTERY}$ [part of V_{IUT}]
	V_{D_IUT}	See Table 181 [part of V_{IUT}] (use 0 V if D_{Rev_Batt} is implemented)
	V_{IUT}	$V_{BATTERY} - V_{BS\_IUT} - V_{D\_IUT}$; see Figure 80
	V_{GND_IUT}	$0,1 \times V_{BATTERY}$; see Figure 80
Test steps	For master IUTs and slave IUTs without making use of synchronization, a LIN communication is established between the test system and the IUT. The IUT bit rate F_{IUT} is measured (master bit rate in synch field, between falling edge of start bit and bit 7; slave bit rate in data byte 1, between falling edge of start bit and bit 7, possible for values 40_{16} to $7F_{16}$). For slave IUTs with making use of synchronization, F_{IUT} is set to the nominal bit rate (i.e. 19,2 kbit/s). The test system bit rate is adjusted to F_{TS} as defined in Table 181. F_{TOL} is 2 % for master IUTs and slave IUTs without making use of synchronization, and 0,5 % for slave IUTs with making use of synchronization.	
Response	256 consecutive IUT communication cycles shall be successful.	
Reference	ISO 17987-4:2016, Table 15, Param 67, Param 68 ISO 17987-4:2016, Figure 5	

Table 181 defines the test cases of "V_{BAT} shift is applied the IUT".

Table 181 — Test cases: V_{BAT} shift is applied the IUT

EPL-CT-TC	F_{TS}	$V_{BATTERY}$	IUT node as	V_{D_IUT}	R_{BUS}
[EPL-CT 98].1	$F_{IUT} \times (1 - F_{TOL})$	18,4 V	Class C device as master	0,4 V	30 kΩ
			Class C device as slave		1 kΩ
[EPL-CT 98].2	$F_{IUT} \times (1 + F_{TOL})$		Class C device as master		30 kΩ
			Class C device as slave		1 kΩ
[EPL-CT 98].3	$F_{IUT} \times (1 - F_{TOL})$	41,4 V	Class C device as master		30 kΩ
			Class C device as slave		1 kΩ
[EPL-CT 98].4	$F_{IUT} \times (1 + F_{TOL})$		Class C device as master		30 kΩ
			Class C device as slave		1 kΩ

8.5.8.6 [EPL-CT 99] Test System V_{BAT} shift test for BR_Range_20K 24 V LIN networks — Dynamic — at 20 kbit/s

Table 182 defines the test system of "V_{BAT} shift is applied the test system".

Table 182 — Test system: V_{BAT} shift is applied the test system

IUT node as	Class C device as master Class C device as slave	[EPL-CT 99].1, [EPL-CT 99].2, [EPL-CT 99].3, [EPL-CT 99].4
Initial state	**Operational conditions:**	
	$V_{BATTERY}$	See Table 183
	V_{BS_DG}	0,03 × $V_{BATTERY}$ [part of $V_{REC\_DG}/V_{Pull\text{-}up}$]
	V_{D_DG}	0,4 V [part of $V_{REC\_DG}/V_{Pull\text{-}up}$] (use 0 V if D_{Rev_Batt} is implemented)
	V_{GND_DG}	0,1 × $V_{BATTERY}$ [part of $V_{REC\_DG}/V_{Pull\text{-}up}$]
	$V_{REC\_DG}/V_{Pull\text{-}up}$	0,710 × ($V_{BATTERY}$ – V_{D_DG} – V_{BS_DG} – V_{GND_DG}); see Figure 80
	V_{DOM_DG}	0,302 × ($V_{BATTERY}$ – V_{D_DG} – V_{BS_DG} – V_{GND_DG}); see Figure 80
	Test system slew rate	$1,67 \times \frac{V_{REC\_DG}}{t_{BIT}}$
	V_{BS_IUT}	[0,5 × sin(2 × π × 5 × t) + 0,5] × 0,1 × $V_{BATTERY}$ 5 Hz sinus signal with offset [part of V_{IUT}]
	V_{D_IUT}	See Table 183 [part of V_{IUT}] (use 0 V if D_{Rev_Batt} is implemented)
	V_{IUT}	$V_{BATTERY}$ – V_{BS_IUT} – V_{D_IUT} – V_{GND_IUT}; see Figure 80
	V_{GND_IUT}	0,03 × $V_{BATTERY}$; see Figure 80
Test steps	For master IUTs and slave IUTs without making use of synchronization, a LIN communication is established between the test system and the IUT. The IUT bit rate F_{IUT} is measured (master bit rate in synch field, between falling edge of start bit and bit 7; slave bit rate in data byte 1, between falling edge of start bit and bit 7, possible for values 40_{16} to $7F_{16}$). For slave IUTs with making use of synchronization, F_{IUT} is set to the nominal bit rate (i.e. 19,2 kbit/s). The test system bit rate is adjusted to F_{TS} as defined in Table 183. F_{TOL} is 2 % for master IUTs and slave IUTs without making use of synchronization, and 0,5 % for slave IUTs with making use of synchronization.	
Response	256 consecutive IUT communication cycles shall be successful.	
Reference	ISO 17987-4:2016, Table 15, Param 67, Param 68 ISO 17987-4:2016, Figure 5	

Table 183 defines the test cases of "V_{BAT} shift is applied the test system".

Table 183 — Test cases: V_{BAT} shift is applied the test system

EPL-CT-TC	F_{TS}	$V_{BATTERY}$	IUT node as	V_{D_IUT}	R_{BUS}
[EPL-CT 99].1	$F_{IUT} \times (1 - F_{TOL})$	18,4 V	Class C device as master	1 V	30 kΩ
			Class C device as slave		1 kΩ
[EPL-CT 99].2	$F_{IUT} \times (1 + F_{TOL})$		Class C device as master		30 kΩ
			Class C device as slave		1 kΩ
[EPL-CT 99].3	$F_{IUT} \times (1 - F_{TOL})$	41,4 V	Class C device as master		30 kΩ
			Class C device as slave		1 kΩ
[EPL-CT 99].4	$F_{IUT} \times (1 + F_{TOL})$		Class C device as master		30 kΩ
			Class C device as slave		1 kΩ

8.5.8.7 [EPL-CT 100] IUT GND shift test for BR_Range_10K 24 V LIN networks — Dynamic — at 10,417 kbit/s

Table 184 defines the test system of "GND shift is applied to the IUT".

Table 184 — Test system: GND shift is applied to the IUT

IUT node as	Class C device as master Class C device as slave	[EPL-CT 100].1, [EPL-CT 100].2, [EPL-CT 100].3, [EPL-CT 100].4
Initial state	**Operational conditions:**	
	$V_{BATTERY}$	See Table 185
	V_{BS_DG}	0,1 × $V_{BATTERY}$ [part of $V_{REC\_DG}/V_{Pull\text{-}up}$]
	V_{D_DG}	1 V [part of $V_{REC\_DG}/V_{Pull\text{-}up}$] (use 0 V if D_{Rev_Batt} is implemented)
	V_{GND_DG}	0 V
	$V_{REC\_DG}/V_{Pull\text{-}up}$	0,744 × ($V_{BATTERY}$ – V_{D_DG} – V_{BS_DG} – V_{GND_DG}); see Figure 80
	V_{DOM_DG}	0,284 × ($V_{BATTERY}$ – V_{D_DG} – V_{BS_DG} – V_{GND_DG}); see Figure 80
	Test system slew rate	$2,18 \times \frac{V_{REC\_DG}}{t_{BIT}}$
	V_{BS_IUT}	0 V, [part of V_{IUT}] see Figure 80
	V_{D_IUT}	See Table 185 [part of V_{IUT}] (use 0 V if D_{Rev_Batt} is implemented)
	V_{IUT}	$V_{BAT} - V_{BS\_IUT} - V_{D\_IUT} - V_{GND\_IUT}$; see Figure 80
	V_{GND_IUT}	(0,5 × sin(2 × π × 5 × t) + 0,5) × 0,1 × $V_{BATTERY}$ 5 Hz sinus signal with offset, [part of V_{IUT}]see Figure 80

Table 184 *(continued)*

Test steps	For master IUTs and slave IUTs without making use of synchronization, a LIN communication is established between the test system and the IUT. The highest bit rate supported by the IUT (but a maximum of 10,417 kbit/s) is used. The IUT bit rate F_{IUT} is measured (master bit rate in synch field, between falling edge of start bit and bit 7; slave bit rate in data byte 1, between falling edge of start bit and bit 7, possible for values 40_{16} to $7F_{16}$). For slave IUTs with making use of synchronization, F_{IUT} is set to the nominal bit rate (i.e. 19,2 kbit/s). The test system bit rate is adjusted to F_{TS} as defined in Table 185. F_{TOL} is 2 % for master IUTs and slave IUTs without making use of synchronization, and 0,5 % for slave IUTs with making use of synchronization.
Response	256 consecutive IUT communication cycles shall be successful.
Reference	ISO 17987-4:2016, Table 15, Param 67, Param 68 ISO 17987-4:2016, Figure 5

Table 185 defines the test cases of "GND shift is applied to the IUT".

Table 185 — Test cases: GND shift is applied to the IUT

EPL-CT-TC	F_{TS}	$V_{BATTERY}$	IUT node as	V_{D_IUT}	R_{BUS}
[EPL-CT 100].1	$F_{IUT} \times (1 - F_{TOL})$	9,2 V	Class C device as master	0,4 V	30 kΩ
			Class C device as slave		1 kΩ
[EPL-CT 100].2	$F_{IUT} \times (1 + F_{TOL})$		Class C device as master		30 kΩ
			Class C device as slave		1 kΩ
[EPL-CT 100].3	$F_{IUT} \times (1 - F_{TOL})$	41,4 V	Class C device as master		30 kΩ
			Class C device as slave		1 kΩ
[EPL-CT 100].4	$F_{IUT} \times (1 + F_{TOL})$		Class C device as master		30 kΩ
			Class C device as slave		1 kΩ

8.5.8.8 [EPL-CT 101] Test System GND shift test for 24 V LIN networks — Dynamic — at 10,417 kbit/s

Table 186 defines the test system of "GND shift is applied to the test system".

Table 186 — Test system: GND shift is applied to the test system

IUT node as	Class C device as master Class C device as slave	[EPL-CT 101].1, [EPL-CT 101].2, [EPL-CT 101].3, [EPL-CT 101].4
Initial state	**Operational conditions:**	
	$V_{BATTERY}$	See Table 187
	V_{BS_DG}	0 V
	V_{D_DG}	0,4 V [part of $V_{REC\_DG}/V_{Pull\text{-}up}$] (use 0 V if D_{Rev_Batt} is implemented)
	V_{GND_DG}	$[0,5 \times \sin(2 \times \pi \times 5 \times t) + 0,5] \times 0,1 \times V_{BATTERY}$ [part of $V_{REC\_DG}/V_{Pull\text{-}up}$]
	$V_{REC\_DG}/V_{Pull\text{-}up}$	$0,744 \times (V_{BATTERY} - V_{D\_DG} - V_{BS\_DG} - V_{GND\_DG})$; see Figure 80
	V_{DOM_DG}	$0,284 \times (V_{BATTERY} - V_{D\_DG} - V_{BS\_DG} - V_{GND\_DG})$, [part of $V_{REC\_DG}/V_{Pull\text{-}up}$]; see Figure 80
	Test system slew rate	$2,18 \times \frac{V_{REC\_DG}}{t_{BIT}}$
	V_{BS_IUT}	$0,1 \times V_{BATTERY}$ [part of V_{IUT}]
	V_{D_IUT}	See Table 187 [part of V_{IUT}] (use 0 V if D_{Rev_Batt} is implemented)
	V_{IUT}	$V_{BATTERY} - V_{BS\_IUT} - V_{D\_IUT} - V_{GND\_IUT}$; see Figure 80
	V_{GND_IUT}	0 V [part of V_{IUT}]; see Figure 80
Test steps	For master IUTs and slave IUTs without making use of synchronization, a LIN communication is established between the test system and the IUT. The highest bit rate supported by the IUT (but a maximum of 10,417 kbit/s) is used. The IUT bit rate F_{IUT} is measured (master bit rate in synch field, between falling edge of start bit and bit 7; slave bit rate in data byte 1, between falling edge of start bit and bit 7, possible for values 40_{16} to $7F_{16}$). For slave IUTs with making use of synchronization, F_{IUT} is set to the nominal bit rate (i.e. 19,2 kbit/s). The test system bit rate is adjusted to F_{TS} as defined in Table 187. F_{TOL} is 2 % for master IUTs and slave IUTs without making use of synchronization, and 0,5 % for slave IUTs with making use of synchronization.	
Response	256 consecutive IUT communication cycles shall be successful.	
Reference	ISO 17987-4:2016, Table 15, Param 67, Param 68 ISO 17987-4:2016, Figure 5	

Table 187 defines the test cases of "GND shift is applied to the test system".

Table 187 — Test cases of: GND shift is applied to the test system

EPL-CT-TC	F_{TS}	$V_{BATTERY}$	IUT node as	V_{D_IUT}	R_{BUS}
[EPL-CT 101].1	$F_{IUT} \times (1 - F_{TOL})$	9,2 V	Class C device as master	1 V	30 kΩ
			Class C device as slave		1 kΩ
[EPL-CT 101].2	$F_{IUT} \times (1 + F_{TOL})$		Class C device as master		30 kΩ
			Class C device as slave		1 kΩ
[EPL-CT 101].3	$F_{IUT} \times (1 - F_{TOL})$	41,4 V	Class C device as master		30 kΩ
			Class C device as slave		1 kΩ
[EPL-CT 101].4	$F_{IUT} \times (1 + F_{TOL})$		Class C device as master		30 kΩ
			Class C device as slave		1 kΩ

8.5.8.9 [EPL-CT 102] IUT V_{BAT} shift test for BR_Range_10K 24 V LIN networks — Dynamic — at 10,417 kbit/s

Table 188 defines the test system of "V_{BAT} shift is applied the IUT".

Table 188 — Test system: V_{BAT} shift is applied the IUT

IUT node as	Class C device as master Class C device as slave	[EPL-CT 102].1, [EPL-CT 102].2, [EPL-CT 102].3, [EPL-CT 102].4
Initial state	**Operational conditions:**	
	$V_{BATTERY}$	See Table 189
	V_{BS_DG}	[0,5 × sin(2 × π × 5 × t) + 0,5] × 0,1 × $V_{BATTERY}$ (5 Hz sinus signal with offset) [part of $V_{REC\_DG}/V_{Pull\text{-}up}$]
	V_{D_DG}	1 V [part of $V_{REC\_DG}/V_{Pull\text{-}up}$] (use 0 V if D_{Rev_Batt} is implemented)
	V_{GND_DG}	0 V [part of $V_{REC\_DG}/V_{Pull\text{-}up}$]
	$V_{REC\_DG}/V_{Pull\text{-}up}$	0,744 × ($V_{BATTERY}$ − V_{D_DG} − V_{BS_DG} − V_{GND_DG}); see Figure 80
	V_{DOM_DG}	0,284 × ($V_{BATTERY}$ − V_{D_DG} − V_{BS_DG} − V_{GND_DG}); see Figure 80
	Test system slew rate	$2,18 \times \frac{V_{REC\_DG}}{t_{BIT}}$
	V_{BS_IUT}	0 V [part of V_{IUT}]
	V_{D_IUT}	See Table 189 [part of V_{IUT}] (use 0 V if D_{Rev_Batt} is implemented)
	V_{IUT}	$V_{BATTERY}$ − V_{BS_IUT} − V_{D_IUT} − V_{GND_IUT}; see Figure 80
	V_{GND_IUT}	0,1 × $V_{BATTERY}$; see Figure 80

Table 188 *(continued)*

Test steps	For master IUTs and slave IUTs without making use of synchronization, a LIN communication is established between the test system and the IUT. The highest bit rate supported by the IUT (but a maximum of 10,417 kbit/s) is used. The IUT bit rate F_{IUT} is measured (master bit rate in synch field, between falling edge of start bit and bit 7; slave bit rate in data byte 1, between falling edge of start bit and bit 7, possible for values 40_{16} to $7F_{16}$). For slave IUTs with making use of synchronization, F_{IUT} is set to the nominal bit rate (i.e. 19,2 kbit/s). The test system bit rate is adjusted to F_{TS} as defined in Table 189. F_{TOL} is 2 % for master IUTs and slave IUTs without making use of synchronization, and 0,5 % for slave IUTs with making use of synchronization.
Response	256 consecutive IUT communication cycles shall be successful.
Reference	ISO 17987-4:2016, Table 15, Param 67, Param 68 ISO 17987-4:2016, Figure 5

Table 189 defines the test cases of "V_{BAT} shift is applied the IUT".

Table 189 — Test cases of: V_{BAT} shift is applied the IUT

EPL-CT-TC	F_{TS}	$V_{BATTERY}$	IUT node as	V_{D_IUT}	R_{BUS}
[EPL-CT 102].1	$F_{IUT} \times (1 - F_{TOL})$	9,2 V	Class C device as master	0,4 V	30 kΩ
			Class C device as slave		1 kΩ
[EPL-CT 102].2	$F_{IUT} \times (1 + F_{TOL})$		Class C device as master		30 kΩ
			Class C device as slave		1 kΩ
[EPL-CT 102].3	$F_{IUT} \times (1 - F_{TOL})$	41,4 V	Class C device as master		30 kΩ
			Class C device as slave		1 kΩ
[EPL-CT 102].4	$F_{IUT} \times (1 + F_{TOL})$		Class C device as master		30 kΩ
			Class C device as slave		1 kΩ

8.5.8.10 [EPL-CT 103] Test System V_{BAT} shift test for BR_Range_10K LIN networks — Dynamic — at 10,417 kbit/s

Table 190 defines the test system of "V_{BAT} shift is applied to the test system".

Table 190 — Test system: V_{BAT} shift is applied to the test system

IUT node as	Class C device as master Class C device as slave	[EPL-CT 103].1, [EPL-CT 103].2, [EPL-CT 103].3, [EPL-CT 103].4
Initial state	**Operational conditions:**	
	$V_{BATTERY}$	See Table 191
	V_{BS_DG}	0 V [part of $V_{REC\_DG}/V_{Pull\text{-}up}$]
	V_{D_DG}	0,4 V [part of $V_{REC\_DG}/V_{Pull\text{-}up}$] (use 0 V if D_{Rev_Batt} is implemented)
	V_{GND_DG}	0,1 × $V_{BATTERY}$, [part of $V_{REC\_DG}/V_{Pull\text{-}up}$]
	$V_{REC\_DG}/V_{Pull\text{-}up}$	0,744 × ($V_{BATTERY}$ – V_{D_DG} – V_{BS_DG} – V_{GND_DG}); see Figure 80
	V_{DOM_DG}	0,284 × ($V_{BATTERY}$ – V_{D_DG} – V_{BS_DG} – V_{GND_DG}); see Figure 80
	Test system slew rate	$2,18 \times \frac{V_{REC\_DG}}{t_{BIT}}$
	V_{BS_IUT}	[0,5 × sin(2 × π × 5 × t) + 0,5] × 0,1 × $V_{BATTERY}$ (5 Hz sinus signal with offset) [part of V_{IUT}]
	V_{D_IUT}	See Table 191 [part of V_{IUT}] (use 0 V if D_{Rev_Batt} is implemented)
	V_{IUT}	$V_{BATTERY}$ – V_{BS_IUT} – V_{D_IUT} – V_{GND_IUT}; see Figure 80
	V_{Gnd_IUT}	0 V [part of V_{IUT}]; see Figure 80
Test steps	For master IUTs and slave IUTs without making use of synchronization, a LIN communication is established between the test system and the IUT. The highest bit rate supported by the IUT (but a maximum of 10,417 kbit/s) is used. The IUT bit rate F_{IUT} is measured (master bit rate in synch field, between falling edge of start bit and bit 7; slave bit rate in data byte 1, between falling edge of start bit and bit 7, possible for values 40_{16} to $7F_{16}$). For slave IUTs with making use of synchronization, F_{IUT} is set to the nominal bit rate (i.e. 19,2 kbit/s). The test system bit rate is adjusted to F_{TS} as defined in Table 191. F_{TOL} is 2 % for master IUTs and slave IUTs without making use of synchronization, and 0,5 % for slave IUTs with making use of synchronization.	
Response	256 consecutive IUT communication cycles shall be successful.	
Reference	ISO 17987-4:2016, Table 15, Param 67, Param 68 ISO 17987-4:2016, Figure 5	

Table 191 defines the test cases of "V_{BAT} shift is applied to the test system".

Table 191 — Test cases of V_{BAT} shift is applied to the test system

EPL-CT-TC	F_{TS}	$V_{BATTERY}$	**IUT node as**	V_{D_IUT}	R_{BUS}
[EPL-CT 103].1	F_{IUT} × (1 – F_{TOL})	9,2 V	Class C device as master	1 V	30 kΩ
			Class C device as slave		1 kΩ
[EPL-CT 103].2	F_{IUT} × (1 + F_{TOL})		Class C device as master		30 kΩ
			Class C device as slave		1 kΩ
[EPL-CT 103].3	F_{IUT} × (1 – F_{TOL})	41,4 V	Class C device as master		30 kΩ
			Class C device as slave		1 kΩ
[EPL-CT 103].4	F_{IUT} × (1 + F_{TOL})		Class C device as master		30 kΩ
			Class C device as slave		1 kΩ

8.5.9 Failure

8.5.9.1 Purpose

The purpose of this test is to check whether some parasitic reverse currents are flowing into the IUT.

8.5.9.2 [EPL–CT 104] Loss of battery

Figure 81 shows the test configuration of the test system "Loss of battery".

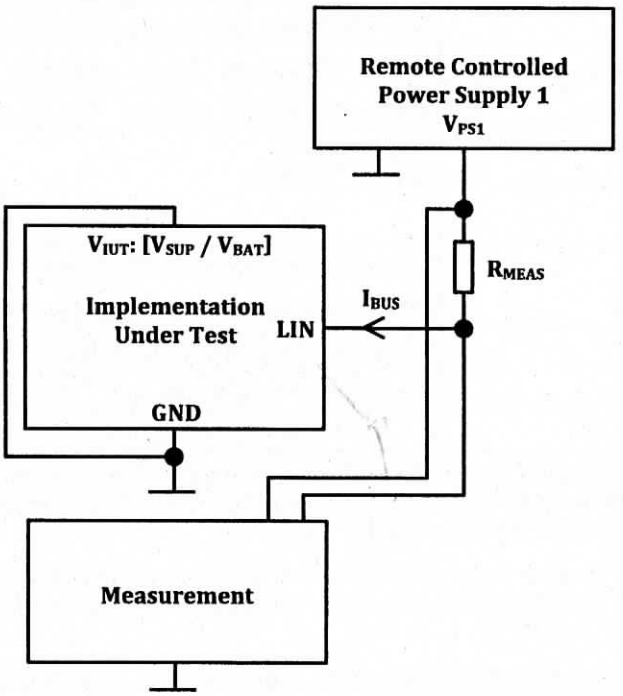

Figure 81 — Test system: Loss of battery

Table 192 defines the test system "Loss of battery".

Table 192 — Test system: Loss of battery

IUT node as	Class C device as master Class C device as slave	[EPL–CT 104].1
Initial state	**Parameters:**	
	R_{MEAS}	10 kΩ (0,1 %)
	Operational conditions:	
	V_{IUT}: [V_{SUP}/V_{BAT}] = GND Failure 0 < V_{PS1} < 36 V	Loss of battery

Table 192 *(continued)*

IUT node as	Class C device as master Class C device as slave	[EPL-CT 104].1
Test steps	The power supply is disconnected from the IUT V_{IUT} PIN. V_{PS1} = Signal with a 2 V/s ramp in the range [0 V to 36 V] up and down.	
Response	During all test, no parasitic current paths shall be formed between the bus line and the IUT. $I_{BUS\_NO\_BAT}$ shall be less than 100 µA, means 1 V voltage drop over R_{MEAS} = 10 kΩ. After reconnecting battery line, the IUT shall restart after failure recovery.	
Reference	ISO 17987-4:2016, Table 15, Param 61 ISO 17987-4:2016, Figure 5	

8.5.9.3 [EPL-CT 105] Loss of GND

Figure 82 shows the test configuration of the test system "Loss of GND".

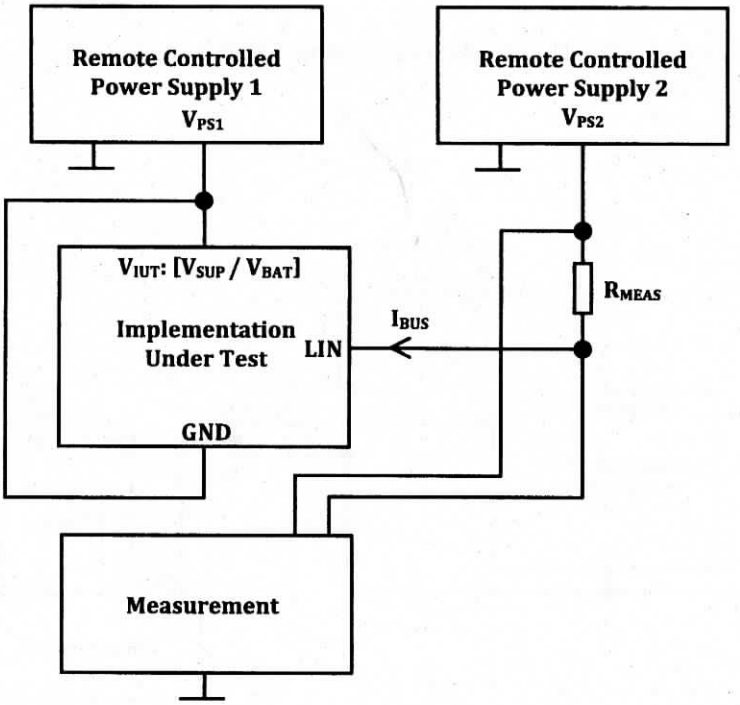

Figure 82 — Test system: Loss of GND

Table 193 defines the test system "Loss of GND".

Table 193 — Test system: Loss of GND

IUT node as	Class C device as slave	[EPL-CT 105].1
Initial state	**Parameters:**	
	R_{MEAS}	1 kΩ (0,1 %)
	Operational conditions:	
	V_{IUT}: [V_{SUP}/V_{BAT}] G_{ND_IUT} = V_{IUT} Failure	V_{IUT} = V_{PS1} = 24 V Local GND shorted to V_{IUT} Loss of ground

Table 193 *(continued)*

IUT node as	Class C device as slave	[EPL-CT 105].1
Test steps	The ground is disconnected from the IUT. V_{PS2} = Signal with a 2 V/s ramp in the range [0 V to 36 V] up and down.	
Response	During all test, no parasitic current paths shall be formed between the bus line and the IUT. $I_{BUS\_NO\_GND}$ shall be included in ±2 mA, means 2 V voltage drop over R_{MEAS} = 1 kΩ. After reconnecting ground line, the IUT shall restart after failure recovery.	
Reference	ISO 17987-4:2016, Table 15, Param 60 ISO 17987-4:2016, Figure 5	

8.5.10 [EPL-CT 106] Verifying internal capacitance and dynamic interference — IUT as slave

The purpose of this test is to check the internal capacitance of the IUT under normal and fault conditions. The IUT shall not interfere dynamically with bus signals when it is in passive (non-transmitting) or unpowered state.

Figure 83 shows the test configuration of the test system "Verifying internal capacitance and dynamic interference — IUT as slave".

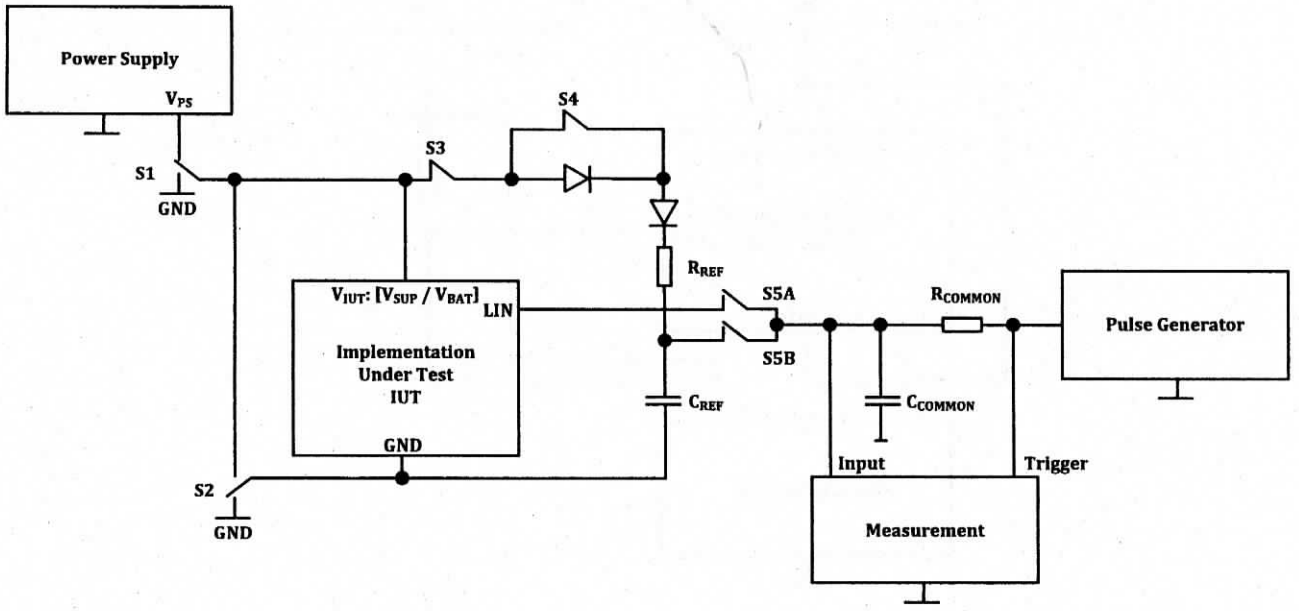

Figure 83 — Test system: Verifying internal capacitance and dynamic interference — IUT as slave

Table 194 defines the Switch settings depending on IUT configuration.

Table 194 — Switch settings depending on IUT configuration

Switch	Setting decription
S3	Normally closed. In case where IUT has switchable and deactivated internal pull-up (e.g. in power loss conditions), open S3.
S4	Normally closed. In case where IUT is a 3-pin node or ECU, where reverse polarity protection is included in IUT, open S4.
S5A/S5B	In case where IUT is connected by a wire harness: During reference measurement, close both S5A and S5B and disconnect IUT from harness. So the harness capacitance is accounted for in the reference.

Table 195 defines the test system "Verifying internal capacitance and dynamic interference — IUT as slave".

Table 195 — Test system: Verifying internal capacitance and dynamic interference — IUT as slave

IUT node as	Class C device as slave	[EPL-CT 106].1, [EPL-CT 106].2, [EPL-CT 106].3
Initial state	**Parameters:**	
	R_{COMMON}	1 kΩ (0,1 %)
	C_{COMMON}	750 pF (1,5 nF + 1,5 nF in series) (1 %)
	R_{REF}	30 kΩ (0,1 %)
	C_{REF}	250 pF (100 pF || 150 pF parallel) (1 %)
	Operational conditions:	
	V_{IUT}: [V_{SUP}/V_{BAT}]	24 V
Test steps	The LIN Bus is driven with a 10 kHz rectangular signal with a duty cycle of 50 %.	
	Rise time ≤40 ns. Slope time measurements are done at 10 %, 90 % of slope voltage.	
	S5B closed: Measuring rise time T_{REF} on a known capacitance of 250 pF + 750 pF.	
	S5A closed: Measuring rise time T_{int} with the IUT internal capacitance + 750 pF.	
Response	C_{SLAVE} shall be less than or equal to 250 pF: $T_{int} \leq T_{REF}$.	
	The IUT shall not interfere with the dynamic stimulus.	
Reference	ISO 17987-4:2016, 5.3.6 Param 37	
	ISO 17987-4:2016, 5.3.9.2	

Table 196 — Test cases: Verifying internal capacitance and dynamic interference — IUT as slave

EPL-CT-TC	Condition	S1	S2
[EPL-CT 106].1	Normal power supply IUT shall be in normal mode.	V_{PS}	GND
[EPL-CT 106].2	IUT loss of GND (IUT GND shorted to power supply).	V_{PS}	V_{PS}
[EPL-CT 106].3	IUT loss of V_{PS} (IUT V_{IUT}: [V_{SUP}/V_{BAT}] shorted to GND).	GND	GND

8.6 Operation mode termination

8.6.1 General

An external resistor R_{meas} is switched to the LIN pin. To get the value of the internal resistor, current and voltage shall be measured. These values are gathered for two different settings, and the internal resistance is calculated using Formulae (1), (2), (3) and (4).

Figure 84 shows the test configuration of the test system "Operation mode".

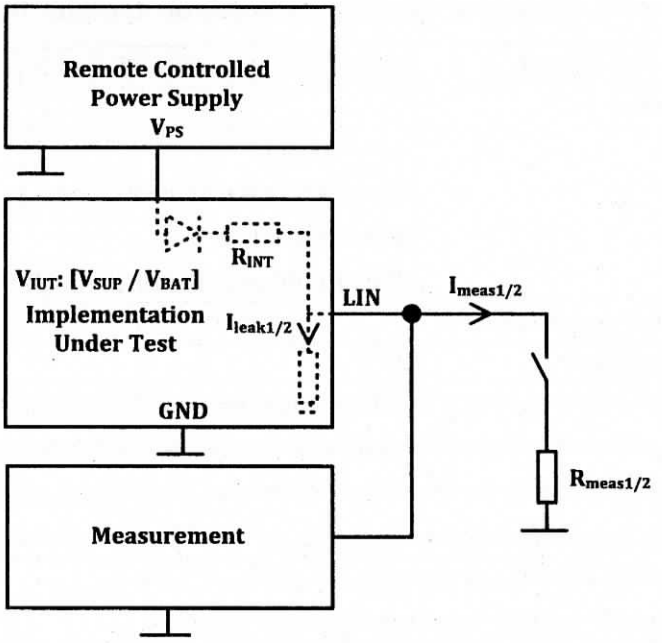

Figure 84 — Test system: Operation mode

8.6.2 [EPL-CT 107] Measuring internal resistor — IUT as slave

Table 197 defines the test system "Measuring internal resistor — IUT as slave".

Table 197 — Test system: Measuring internal resistor — IUT as slave

IUT node as	Class C device as slave	[EPL-CT 107].1
Initial state	**Parameters:**	
	R_{meas1}	10 kΩ (0,1 %)
	R_{meas2}	20 kΩ (0,1 %)
	Operational conditions:	
	V_{IUT}: [V_{SUP}/V_{BAT}]	24 V
Test steps	The IUT shall be in operational/active mode. There is no communication on the LIN bus. If the IUT incorporates a bus dominant state timeout detection, which disables the IUT's pull-up resistor, the measurement shall take place before a timeout is detected.	
Response	R_{int} value shall be included in the range [20 kΩ; 60 kΩ]; see Formula (4).	
Reference	ISO 17987-4:2016, Table 16, Param 71	

8.6.3 [EPL-CT 108] Measuring internal resistor — IUT as master

Table 198 defines the test system "Measuring internal resistor — IUT as master".

Table 198 — Test system: Measuring internal resistor — IUT as master

IUT node as	Class C device as master	[EPL-CT 108].1
Initial state	**Parameters:**	
	R_{meas1}	1 kΩ (0,1 %)
	R_{meas2}	2 kΩ (0,1 %)
	Operational conditions:	
	V_{IUT}: [V_{SUP}/V_{BAT}]	24 V

Table 198 *(continued)*

IUT node as	Class C device as master	[EPL–CT 108].1
Test steps	The IUT shall be in operational/active mode. There is no communication on the LIN bus. If the IUT incorporates a bus dominant state timeout detection, which disables the IUT's pull-up resistor, the measurement shall take place before a timeout is detected.	
Response	R_{int} value shall be included in the range [900 Ω; 1 100 kΩ]; see Formula (4). R_{meas1} = 1 kΩ (0,1 %); R_{meas2} = 2 kΩ (0,1 %).	
Reference	ISO 17987–4:2016, Table 16, Param 70	

8.7 Static test cases

The motivation of static test cases is to check the availability and the boundaries in the datasheet of the IUT.

For all integrated circuits every related parameter in Table 199 shall be part of the datasheet and fulfil the specified boundaries in terms of physical worst case condition. Datasheet parameter names may deviate from the names in Table 199, but in this case a cross-reference list (datasheet versus Table 199) shall be provided for this test. Parameter conditions may deviate from the conditions in Table 199, if the datasheet conditions are according to the physical worst case context in Table 199 at least.

If one parameter does not pass this test, the result of the whole conformance test is "Failed". See ISO 17987–4:2016, 5.1.2, 5.3.5.1, 5.3.5.2 and 5.3.8.

Table 199 defines the test system "LIN static test parameters for datasheets of integrated circuits".

Table 199 — Test system: LIN static test parameters for datasheets of integrated circuits

No	Reference	Parameter	Min.	Max.	Unit	Comment/ condition	Valid for	Conformance test is passed if value is	
								≤	≥
1.	Param 6	t_{BFS}	—	2/16	t_{BIT}	Value of accuracy of the byte field detection	All devices	Max.	—
2.	Param 7	t_{EBS}	7/16		t_{BIT}	Earliest bit sample time, $t_{EBS} \leq t_{LBS}$	All devices	—	Min.
3.	Param 8	t_{LBS}	—	10/16	t_{BIT}	Latest bit sample, $t_{LBS} \geq t_{EBS}$	All devices	Max.	—
4.	Param 52	V_{BAT}[a]	16,0	36,0	V	ECU operating voltage range	All devices with integrated reverse polarity diode	Min.	Max.
5.	Param 53	V_{SUP}[b]	15,0	36,0	V	Supply voltage range	All devices without integrated reverse polarity diode	Min.	Max.
6.	Param 54	V_{BAT}[a]	8,0	36,0	V	ECU operating voltage range	All devices with integrated reverse polarity diode	Min.	Max.
7.	Param 55	V_{SUP}[b]	7,0	36,0	V	Supply voltage range	All devices without integrated reverse polarity diode	Min.	Max.
8.	Param 56	$V_{SUP\_NON\_OP}$	−0,3	40,0	V	Voltage range within which the device is not destroyed; no guarantee of correct operation.	All devices	Min.	Max.
9.	Param 57	I_{BUS_LIM}[c]	75	300	mA	Current limitation for driver dominant state driver on $V_{BUS} = V_{BAT\_max}$[d]	All devices with integrated LIN transmitter	Max.	Min.

Table 199 *(continued)*

No	Reference	Parameter	Min.	Max.	Unit	Comment/ condition	Valid for	Conformance test is passed if value is	
								≤	≥
10.	Param 58	$I_{BUS\_PAS\_dom}$	−2	—	mA	Input leakage current at the Receiver incl. slave pull-up resistor as specified in Param 71 driver off V_{BUS} = 0 V V_{BAT} = 24 V	All devices with integrated slave pull-up resistor	—	Min.
12.	Param 60	$I_{BUS\_NO\_GND}$	−2	2	mA	Control unit disconnected from ground $GND_{Device} = V_{SUP}$ 0 V < V_{BUS} < 36 V V_{BAT} = 24 V Loss of local ground shall not affect communication in the residual network.	All devices	Max.	Min.
13.	Param 61	$I_{BUS\_NO\_BAT}$	—	100	µA	V_{BAT} disconnected V_{SUP} = GND 0 < V_{BUS} < 36 V Node shall sustain the current that can flow under this condition. Bus shall remain operational under this condition.	All devices	Max.	—
14.	Param 62	V_{BUS_dom}	—	0,4	V_{SUP}	Receiver dominant state	All devices with integrated LIN receiver	—	Max.
15.	Param 63	V_{BUS_rec}	0,6	—	V_{SUP}	Receiver recessive state	All devices with integrated LIN receiver	Min.	—
16.	Param 64	V_{BUS_CNT}	0,475	0,525	V_{SUP}	$V_{BUS\_CNT} = (V_{th\_dom} + V_{th\_rec})/2$[e]	All devices with integrated LIN receiver	Max.	Min.
17.	Param 65	V_{HYS}	—	0,175	V_{SUP}	$V_{HYS} = V_{th\_rec} - V_{th\_dom}$	All devices with integrated LIN receiver	Max.	—
18.	Param 72	D1 (Duty Cycle 1)	0,330	—	—	$TH_{Rec(max)}$ = 0,710 × V_{SUP}; $TH_{Dom(max)}$ = 0,554 × V_{SUP}; V_{SUP} = 15,0 V to 36 V; t_{BIT} = 50 µs; $D1 = t_{Bus\_rec(min)}/(2 \times t_{BIT})$	All devices with integrated LIN transmitter D1 valid for 20 kbit/s	—	Min.
19.	Param 73	D2 (Duty Cycle 2)	—	0,642		$TH_{Rec(min)}$ = 0,446 × V_{SUP}; $TH_{Dom(min)}$ = 0,302 × V_{SUP}; V_{SUP} = 15,6 V to 36 V; t_{BIT} = 50 µs; $D2 = t_{Bus\_rec(max)}/(2 \times t_{BIT})$	All devices with integrated LIN transmitter D2 valid for 20 kbit/s	Max.	—
20.	Param 74	D3 (Duty Cycle 3)	0,386	—	—	$TH_{Rec(max)}$ = 0,744 × V_{SUP}; $TH_{Dom(max)}$ = 0,581 × V_{SUP}; V_{SUP} = 7,0 V to 36 V; t_{BIT} = 96 µs; $D3 = t_{Bus\_rec(min)}/(2 \times t_{BIT})$	All devices with integrated LIN transmitter D3 valid for 10,417 kbit/s	—	Min.

Table 199 *(continued)*

No	Reference	Parameter	Min.	Max.	Unit	Comment/ condition	Valid for	Conformance test is passed if value is	
								≤	≥
21.	Param 75	D4 (Duty Cycle 4)	—	0,591	—	$TH_{Rec(min)} = 0{,}422 \times V_{SUP}$; $TH_{Dom(min)} = 0{,}284 \times V_{SUP}$; V_{SUP} = 7,6 V to 36 V; t_{BIT} = 96 µs; $D4 = t_{Bus\_rec(max)}/(2 \times t_{BIT})$	All devices with integrated LIN transmitter D4 valid for 10,417 kbit/s	Max.	—
22.	Param 76	t_{rx_pd}	—	6	µs	Propagation delay of receiver	All devices with integrated LIN receiver	Max.	—
23.	Param 77	t_{rx_sym}	-2	2	µs	Symmetry of receiver propagation delay rising edge with respect to falling edge	All devices with integrated LIN receiver	Max.	Min.
24.	Param 71	R_{SLAVE}	20	60	kΩ	The serial diode is mandatory.	All devices with integrated slave pull-up resistor	Max.	Min.
25.	Param 70	R_{MASTER}	900	1 100	Ω	The serial diode is mandatory. Only for valid for transceiver with integrated master pull-up resistor	All devices with integrated master pull-up resistor	Max.	Min.
26.	Param 37	C_{SLAVE}	—	250	pF	Capacitance of slave node	All LIN slave devices	Max.	—
27.	6.3.7.1	LIN device states changes	—	—	—	All LIN device state changes on conditional events (e.g. temperature shut-down) shall be specified in the LIN device datasheet.	All devices	—	—
28.	—	LIN transceiver input capacitance	—	—	—	A maximum LIN transceiver input capacitance shall be specified in the LIN device datasheet. Please consider the datasheet limits (e.g. voltage, temperature).		—	—

[a] V_{BAT} denotes the supply voltage at the connector of the control unit and may be different from the internal supply V_{SUP} for electronic components (see ISO 17987-4:2016, 5.3.2).

[b] V_{SUP} denotes the supply voltage at the transceiver inside the control unit and may be different from the external supply V_{BAT} for control units (see ISO 17987-4:2016, 5.3.2).

[c] I_{BUS}: Current flowing into the node.

[d] A transceiver shall be capable to sink at least 40mA. The maximum current flowing into the node shall not exceed 200 mA under DC conditions to avoid possible damage.

[e] V_{th_dom}: receiver threshold of the recessive to dominant LIN bus edge. V_{th_rec}: receiver threshold of the dominant to recessive LIN bus edge.

Bibliography

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[3] ISO 14229-1, *Road vehicles — Unified diagnostic services (UDS) — Part 1: Specification and requirements*

[4] ISO 14229-2, *Road vehicles — Unified diagnostic services (UDS) — Part 2: Session layer services*

[5] ISO 14229-7, *Road vehicles — Unified diagnostic services (UDS) — Part 7: UDS on local interconnect network (UDSonLIN)*

[6] ISO 17987-2, *Road vehicles — Local Interconnect Network (LIN) — Part 2: Transport protocol and network layer services*

[7] ISO 17987-3, *Road vehicles — Local Interconnect Network (LIN) — Part 3: Protocol specification*

[8] ISO 17987-6:2016, *Road vehicles — Local Interconnect Network (LIN) — Part 6: Protocol conformance test specification*