National Semiconductor

MM4025/MM5025 Dual 1024-Bit Dynamic Shift Register
MM4026/MM5026 Dual 1024-Bit Dynamic Shift Register
MM4027/MM5027 2048-Bit Dynamic Shift Register

general description

These 2048-bit dynamic shift registers are MOS monolithic integrated circuits using P-channel silicon gate technology. They employ a push-pull output for bipolar compatability and on-chip multiplexing to achieve a 6 MHz data rate. The clock rate is one-half the data rate, i.e., one data bit is entered for each ϕ_1 and ϕ_2 clock pulse.

The MM4025/MM5025 and MM4027/MM5027 have on-chip logic to load and recirculate data.

The MM4026/MM5026 has an individual logic-select line to load one of the two inputs on each of the 1024-bit registers.

features

- Bipolar compatibility — Standard +5V, −12V power supplies
- High frequency of operation — 6 MHz guaranteed
- Low power dissipation — 120 μW/bit at 1 MHz ϕ rate 0°C, guaranteed
- Low clock capacitance — 190 pF max
- Wide operating temperature range
  MM4025,MM4026,MM4027 −55°C to +125°C
  MM5025,MM5026,MM5027 0°C to 70°C

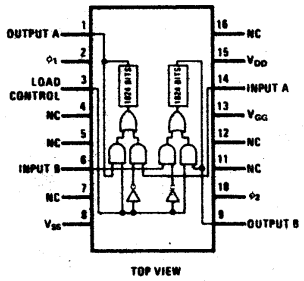
applications

- "Silicon store" replacement for drum and disc memories
- CRT displays
- Buffer memories

logic and connection diagrams

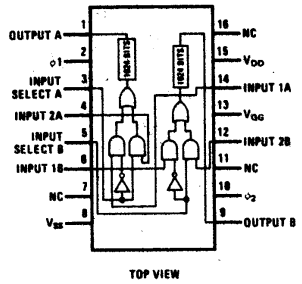
Military Temperature Range

Dual-In-Line Package



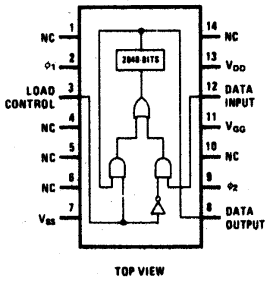
Order Number MM4025D or MM5025D
See NS Package D16C

Dual-In-Line Package



Order Number MM4026D or MM5026D
See NS Package D16C

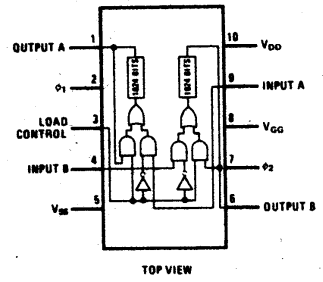
Flat Package



Order Number MM4027F or MM5027F
See NS Package F14B

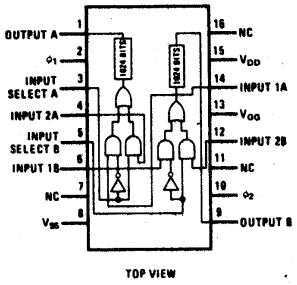
Commercial Temperature Range

Dual-In-Line Package



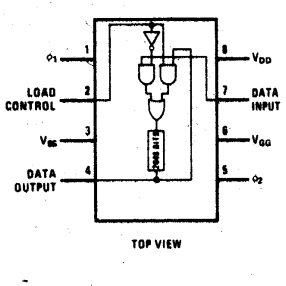
Order Number MM5025N
See NS Package N10B

Dual-In-Line Package



Order Number MM5026N
See NS Package N16A

Dual-In-Line Package



Order Number MM5027N
See NS Package N08B

absolute maximum ratings

Voltage at Any Pin With Respect to V_{SS}	+0.3 to −20.0V
Operating Ambient Temperature Range	
MM4025,MM4026,MM4027	−55°C to +125°C
MM5025,MM5026,MM5027	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C

electrical characteristics V_{SS} = +5.0V ± 5%, V_{DD} = GND, V_{GG} = −12.0V ±10%

T_A within operating temperature range unless otherwise stated.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Data Input Levels					
Logical High Level (V_{IH})		V_{SS}−1.5		V_{SS} + 0.3	V
Logical Low Level (V_{IL})		V_{SS}−10		V_{SS} − 4.2	V
Data Input Leakage	V_{IN} = −10V, T_A = 25°C, All other pins GND		0.01	1.0	μA
Data Input Capacitance	V_{IN} = 0V, f = 1 MHz, All other pins GND (Note 1)		2.5	5.0	pF
Load/Select Input Levels					
Logical High Level (V_{IH})		V_{SS}−1.5		V_{SS} + 0.3	V
Logical Low Level (V_{IL})		V_{SS} − 10		V_{SS} − 4.2	V
Load/Select Input Leakage	V_{IN} = −10V, T_A = 25°C, All other pins GND		0.01	1.0	μA
Load/Select Input Capacitance	V_{IN} = 0V, f = 1 MHz, All other pins GND (Note 1)		4.0	7.0	pF
Clock Input Levels					
Logical High Level ($V_{\phi H}$)		V_{SS} − 1.0		V_{SS} + 0.3	V
Logical Low Level ($V_{\phi L}$)		V_{SS} − 18.5		V_{SS} − 14.5	V
Clock Input Leakage	V_ϕ = −15V, T_A = 25°C, All other pins GND		.05	1.0	μA
Clock Input Capacitance	V_ϕ = 0V, f = 1 MHz, All other pins GND (Note 1)		165	190	pF
Data Output Levels					
Logical High Level (V_{OH})	I_{SOURCE} = −0.5 mA	2.4		V_{SS}	V
Logical Low Level (V_{OL})	I_{SINK} = 1.6 mA	0.0		0.4	V
Power Supply Current					
I_{GG}	T_A = 25°C, V_{GG} = −12.0V, ϕ_{PW} = 160 ns V_{SS} = 5.0V, $V_{\phi L}$ = −12.0V, DATA = Note 4 V_{DD} = 0.0V				
	0.01 MHz ≤ ϕ_f ≤ 0.1 MHz		2	3.5	mA
	ϕ_f = 1.0 MHz		2	3.5	mA
	ϕ_f = 3.0 MHz		2	3.5	mA
I_{DD}	0.01 MHz ϕ_f ≤ 0.1 MHz		8	15	mA
	ϕ_f = 1.0 MHz		22	32	mA
	ϕ_f = 3.0 MHz		48	70	mA
Clock Frequency (ϕ_f)					
MM4025,MM4026,MM4027	$\phi t_r = \phi t_f$ = 20 ns (Note 2, Note 3 & Note 5)	0.03	2.0	1.0	MHz
MM5025,MM5026,MM5027		0.003	4.0	1.25	MHz
Clock Pulsewidth (ϕ_{PW})					
MM4025,MM4026,MM4027	$\phi t_r = \phi t_f$ = 20 ns, Data Rate = 2 ϕ_f	0.240		8.0	μs
MM5025,MM5026,MM5027		0.240		10	μs
Clock Phase Delay Times (ϕ_d,$\bar{\phi}_d$)	See Curves	10			ns
Clock Transition Times (ϕt_r, ϕt_f)				0.5	μs
Partial Bit Times (T)	(Note 2, Note 3)				
T_1 Partial Bit Time					
MM4025,MM4026,MM4027		0.5		16.5	μs
MM5025,MM5026,MM5027		0.4		165	μs
T_2 Partial Bit Time					
MM4025,MM4026,MM4027		0.5		16.5	μs
MM5025,MM5026,MM5027		0.4		165	
Data & Load/Select Input Setup Time (t_{ds})		35			ns
Data & Load/Select Input Hold Time (t_{dh})		20			ns
Data Output Propogation Delay from ϕ					
Delay to High Level (t_{pdH})	15 pF Output Capacitance			160	ns
Delay to Low Level (t_{pdL})				160	ns

Note 1: Capacitance is guaranteed by periodic testing.

Note 2: Minimum clock frequency is a function of temperature and partial bit times (T_1 and T_2) as shown by ϕ_f versus temperature and T_1, T_2 versus temperature curves. The lowest guaranteed clock frequency for any temperature can be attained by making T_1 equal to T_2. The minimum guaranteed clock frequency: ϕ_f (min) = 1/(T_1 + T_2) where T_1 and T_2 do not exceed the guaranteed maximum.

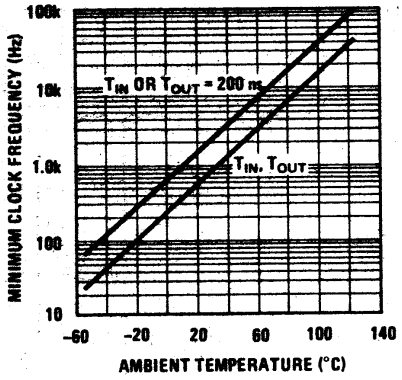
Note 3: Minimum clock frequency and partial bit time curves are guaranteed by testing at a high temperature point.

Note 4: For data pattern of 1111000011110000 etc.

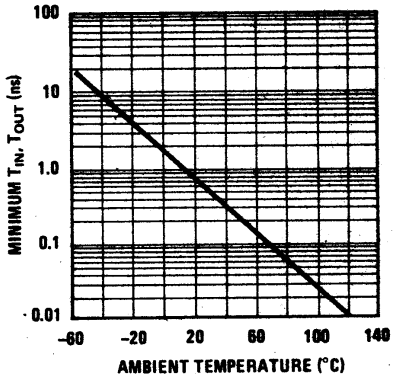
Note 5: Maximum frequency limited by maximum package power dissipation for MM4025, MM4026 and MM4027.

typical performance characteristics

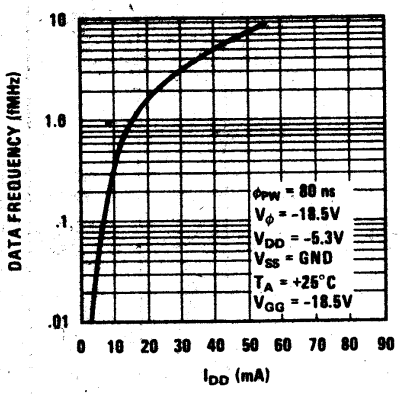
Typical Minimum Clock Frequency vs Temperature (Note 2)



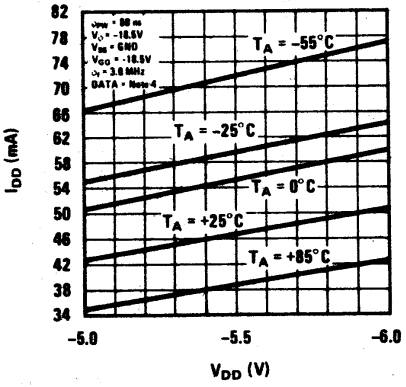
Typical Maximum T_1 and T_2 vs Temperature (Note 2)



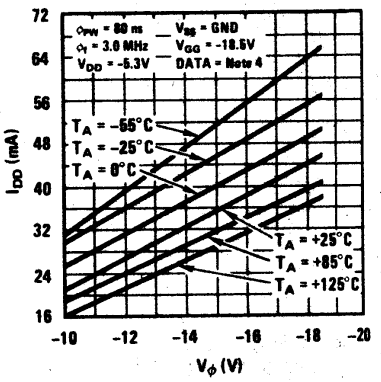
Power Supply Current vs Data Rate



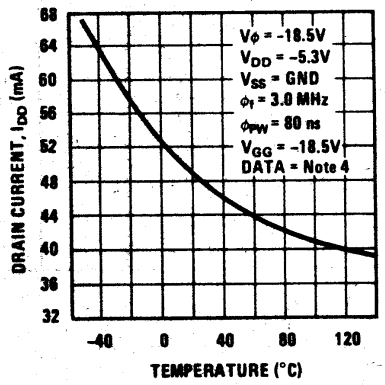
Power Supply Current vs V_{DD}



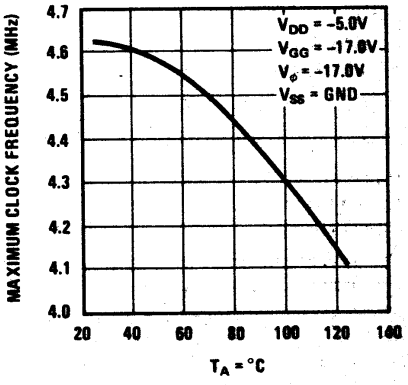
Power Supply Current vs Clock Voltage V_ϕ



Power Supply Current vs Temperature

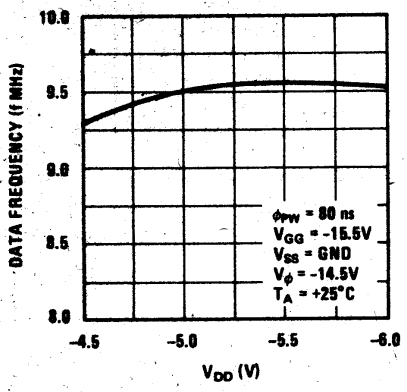


Maximum Clock Frequency vs Temperature

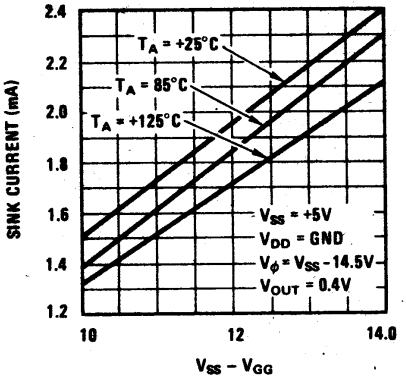


typical performance characteristics (con't)

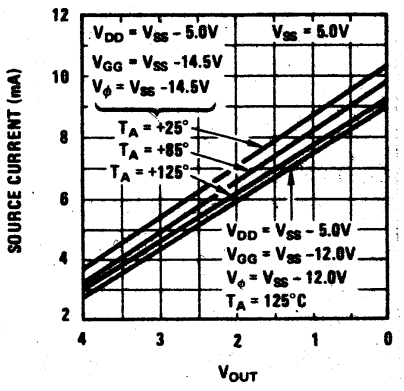
Maximum Data Rate vs V_{DD}



Typical Sink Current vs V_{GG}

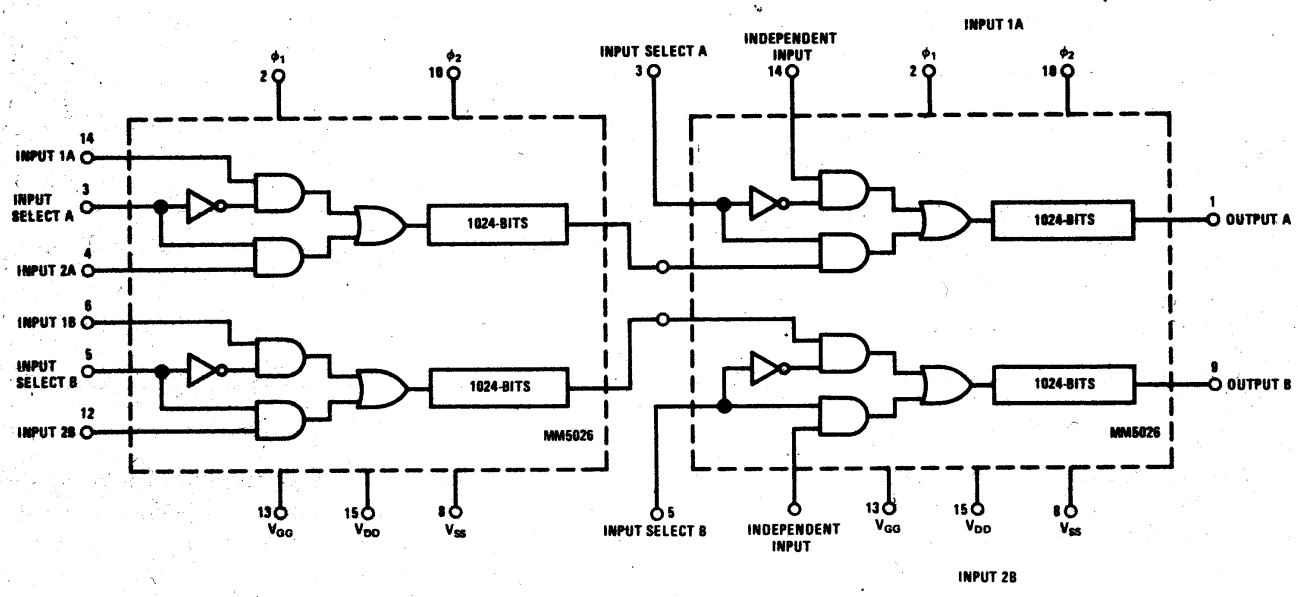


Typical Data Output Source Current vs Data Output Voltage

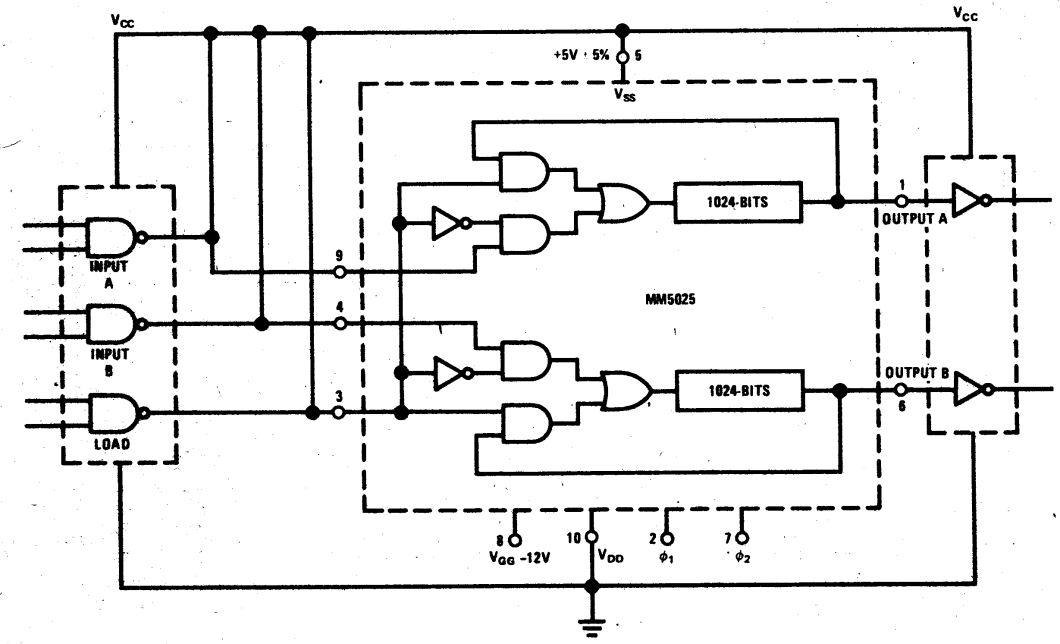


typical applications

Memory Expansion



TTL/MOS Interface



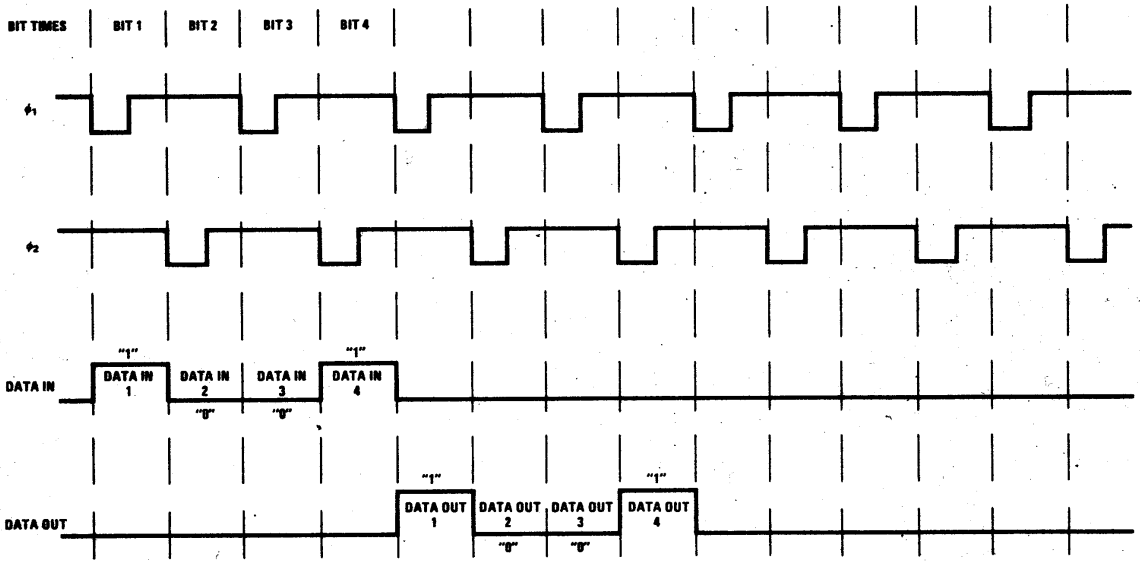
truth tables

Positive Logic
Logic "1" = V_{IH} = Logical High Level
Logic "0" = V_{IL} = Logical Low Level

Write/Recirculate	Function
1	Recirculate
0	Load Data

Input Select A	Function
1	Select Input 2A
0	Select Input 1A
Input Select B	**Function**
1	Select Input 2B
0	Select Input 1B

switching time waveforms



Shown is a simplified illustration of the timing of a 4-bit multiplexed register showing input output relationships with respect to the clock. If data enters the register at ϕ_1 time, it exits at ϕ_1 time, (beginning on $\phi_{1's}$ negative going edge and ending on the succeeding $\phi_{2's}$ negative going edge).

timing diagram