

汕头市众利电子科技有限公司

产 品 说 明 书

ZL12864C2

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一.概述

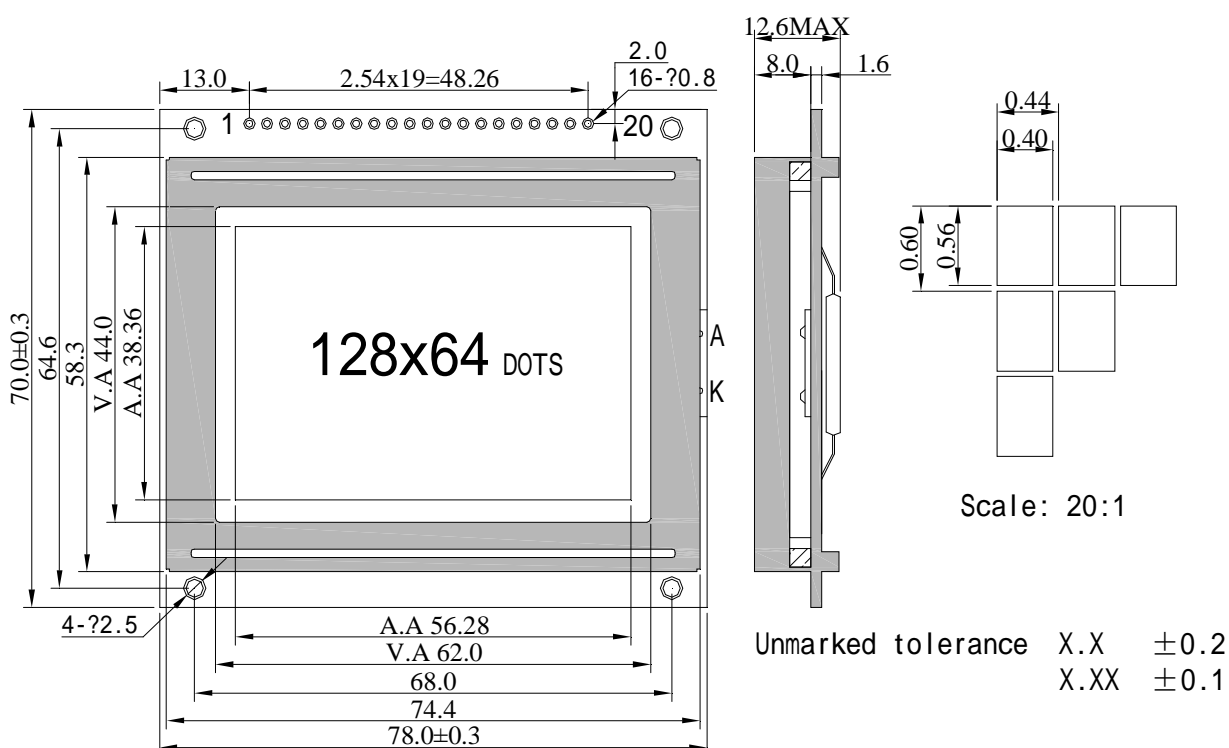
ZL12864C2 是一种图形点阵液晶显示器。它主要采用动态驱动原理由行驱动器、控制器和列驱动器三部分组成了 128(列) × 64(行)的全点阵液晶显示。此显示器采用了 SMD 的硬封装方式,通过导电橡胶和压框连接 LCD,使其寿命长,连接可靠。

二.特性

- 1.工作电压为 $+5V \pm 10%$,可自带驱动 LCD 所需的负电压。
- 2.全屏幕点阵,点阵数为 128(列) × 64(行),可显示 8(行) × 4(行)个(16 × 16 点阵)汉字,也可完成图形,字符的显示。
- 3.与 CPU 接口采用 4 条位控制总线和 8 位并行数据总线输入输出,适配 Inter8080 系列时序。
- 4.内部有显示数据锁存器,和用于文本显示的 6 × 8 和 8 × 8 的字符库。
- 5.简单的操作指令。

三.外形尺寸

- 1.外形尺寸图



2. 主要外形尺寸

项 目	标 准 尺 寸	单 位
模 块 体 积	78.0 × 70.0 × 14	mm
定 位 尺 寸	68.0 × 65.0	mm
视 域	62.0 × 44.0	mm
行 列 点 阵 数	128 × 64	dots
点 距 离	0.44 × 0.60	mm
点 大 小	0.40 × 0.56	mm

四. 硬件说明

1. 引脚特性

引脚号	引脚名称	级 别	引 脚 功 能 描 述
1	FG	0V	压框地
2	VSS	0V	电源地
3	VDD	+5V	电源电压
4	V0	-	液晶显示驱动电
5	/WR	H/L	低电平有效。写操作信号
6	/RD	H/L	低电平有效。读操作信号
7	/CE	H/L	低电平有效。片选信号
8	C/D	H/L	通道选择信号 C/D=H 为指令通道 C/D=L 为数据通道
9	/RESET	H/L	复位信号,低有效
10	DB0	H/L	八位三态并行数据总线
11	DB1		
12	DB2		
13	DB3		
14	DB4		
15	DB5		
16	DB6		
17	DB7		
18	FS	H/L	字体选择。 FS=H, 6 × 8 点阵字体 FS=L, 8 × 8 点阵字体
20	A	+5V	背光电源, $I_{dd} \leq 960\text{mA}$
21	K	0V	

五、IC 说明及指令表

T6963C is LCD controller designed to be used for control LCD driver LCD driver LSIs and display data Memory, It has an 8 bit parallel data bus And control lines for reading or writing through a MPU I/F.

It has 128 words character generator ROM with the capability to control External display RAM of up to 128K bytes. Allocation of text, graphics And external generator RAM can be easily made and the display window can Be freely moved within the allocated memory range.

It supports a very board range of LCD formats by selecting different Combinations on a set of programmable inputs. It can be used in text, graphic Modes and has various attribute functions.

指令表：

表 2

COMMAND	CODE	D1	D2	FUNCTION
Register Set	00100001	X address	Y address	Cursor pointer set
	00100010	Data	00H	Off register
	00100100	Low address	High address	Address pointer set
Control Word set	01000000	Low address	High address	Text home address set
	01000001	Columns	00H	Text area set
	01000010	Low address	High address	Graphic home address set
	01000011	Columns	00H	Graphic area set
Mode set	1000x000	-	-	"OR" mode
	1000x001	-	-	"EXOR" mode
	1000x011	-	-	"AND" mode
	1000x100	-	-	"Text attribute" mode
	10000xxx	-	-	Internal CGROM mode
	10001xxx	-	-	External CGRAM mode
Display Mode	10010000	-	-	Display off
	1001xx10	-	-	Cursor on, blink off
	1001xx11	-	-	Cursor on, blink on
	100101xx	-	-	Text on, graphic off
	100110xx	-	-	Text off, graphic on
	100111xx	-	-	Text on, graphic on
Cursor Pattern Select	10100000	-	-	1 line cursor
	10100001	-	-	2 line cursor
	10100010	-	-	3 line cursor
	10100011	-	-	4 line cursor
	10100100	-	-	5 line cursor
	10100101	-	-	6 line cursor
	10100110	-	-	7 line cursor
	10100111	-	-	8 line cursor
Data auto Read/write	10110000	-	-	Data auto write set
	10110001	-	-	Data auto read set
	10110010	-	-	Auto reset

Data read Write	11000000	Data	-	Data write and ADP increment
	11000001	-	-	Data read and ADP increment
	11000010	Data	-	Data write and ADP decrement
	11000011	-	-	Data read and ADP decrement
	11000100	Data	-	Data write and ADP no variable
	11000101	-	-	Data read and ADP no variable
Screen peek	11100000	-	-	Screen peek
Screen copy	11101000	-	-	Screen copy
Bit Set/Reset	11110XX	-	-	Bit reset
	11111XXX	-	-	Bit set
	1111X000	-	-	Bit 0(LSB)
	1111X001	-	-	Bit 1
	1111X010	-	-	Bit 2
	1111X011	-	-	Bit 3
	1111X100	-	-	Bit 4
	1111X101	-	-	Bit 5
1111X110	-	-	Bit 6	
1111X111	-	-	Bit 7(MSB)	

六、电气参数

1. ABSOLUTE MAXIMUM RATING

Item	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage(logic)	VDD-VSS	-	-0.3	-	7	V
Supply Voltage(LCD Drive)	VDD-VO	-	VDD+0.3	-	VDD-0.3	V
Input Voltage	VI	-	-0.3	-	VDD+0.3	V
Operating Temperature	Topr	-	-10	-	+55	° C
Storage Temperature	Tstg	-	-20	-	+60	° C

2. OPTICAL DATA Ta=25° C

Item	Symbol	Condition	Standard Value			Unit	
			min	typ	max		
Supply voltage(Logic)	VDD-VSS	-	4.75	5	5.25	V	
Supply voltage(LCD Drive)	VDD-VO	-	-	-	-	V	
Supply current	IDD	-	-	12.0	17.0	mA	
	IO	-	-	1.8	2.5	mA	
EL Backlight current	IEL	-	-	100	-	mA	
Input high voltage	VIH	High level	0.7VDD	-	VDD	V	
Input low voltage	VIL	Low level	0	-	0.3VDD	V	
Supply voltage for LCD Drive (1/80 duty)	VDD-VO	Ta=0° C	14.2	14.5	14.8	V	
		Ta=25° C	13.3	13.6	13.9	V	
		Ta=50° C	12.3	12.6	12.9	V	
Contrast Ratio	CR		-	4	-	-	
Viewing Angle	-	CR≥2	θ	-10	-	20	deg
			θ	60	-	120	deg
Response Time (rise)	Tr	Note 1	Ta=2	-	130	200	ms

			5°				
Response Time (delay)	Td	Note 2	Ta=2 5°	-	150	230	ms

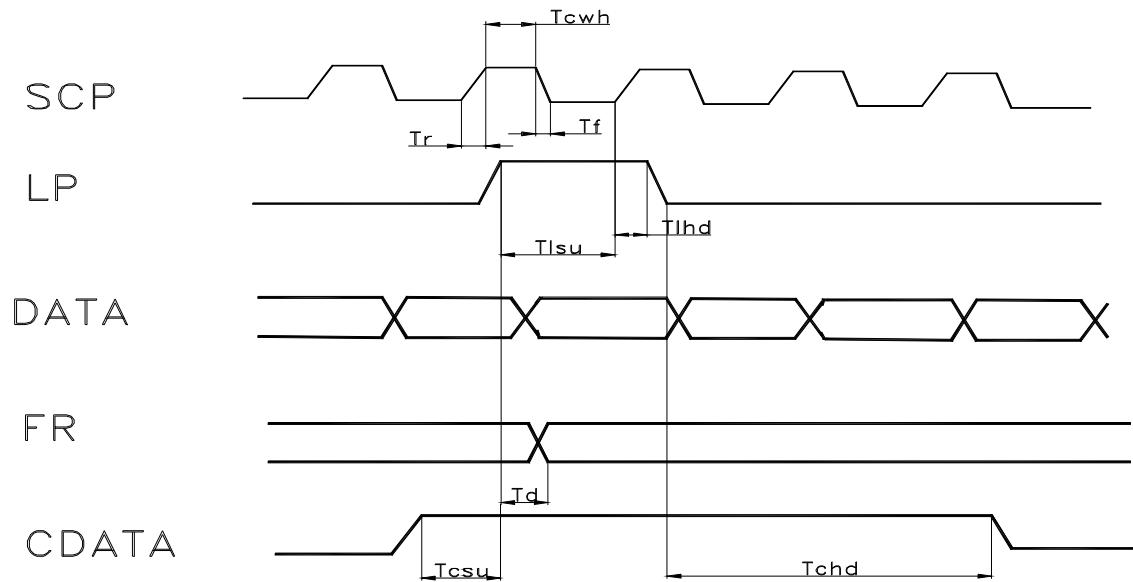
NOTE 1: Required time for blackening ratio of segment goes up from 0% to 90% when Wave from is switched from one selected one ($\theta = 10^\circ$, $\phi = 90^\circ$)

Note 2: Required time for blackening ratio of segment goes down from 100% to 10% When wave from is switched from one selected one ($\theta = 10^\circ$, $\phi = 90^\circ$)

3. TIMING CHARACTERISTICS

Item	Symbol	Min	Max	Unit
Operating frequency	fSCP	-	2.75	MHZ
SCP pulse width	Tcwh, Tcwl	150		ns
SCP rise/fall time	Tr	-	30	ns
LP set up time	Tlsu	150	290	ns
LP hold time	Tlhd	5	40	ns
Data set up time	Tdsu	170	-	ns
Data hold time	Tdhd	80	-	ns
FR delay time	Td	0	90	ns
CDATA set up time	Tcsu	450	850	ns
CDATA hold time	Tchd	450	950	ns

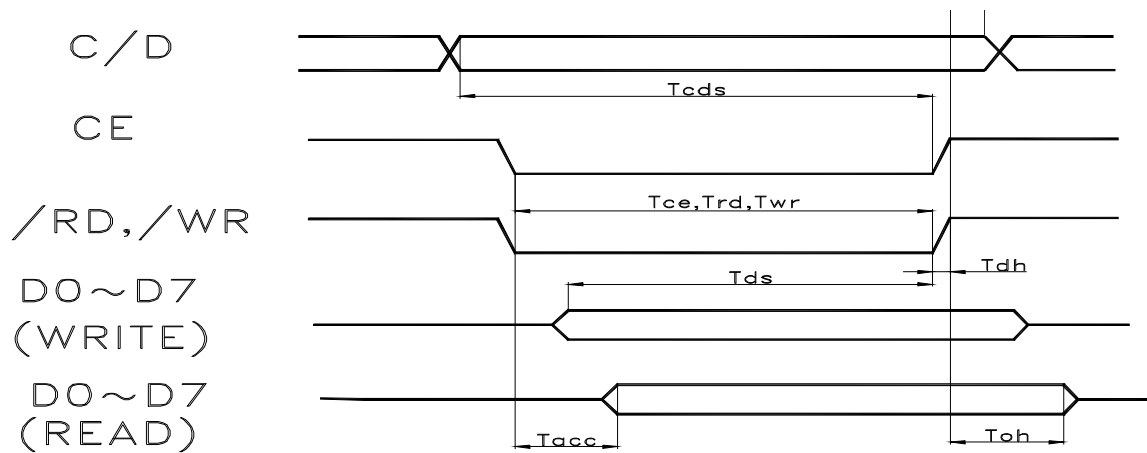
Condition: DV=+5.0V ± 10%, Ta=-10~+70° C



驱动波形图

4.INTERFACE TIMING

Item	Symbol	Min	Max	Unit
C/D set up time	Tcds	100	-	ns
C/D hold time	Tcdh	10	-	ns
CE, RD, WR pulse width	Tce, Trd, Twr	80	-	ns
DATA set up time	Tds	80	-	ns
DATA hold time	Tdh	40	-	ns
Access time	Tacc	-	150	ns
Output hold time	Toh	10	50	ns



读写时序图

5.EL Backlight Electrical Characteristics

Ta=25° C VDD=5V

Symbol	Parameter	Min	Type	Max	Units
IIN	VDD supply current	10		150	mA
VA-B	Output voltage across lamp	37	40	43	V
		75	80	85	V
FEL	VA-B output drive frequency	600	800	1000	V
VDD	Supply voltage	4.5		12	V
CL	Load capacitance	0		25	nF
TA	Operating temperature	0		50	° C

Note: EL Backlight with white lamp.

七、功能描述

7.1 STATUS READ

Before sending data(read/write), command it is necessary to check the Status.

Status check

Status of T6963c can read from data lines.

/RD L

/WR H

/CE L

C/D H

D0~D7 Status word

T6963C status word format is following

MSB				LSB			
STA7	STA6	STA5	STA4	STA3	STA2	STA1	STA0
D7	D6	D5	D4	D3	D2	D1	D0

STA0	Check capability of command execution	0: Disable 1: Enable
STA1	Check capability of data read/write	0: Disable 1: Enable
STA2	Check capability of auto mode data read	0: Disable 1: Enable
STA3	Check capability of auto mode data write	0: Disable 1: Enable
STA4	Not use	
STA5	Check capability of controller operation	0: Disable 1: Enable
STA6	Error flag. Using screen peek/copy command	0: No error 1: error
STA7	Check the condition blink	0: Disable 1: Enable

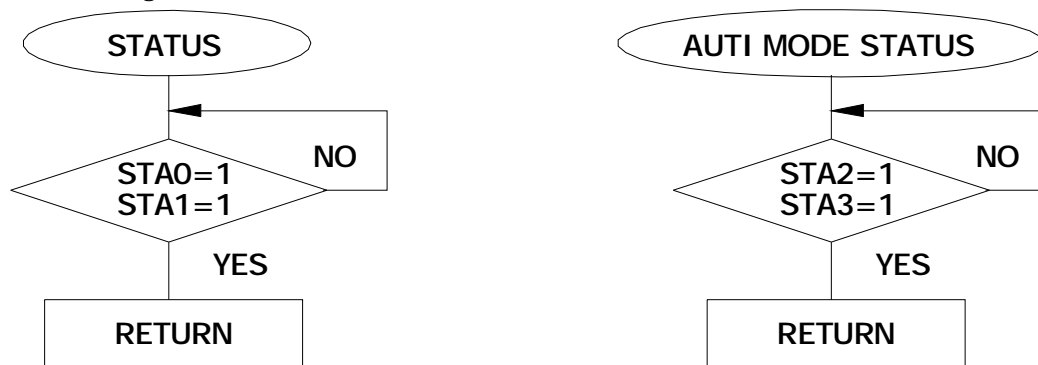
Note 1: It is necessary to check STA0 and STA1 at the same time, The error

Is happened by sending data at executing command.

2: The status check will be enough to check STA0/STA1.

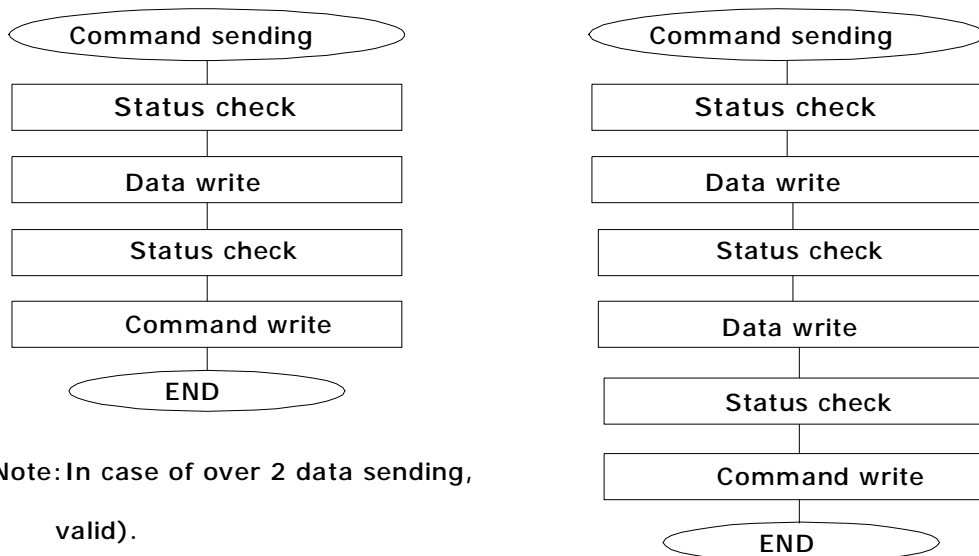
3: STA2/STA3 are valid in auto mode STA0/STA1 are invalid.

Status checking flow:



7.2 DATA SET

In T6963C, the data have been set and command executes.
The order of procedure of command sending



7.31 Description of command

1. Register set

CODE	HEX	FUNCTION	D1	D2
00100001	21H	Cursor pointer set	X address	Y address
00100010	22H	Offset register set	Data	00H
00100100	24H	Address pointer set	Low address	High address

(1) Cursor pointer set

The position of cursor is specified by X address. The cursor position is moved only by this command. The cursor pointer doesn't have the function of increment and decrement. The shift of cursor set by this command. X address, Y address are specified following.

X address 00H - - - - 4FH (Low 7bits are valid)

Y address 00H - - - - 1FH (Low 5bits are valid)

1 Screen drive

X address 00H - - - - 4FH

Y address 00H - - - - 0FH

(2) Offset register set

The offset register is used to determine external character generator RAM area.

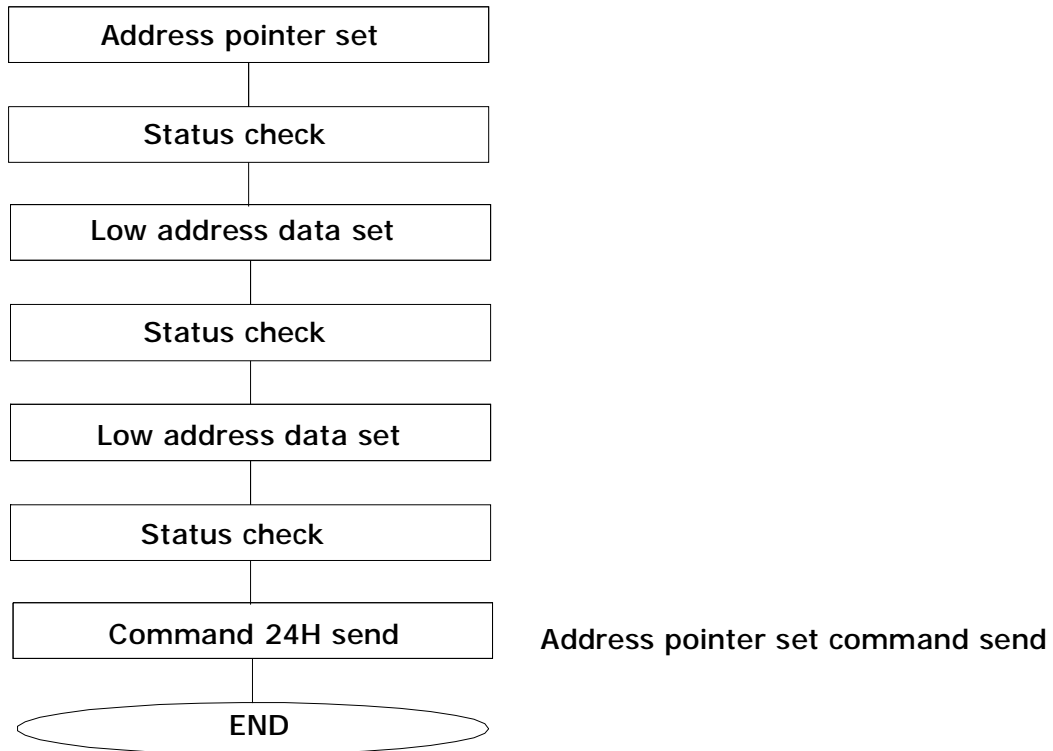
T6963C has 16 bits address lines as follow:

MSB													LSB			
Ad15	Ad14	Ad13	Ad12	Ad11	Ad10	Ad9	Ad8	Ad7	Ad6	Ad5	Ad4	Ad3	Ad2	Ad1	Ad0	

The upper 5 bits (ad15 - ad11) are determined by offset register. The middle 8 bits (ad10 - ad3) are determined by character code. The lower 3 bit (ad2 - ad0) are determined by vertical counter. The lower 5 bit of D1(data) are valid. The data format of external character Generator RAM

(3) Address pointer set

The address pointer set command is used to indicate the start address for writing (or reading) to external RAM. The flow chart for the address pointer set command is as follows:



7.32 Control word set

CODE	HEX	FUNCTION	D1	D2
01000000	40H	Text home address set	Low address	High address
01000001	41H	Text area set	Columns	00H
01000010	42H	Graphic home address set	Low address	High address
01000011	43H	Graphic area set	Columns	00H

The home address and column size are defined by this command

(1) Text home address and area set

The starting address of external display RAM for text display is defined by this command. The text home address shows the left end and most upper position.

The relationship of external display RAM address and display position

Example:

Text home address: 0000H
 Text area: 00A0H
 MD2=0, MD3=0: 80 COLUMN
 DUAL=0, MDS=1, MD0=1, MD1=0: 28 LINES

Display plane:

0000H	0001H	- - - - -	004EH	004FH	1 Line
00A0H	00A1H	- - - - -	00EEH	00EFH	2 Line
:	:	:	:	:	:
:	:	:	:	:	:
:	:	:	:	:	:
10E0H	10E1H	- - - - -	112EH	112FH	28 Lines

(2) Graphic home address and area set

The starting address of external display RAM for Graphic display is Defined by this command. The graphic home address shows the left end most Upper line.

The relationship of external display RAM address and display position.

Example:

Graphic home address: 0000H
 Graphic area: 0020H
 MD2=H, MD3=H: 32 COLUMNS
 DUAL=H, MDS=L, MD0=H, MD1=H: 2 LINES

Example:

Display plane:

0000H	0001H	- - - - -	001EH	001FH
0020H	0021H	- - - - -	003EH	003FH
⋮	⋮	⋮	⋮	⋮
01E0H	01E1H		01FEH	01FFH

7.33 MODE SET

The display mode is defined by this command. The display mode don't have changed until to send next this command. Logically "OR", "EXOR", "AND" of text and graphic display can be displayed.

When internal character generator mode is selected, character code 00H - 7FH are selected from built-in character generator ROM. The character code 80H-FFH are automatically selected external character generator RAM

NOTE: Only text display is attributed, because attributed data is located.

Attribute function

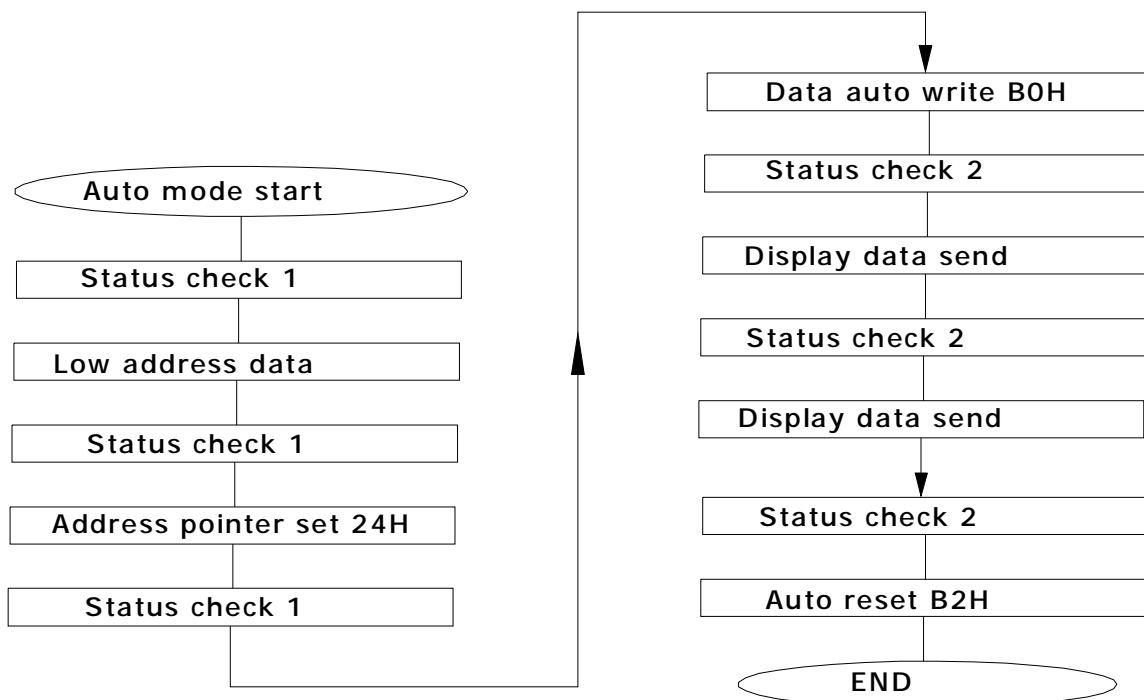
"Reverse display", "Character blink" and "Inhibit" are called "Attribute". The attribute data is written in the graphic area defined by control word set command. The mode set command selects text display only and graphic the mode set command selects text display only and graphic display cannot be displayed. The attribute data of the 1st character in text area is written at the 1st byte in graphic area, and attribute data of n-th 1byte in graphic area. Attribute function is defined as follow.

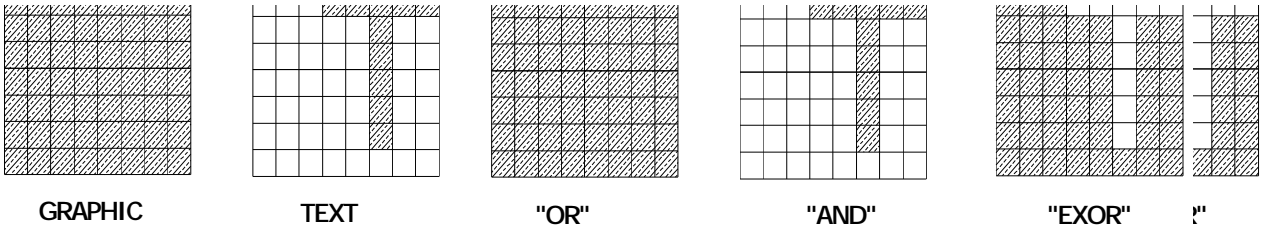
Attribute RAM 1byte

X	X	X	X	D3	D2	D1	D0
---	---	---	---	----	----	----	----

X: don't care

D3	D2	D1	D0	FUNCTION
0	0	0	0	Normal display
0	1	0	1	Reverse display
0	0	1	1	Inhibit display
1	0	0	0	Blink of normal display
1	1	0	0	Blink of reverse display
1	0	1	1	Blink of inhibit display





7.34 DATA AUTO READ/WRITE

CODE	HEX	FUNCTION	OPERAND
10110000	B0H	Data auto write set	-
10110001	B1H	Data auto read set	-
10110010	B2H	Auto reset	-

This command is convenient to send full screen data from external display RAM. After setting auto mode, "Data write(or read)" command is not necessary between each data. "Data auto write (or read)" command should follow the "Address pointer set" and address pointer is automatically increment by + 1 after each data. After sending (or receiving) all data "Auto reset" is necessary to return normal operation because all data is regarded "Display data" and no command can be accepted in the auto mode.

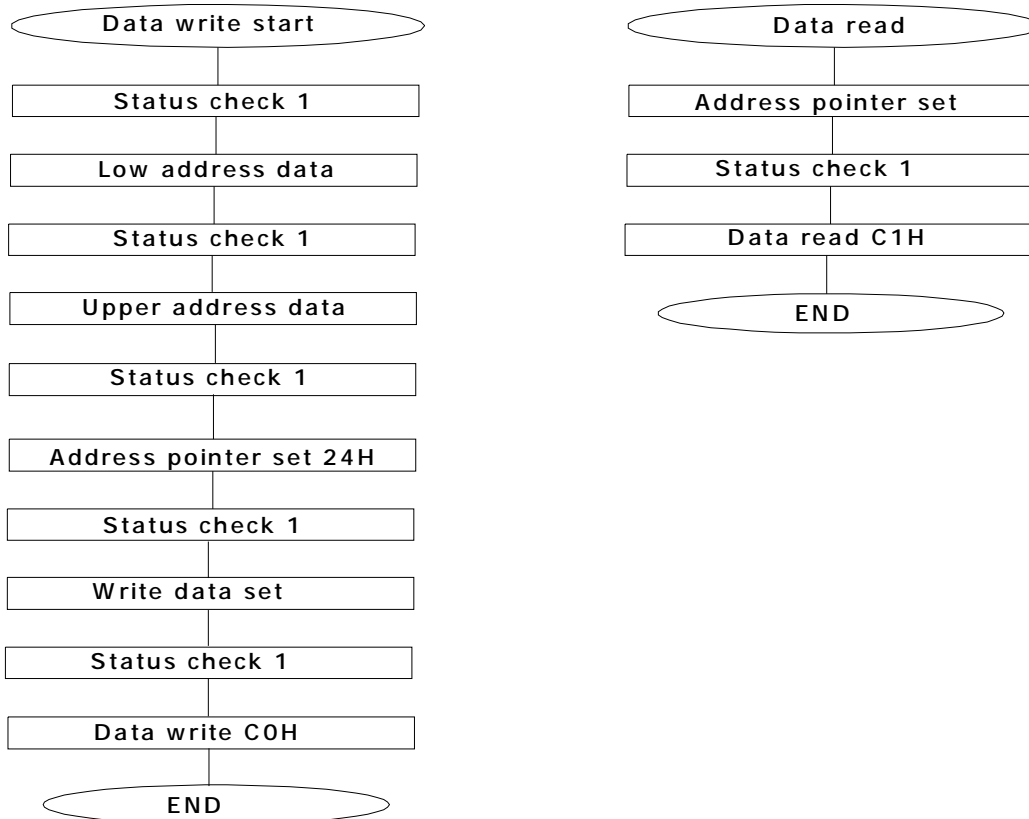
Note: status check for auto mode(STA2, STA3 should be checked between each Data. Auto reset should be performed after checking (STA3=1 STA2=1)

7.35 DATA READ WRITE

CODE	HEX	FUNCTION	OPERAND
11000000	C0H	Data write and ADP increment	Data
11000001	C1H	Data read and ADP increment	Data
11000010	C2H	Data write and ADP decrement	Data
11000011	C3H	Data read and ADP decrement	Data
11000100	C4H	Data write and ADP nonvariable	Data
11000101	C5H	Data read and ADP nonvariable	Data

This command is used for data write from MPU to external display RAM AND data read external display RAM to MPU. Data write/data read should be executed after setting address by address pointer set command. Address Pointer can be automatically increment by setting this command.

Note: this command is necessary for each 1 byte data. Please refer following flow chart.



NOTE:

- (1) After power on, it is necessary to reset. /RESET is kept "L" between 5 CLOCK up(oscillation clock).
- (2) When /HALT has been "L", the oscillation is stopped. It is necessary To turn off power supply for LCD, because LCD goes down by DC bias.
- (3) The HALF function contains the RESET function.
- (4) After state of RESET/HALT.

TERMINAL	HALT	RESET
D0-D7	F	F
D0-d7	F	F
R/w	H	H
/ce	H (NOTE 1)	H (NOTE 1)
Ad0-ad15	H (NOTE 2)	H (NOTE 2)
/ce0, /ce1	H (NOTE 1)	H (NOTE 1)
ED, HOD	Final Data	Final Data
HSCP	L	L
LP	L	L
CDATA	H	H
FR	H	H
CH1	L	K0
CH2	L	VEND
DSPON	L	L
X0	H	OSC CLOCK

L: Level L

F: Floating (High impedance)

K0: Internal state (TEXT data access) normally open

VEND: End signal of V-counter(Line count) if MDS=H, T2=L,

HEND (end signal of H-count) normally open.

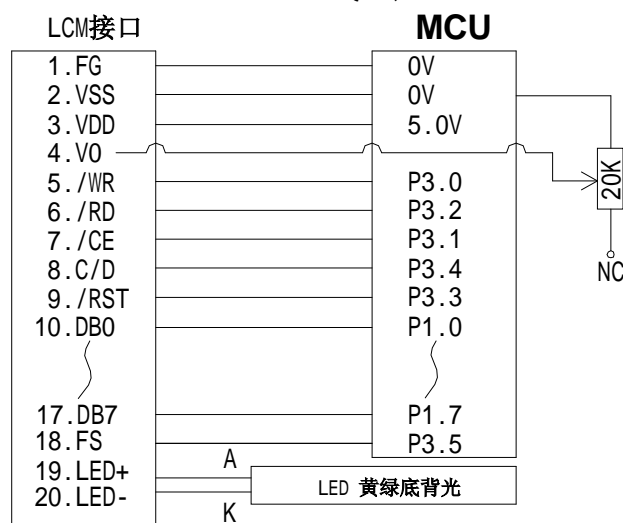
Note 1: In Attribute mode, H or L by state of Graphinc pointer.

Note 2: In Attribute mode, DATA of Graphinc pointer.

八. 应用举例

;

12864连线图



```

driver = T6963C    (TOSHIBA)
; for 12864 LCD module!
R      EQU    P3.2
W      EQU    P3.0
CE     EQU    P3.1
CD     EQU    P3.4
RESET  EQU    P3.3
FS1    EQU    P3.5
SW     EQU    P3.7
;table  equ    0500h
TXHOME EQU    40H
TXAREA EQU    41H
GRHOME EQU    42H
GRAREA EQU    43H
OFFSET EQU    22H
ADPSET EQU    24H
AVRON  EQU    0B0H
AWROFF EQU    0B2H
      ORG    0000H
      AJMP   START
      ORG    000BH
      AJMP   TIME
      ORG    0030H
TIME:
      MOV    TLO, #00H
      MOV    TH0, #0B2H
      RETI
START:
      MOV    SP, #40H
      MOV    PSW, #00H
      CLR    RESET
;      setb  p3.7
      NOP
      NOP      ; five clocks up
      NOP
      NOP
      NOP
      SETB   RESET
;-----
; display size: 128 columns x 16 (128dots) lines
; character font: select by fs1  6x8 font
;-----
      CLR    CE
      CLR    FS1

```

```

MOV    DPTR, #0000H    ;text home address
LCALL  WD2
MOV    A, #TXHOME
LCALL  WC
MOV    DPTR, #0016H    ;set text area 132 segments
LCALL  WD2
MOV    A, #TXAREA
LCALL  WC
MOV    DPTR, #8000H    ;graphic home address
LCALL  WD2
MOV    A, #GRHOME
LCALL  WC
MOV    DPTR, #0010H    ;set graphic area 16 columns
LCALL  WD2
MOV    A, #GRAREA
LCALL  WC
MOV    A, #80h        ;mode set : inter cg ram or
LCALL  WC
MOV    DPTR, #0002H    ; set offset register
LCALL  WD2
MOV    A, #OFFSET
LCALL  WC
MOV    A, #0A0H        ;1-line cursor
LCALL  WC
MOV    A, #0COH
LCALL  WC
;-----
MOV    DPTR, #1400H    ;cg ram address =1400H
LCALL  WD2            ;code = 80H
MOV    A, #ADPSET
LCALL  WC
MOV    A, #AWRON
LCALL  WC
MOV    R1, #08H
WDOT1:
MOV    A, R1
JB     ACC. 0, ODD
MOV    A, #0AAH
ODD_EVE:
LCALL  AWD            ;code = 80h
DJNZ  R1, WDOT1
MOV    R1, #08H
WDOT2:
MOV    A, #OFFH        ;code = 81h

```



```

        LCALL    AWD
        DJNZ    R1, WDOT2
        MOV     R1, #08H
        AJMP   WDOT3
ODD:
        MOV     A, #055H
        AJMP   ODD_EVE
EVEN:
        MOV     A, #055H
        AJMP   ODD_EVEN
WDOT3:
        MOV     A, R1
        JNB    ACC. 0, EVEN
        MOV     A, #0AAH
ODD_EVEN:
        LCALL   AWD                ; code =82H
        DJNZ   R1, WDOT3
        LCALL   CH_STA2
        MOV    A, #AWROFF
        LCALL   WC
;-----
        LCALL   CLMAP
        LCALL   CLEAR
MAIN:
        SETB   FS1
        MOV    A, #94H                ; text mode
        LCALL   WC
        MOV    DPTR, #0000H          ; 0 lines 0 column
        LCALL   WD2
        MOV    A, #ADPSET
        LCALL   WC
        MOV    A, #AWRON
        LCALL   WC
        MOV    R2, #OBOH            ; CHARACTER NUMBER
        MOV    DPTR, #TAB_TEXT_02
MATRIX:
        MOV    A, #00h
        MOC    A, @A+DPTR
        LCALL   AWD
        INC    DPTR
        DJNZ   R2, MATRIX
        LCALL   CH_STA2
        MOV    A, #AWROFF
        LCALL   WC

```

```

;      LCALL  WAIT
      LCALL  DELAY_1s
;-----
      LCALL  CLEAR
      MOV    A, #98H          ; graphic mode
      LCALL  WC
      CLR    FS1
      LCALL  SCREEN_3
      LCALL  DELAY_1s
;      LCALL  WAIT
      LCALL  CLMAP
      AJMP   MAIN
;-----
screen_3:
      MOV    DPTR, #8000H
      LCALL  WD2
      MOV    A, #ADPSET
      LCALL  WC
      MOV    A, #AWRON
      LCALL  WC
      MOV    DPTR, #TABLE_3
      MOV    R1, #40H        ; 64 COM
GRAPH_3:
      MOV    RO, #10H       ; 16X8=128
GRAPHC:
      CLR    A
      MOVC   A, @A+DPTR
      LCALL  AWD
      INC    DPTR
      DJNZ   RO, GRAPHC
      DJNZ   R1, GRAPH_3
      LCALL  CH_STA2
      MOV    A, #AVROFF
      LCALL  WC
      RET
;-----subroutine-----
DPTDEC:
      MOV    A, DPL
      CLR    C
      SUBB   A, #20H
      MOV    DPL, A
      MOV    A, DPH
      SUBB   A, #00H
      MOV    DPH, A

```

```

    RET
;-----
WAIT:
;    MOV    TMDD, #01H
;    MOV    TLO, #00H
;    MOV    TH0, #0B2H
;    MOV    IE, #82H
;    SETB   TR0
;    MOV    R5, #80D
;WAIT5:
;    MOV    PCON, #01H
;    DJNZ   R5, WAIT5
;    MOV    IE, #00H
;    MOV    PCON, #00H
    SETB   SW
WAIT00:
    JB     SW, WAIT00
WAIT01:
    JNB    SW, WAIT01
    RET
;-----subroutine-----
WD2:
    MOV    A, DPL
    LCALL  WD1
    MOV    A, DPH
    LCALL  WD1
    RET
WDD2:
    MOV    A, R4
    LCALL  WD1
    MOV    A, R3
    LCALL  WD1
    RET
;-----
WD1:
    PUSH   Acc
    ACALL  CH_STA1
    CLR    CD
    POP    Acc
    CLR    W
    MOV    P1, A
    NOP
    NOP
    SETB   W

```

```
    SETB    CD
    RET
```

```
;-----
AWD:
```

```
    PUSH    Acc
    LCALL   CH_STA2
    CLR     CD
    POP     Acc
    CLR     W
    MOV     P1, A
    NOP
    NOP
    SETB    W
    SETB    CD
    RET
```

```
;-----
WC:
```

```
    PUSH    ACC
    LCALL   CH_STA1
    SETB    CD
    POP     Acc
    CLR     W
    MOV     P1, A
    NOP
    NOP
    SETB    W
    SETB    CD
    RET
```

```
;-----
CH_STA2:
```

```
    SETB    CD
    MOV     P1, #0FFH
    CLR     R
    NOP
    NOP
    SETB    R
    MOV     A, P1
    ANL     A, #08H
    CJNE    A, #08H, CH_STA2
    RET
```

```
;-----
CH_STA1:
```

```
    SETB    CD
    MOV     P1, #0FFH
```

```

        CLR     R
        NOP
        NOP
        SETB   R
        MOV    A, P1
        ANL   A, #03H
        CJNE  A, #03H, CH_STA1
        RET

;-----
DELAY_10ms:
        PUSH   01H
        PUSH   00H
        MOV    R0, #0FFH
DLY:
        MOV    R1, #0FAH
DELY:
        DJNZ   R1, DELY
        DJNZ   R0, DLY
        POP    00H
        POP    01H
        RET

;-----
DELAY_1s:
        PUSH   02H
        MOV    R2, #014H
DELL:
        ACALL  DELAY_10ms
        DJNZ   R2, DELL
        POP    02H
        RET

;-----
DELAY:                                     ; 50us
        PUSH   07H
        MOV    R7, #0FFH
LAY:
        DJNZ   R7, LAY
        POP    07H
        RET

;-----
CLEAR:
        MOV    DPTR, #0000H      ; set address pointer
        LCALL  WD2
        MOV    A, #ADPSET
        LCALL  WC

```

```

        MOV     A, #AWRON           ; set data auto write
        LCALL  WC
        MOV     DPTR, #0000h
CLEA:
        MOV     A, #00H             ; clear screen data
        LCALL  AWD                 ; write blank code
        INC     DPTR
        MOV     A, DPH
        CJNE   A, #01, CLEA
        MOV     A, DPL
        CJNE   A, #0EOH, CLEA
        LCALL  CH_STA2
        MOV     A, #AWROFF
        LCALL  WC
        RET

;-----
CLMAP:
        MOV     DPTR, #8000H       ; set Address pointer
        LCALL  WD2
        MOV     A, #ADPSET
        LCALL  WC
        MOV     A, #AWRON
        LCALL  WC
        MOV     DPTR, #8000H
OFF:
        MOV     A, #00H
        LCALL  AWD
        INC     DPTR
        MOV     A, DPH
        CJNE   A, #87H, OFF
        MOV     A, DPL
        CJNE   A, #80H, OFF
        LCALL  CH_STA2
        MOV     A, #AWROFF
        LCALL  WC
        RET

TAB_TEXT_02:

DB     021H, 021H, 021H, 021H, 021H, 021H, 021H, 021H, 021H, 021H, 021H, 021H, 021H, 021H, 021H, 021H, 021H, 021H, 021H, 021H
DB     022H, 022H, 022H, 022H, 022H, 022H, 022H, 022H, 022H, 022H, 022H, 022H, 022H, 022H, 022H, 022H, 022H, 022H, 022H, 022H
DB     023H, 023H, 023H, 023H, 023H, 023H, 023H, 023H, 023H, 023H, 023H, 023H, 023H, 023H, 023H, 023H, 023H, 023H, 023H, 023H
DB     024H, 024H, 024H, 024H, 024H, 024H, 024H, 024H, 024H, 024H, 024H, 024H, 024H, 024H, 024H, 024H, 024H, 024H, 024H, 024H
DB     025H, 025H, 025H, 025H, 025H, 025H, 025H, 025H, 025H, 025H, 025H, 025H, 025H, 025H, 025H, 025H, 025H, 025H, 025H, 025H

```


DB 086H, 01CH, 01CH, 000H, 060H, 061H, 086H, 030H, 063H, 000H, 0C0H, 081H, 000H, 001H, 083H, 0E1H
DB 08CH, 030H, 000H, 001H, 0F8H, 07FH, 083H, 0E0H, 03EH, 003H, 0F0H, 0C2H, 000H, 001H, 080H, 0C1H
DB 080H, 000H, 000H, 000H, 000H, 000H, 000H, 000H, 000H, 000H, 000H, 03CH, 000H, 000H, 000H, 001H
DB 080H, 000H, 000H, 000H, 000H, 000H, 000H, 000H, 000H, 000H, 000H, 000H, 000H, 000H, 000H, 001H
DB 080H, 000H, 000H, 000H, 000H, 000H, 000H, 000H, 000H, 000H, 000H, 000H, 000H, 000H, 000H, 001H
DB 082H, 000H, 004H, 080H, 087H, 0CFH, 080H, 000H, 000H, 000H, 000H, 000H, 000H, 000H, 000H, 001H
DB 082H, 004H, 006H, 080H, 084H, 048H, 080H, 000H, 000H, 000H, 000H, 000H, 000H, 000H, 000H, 001H
DB 082H, 002H, 004H, 084H, 084H, 048H, 080H, 000H, 000H, 000H, 000H, 000H, 000H, 000H, 000H, 001H
DB 09FH, 0BFH, 0C7H, 0F4H, 087H, 0CFH, 080H, 000H, 01FH, 0C3H, 083H, 003H, 087H, 087H, 0C0H, 001H
DB 082H, 020H, 088H, 084H, 080H, 022H, 000H, 000H, 012H, 044H, 084H, 084H, 088H, 048H, 040H, 001H
DB 082H, 00AH, 000H, 084H, 080H, 021H, 000H, 000H, 002H, 008H, 008H, 048H, 008H, 048H, 040H, 001H
DB 082H, 091H, 08FH, 0F4H, 09FH, 0FFH, 080H, 000H, 002H, 008H, 008H, 048H, 000H, 090H, 000H, 001H
DB 083H, 020H, 080H, 084H, 080H, 0D8H, 000H, 000H, 002H, 00BH, 008H, 04BH, 003H, 010H, 000H, 001H
DB 086H, 000H, 007H, 0F4H, 083H, 006H, 000H, 000H, 002H, 00CH, 084H, 0CCH, 080H, 090H, 000H, 001H
DB 09AH, 03FH, 084H, 094H, 09CH, 001H, 0C6H, 000H, 002H, 008H, 043H, 048H, 040H, 050H, 000H, 001H
DB 082H, 004H, 004H, 094H, 087H, 0DFH, 086H, 000H, 002H, 008H, 040H, 048H, 040H, 050H, 000H, 001H
DB 082H, 004H, 004H, 094H, 084H, 051H, 000H, 000H, 002H, 008H, 040H, 048H, 048H, 048H, 040H, 001H
DB 082H, 004H, 004H, 090H, 084H, 051H, 006H, 000H, 002H, 004H, 084H, 084H, 088H, 088H, 080H, 001H
DB 082H, 004H, 004H, 0F0H, 084H, 051H, 006H, 000H, 007H, 003H, 007H, 003H, 007H, 007H, 000H, 001H
DB 08AH, 07FH, 0C0H, 0A2H, 087H, 0DFH, 000H, 000H, 000H, 000H, 000H, 000H, 000H, 000H, 000H, 001H
DB 084H, 000H, 000H, 081H, 000H, 000H, 000H, 000H, 000H, 000H, 000H, 000H, 000H, 000H, 000H, 001H
DB 080H, 000H, 000H, 000H, 000H, 000H, 000H, 000H, 000H, 000H, 000H, 000H, 000H, 000H, 000H, 001H
DB 080H, 000H, 000H, 000H, 000H, 000H, 000H, 000H, 000H, 000H, 000H, 000H, 000H, 000H, 000H, 001H
DB 080H, 000H, 000H, 000H, 000H, 000H, 000H, 000H, 000H, 000H, 000H, 000H, 000H, 000H, 000H, 001H
DB 080H, 000H, 000H, 000H, 000H, 000H, 000H, 000H, 000H, 000H, 000H, 000H, 000H, 000H, 000H, 001H
DB 080H, 000H, 000H, 000H, 000H, 000H, 000H, 000H, 000H, 000H, 000H, 000H, 000H, 000H, 000H, 001H
DB 0FFH, 0FFH, 0FFH, 0FFH, 0FFH, 0FFH, 0FFH, 0FFH, 0FFH, 0FFH, 0FFH, 0FFH, 0FFH, 0FFH, 0FFH, 0FFH

END

显示内容



完毕

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