LGDP4524

176RGBx220-dot, 262,144-color 1-chip TFT LCD driver IC

Rev 0.9.0
2007-05-21

Description

The LGDP4524 is a 262,144-color one-chip controller driver LSI for a TFT liquid crystal display with resolution of 176 RGB x 220 dots, comprising a 528-channel source driver, RAM for graphics data of 176 RGB x 220 dots at maximum, a gate driver and a power supply circuit.

The LGDP4524 supports high-speed parallel interfaces to 8-, 9-, 16-, 18-bit ports and a function to write RAM data in high speed for transferring data efficiently and rewriting RAM graphics data in high speed. In addition, the LGDP4524 incorporates 6-, 16-, 18-bit RGB interfaces (VSYNC, HSYNC, DOTCLK, ENABLE, and DB[17:0]) and a VSYNC interface (system interface + VSYNC) for displaying a moving picture, which, with use of window address function, enable the LGDP4524 to display a moving picture easily at a position specified by a user and still pictures in other areas on the screen simultaneously. Since this combination allows transferring only moving picture data while retaining still picture data in the internal RAM intact, data transfer can be minimized and power consumption by the entire system is reduced.

The LGDP4524 can operate with low I/O interface power supply up to 1.65V, with an incorporated voltage follower circuit to generate voltage levels for driving an LCD. The LGDP4524 also supports a function to display in 8 colors and a standby mode, allowing for precise power control by software. These features make the LGDP4524 an ideal LCD driver for medium or small sized portable products supporting WWW browsers such as digital cellular phones or small PDAs, where long battery life is a measure concern.

Features

- A controller driver for a liquid crystal TFT display with resolution of 176RGB x 220-dot, capable of graphics display in 262,144 colors
- Single chip solution for a liquid crystal TFT display
- System interfaces
  - High-speed interfaces to 8-, 9-, 16-, 18-bit parallel ports
  - Serial Peripheral Interface (SPI)
- Interfaces for moving picture display
  - 6-, 16-, 18-bit RGB interfaces (VSYNC, HSYNC, DOTCLK, ENABLE, DB[17:0])
  - VSYNC interface (System interface + VSYNC)
- Window address function to specify a rectangular area on the internal RAM for moving picture display
  - Facilitate moving picture display at any area on the screen via a moving picture display interface
  - Limit the data rewriting area and reduce data transfer
  - Enable moving and still picture display at the same time
- Bit operation function for facilitating graphics data processing
  - Bit-unit write data mask function
  - Pixel-unit logical/conditional write function
- Abundant functions for color display control
  - γ-correction function enabling display in 262,144 colors
  - Line-unit vertical scrolling function
- Low -power consumption architecture
  - Low operating power supplies: Vcc = 2.5 to 3.3 V (To generate logic voltage)
VDD = 1.7 to 1.9 V (internal logic)
IOVcc = 1.65 to 3.3 V (interface I/O)
Vci = 2.5 to 3.3 V (analog)
  - Low voltage drive: DDVDH = 4.5 to 5.5 V
  - Power saving functions (standby mode etc.)
  - Liquid crystal partial drive function, enabling partially driving an LCD panel at positions specified by a user
  - A voltage follower circuit for generating LCD driving voltage levels with a small direct current through bleeder resistors
- Incorporate step-up circuits for stepping up a liquid crystal drive voltage level up to 6 times (x6)
- 87,120 byte internal RAM
- Incorporate a 528-channel source driver and a 220-channel gate driver
- n-line liquid crystal AC drive: invert polarity at an interval of arbitrarily set n lines (n: 0 ~ 64)
- Internal oscillator and hardware reset
- Reversible source driver shift direction
- For Cst structure only
- Internal 28-bit EPROM for VcomH level setting (4-times programmable)

Power Supply Specifications

Table 1

No.	Item		LGDP4524
1	TFT source lines		528 pins (176 x RGB)
2	TFT gate lines		220 pins
3	Capacitor structure of TFT display		Cst structure only (common Vcom formula)
4	Liquid crystal drive output	S1 to S528	V0 to V63 grayscales
		G1 to G220	VGH to VGL
		Vcom1/11/2/21	VcomH – VcomL: amplitude = electronic volumes VcomH = VcomR: adjusted with an external resistor
5	Input voltage	IOVcc	1.65 – 3.30 V
		Vcc	2.50 – 3.30 V
		VDD	1.70 – 1.90 V
		Vci	2.50 – 3.30 V
6	Internal step-up circuits	DDVDH	Vci1 ×2
		VGH	Vci1 ×4, ×5, ×6
		VGL	Vci1 ×-3, ×-4, ×-5
		VCL	Vci1 ×-1

Block Diagram

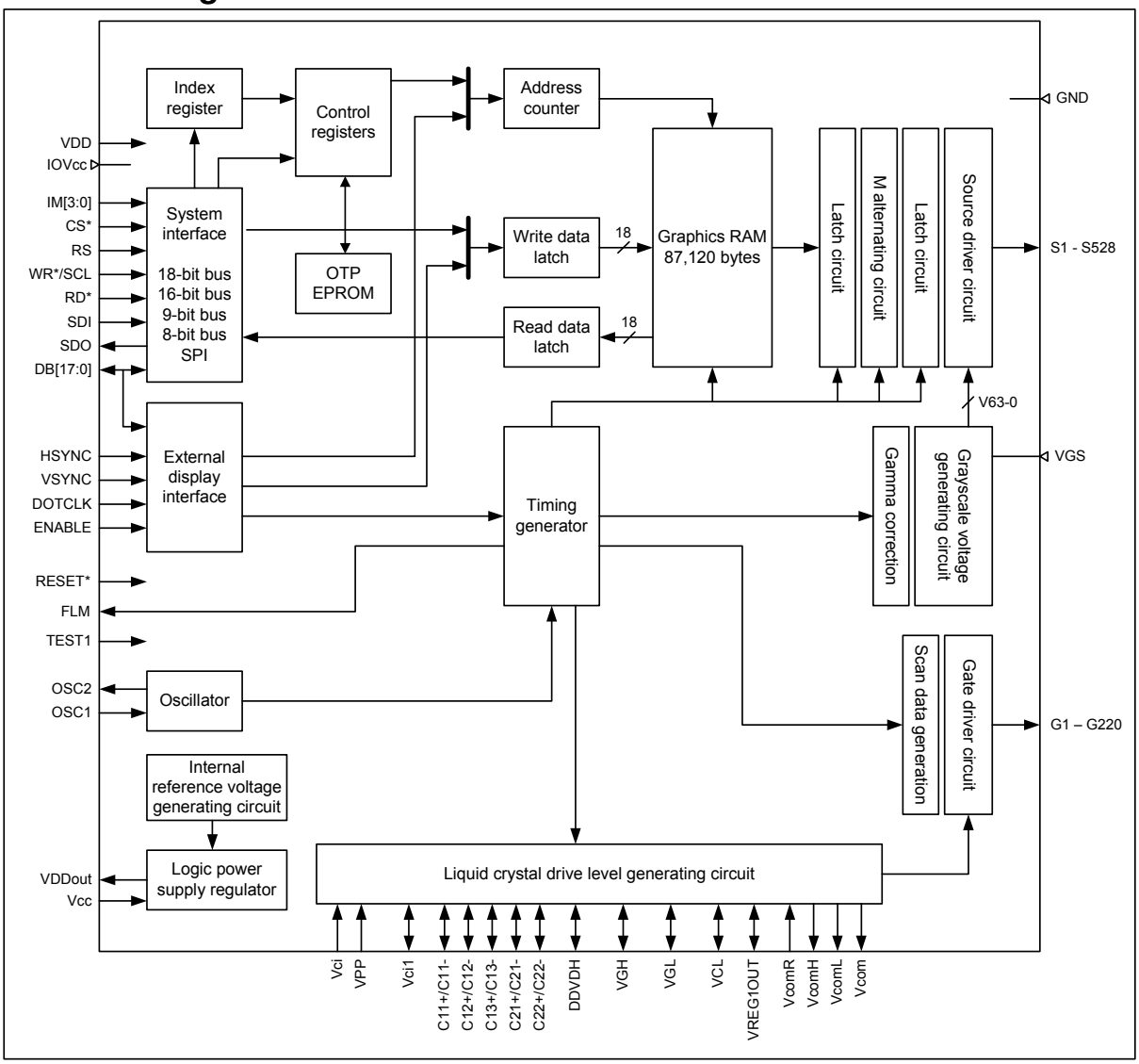


Figure 1 Block Diagram of LGDP4524

Pin Function

Table 2

<table>
<tr><th>Name</th><th># pins</th><th>I/O</th><th>Connected to</th><th>Function</th></tr>
<tr><td>IM[0]_ID,
IM[3:1]</td><td>4</td><td>I</td><td>GND/IOVcc</td><td>MPU interface mode select signal.
In SPI mode, the IM[0] pin is used to set the ID of device code.

<table><tr><th>IM[3:0]</th><th>Interface mode</th><th>Data pins</th></tr><tr><td>000*</td><td>Setting disabled</td><td>-</td></tr><tr><td>0010</td><td>80-system 16-bit interface</td><td>DB[17:10],
DB[8:1]</td></tr><tr><td>0011</td><td>80-system 8-bit interface</td><td>DB[17:10]</td></tr><tr><td>010*</td><td>Serial peripheral interface (SPI)</td><td>SDI, SDO</td></tr><tr><td>011*</td><td>Setting disabled</td><td>-</td></tr><tr><td>100*</td><td>Setting disabled</td><td>-</td></tr><tr><td>1010</td><td>80-system 18-bit interface</td><td>DB[17:0]</td></tr><tr><td>1011</td><td>80-system 9-bit interface</td><td>DB[17:9]</td></tr><tr><td>11**</td><td>Setting disabled</td><td>-</td></tr></table></td></tr>
<tr><td>CS*</td><td>1</td><td>I</td><td>MPU</td><td>Chip select signal (active low).
Low: LGDP4524 is selected and accessible.
High: LGDP4524 is not selected and not accessible.
Fix to the GND level when not in use.</td></tr>
<tr><td>RS</td><td>1</td><td>I</td><td>MPU</td><td>Register select signal.
Low: selects the index/status register.
High: selects a control register.</td></tr>
<tr><td>WR*_SCL</td><td>1</td><td>I</td><td>MPU</td><td>Write strobe (active low) in 80-system bus interface mode.
Serial clock input in SPI mode.</td></tr>
<tr><td>RD*</td><td>1</td><td>I</td><td>MPU</td><td>Read strobe (active low) in 80-system bus interface mode.
Fix to either IOVcc or GND level in SPI mode.</td></tr>
<tr><td>SDI</td><td>1</td><td>I</td><td>MPU</td><td>Serial data input in SPI mode.
Data are input on the rising edge of the SCL signal. Fix to either IOVcc or GND level when not in use.</td></tr>
<tr><td>SDO</td><td>1</td><td>O</td><td>MPU</td><td>Serial data output in SPI mode.
Data are output on the falling edge of the SCL signal. Leave the pin open when not in use.</td></tr>
<tr><td>DB[17:0]</td><td>18</td><td>I/O</td><td>MPU</td><td>Parallel bidirectional data bus.
Unused pins must be fixed either IOVcc or GND level.</td></tr>
<tr><td>ENABLE</td><td>1</td><td>I</td><td>MPU</td><td>Data enable signal in RGB interface mode.
Low: select (accessible).
High: not select (inaccessible).
The EPL bit inverts the polarity of the ENABLE signal. Fix to either IOVcc or GND level when not in use.</td></tr>
<tr><td>VSYNC</td><td>1</td><td>I</td><td>MPU</td><td>Frame synchronization signal.
When VSPL = “0”, it is active low.
When VSPL = “1”, it is active high.
Fix to either IOVcc or GND level when not in use.</td></tr>
<tr><td>HSYNC</td><td>1</td><td>I</td><td>MPU</td><td>Line synchronization signal.
When HSPL = “0”, it is active low.
When HSPL = “1”, it is active high.
Fix to either IOVcc or GND level when not in use.</td></tr>
<tr><td>DOTCLK</td><td>1</td><td>I</td><td>MPU</td><td>Dot clock signal.
When DPL = “0”, input data on the rising edge of DOTCLK.
When DPL = “1”, input data on the falling edge of DOTCLK.
Fix to either IOVcc or GND level when not in use.</td></tr>
<tr><td>RESET*</td><td>1</td><td>I</td><td>MPU or external RC circuit</td><td>Hardware reset (active low).
Be sure to execute a power-on reset after supplying power.</td></tr>
<tr><td>FLM</td><td>1</td><td>O</td><td>MPU or OPEN</td><td>Frame head pulse signal.
This is used when writing RAM data in synchronization with display frame. Leave the pin open when not in use.</td></tr>
</table>

Name	# pins	I/O	Connected to	Function
S1 to S528	528	O	LCD	Source line outputs to LCD.
G1 to G220	220	O	LCD	Gate line outputs to LCD.
Vcom	1	O	TFT panel common electrode	Supply voltage to the common electrode of TFT panel. Vcom is AC voltages alternating between the VcomH and VcomL levels. The alternating cycle is set by M signal. Connect to the common electrode of TFT panel. All outputs come from the same node.
VcomH	1	O	Stabilizing capacitor	The high level of Vcom AC voltage. Connect to a stabilizing capacitor.
VcomL	1	O	Stabilizing capacitor or OPEN	The low level of Vcom AC voltage. Adjust the VcomL level with the VDV bits. Connect to a stabilizing capacitor. To fix the VcomL level to GND, set VCOMG to “0”. In this case, capacitor connection is not necessary.
VcomR	1	I	Variable resistor or OPEN	Reference level to generate the VcomH level either with an externally connected variable resistor or by setting the register of the LGDP4524. When using a variable resistor, halt the internal VcomH adjusting circuit by setting the register and place the resister between VREG1OUT and GND. When generating the VcomH level by setting the register, leave this pin open.
C11P, C11N	2	-	Step-up capacitor	Pins to connect a capacitor for the internal step-up circuit 1.
C12P, C12N	2	-	Step-up capacitor or GND or OPEN	Pins to connect a capacitor when using the dual mode step-up1 circuit. Leave the pins open or connect to GND, when not using the dual mode step-up1 circuit.
C13P, C13N C21P, C21N C22P, C22N	6	-	Step-up capacitor	Pins to connect capacitors for the internal step-up circuit 2. Connect capacitors according to step-up rate. Leave the pins open when not using the circuit.
OSC1, OSC2	2	I/O	Oscillation resistor	Pins to connect a resistor for RC oscillation.
Vci	1	I	Power supply	Supply voltage to the analog circuit. Connect to an external power supply of 2.5 to 3.3V.
Vci1	1	I/O	Stabilizing capacitor	Internal reference voltage level of amplitude Vci−GND. Place a stabilizing capacitor between GND. Reference voltage input to the step-up circuit 1. When not using the internal reference voltage, connect to an external power supply up to 2.75V.
DDVDH	1	I/O	Stabilizing capacitor, Schottky diode	Output voltage from the step-up circuit 1. Place a stabilizing capacitor between GND. Place a schottky diode between VGH. DDVDH = 4.5 to 5.5V (twice the Vci1 level).Power supply to the source driver’s LCD output unit and an input voltage to the step-up circuit 2.
VGH	1	I/O	Stabilizing capacitor, Schottky diode	An output voltage from the step-up circuit 2. The step-up rate is set with the BT bits. Place a stabilizing capacitor between GND. Place a schottky diode between DDVDH. VGH = max 16.5V (4 to 6 times the Vci1 level) A supply voltage to drive gate lines of the TFT panel.
VGL	1	I/O	Stabilizing capacitor, Schottky diode	An output voltage from the step-up circuit 2. The step-up rate is set with the BT bits. Place a stabilizing capacitor between GND. Place a schottky diode between GND. VGL = min −16.5V (−3 to −5 times the Vci1 level) A supply voltage to drive gate lines of the TFT panel.
VCL	1	I/O	Stabilizing capacitor	An output voltage from the step-up circuit 2. Place a stabilizing capacitor between GND. VCL = 0 to −3.3V (−1 times the Vci1 level) A supply voltage to generate the VcomL level.

Name	# pins	I/O	Connected to	Function
VREG1OUT	1	I/O	Stabilizing capacitor or power supply, variable resistor when generating VcomR	A voltage level of DDVDH−GND, generated from the reference level of Vci−GND according to the rate set with the VRH bits. VREG1OUT is (1) a source driver grayscale reference voltage VDH, (2) a VcomH level reference voltage, and (3) a Vcom amplitude reference voltage. Connect to a stabilizing capacitor. VREG1OUT = 3.0 to (DDVDH – 0.5) V. When using a variable resistor for VcomH(VcomR), place the resister between VREG1OUT and GND.
Vcc	1	-	Power supply	Power supply to generate the internal logic power supply. Vcc= 2.5 to 3.3V
VDD	1	-	Power supply	Generated power supply to the internal logic. VDD = 1.7 to 1.9V
VDDout	1	I/O	Stabilizing capacitor, VDD	Internal logic regulator output.
IOVcc	1	-	Power supply	Power supply to the interface pins: IOVcc = 1.65 to 3.3V. IOVcc and the internal logic voltage VDD must be supplied in the same condition. In case of COG, connect to VDD on the FPC if IOVcc = VDD to prevent noise.
GND	1	-	Power supply	Circuit ground: GND = 0V. In case of COG, connect to GND on the FPC to prevent noise.
TEST1	1	I	GND	Test pin. Be sure to connect to GND. Tie to GNDDUM(Pad No.18) when connecting TEST1 to GND within panel.
VGS	1		GND or external resistor	Reference level for the grayscale voltage generation circuit. The VGS level can be changed by connecting to an external resistor.
VPP	1	I/O	Power Supply Only when EPROM writing , OPEN when not using	7.5V Power supply for internal EPROM writing. After writing, it can be floating.
IOVccDUM	1	-	IOVcc or OPEN	IOVcc Dummy pins.
GNDDUM	1	-	GND or OPEN	GND Dummy pins.
VGLDUM	1	-	VGL or OPEN	VGL Dummy pins.
DUMMY	1	-	OPEN	Dummy pins. Leave them open.

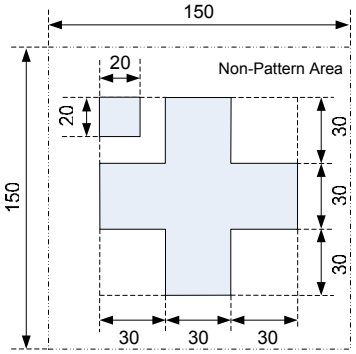
PAD Arrangement

- Chip size: 15.19 mm x 1.06 mm
  (With seal ring but without scribe line)
- Chip thickness: 400 um
- PAD coordinate: PAD center

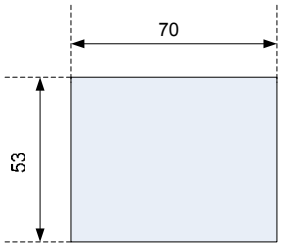
- Au bump size
  1) Nos. 1-208: 50 um x 80 um
  2) Nos. 209-968: 19 um x 110 um

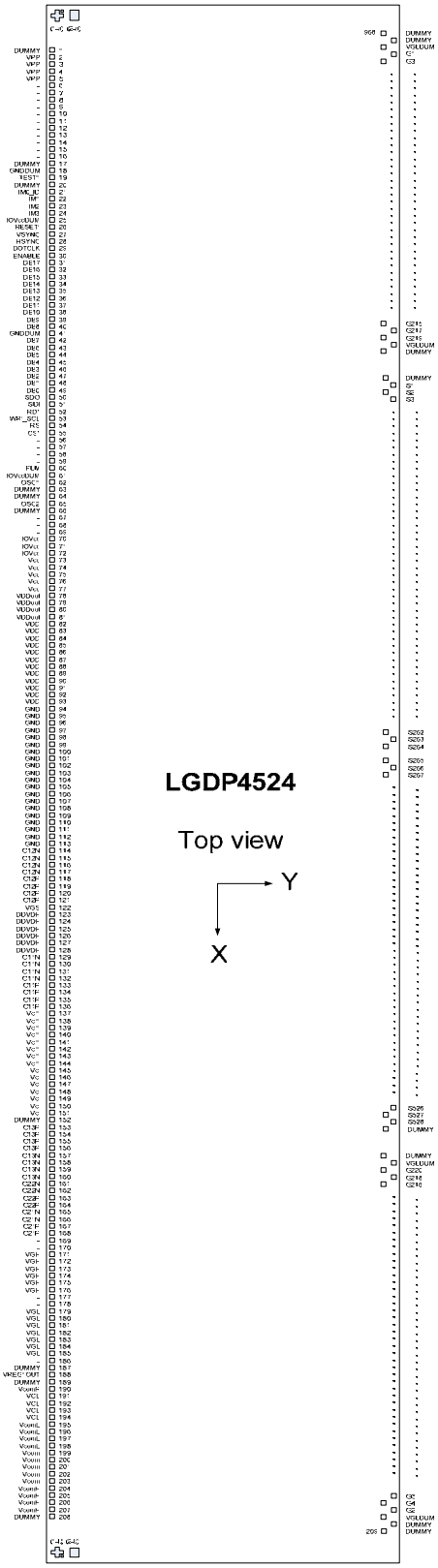
- Alignment marks

1-a, 1-b) Coordinate (X, Y) = (±7465.0, -400.0)



2-a), 2-b) Coordinate (X, Y) = (±7500, -293.0)





PAD Coordinate

Pad #	Pad name	X	Y
1	DUMMY	-7245	-430
2	VPP	-7175	-430
3	VPP	-7105	-430
4	VPP	-7035	-430
5	VPP	-6965	-430
6	-	-6895	-430
7	-	-6825	-430
8	-	-6755	-430
9	-	-6685	-430
10	-	-6615	-430
11	-	-6545	-430
12	-	-6475	-430
13	-	-6405	-430
14	-	-6335	-430
15	-	-6265	-430
16	-	-6195	-430
17	DUMMY	-6125	-430
18	GNDDUM	-6055	-430
19	TEST1	-5985	-430
20	DUMMY	-5915	-430
21	IM0_ID	-5845	-430
22	IM1	-5775	-430
23	IM2	-5705	-430
24	IM3	-5635	-430
25	IOVccDUM	-5565	-430
26	RESET*	-5495	-430
27	VSYNC	-5425	-430
28	HSYNC	-5355	-430
29	DOTCLK	-5285	-430
30	ENABLE	-5215	-430
31	DB17	-5145	-430
32	DB16	-5075	-430
33	DB15	-5005	-430
34	DB14	-4935	-430
35	DB13	-4865	-430
36	DB12	-4795	-430
37	DB11	-4725	-430
38	DB10	-4655	-430
39	DB9	-4585	-430
40	DB8	-4515	-430
41	GNDDUM	-4445	-430
42	DB7	-4375	-430
43	DB6	-4305	-430
44	DB5	-4235	-430
45	DB4	-4165	-430
46	DB3	-4095	-430
47	DB2	-4025	-430
48	DB1	-3955	-430
49	DB0	-3885	-430
50	SDO	-3815	-430
51	SDI	-3745	-430
52	RD	-3675	-430
53	WR_SCL	-3605	-430
54	RS	-3535	-430
55	CS	-3465	-430
56	-	-3395	-430
57	-	-3325	-430
58	-	-3255	-430
59	-	-3185	-430
60	FLM	-3115	-430
61	IOVccDUM	-3045	-430
62	OSC1	-2975	-430
63	DUMMY	-2905	-430
64	DUMMY	-2835	-430
65	OSC2	-2765	-430
66	DUMMY	-2695	-430
67	-	-2625	-430
68	-	-2555	-430
69	-	-2485	-430
70	IOVcc	-2415	-430
71	IOVcc	-2345	-430
72	IOVcc	-2275	-430
73	Vcc	-2205	-430
74	Vcc	-2135	-430
75	Vcc	-2065	-430
76	Vcc	-1995	-430
77	Vcc	-1925	-430
78	VDDout	-1855	-430
79	VDDout	-1785	-430
80	VDDout	-1715	-430
81	VDDout	-1645	-430
82	VDD	-1575	-430
83	VDD	-1505	-430
84	VDD	-1435	-430
85	VDD	-1365	-430
86	VDD	-1295	-430
87	VDD	-1225	-430
88	VDD	-1155	-430
89	VDD	-1085	-430
90	VDD	-1015	-430
91	VDD	-945	-430
92	VDD	-875	-430
93	VDD	-805	-430
94	GND	-735	-430
95	GND	-665	-430
96	GND	-595	-430
97	GND	-525	-430
98	GND	-455	-430
99	GND	-385	-430
100	GND	-315	-430
101	GND	-245	-430
102	GND	-175	-430
103	GND	-105	-430
104	GND	-35	-430
105	GND	35	-430
106	GND	105	-430
107	GND	175	-430
108	GND	245	-430
109	GND	315	-430
110	GND	385	-430
111	GND	455	-430
112	GND	525	-430
113	GND	595	-430
114	C12N	665	-430
115	C12N	735	-430
116	C12N	805	-430
117	C12N	875	-430
118	C12P	945	-430
119	C12P	1015	-430
120	C12P	1085	-430
121	C12P	1155	-430
122	VGS	1225	-430
123	DDVDH	1295	-430
124	DDVDH	1365	-430
125	DDVDH	1435	-430
126	DDVDH	1505	-430
127	DDVDH	1575	-430
128	DDVDH	1645	-430
129	C11N	1715	-430
130	C11N	1785	-430
131	C11N	1855	-430
132	C11N	1925	-430
133	C11P	1995	-430
134	C11P	2065	-430
135	C11P	2135	-430
136	C11P	2205	-430
137	Vci1	2275	-430
138	Vci1	2345	-430
139	Vci1	2415	-430
140	Vci1	2485	-430
141	Vci1	2555	-430
142	Vci1	2625	-430
143	Vci1	2695	-430
144	Vci1	2765	-430
145	Vci	2835	-430
146	Vci	2905	-430
147	Vci	2975	-430
148	Vci	3045	-430
149	Vci	3115	-430
150	Vci	3185	-430
151	Vci	3255	-430
152	DUMMY	3325	-430
153	C13P	3395	-430
154	C13P	3465	-430
155	C13P	3535	-430
156	C13P	3605	-430
157	C13N	3675	-430
158	C13N	3745	-430
159	C13N	3815	-430
160	C13N	3885	-430
161	C22N	3955	-430
162	C22N	4025	-430
163	C22P	4095	-430
164	C22P	4165	-430
165	C21N	4235	-430
166	C21N	4305	-430
167	C21P	4375	-430
168	C21P	4445	-430
169	-	4515	-430
170	-	4585	-430
171	VGH	4655	-430
172	VGH	4725	-430
173	VGH	4795	-430
174	VGH	4865	-430
175	VGH	4935	-430
176	VGH	5005	-430
177	-	5075	-430
178	-	5145	-430
179	VGL	5215	-430
180	VGL	5285	-430
181	VGL	5355	-430
182	VGL	5425	-430
183	VGL	5495	-430
184	VGL	5565	-430
185	VGL	5635	-430
186	-	5705	-430
187	DUMMY	5775	-430
188	VREG1OUT	5845	-430
189	DUMMY	5915	-430
190	VcomR	5985	-430
191	VCL	6055	-430
192	VCL	6125	-430
193	VCL	6195	-430
194	VCL	6265	-430
195	VcomL	6335	-430
196	VcomL	6405	-430
197	VcomL	6475	-430
198	VcomL	6545	-430
199	Vcom	6615	-430
200	Vcom	6685	-430
201	Vcom	6755	-430
202	Vcom	6825	-430
203	Vcom	6895	-430
204	VcomH	6965	-430
205	VcomH	7035	-430
206	VcomH	7105	-430
207	VcomH	7175	-430
208	DUMMY	7245	-430
209	DUMMY	7429	278
210	DUMMY	7410	413
211	VGLDUM	7391	278
212	G2	7372	413
213	G4	7353	278
214	G6	7334	413
215	G8	7315	278
216	G10	7296	413
217	G12	7277	278
218	G14	7258	413
219	G16	7239	278
220	G18	7220	413
221	G20	7201	278
222	G22	7182	413
223	G24	7163	278
224	G26	7144	413
225	G28	7125	278
226	G30	7106	413
227	G32	7087	278
228	G34	7068	413
229	G36	7049	278
230	G38	7030	413
231	G40	7011	278
232	G42	6992	413
233	G44	6973	278
234	G46	6954	413
235	G48	6935	278
236	G50	6916	413
237	G52	6897	278
238	G54	6878	413
239	G56	6859	278
240	G58	6840	413
241	G60	6821	278
242	G62	6802	413
243	G64	6783	278
244	G66	6764	413
245	G68	6745	278
246	G70	6726	413
247	G72	6707	278
248	G74	6688	413
249	G76	6669	278

Pad #	Pad name	X	Y
250	G78	6650	413
251	G80	6631	278
252	G82	6612	413
253	G84	6593	278
254	G86	6574	413
255	G88	6555	278
256	G90	6536	413
257	G92	6517	278
258	G94	6498	413
259	G96	6479	278
260	G98	6460	413
261	G100	6441	278
262	G102	6422	413
263	G104	6403	278
264	G106	6384	413
265	G108	6365	278
266	G110	6346	413
267	G112	6327	278
268	G114	6308	413
269	G116	6289	278
270	G118	6270	413
271	G120	6251	278
272	G122	6232	413
273	G124	6213	278
274	G126	6194	413
275	G128	6175	278
276	G130	6156	413
277	G132	6137	278
278	G134	6118	413
279	G136	6099	278
280	G138	6080	413
281	G140	6061	278
282	G142	6042	413
283	G144	6023	278
284	G146	6004	413
285	G148	5985	278
286	G150	5966	413
287	G152	5947	278
288	G154	5928	413
289	G156	5909	278
290	G158	5890	413
291	G160	5871	278
292	G162	5852	413
293	G164	5833	278
294	G166	5814	413
295	G168	5795	278
296	G170	5776	413
297	G172	5757	278
298	G174	5738	413
299	G176	5719	278
300	G178	5700	413
301	G180	5681	278
302	G182	5662	413
303	G184	5643	278
304	G186	5624	413
305	G188	5605	278
306	G190	5586	413
307	G192	5567	278
308	G194	5548	413
309	G196	5529	278
310	G198	5510	413
311	G200	5491	278
312	G202	5472	413
313	G204	5453	278
314	G206	5434	413
315	G208	5415	278
316	G210	5396	413
317	G212	5377	278
318	G214	5358	413
319	G216	5339	278
320	G218	5320	413
321	G220	5301	278
322	VGLDUM	5282	413
323	DUMMY	5263	278
324	DUMMY	5035	278
325	S528	5016	413
326	S527	4997	278
327	S526	4978	413
328	S525	4959	278
329	S524	4940	413
330	S523	4921	278
331	S522	4902	413
332	S521	4883	278
333	S520	4864	413
334	S519	4845	278
335	S518	4826	413
336	S517	4807	278

Pad #	Pad name	X	Y
337	S516	4788	413
338	S515	4769	278
339	S514	4750	413
340	S513	4731	278
341	S512	4712	413
342	S511	4693	278
343	S510	4674	413
344	S509	4655	278
345	S508	4636	413
346	S507	4617	278
347	S506	4598	413
348	S505	4579	278
349	S504	4560	413
350	S503	4541	278
351	S502	4522	413
352	S501	4503	278
353	S500	4484	413
354	S499	4465	278
355	S498	4446	413
356	S497	4427	278
357	S496	4408	413
358	S495	4389	278
359	S494	4370	413
360	S493	4351	278
361	S492	4332	413
362	S491	4313	278
363	S490	4294	413
364	S489	4275	278
365	S488	4256	413
366	S487	4237	278
367	S486	4218	413
368	S485	4199	278
369	S484	4180	413
370	S483	4161	278
371	S482	4142	413
372	S481	4123	278
373	S480	4104	413
374	S479	4085	278
375	S478	4066	413
376	S477	4047	278
377	S476	4028	413
378	S475	4009	278
379	S474	3990	413
380	S473	3971	278
381	S472	3952	413
382	S471	3933	278
383	S470	3914	413
384	S469	3895	278
385	S468	3876	413
386	S467	3857	278
387	S466	3838	413
388	S465	3819	278
389	S464	3800	413
390	S463	3781	278
391	S462	3762	413
392	S461	3743	278
393	S460	3724	413
394	S459	3705	278
395	S458	3686	413
396	S457	3667	278
397	S456	3648	413
398	S455	3629	278
399	S454	3610	413
400	S453	3591	278
401	S452	3572	413
402	S451	3553	278
403	S450	3534	413
404	S449	3515	278
405	S448	3496	413
406	S447	3477	278
407	S446	3458	413
408	S445	3439	278
409	S444	3420	413
410	S443	3401	278
411	S442	3382	413
412	S441	3363	278
413	S440	3344	413
414	S439	3325	278
415	S438	3306	413
416	S437	3287	278
417	S436	3268	413
418	S435	3249	278
419	S434	3230	413
420	S433	3211	278
421	S432	3192	413
422	S431	3173	278
423	S430	3154	413

Pad #	Pad name	X	Y
424	S429	3135	278
425	S428	3116	413
426	S427	3097	278
427	S426	3078	413
428	S425	3059	278
429	S424	3040	413
430	S423	3021	278
431	S422	3002	413
432	S421	2983	278
433	S420	2964	413
434	S419	2945	278
435	S418	2926	413
436	S417	2907	278
437	S416	2888	413
438	S415	2869	278
439	S414	2850	413
440	S413	2831	278
441	S412	2812	413
442	S411	2793	278
443	S410	2774	413
444	S409	2755	278
445	S408	2736	413
446	S407	2717	278
447	S406	2698	413
448	S405	2679	278
449	S404	2660	413
450	S403	2641	278
451	S402	2622	413
452	S401	2603	278
453	S400	2584	413
454	S399	2565	278
455	S398	2546	413
456	S397	2527	278
457	S396	2508	413
458	S395	2489	278
459	S394	2470	413
460	S393	2451	278
461	S392	2432	413
462	S391	2413	278
463	S390	2394	413
464	S389	2375	278
465	S388	2356	413
466	S387	2337	278
467	S386	2318	413
468	S385	2299	278
469	S384	2280	413
470	S383	2261	278
471	S382	2242	413
472	S381	2223	278
473	S380	2204	413
474	S379	2185	278
475	S378	2166	413
476	S377	2147	278
477	S376	2128	413
478	S375	2109	278
479	S374	2090	413
480	S373	2071	278
481	S372	2052	413
482	S371	2033	278
483	S370	2014	413
484	S369	1995	278
485	S368	1976	413
486	S367	1957	278
487	S366	1938	413
488	S365	1919	278
489	S364	1900	413
490	S363	1881	278
491	S362	1862	413
492	S361	1843	278
493	S360	1824	413
494	S359	1805	278
495	S358	1786	413
496	S357	1767	278
497	S356	1748	413
498	S355	1729	278
499	S354	1710	413
500	S353	1691	278
501	S352	1672	413
502	S351	1653	278
503	S350	1634	413
504	S349	1615	278
505	S348	1596	413
506	S347	1577	278
507	S346	1558	413
508	S345	1539	278
509	S344	1520	413
510	S343	1501	278

Pad #	Pad name	X	Y
511	S342	1482	413
512	S341	1463	278
513	S340	1444	413
514	S339	1425	278
515	S338	1406	413
516	S337	1387	278
517	S336	1368	413
518	S335	1349	278
519	S334	1330	413
520	S333	1311	278
521	S332	1292	413
522	S331	1273	278
523	S330	1254	413
524	S329	1235	278
525	S328	1216	413
526	S327	1197	278
527	S326	1178	413
528	S325	1159	278
529	S324	1140	413
530	S323	1121	278
531	S322	1102	413
532	S321	1083	278
533	S320	1064	413
534	S319	1045	278
535	S318	1026	413
536	S317	1007	278
537	S316	988	413
538	S315	969	278
539	S314	950	413
540	S313	931	278
541	S312	912	413
542	S311	893	278
543	S310	874	413
544	S309	855	278
545	S308	836	413
546	S307	817	278
547	S306	798	413
548	S305	779	278
549	S304	760	413
550	S303	741	278
551	S302	722	413
552	S301	703	278
553	S300	684	413
554	S299	665	278
555	S298	646	413
556	S297	627	278
557	S296	608	413
558	S295	589	278
559	S294	570	413
560	S293	551	278
561	S292	532	413
562	S291	513	278
563	S290	494	413
564	S289	475	278
565	S288	456	413
566	S287	437	278
567	S286	418	413
568	S285	399	278
569	S284	380	413
570	S283	361	278
571	S282	342	413
572	S281	323	278
573	S280	304	413
574	S279	285	278
575	S278	266	413
576	S277	247	278
577	S276	228	413
578	S275	209	278
579	S274	190	413
580	S273	171	278
581	S272	152	413
582	S271	133	278
583	S270	114	413
584	S269	95	278
585	S268	76	413
586	S267	57	278
587	S266	38	413
588	S265	19	278
589	S264	-19	278
590	S263	-38	413
591	S262	-57	278
592	S261	-76	413
593	S260	-95	278
594	S259	-114	413
595	S258	-133	278
596	S257	-152	413
597	S256	-171	278

Pad #	Pad name	X	Y
598	S255	-190	413
599	S254	-209	278
600	S253	-228	413
601	S252	-247	278
602	S251	-266	413
603	S250	-285	278
604	S249	-304	413
605	S248	-323	278
606	S247	-342	413
607	S246	-361	278
608	S245	-380	413
609	S244	-399	278
610	S243	-418	413
611	S242	-437	278
612	S241	-456	413
613	S240	-475	278
614	S239	-494	413
615	S238	-513	278
616	S237	-532	413
617	S236	-551	278
618	S235	-570	413
619	S234	-589	278
620	S233	-608	413
621	S232	-627	278
622	S231	-646	413
623	S230	-665	278
624	S229	-684	413
625	S228	-703	278
626	S227	-722	413
627	S226	-741	278
628	S225	-760	413
629	S224	-779	278
630	S223	-798	413
631	S222	-817	278
632	S221	-836	413
633	S220	-855	278
634	S219	-874	413
635	S218	-893	278
636	S217	-912	413
637	S216	-931	278
638	S215	-950	413
639	S214	-969	278
640	S213	-988	413
641	S212	-1007	278
642	S211	-1026	413
643	S210	-1045	278
644	S209	-1064	413
645	S208	-1083	278
646	S207	-1102	413
647	S206	-1121	278
648	S205	-1140	413
649	S204	-1159	278
650	S203	-1178	413
651	S202	-1197	278
652	S201	-1216	413
653	S200	-1235	278
654	S199	-1254	413
655	S198	-1273	278
656	S197	-1292	413
657	S196	-1311	278
658	S195	-1330	413
659	S194	-1349	278
660	S193	-1368	413
661	S192	-1387	278
662	S191	-1406	413
663	S190	-1425	278
664	S189	-1444	413
665	S188	-1463	278
666	S187	-1482	413
667	S186	-1501	278
668	S185	-1520	413
669	S184	-1539	278
670	S183	-1558	413
671	S182	-1577	278
672	S181	-1596	413
673	S180	-1615	278
674	S179	-1634	413
675	S178	-1653	278
676	S177	-1672	413
677	S176	-1691	278
678	S175	-1710	413
679	S174	-1729	278
680	S173	-1748	413
681	S172	-1767	278
682	S171	-1786	413
683	S170	-1805	278
684	S169	-1824	413

Pad #	Pad name	X	Y
685	S168	-1843	278
686	S167	-1862	413
687	S166	-1881	278
688	S165	-1900	413
689	S164	-1919	278
690	S163	-1938	413
691	S162	-1957	278
692	S161	-1976	413
693	S160	-1995	278
694	S159	-2014	413
695	S158	-2033	278
696	S157	-2052	413
697	S156	-2071	278
698	S155	-2090	413
699	S154	-2109	278
700	S153	-2128	413
701	S152	-2147	278
702	S151	-2166	413
703	S150	-2185	278
704	S149	-2204	413
705	S148	-2223	278
706	S147	-2242	413
707	S146	-2261	278
708	S145	-2280	413
709	S144	-2299	278
710	S143	-2318	413
711	S142	-2337	278
712	S141	-2356	413
713	S140	-2375	278
714	S139	-2394	413
715	S138	-2413	278
716	S137	-2432	413
717	S136	-2451	278
718	S135	-2470	413
719	S134	-2489	278
720	S133	-2508	413
721	S132	-2527	278
722	S131	-2546	413
723	S130	-2565	278
724	S129	-2584	413
725	S128	-2603	278
726	S127	-2622	413
727	S126	-2641	278
728	S125	-2660	413
729	S124	-2679	278
730	S123	-2698	413
731	S122	-2717	278
732	S121	-2736	413
733	S120	-2755	278
734	S119	-2774	413
735	S118	-2793	278
736	S117	-2812	413
737	S116	-2831	278
738	S115	-2850	413
739	S114	-2869	278
740	S113	-2888	413
741	S112	-2907	278
742	S111	-2926	413
743	S110	-2945	278
744	S109	-2964	413
745	S108	-2983	278
746	S107	-3002	413
747	S106	-3021	278
748	S105	-3040	413
749	S104	-3059	278
750	S103	-3078	413
751	S102	-3097	278
752	S101	-3116	413
753	S100	-3135	278
754	S99	-3154	413
755	S98	-3173	278
756	S97	-3192	413
757	S96	-3211	278
758	S95	-3230	413
759	S94	-3249	278
760	S93	-3268	413
761	S92	-3287	278
762	S91	-3306	413
763	S90	-3325	278
764	S89	-3344	413
765	S88	-3363	278
766	S87	-3382	413
767	S86	-3401	278
768	S85	-3420	413
769	S84	-3439	278
770	S83	-3458	413
771	S82	-3477	278

Pad #	Pad name	X	Y
772	S81	-3496	413
773	S80	-3515	278
774	S79	-3534	413
775	S78	-3553	278
776	S77	-3572	413
777	S76	-3591	278
778	S75	-3610	413
779	S74	-3629	278
780	S73	-3648	413
781	S72	-3667	278
782	S71	-3686	413
783	S70	-3705	278
784	S69	-3724	413
785	S68	-3743	278
786	S67	-3762	413
787	S66	-3781	278
788	S65	-3800	413
789	S64	-3819	278
790	S63	-3838	413
791	S62	-3857	278
792	S61	-3876	413
793	S60	-3895	278
794	S59	-3914	413
795	S58	-3933	278
796	S57	-3952	413
797	S56	-3971	278
798	S55	-3990	413
799	S54	-4009	278
800	S53	-4028	413
801	S52	-4047	278
802	S51	-4066	413
803	S50	-4085	278
804	S49	-4104	413
805	S48	-4123	278
806	S47	-4142	413
807	S46	-4161	278
808	S45	-4180	413
809	S44	-4199	278
810	S43	-4218	413
811	S42	-4237	278
812	S41	-4256	413
813	S40	-4275	278
814	S39	-4294	413
815	S38	-4313	278
816	S37	-4332	413
817	S36	-4351	278
818	S35	-4370	413
819	S34	-4389	278
820	S33	-4408	413
821	S32	-4427	278
822	S31	-4446	413
823	S30	-4465	278
824	S29	-4484	413
825	S28	-4503	278
826	S27	-4522	413
827	S26	-4541	278
828	S25	-4560	413
829	S24	-4579	278
830	S23	-4598	413
831	S22	-4617	278
832	S21	-4636	413
833	S20	-4655	278
834	S19	-4674	413
835	S18	-4693	278
836	S17	-4712	413
837	S16	-4731	278
838	S15	-4750	413
839	S14	-4769	278
840	S13	-4788	413

Pad #	Pad name	X	Y
841	S12	-4807	278
842	S11	-4826	413
843	S10	-4845	278
844	S9	-4864	413
845	S8	-4883	278
846	S7	-4902	413
847	S6	-4921	278
848	S5	-4940	413
849	S4	-4959	278
850	S3	-4978	413
851	S2	-4997	278
852	S1	-5016	413
853	DUMMY	-5035	278
854	DUMMY	-5263	278
855	VGLDUM	-5282	413
856	G219	-5301	278
857	G217	-5320	413
858	G215	-5339	278
859	G213	-5358	413
860	G211	-5377	278
861	G209	-5396	413
862	G207	-5415	278
863	G205	-5434	413
864	G203	-5453	278
865	G201	-5472	413
866	G199	-5491	278
867	G197	-5510	413
868	G195	-5529	278
869	G193	-5548	413
870	G191	-5567	278
871	G189	-5586	413
872	G187	-5605	278
873	G185	-5624	413
874	G183	-5643	278
875	G181	-5662	413
876	G179	-5681	278
877	G177	-5700	413
878	G175	-5719	278
879	G173	-5738	413
880	G171	-5757	278
881	G169	-5776	413
882	G167	-5795	278
883	G165	-5814	413
884	G163	-5833	278
885	G161	-5852	413
886	G159	-5871	278
887	G157	-5890	413
888	G155	-5909	278
889	G153	-5928	413
890	G151	-5947	278
891	G149	-5966	413
892	G147	-5985	278
893	G145	-6004	413
894	G143	-6023	278
895	G141	-6042	413
896	G139	-6061	278
897	G137	-6080	413
898	G135	-6099	278
899	G133	-6118	413
900	G131	-6137	278
901	G129	-6156	413
902	G127	-6175	278
903	G125	-6194	413
904	G123	-6213	278
905	G121	-6232	413
906	G119	-6251	278
907	G117	-6270	413
908	G115	-6289	278
909	G113	-6308	413

Pad #	Pad name	X	Y
910	G111	-6327	278
911	G109	-6346	413
912	G107	-6365	278
913	G105	-6384	413
914	G103	-6403	278
915	G101	-6422	413
916	G99	-6441	278
917	G97	-6460	413
918	G95	-6479	278
919	G93	-6498	413
920	G91	-6517	278
921	G89	-6536	413
922	G87	-6555	278
923	G85	-6574	413
924	G83	-6593	278
925	G81	-6612	413
926	G79	-6631	278
927	G77	-6650	413
928	G75	-6669	278
929	G73	-6688	413
930	G71	-6707	278
931	G69	-6726	413
932	G67	-6745	278
933	G65	-6764	413
934	G63	-6783	278
935	G61	-6802	413
936	G59	-6821	278
937	G57	-6840	413
938	G55	-6859	278
939	G53	-6878	413
940	G51	-6897	278
941	G49	-6916	413
942	G47	-6935	278
943	G45	-6954	413
944	G43	-6973	278
945	G41	-6992	413
946	G39	-7011	278
947	G37	-7030	413
948	G35	-7049	278
949	G33	-7068	413
950	G31	-7087	278
951	G29	-7106	413
952	G27	-7125	278
953	G25	-7144	413
954	G23	-7163	278
955	G21	-7182	413
956	G19	-7201	278
957	G17	-7220	413
958	G15	-7239	278
959	G13	-7258	413
960	G11	-7277	278
961	G9	-7296	413
962	G7	-7315	278
963	G5	-7334	413
964	G3	-7353	278
965	G1	-7372	413
966	VGLDUM	-7391	278
967	DUMMY	-7410	413
968	DUMMY	-7429	278

Alignment mark	X	Y
(1-a)	-7465	-400
(1-b)	7465	-400
(2-a)	-7500	-293
(2-b)	7500	-293

Bump Arrangement

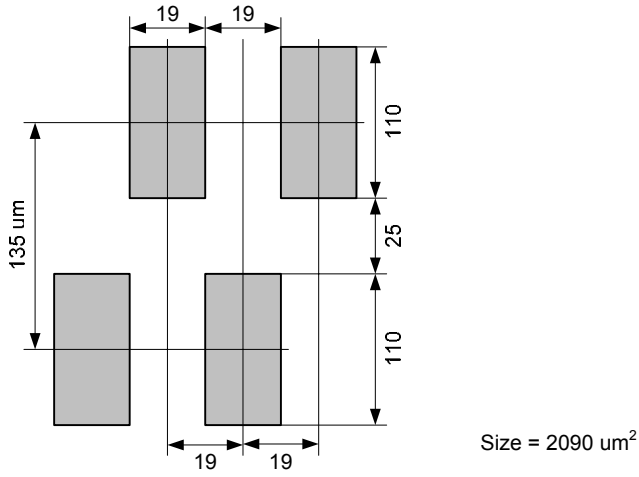
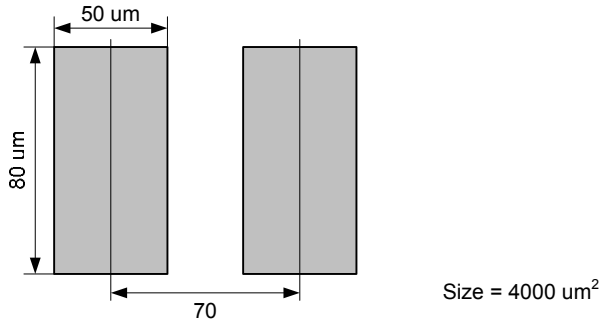
S1 – S528 G1 – G220	
I/O pins	

Figure 2 Bump Arrangement

Block Function

System Interface

The LGDP4524 supports 2-system high-speed interfaces: 80-system high-speed interfaces to 8-, 9-, 16-, 18-bit parallel ports and a Serial Peripheral Interface (SPI). The interface mode is selected by setting the IM[3:0] pins.

The LGDP4524 has a 16-bit index register (IR); an 18-bit write-data register (WDR); and an 18-bit read-data register (RDR). The IR is the register to store index information from control registers and the internal GRAM. The WDR is the register to temporarily store data to be written to control registers and the internal GRAM. The RDR is the register to temporarily store data read from the GRAM. Data from the MPU to be written to the internal GRAM are first written to the WDR and then automatically written to the internal GRAM in internal operation. Data are read via the RDR from the internal GRAM. Therefore, invalid data are read out to the data bus when the LGDP4524 read the first data from the internal GRAM. Valid data are read out after the LGDP4524 performs the second read operation.

Instructions are written consecutively as the instruction execution time except starting oscillator takes 0 clock cycle.

Table 3: Register Selection (80-system 8-/9-/16-/18-bit Parallel Interface)

80-system I/F			Function
WR*	RD*	RS	
0	1	0	Write an index to IR
1	0	0	Read an internal status
0	1	1	Write to control registers or the internal GRAM via WDR
1	0	1	Read from the internal GRAM via RDR

Table 4: Register Selection (Serial Peripheral Interface)

Start Byte (SPI)		Function
R/W	RS	
0	0	Write an index to IR
1	0	Read an internal status
0	1	Write into control registers and the internal GRAM via WDR
1	1	Read from the internal GRAM via RDR

External Display Interface

The LGDP4524 supports the RGB interface and the VSYNC interface as the external interface for displaying a moving picture. When the RGB interface is selected, display operations are synchronized with externally supplied signals, VSYNC, HSYNC, and DOTCLK. In RGB interface mode, data (DB[17:0]) are written in synchronization with these signals according to the polarity of enable signal (ENABLE) to prevent flicker on display while updating display data.

In VSYNC interface mode, the display operation is synchronized with the internal clock except frame synchronization, where the operation is synchronized with the VSYNC signal. Display data are written to the internal GRAM via the system interface. In this case, there are constraints in speed and method in writing data to the internal RAM. For details, see the “External Display Interface” section.

The LGDP4524 allows for switching between the external display interface and the system interface by instruction so that the optimum interface is selected for the kind of picture to be displayed on the screen (still and/or moving picture(s)). The RGB interface, by writing all display data to the internal RAM, allows for transferring data only when updating the frames of a moving picture, contributing to low power requirement for moving picture display.

Bit Operations

The LGDP4524 supports a write data mask function for selectively writing data to the internal RAM in units of bits and a logical/compare operation to write data to the GRAM only when a condition is met as a result of comparing the data and the compare register bits.

Address Counter (AC)

The address counter (AC) gives an address to the internal GRAM. When the index of the register for setting a RAM address in the AC is written to the IR, the address information is sent from the IR to the AC. As writing data to the internal GRAM, the address in the AC is automatically updated plus or minus 1. The window address function enables writing data only in the rectangular area arbitrarily set by users on the GRAM.

Graphics RAM (GRAM)

GRAM is graphics RAM storing bit-pattern data of 87,120 (176 x 220 x 18/8) bytes, using 18 bits per pixel.

Grayscale Voltage Generating Circuit

The grayscale voltage generating circuit generates a liquid crystal drive voltage according to grayscale data set in the γ-correction register to display in 262,144 colors. For details, see the "γ-Correction Function" section.

Timing Generator

The timing generator generates a timing signal for operation of internal circuits such as the internal GRAM. The timing for the display operation such as RAM read operation and the timing for the internal operation such as access from the MPU are generated in the way not to interfere each other.

Oscillator (OSC)

The LGDP4524 generates RC oscillation with an external oscillation resistor placed between the OSC1 and OSC2 pins. The oscillation frequency is changed according to the value of an external resistor. Adjust the oscillation frequency in accordance to the operating voltage or the frame frequency. An operating clock can be input externally. During standby mode, RC oscillation is halted to reduce power consumption. For details, see "Oscillator" section.

LCD Driver Circuit

The LCD driver circuit of the LGDP4524 consists of a 528-output source driver (S1 to S528) and a 220-output gate driver (G1 to G220). Display pattern data are latched when the 528th bit data are input. The latched data control the source driver and generate a drive waveform. The gate driver for scanning gate lines outputs either VGH or VGL level. The shift direction of 528-bit source outputs from the source driver is set with the SS bit and the shift direction of gate outputs from the gate driver is set with the GS bit. The scan mode by the gate driver is set with the SM bit. These bits allow setting an appropriate scan method for an LCD module.

LCD Drive Power Supply Circuit

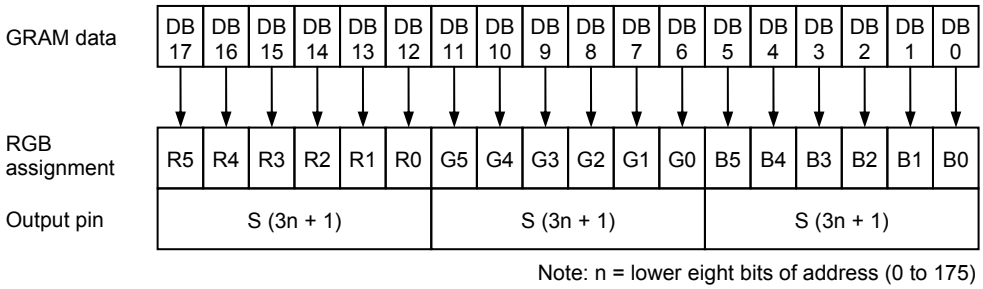
The LCD drive power supply circuit generates the voltage levels VREG1OUT, VGH, VGL and Vcom for driving an LCD.

GRAM Address MAP

Table 5: GRAM address and display panel position (SS = "0", BGR = "0")

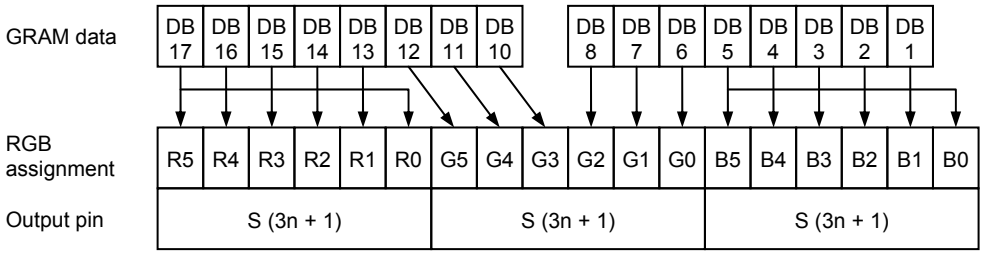
S/G pin		S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	…	S517	S518	S519	S520	S521	S522	S523	S524	S525	S526	S527	S528
GS=0	GS=1	DB[17:0]			DB[17:0]			DB[17:0]			DB[17:0]			…	DB[17:0]			DB[17:0]			DB[17:0]			DB[17:0]		
G1	G240	0000			0001			0002			0003			…	00AC			00AD			00AE			00AF		
G2	G239	0100			0101			0102			0103			…	01AC			01AD			01AE			01AF		
G3	G238	0200			0201			0202			0203			…	02AC			02AD			02AE			02AF		
G4	G237	0300			0301			0302			0303			…	03AC			03AD			03AE			03AF		
G5	G236	0400			0401			0402			0403			…	04AC			04AD			04AE			04AF		
G6	G235	0500			0501			0502			0503			…	05AC			05AD			05AE			05AF		
G7	G234	0600			0601			0602			0603			…	06AC			06AD			06AE			06AF		
G8	G233	0700			0701			0702			0703			…	07AC			07AD			07AE			07AF		
G9	G232	0800			0801			0802			0803			…	08AC			08AD			08AE			08AF		
G10	G231	0900			0901			0902			0903			…	09AC			09AD			09AE			09AF		
G11	G230	0A00			0A01			0A02			0A03			…	0AAC			0AAD			0AAE			0AAF		
G12	G229	0B00			0B01			0B02			0B03			…	0BAC			0BAD			0BAE			0BAF		
G13	G228	0C00			0C01			0C02			0C03			…	0CAC			0CAD			0CAE			0CAF		
G14	G227	0D00			0D01			0D02			0D03			…	0DAC			0DAD			0DAE			0DAF		
G15	G226	0E00			0E01			0E02			0E03			…	0EAC			0EAD			0EAE			0EAF		
G16	G225	0F00			0F01			0F02			0F03			…	0FAC			0FAD			0FAE			0FAF		
G17	G224	1000			1001			1002			1003			…	10AC			10AD			10AE			10AF		
G18	G223	1100			1101			1102			1103			…	11AC			11AD			11AE			11AF		
G19	G222	1200			1201			1202			1203			…	12AC			12AD			12AE			12AF		
G20	G221	1300			1301			1302			1303			…	13AC			13AD			13AE			13AF		
⋮	⋮	⋮			⋮			⋮			⋮			⋮	⋮			⋮			⋮			⋮		
G233	G8	E800			E801			E802			E803			…	E8AC			E8AD			E8AE			E8AF		
G234	G7	E900			E901			E902			E903			…	E9AC			E9AD			E9AE			E9AF		
G235	G6	EA00			EA01			EA02			EA03			…	EAAC			EAAD			EAAE			EAAF		
G237	G5	EB00			EB01			EB02			EB03			…	EBAC			EBAD			EBAE			EBAF		
G237	G4	EC00			EC01			EC02			EC03			…	ECAC			ECAD			ECAE			ECAF		
G238	G3	ED00			ED01			ED02			ED03			…	EDAC			EDAD			EDAE			EDAF		
G239	G2	EE00			EE01			EE02			EE03			…	EEAC			EEAD			EEAE			EEAF		
G240	G1	EF00			EF01			EF02			EF03			…	EFAC			EFAD			EFAE			EFAF		

18-bit interface (262k colors)



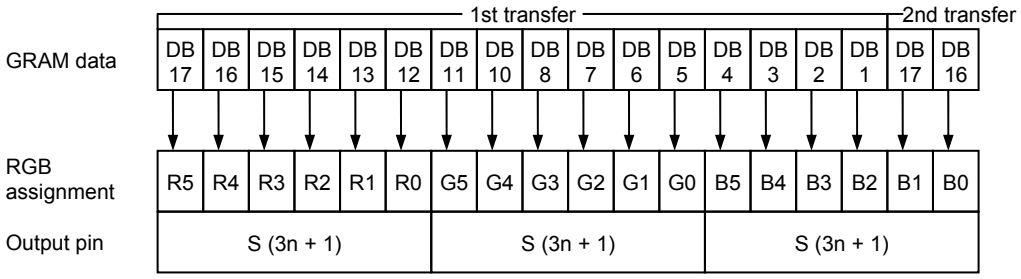
Note: n = lower eight bits of address (0 to 175)

16-bit interface (65k colors) – TRI = "0"



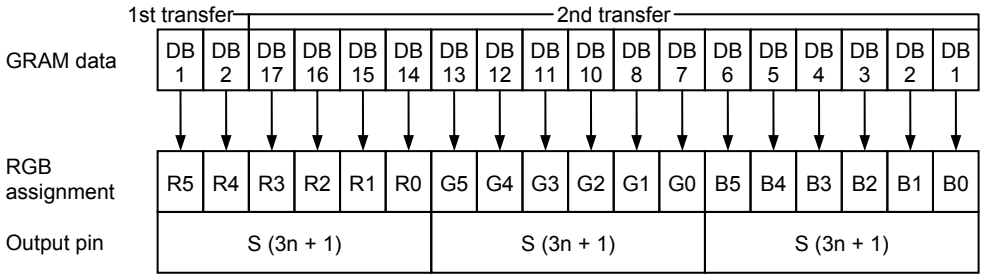
Note: n = lower eight bits of address (0 to 175)

16-bit interface (2 transfers/pixel, 262k colors) – TRI = "1", DFM = "0"



Note: n = lower eight bits of address (0 to 175)

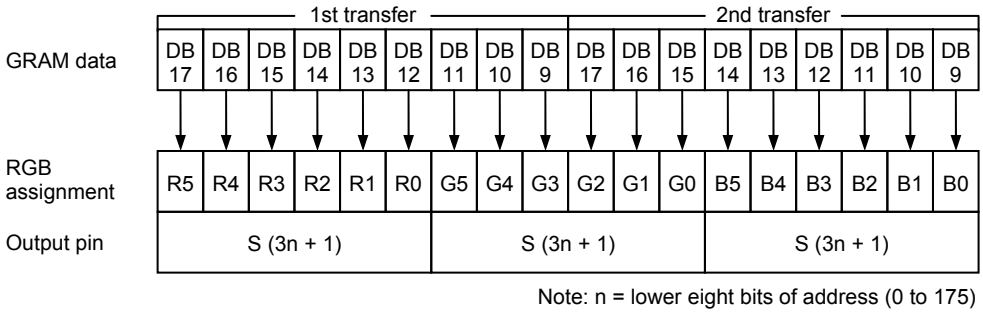
16-bit interface (2 transfers/pixel, 262k colors) – TRI = "1", DFM = "1"



Note: n = lower eight bits of address (0 to 175)

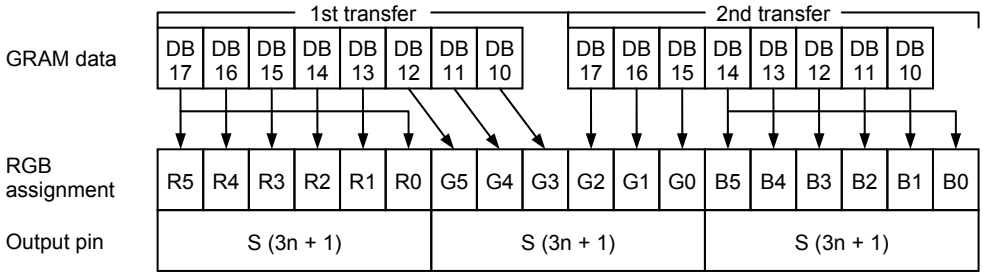
Figure 3: GRAM data and display data: system interface (SS = "0", BGR = "0")

9-bit interface (262k colors)



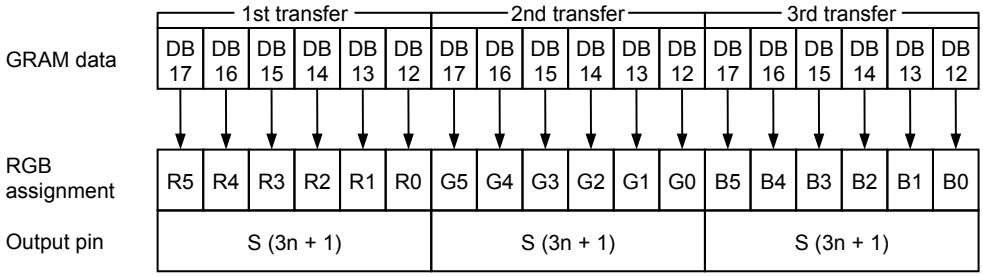
Note: n = lower eight bits of address (0 to 175)

8-bit interface or SPI (2 transfers/pixel, 65k colors) – TRI = "0"



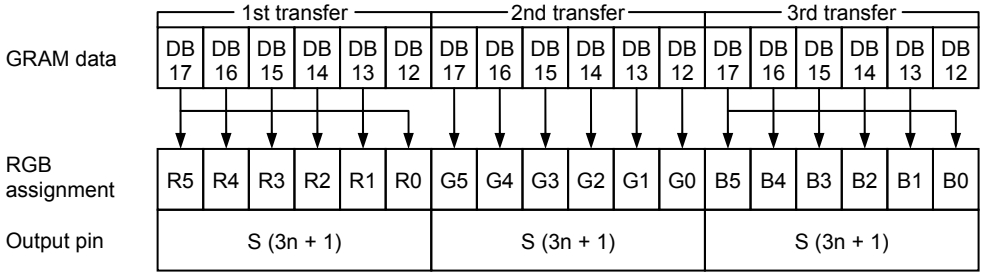
Note: n = lower eight bits of address (0 to 175)

8-bit interface or SPI (3 transfers/pixel, 262k colors) – TRI = "1", DFM = "0"



Note: n = lower eight bits of address (0 to 175)

8-bit interface (3 transfers/pixel, 65k colors) – TRI = "1", DFM = "1"



Note: n = lower eight bits of address (0 to 175)

Figure 4: GRAM data and display data: system interface (SS = "0", BGR = "0")

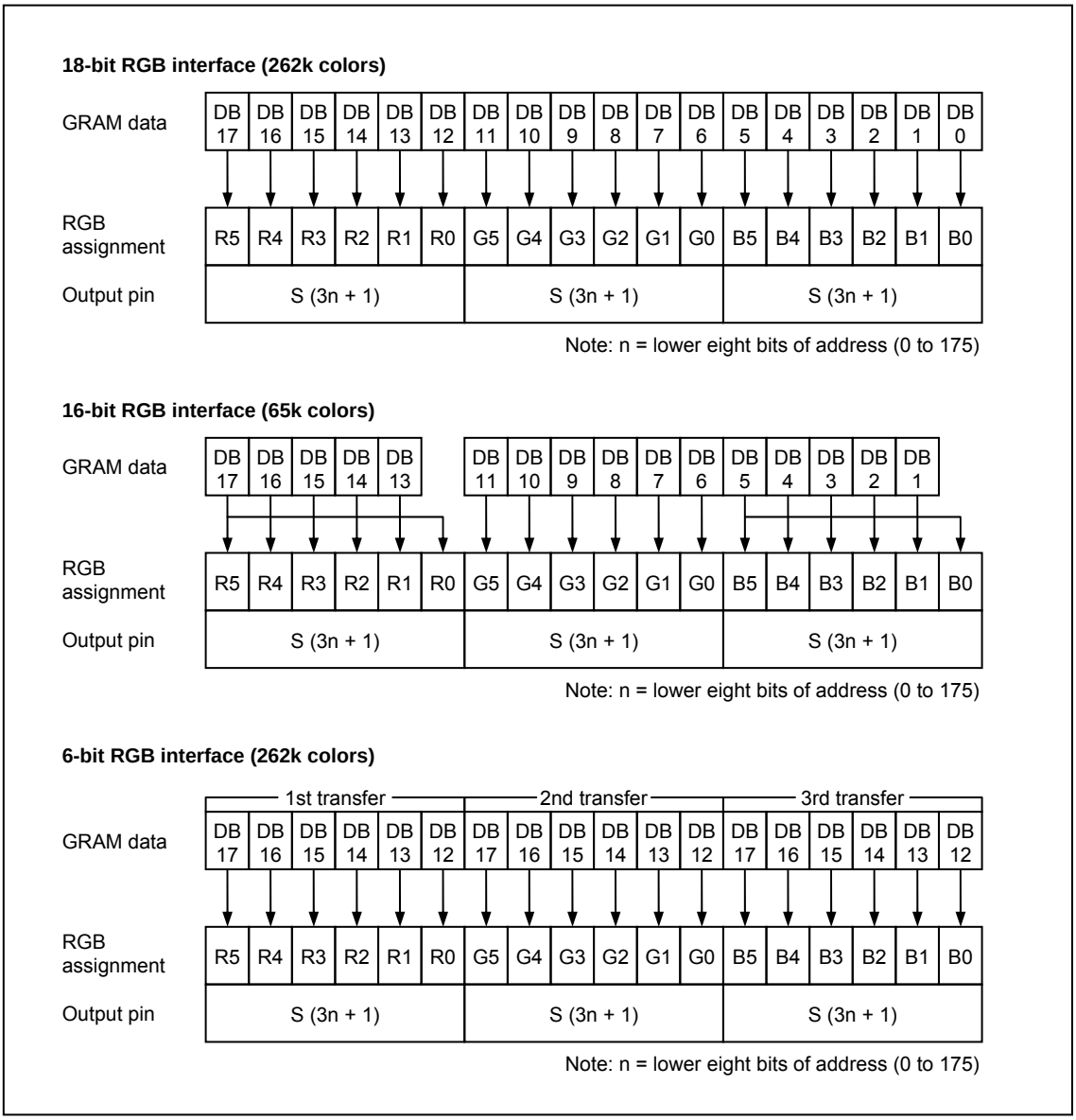
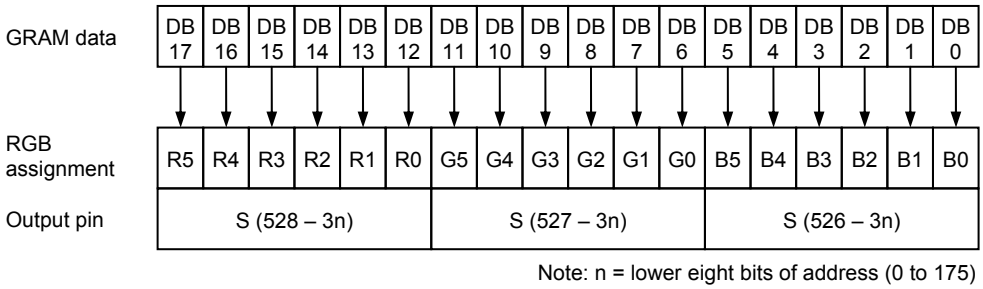


Figure 5: GRAM data and display data: system interface (SS = "0", BGR = "0")

Table 6: GRAM address and display panel position (SS = “1”, BGR = “1”)

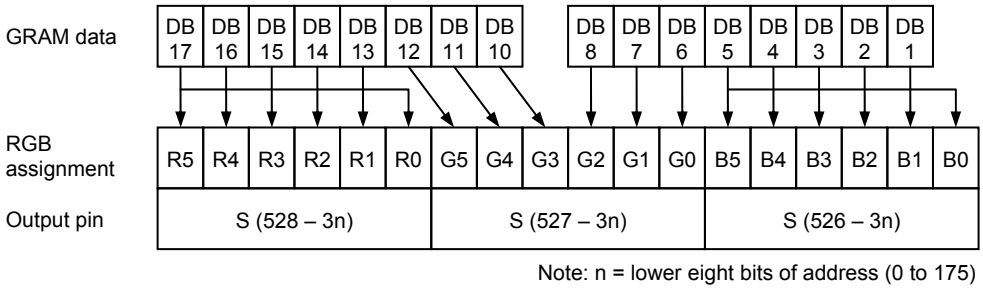
S/G pin		S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	…	S517	S518	S519	S520	S521	S522	S523	S524	S525	S526	S527	S528
GS=0	GS=1	DB[17:0]			DB[17:0]			DB[17:0]			DB[17:0]			…	DB[17:0]			DB[17:0]			DB[17:0]			DB[17:0]		
G1	G240	00AF			00AE			00AD			00AC			…	0003			0002			0001			0000		
G2	G239	01AF			01AE			01AD			01AC			…	0103			0102			0101			0100		
G3	G238	02AF			02AE			02AD			02AC			…	0203			0202			0201			0200		
G4	G237	03AF			03AE			03AD			03AC			…	0303			0302			0301			0300		
G5	G236	04AF			04AE			04AD			04AC			…	0403			0402			0401			0400		
G6	G235	05AF			05AE			05AD			05AC			…	0503			0502			0501			0500		
G7	G234	06AF			06AE			06AD			06AC			…	0603			0602			0601			0600		
G8	G233	07AF			07AE			07AD			07AC			…	0703			0702			0701			0700		
G9	G232	08AF			08AE			08AD			08AC			…	0803			0802			0801			0800		
G10	G231	09AF			09AE			09AD			09AC			…	0903			0902			0901			0900		
G11	G230	0AAF			0AAE			0AAD			0AAC			…	0A03			0A02			0A01			0A00		
G12	G229	0BAF			0BAE			0BAD			0BAC			…	0B03			0B02			0B01			0B00		
G13	G228	0CAF			0CAE			0CAD			0CAC			…	0C03			0C02			0C01			0C00		
G14	G227	0DAF			0DAE			0DAD			0DAC			…	0D03			0D02			0D01			0D00		
G15	G226	0EAF			0EAE			0EAD			0EAC			…	0E03			0E02			0E01			0E00		
G16	G225	0FAF			0FAE			0FAD			0FAC			…	0F03			0F02			0F01			0F00		
G17	G224	10AF			10AE			10AD			10AC			…	1003			1002			1001			1000		
G18	G223	11AF			11AE			11AD			11AC			…	1103			1102			1101			1100		
G19	G222	12AF			12AE			12AD			12AC			…	1203			1202			1201			1200		
G20	G221	13AF			13AE			13AD			13AC			…	1303			1302			1301			1300		
⋮	⋮	⋮			⋮			⋮			⋮			⋮	⋮			⋮			⋮			⋮		
G233	G8	E8AF			E8AE			E8AD			E8AC			…	E803			E802			E801			E800		
G234	G7	E9AF			E9AE			E9AD			E9AC			…	E903			E902			E901			E900		
G235	G6	EAAF			EAAE			EAAD			EAAC			…	EA03			EA02			EA01			EA00		
G237	G5	EBAF			EBAE			EBAD			EBAC			…	EB03			EB02			EB01			EB00		
G237	G4	ECAF			ECAE			ECAD			ECAC			…	EC03			EC02			EC01			EC00		
G238	G3	EDAF			EDAE			EDAD			EDAC			…	ED03			ED02			ED01			ED00		
G239	G2	EEAF			EEAE			EEAD			EEAC			…	EE03			EE02			EE01			EE00		
G240	G1	EFAF			EFAE			EFAD			EFAC			…	EF03			EF02			EF01			EF00		

18-bit interface (262k colors)



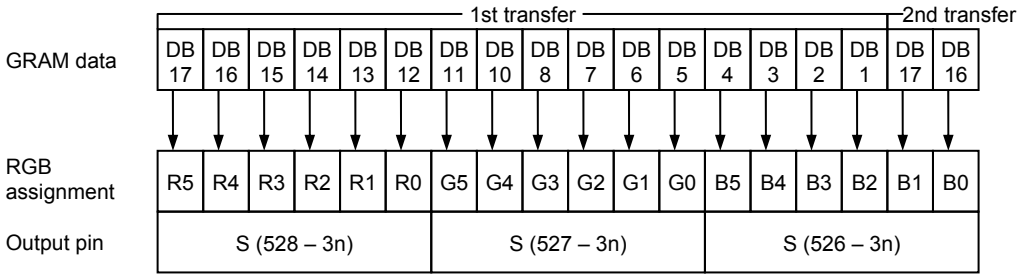
Note: n = lower eight bits of address (0 to 175)

16-bit interface (65k colors) – TRI = "0"



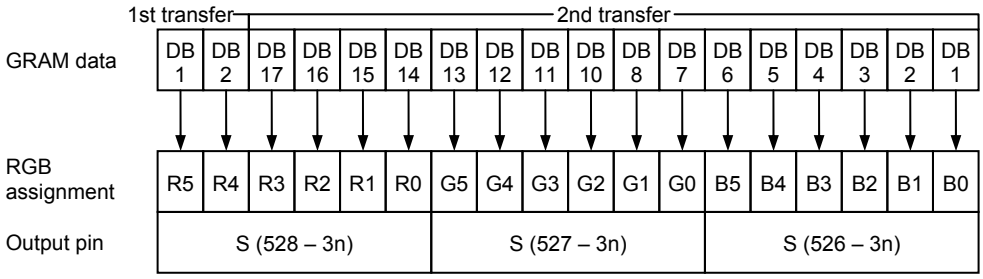
Note: n = lower eight bits of address (0 to 175)

16-bit interface (2 transfers/pixel, 262k colors) – TRI = "1", DFM = "0"



Note: n = lower eight bits of address (0 to 175)

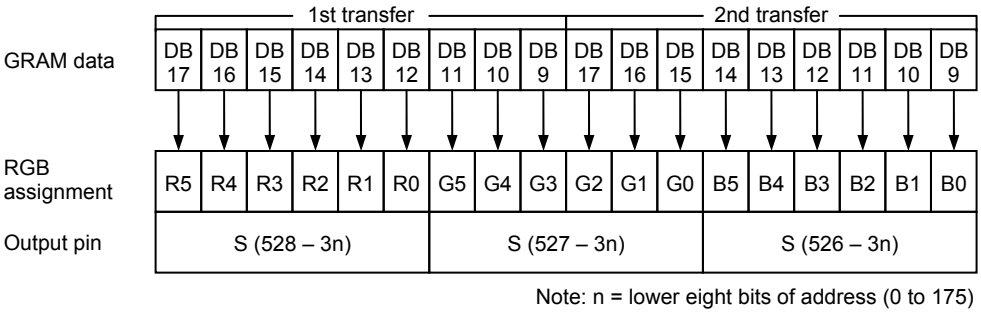
16-bit interface (2 transfers/pixel, 262k colors) – TRI = "1", DFM = "1"



Note: n = lower eight bits of address (0 to 175)

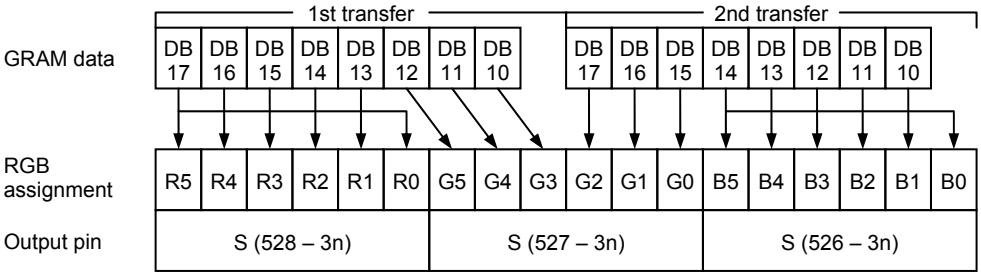
Figure 6: GRAM data and display data: system interface (SS = "1", BGR = "1")

9-bit interface (262k colors)



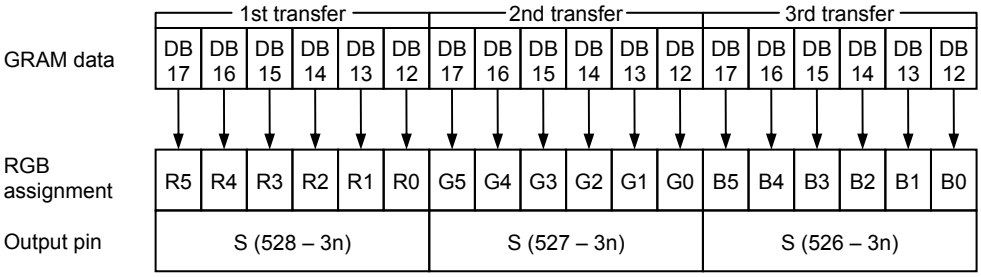
Note: n = lower eight bits of address (0 to 175)

8-bit interface or SPI (2 transfers/pixel, 65k colors) – TRI = "0"



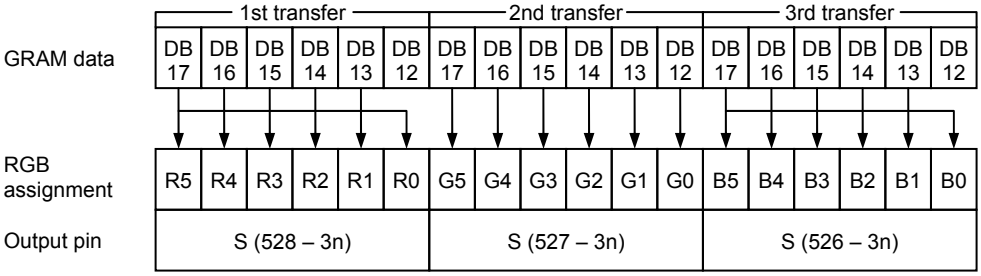
Note: n = lower eight bits of address (0 to 175)

8-bit interface or SPI (3 transfers/pixel, 262k colors) – TRI = "1", DFM = "0"



Note: n = lower eight bits of address (0 to 175)

80-system 8-bit interface (3 transfers/pixel, 65k colors) – TRI = "1", DFM = "1"



Note: n = lower eight bits of address (0 to 175)

Figure 7: GRAM data and display data: system interface (SS = "1", BGR = "1")

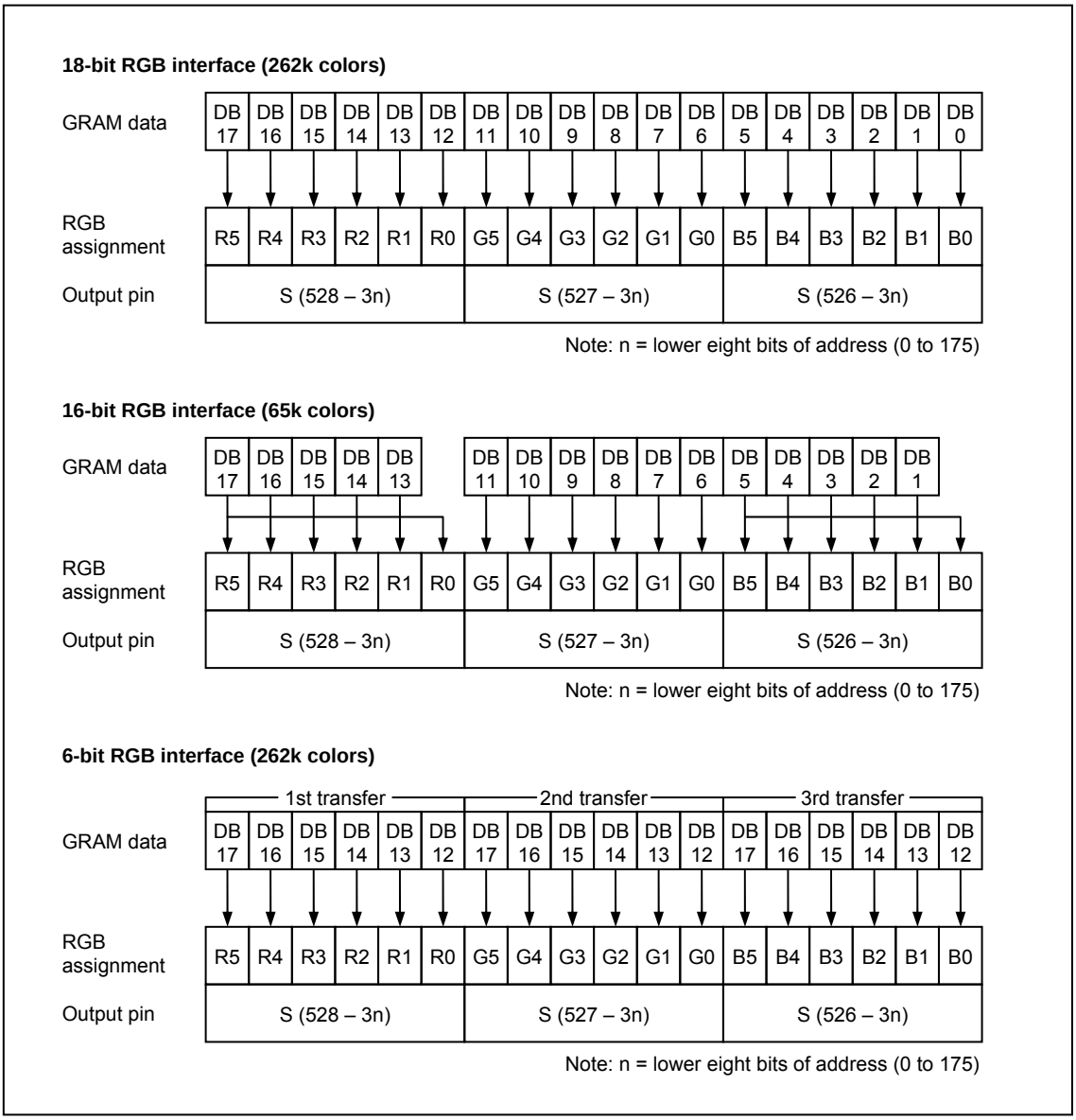


Figure 8: GRAM data and display data: system interface (SS = "1", BGR = "1")

Instructions

Outline

The LGDP4524 adopts 18-bit bus architecture to interface to a high-performance microcomputer. The LGDP4524 starts internal processing after storing control information of externally sent 18-, 16-, 9-, 8-bit data in the instruction register IR and the data register DR. Since internal operations of the LGDP4524 are controlled by the signals sent from the microcomputer, the register selection signal RS, the read/write signal R/W, and the internal 16-bit data bus signals IB[15:0] are called instructions. The LGDP4524 use the 18-bit format internally for operations involving internal GRAM access. The instructions of the LGDP4524 are categorized into the following groups.

1. Specify the index of register
2. Read a status
3. Display control
4. Power management Control
5. Graphics data processing
6. Set internal GRAM address
7. Transfer data to and from the internal GRAM
8. γ-correction

Normally, the instruction for writing data to the internal GRAM is used the most often. Since the LGDP4524 can update internal GRAM address automatically as it writes data to the internal GRAM and minimize data transfer by using the window address function, there is less load on the program in the microcomputer. Since instructions are executed in 0 cycles, it is possible to write instructions consecutively.

As the following figure shows, the way of assigning data to the 16 instruction bits IB[15:0] varies for each interface. Send instructions in accordance with the following data transfer format.

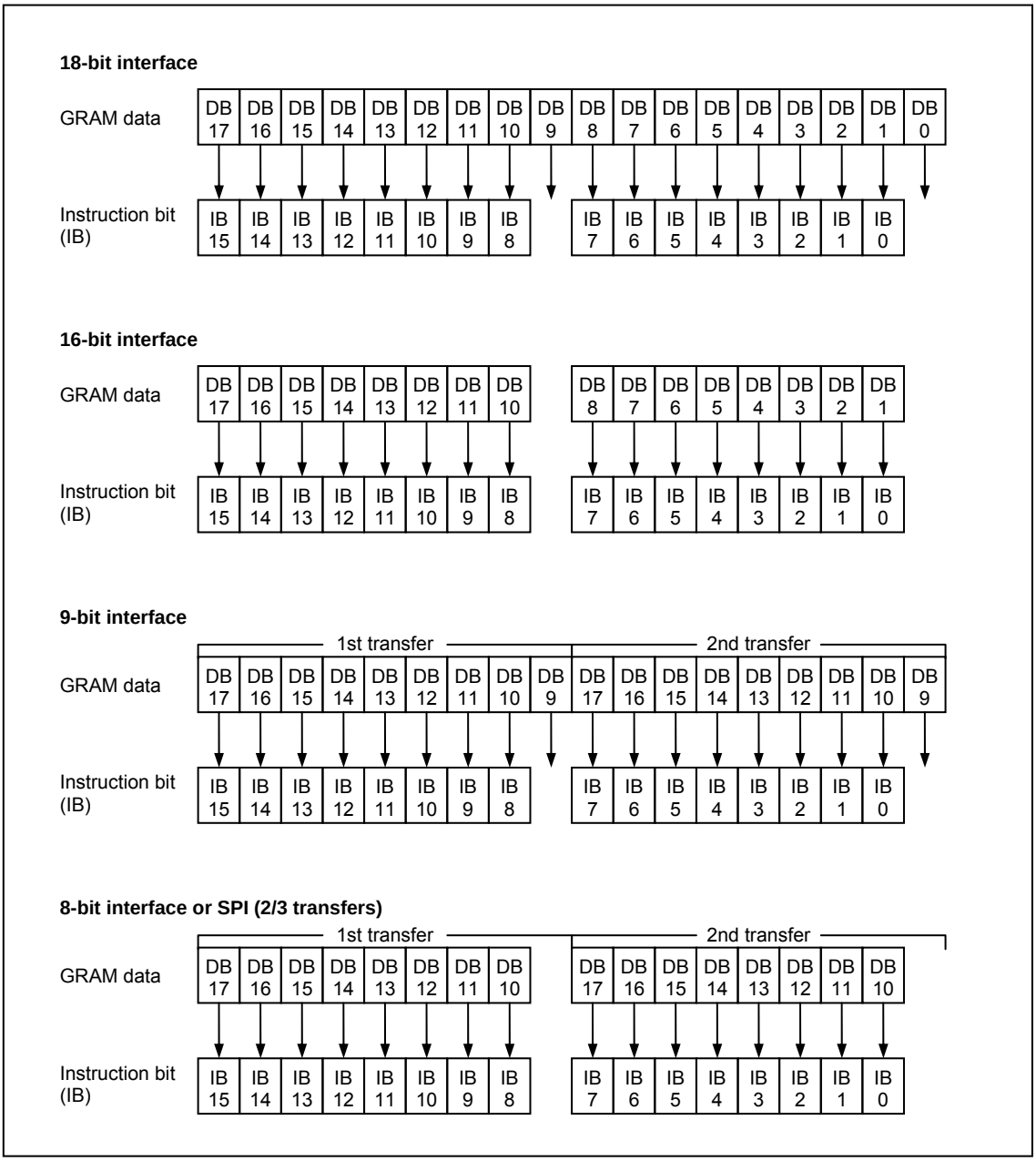


Figure 9: Instruction bits

Explanation of each instruction

The following are detailed explanations of instructions with illustrations of instruction bits IB[15:0] assigned to each interface.

Index (IR)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	0	*	*	*	*	*	*	*	*	*	ID6	ID5	ID4	ID3	ID2	ID1	ID0

The index register specifies the index (R00h to R7Fh) of a control register or RAM control to be accessed using binary numbers “000_0000” to “111_1111”. An access to the register as well as instruction bits contained in it is prohibited unless its index is represented in this register.

Status Read (SR)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R	0	L[7:0]								0	0	0	0	0	0	0	0

The SR bits represent an internal status of the LGDP4524.

L[7:0] – Indicates the position of the line that is currently driving liquid crystal.

Start Oscillation (R00h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	1
R	1	0	1	0	0	0	1	0	1	0	0	1	0	0	0	1	0

The start oscillation instruction restarts an oscillator in halt state in standby mode. After executing this instruction, wait at least 10 ms for stabilizing oscillator before issuing a next instruction.

The device code 4524 is read out when reading out this register forcibly.

Driver Output Control (R01h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	VSPL	HSPL	DPL	EPL	SM	GS	SS	0	0	0	NL[4:0]				

SS – Selects the shift direction of outputs from the source pins.

If SS = “0”, the source pins output from S1 to S528.
If SS = “1”, the source pins output from S528 to S1.

The combination of SS and BGR bits controls the order of assigning RGB dots to the source driver pins S1 to S528.

If SS = “0” and BGR = “0”, RGB dots are assigned interchangeably from S1 to S528.
If SS = “1” and BGR = “1”, RGB dots are assigned interchangeably from S528 to S1.

When changing SS or BGR bits, RAM data must be rewritten.

GS – Sets the shift direction of outputs from the gate driver. GS enables setting the scan order in accordance to the scan mode adopted in the module.

SM – Sets the scan order by the gate driver. SM enables setting the scan order in accordance to the scan mode adopted in the module. See “Scan Mode Setting” section for details.

EPL – Sets the polarity of the signal from the ENABLE pin in RGB interface mode.

If EPL = “0”, ENABLE is low active.
If EPL = “1”, ENABLE is high active.

The following table shows the relationship between the EPL, ENABLE bits, and RAM access.

Table 7

EPL	ENABLE	RAM write	RAM address
0	0	Enabled	Updated
0	1	Inhibited	Retained
1	0	Inhibited	Retained
1	1	Enabled	Updated

VSPL – Inverts the polarity of signals from the VSYNC pin.

If VSPL = “0”, VSYNC is low active.
If VSPL = “1”, VSYNC is high active.

HSPL – Inverts the polarity of signals from the HSYNC pin.

If HSPL = “0”, HSYNC is low active.
If HSPL = “1”, HSYNC is high active.

DPL – Inverts the polarity of signals from the DOTCLK pin.

If DPL = “0”, data are read on the rising edge of the DOTCLK.
If DPL = “1”, data are read on the falling edge of the DOTCLK.

NL[4:0] – Sets the number of gate lines for driving a liquid crystal display panel at an interval of 8 lines as the following table. The GRAM address mapping is independent from the number of gate lines set with the NL bits. Select the number of gate lines that is equal to or more than that of the panel in use.

Table 8

NL[4:0]	Display size	Lines	Driven gate lines
00h	Setting disabled		
01h	528 x 16 dots	16	G1 to G16
02h	528 x 24 dots	24	G1 to G24
03h	528 x 32 dots	32	G1 to G32
04h	528 x 40 dots	40	G1 to G40
05h	528 x 48 dots	48	G1 to G48
06h	528 x 56 dots	56	G1 to G56
07h	528 x 64 dots	64	G1 to G64
08h	528 x 72 dots	72	G1 to G72
09h	528 x 80 dots	80	G1 to G80
0Ah	528 x 88 dots	88	G1 to G88
0Bh	528 x 96 dots	96	G1 to G96
0Ch	528 x 104 dots	104	G1 to G104
0Dh	528 x 112 dots	112	G1 to G112
0Eh	528 x 120 dots	120	G1 to G120
0Fh	528 x 128 dots	128	G1 to G128
10h	528 x 136 dots	136	G1 to G136
11h	528 x 144 dots	144	G1 to G144
12h	528 x 152 dots	152	G1 to G152
13h	528 x 160 dots	160	G1 to G160
14h	528 x 168 dots	168	G1 to G168
15h	528 x 176 dots	176	G1 to G176
16h	528 x 184 dots	184	G1 to G184
17h	528 x 192 dots	192	G1 to G192
18h	528 x 200 dots	200	G1 to G200
19h	528 x 208 dots	208	G1 to G208
1Ah	528 x 216 dots	216	G1 to G216
1Bh	528 x 220 dots	220	G1 to G220

LCD Driving Waveform Control (R02h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	FLD[1:0]		B/C	EOR	0	0	NW[5:0]					

NW[5:0] – Specifies “n”, the number of gate lines from 1 to 64, to set the interval of inverting polarity when the LGDP4524 is set to generate a C-pattern waveform (B/C = “1”). The polarity is inverted at an interval of n+1 gate lines.

EOR – When EOR = “1”, the polarity is inverted according to the result of EOR (exclusive OR) operation, which is performed on a signal for selecting either odd or even frames and a signal for inverting polarity in units of n lines when the LGDP4524 is set to generate a C-pattern waveform (B/C = “1”). This instruction is used when the number of gate lines for driving an LCD panel is at odds with the interval of n lines set for inverting polarity. For details, see “n-Line Inversion AC Drive” section.

B/C – When the LGDP4524 is set to generate a field-inversion waveform (B/C = “0”), polarity is inverted at an interval of fields. The LGDP4524 inverts polarity at an interval of n lines, when a C-pattern waveform is generated (B/C = “1”) according to NW and EOR bits. For details, see “n-Line Inversion AC Drive”.

FLD[1:0] – Sets the number of fields for n-field interlaced scan. See “Interlaced Scan” for details. The FLD bits are disabled in external display interface mode. When using the external display interface, set FLD[1:0] = “01”.

Table 9

FLD	Number of fields
00	Setting disabled
01	1 field (= 1 frame)
10	Setting disabled
11	3 fields

Entry Mode (R03h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	TRI	DFM	0	BGR	0	0	0	0	0	0	I/D[1:0]		AM	0	0	0

The LGDP4524 modifies data sent from a microcomputer before writing them to the internal GRAM in order to write the GRAM data in high speed and reduce software processing load on the microcomputer.

TRI – When TRI = “1”, data are transferred to the internal RAM in 8-bit x 3 transfers mode via the 8-bit interface. It is also possible to send data via the 16-bit interface or SPI in the transfer mode that realizes display in 262k colors in combination with DFM bits. When not using these interface modes, be sure to set TRI to “0”.

DFM – Sets the mode of transferring data to the internal RAM when TRI = “1”. See the following figures for details.

Table 10

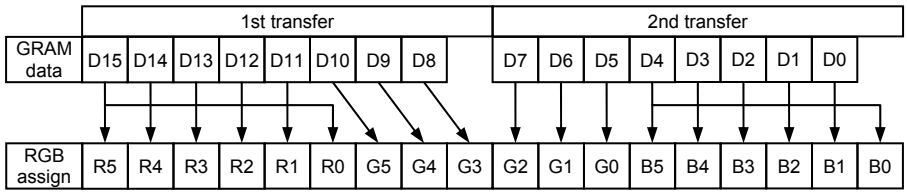
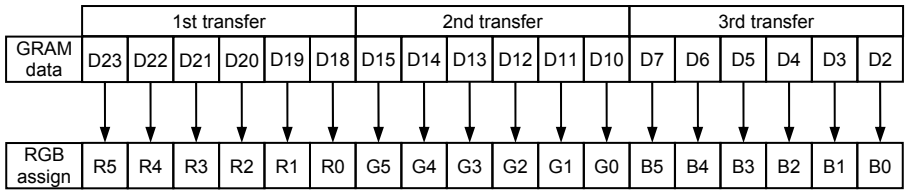
TRI	DFM	RAM write data transfer via serial peripheral interface (SPI)
0	*	SPI (2 transfers/pixel) – 65k colors available 
1	0	SPI (3 transfers/pixel) – 262k colors available 
1	1	Setting disabled

Table 11

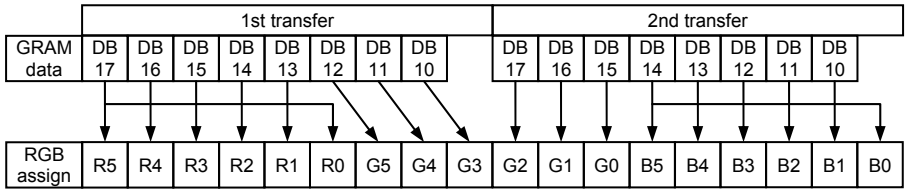
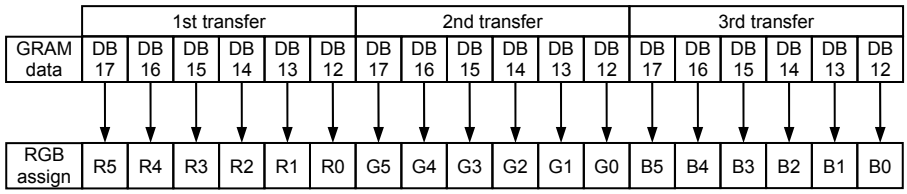
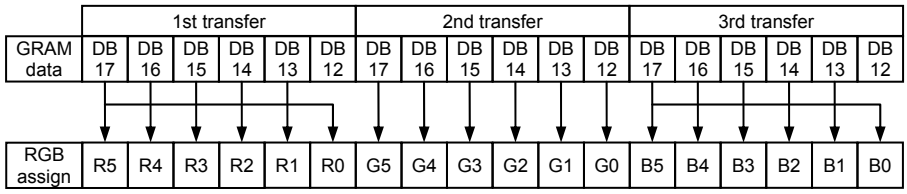
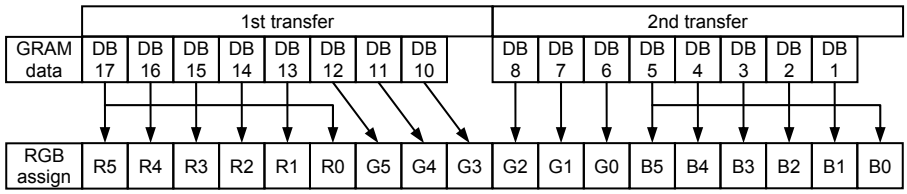
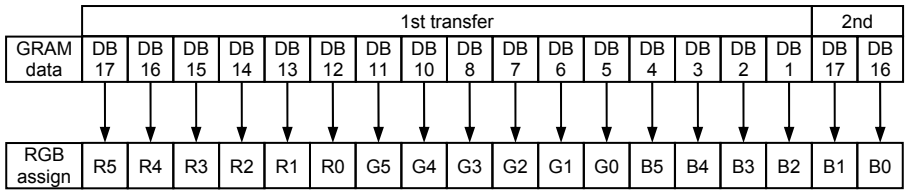
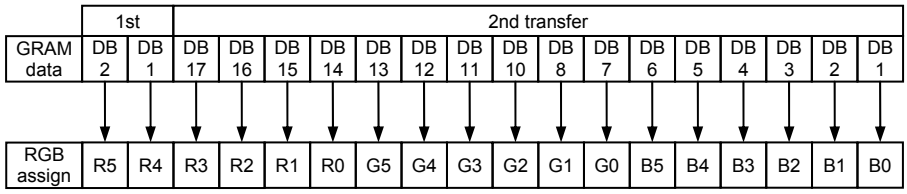
TRI	DFM	RAM write data transfer via 8-bit interface
0	*	8-bit interface (2 transfers/pixel) – 65k colors available 
1	0	8-bit interface (3 transfers/pixel) – 262k colors available 
1	1	8-bit interface (3 transfers/pixel) – 65k colors available 

Table 12

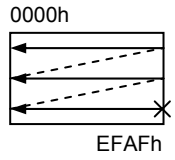
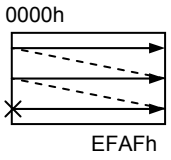
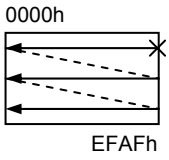
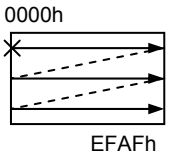
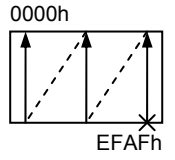
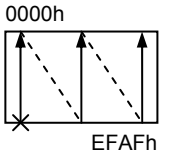
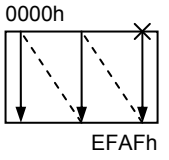
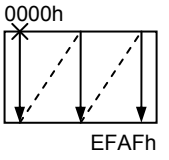
<table>
<tr><th>TRI</th><th>DFM</th><th>RAM write data transfer via 16-bit interface</th></tr>
<tr><td>0</td><td>*</td><td>16-bit interface (1 transfers/pixel) – 65k colors available
 
</td></tr>
<tr><td>1</td><td>0</td><td>16-bit interface MSB mode (2 transfers/pixel) – 262k colors available
 
</td></tr>
<tr><td>1</td><td>1</td><td>16-bit interface LSB mode (2 transfers/pixel) – 262k colors available
 
</td></tr>
</table>

BGR – Reverses the order of RGB dots to BGR when writing 18-bit pixel data to the internal GRAM. Note that the orders of RGB dots in both WM[17:0] and CP[17:0] bits are automatically changed upon setting BGR to “1”.

I/D[1:0] – The address counter is automatically incremented by 1 as writing data to the internal GRAM when I/D = “1”. The address counter is automatically decremented by 1 as writing data to the internal GRAM when I/D = “0”. The increment/decrement can be set separately to each upper (AD[15:8]) / lower (AD[7:0]) byte of address. The transition direction of address (vertical/horizontal) when writing data to the internal GRAM is set with the AM bit.

AM – Sets the direction of automatically updating address for writing data to the internal RAM in the address counter (AC). When AM = “0”, the address is updated in horizontal writing direction. When AM = “1”, the address is updated in vertical writing direction. When a window address area is set, data are written only to the GRAM area specified with window address in the writing direction set with I/D[1:0] and AM bits.

Table 13: Address transition directions

	I/D[1:0] = "00" Horizontal decrement Vertical decrement	I/D[1:0] = "01" Horizontal increment Vertical decrement	I/D[1:0] = "10" Horizontal decrement Vertical increment	I/D[1:0] = "11" Horizontal increment Vertical increment
AM = "0" Horizontal				
AM = "1" Vertical				

Resize Control (R04h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	RCV[1:0]		0	0	RCH[1:0]		0	0	RSZ[1:0]	

RSZ[1:0] – Sets the resizing factor. When the RSZ bits are set for resizing, the LGDP4524 writes the data of the resized image in both horizontal and vertical directions according to the resizing factor on the internal GRAM.

RCH[1:0] – Sets the number of pixels made as the remainder in horizontal direction as a result of resizing a picture. By specifying the number of remainder pixels with RCH bits, the data can be transferred without taking the reminder pixels into consideration. Make sure that RCH = 2'h0 when not using the resizing function (RSZ = 2'h0) or there are no remainder pixels.

RCV[1:0] – Sets the number of pixels made as the remainder in vertical direction as a result of resizing a picture. By specifying the number of remainder pixels with the RCV bits, the data can be transferred without taking the reminder pixels into consideration. Make sure that RCV = 2'h0 when not using the resizing function (RSZ = 2'h0) or there are no remainder pixels.

Table 14: Resizing scale

RSZ[1:0]	Resizing scale
00	No resizing (x 1)
01	x 1/2
10	Setting disabled
11	x 1/4

Table 15: Surplus pixels in horizontal/vertical directions

RCH[1:0]/RCV[1:0]	Surplus pixels
00	0 pixel
01	1 pixel
10	2 pixels
11	3 pixels

Display Control 1 (R07h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	PTS[2:0]			VLE[1:0]		SPT	0	0	GON	DTE	CL	REV	D[1:0]	

PTS[2:0] – Sets the kind of source output in non-display area in partial display mode. For details, see the "Partial Display Function" section.

Table 16

PTS	Source output in non-display area		Operating grayscale amplifier in non-display area
	Positive polarity	Negative polarity	
000	V63	V0	V0 to V63
001	Setting disabled	Setting disabled	-
010	GND	GND	V0 to V63
011	High impedance	High impedance	V0 to V63
100	V63	V0	V0, V63
101	Setting disabled	Setting disabled	-
110	GND	GND	V0, V63
111	High impedance	High impedance	V0, V63

VLE[1:0] – When VLE[0] = "1", the first display is scrolled up in vertical direction. When VLE[1] = "1", the second display is scrolled up in vertical direction. The first and second displays cannot be scrolled simultaneously. This function is not available with the external display interface. In this case, set VLE to "00".

Table 17

VLE	2nd display image	1st display image
00	Fixed	Fixed
01	Fixed	Scroll up
10	Scroll up	Fixed
11	Setting disabled	

SPT – When SPT = "1", the LCD is driven in 2 split screens. For details, see the "Partial Display Function" section. This function is not available with the external display interface. In this case, set SPT to "0".

GON, DTE – Sets the output level of gate lines G1 to G220 as follows.

Table 18

GON	DTE	Gate output G1 to G220
0	0	VGH
0	1	VGH
1	0	VGL
1	1	VGH/VGL

CL – When CL = "1", the 8-color display mode is selected. For details, see the "8-Color Display Mode" section. The 8-color display mode is not available in external interface mode.

REV – By setting REV = "1", the grayscale levels can be inverted. This means, the REV bit allows both normally black and normally white panels to display a same image from the same data. The source output level during front and back porch periods and a blank period in partial display mode is set with the PTS bits.

Table 19

REV	GRAM data (RGB each)	Source output in display area	
		Positive polarity	Negative polarity
0	00h	V63	V0
	⋮	⋮	⋮
	3Fh	V0	V63
1	00h	V0	V63
	⋮	⋮	⋮
	3Fh	V63	V0

D[1:0] – A graphics display appears on the screen when D[1] = "1", and is turned off upon setting D[1] = "0". When setting D[1] = "0", the graphics display data are retained in the internal GRAM and the display appears instantly on the screen upon setting D[1] to "1". When the D[1] bit is "0", i.e. while no display is

shown on the screen, all source outputs are at the GND level to reduce charging/discharging current on liquid crystal cells, which is generated during liquid crystal AC drive.

Upon setting D = “00”, the display is turned off and internal display operations are halted completely.In combination with the GON, DTE bit, the D[1:0] bits controls ON/OFF of graphics display. For details, see the flowcharts in the “Instruction Setting” section.

Table 20

D[1:0]	Source and Vcom outputs	IC internal operation
00	GND	Halt
01	GND	Operate
10	Non-lit display	Operate
11	Display	Operate

Notes:

1. Data write operations from the microcomputer are performed irrespective of the D[1:0] bits.
2. When D[1:0] = “00”, the LGDP4524 is in the same state as the standby mode. However, this does not mean the D[1:0] bits are written over to “00” upon setting the standby mode.

Display Control 2 (R08h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	FP[3:0]				0	0	0	0	BP[3:0]			

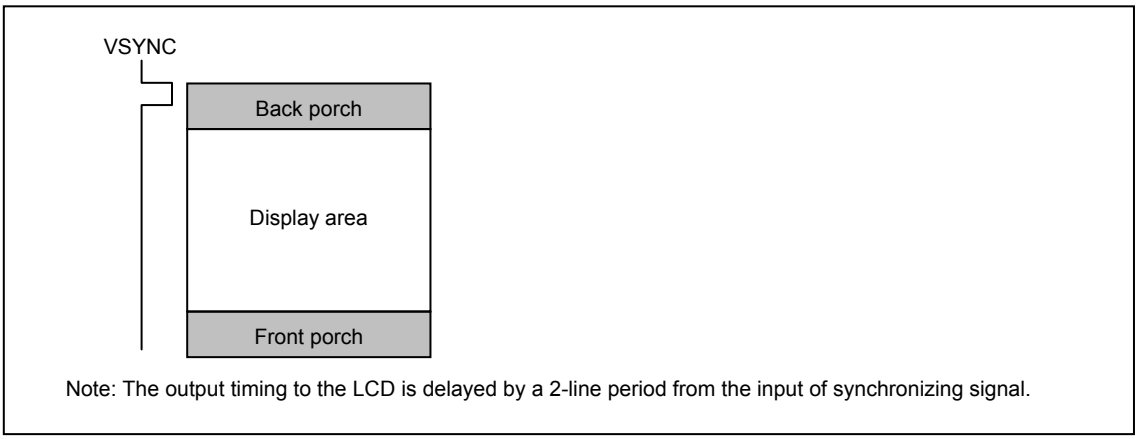
FP[3:0]/BP[3:0] – Sets the blank period made at the beginning and the end of a display (front porch and back porch, respectively). The FP[3:0] and BP[3:0] bits specify the number of lines for the front and back porch periods, respectively. In setting, be sure:

BP + FP ≤ 16 lines
FP ≥ 2 lines
BP ≥ 2 lines

In external display interface mode, a back porch (BP) period starts on the falling edge of the VSYNC signal, followed by a display operation period. After driving the number of lines set with NL bits, a front porch period starts. After the front porch period, a blank period continues until the next input of VSYNC signal.

Table 21

FP/BP	Number of lines for the front/back porches
0	Setting disabled
1	Setting disabled
2	2 lines
3	3 lines
4	4 lines
5	5 lines
6	6 lines
7	7 lines
8	8 lines
9	9 lines
10	10 lines
11	11 lines
12	12 lines
13	13 lines
14	14 lines
15	Setting disabled



Note: The output timing to the LCD is delayed by a 2-line period from the input of synchronizing signal.

Figure 10: Back/front porches

Set the BP[3:0], FP[3:0] bits as follows in each operation mode.

Table 22

Internal clock operation	**FLD[1:0] = "01"**	BP ≥ 2 lines	FP ≥ 2 lines	FP + BP ≤ 16 lines
	FLD[1:0] = "11"	BP = 3 lines	FP = 5 lines	
RGB interface		BP ≥ 2 lines	FP ≥ 2 lines	FP + BP ≤ 16 lines
VSYNC interface		BP ≥ 2 lines	FP ≥ 2 lines	FP + BP = 16 lines

Display Control 3 (R09h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	PTG[1:0]		ISC[3:0]			

PTG[1:0] – Sets the scan mode by the gate driver in non-display area.

Table 23

PTG	Gate outputs in non-display area
00	Normal scan
01	VGL (fixed)
10	Interval scan
11	Setting disabled

ISC[3:0] – Sets the scan cycle by the gate driver when the PTG bits are set to the interval scan mode in non-display area. The scan cycle can be set as (2 * ISC + 1) frames, where ISC is from 1 to 15. In this case, polarity is inverted as gate lines are scanned.

Frame Cycle Control (R0Bh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	NO[1:0]		SDT[1:0]		EQ[1:0]		DIV[1:0]		0	RTN[6:0]						

RTN[6:0] - Sets the 1H (1 line) period in internal oscillator cycles. RTN[6:0] should be greater than or equal to 44 (= 16h).

Table 24

RTN[6:0]	Clock cycles per line
2Ch	44
2Dh	45
2Eh	46
2Fh	47
30h	48
….	….
7Ah	125
7Ch	126
7Eh	127

DIV[1:0] – The internal operation is synchronized with the clock, which is divided with the division ratio set with the DIV bits. Set the RTN and DIV bits to adjust frame frequency. If the number of lines for driving liquid crystal is changed, the frame frequency must also be adjusted. See “Frame Frequency Adjustment Function”. In RGB interface mode, the DIV bits are disabled.

Table 25

DIV	Division ratio	Internal operation clock frequency
0	N/A	N/A
1	2	fosc/2
2	4	fosc/4
3	8	fosc/8

Note: fosc = Frequency of RC oscillation

Formula to calculate frame frequency

$$Frame\ frequency = \frac{Fosc}{(Clock\ cycles\ per\ line * Division\ ratio * (Active\ line + BP + FP))}$$

Where,

fosc = frequency of RC oscillation,
Active line = number of active lines for driving liquid crystal (NL bits),
Division ratio = DIV bits,
Clock cycles per line = RTN bits,
FP = the number of lines for the front porch period and
BP = the number of lines for the back porch period.

EQ[1:0] – Sets the equalization. Recommend that EQ[1:0] sets 11.

SDT[1:0] – Sets the source output delay from the falling edge of gate output.

Table 26

SDT[1:0]	Source output delay	
	Internal operation (internal oscillator)	RGB I/F operation (DOTCLK)
0	2 clocks	8 clocks
1	4 clocks	16 clocks
2	6 clocks	24 clocks
3	8 clocks	32 clocks

NO[1:0] – Sets the non-overlap period of outputs from adjacent gate lines.

Table 27

NO[1:0]	Gate output non-overlap period	
	Internal operation (internal oscillator)	RGB I/F operation (DOTCLK)
0	0 clocks	0 clocks
1	8 clocks	32 clocks
2	12 clocks	48 clocks
3	16 clocks	64 clocks

Note that the clock mentioned in the above description refers to different clocks according to the interface mode in use as follows.

Table 28

Interface mode in use	Reference clock
Internal operation mode	Internal oscillator
RGB interface mode	DOTCLK
VSYNC interface mode	Internal oscillator

External Display Interface Control 1 (R0Ch)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	RM	0	0	DM[1:0]		0	0	RIM[1:0]	

RM – Selects the interface to access the LGDP4524's internal GRAM. The RAM access is possible only via the interface selected with the RM bit. Set RM to "1" when writing display data via the RGB interface. The LGDP4524 allows for setting the RM bit not constrained by the mode used for the display operation. This means it is possible to rewrite display data via a system interface by setting RM = "0" even while display operations are performed via the RGB interface.

Table 29: RM bit

RM	Interface for RAM access
0	System interface/VSYNC interface
1	RGB interface

RIM[1:0] – Selects one of the following RGB interface modes when the RGB interface mode is selected with the RM and DM bits. Make this setting before display operation via external display interface. Do not make changes to the setting during display operation.

Table 30: RIM[1:0] bits

RIM	RGB interface mode
0	18-bit RGB interface (1 transfer/pixel)
1	16-bit RGB interface (1 transfer/pixel)
2	6-bit RGB interface (3 transfers/pixel)
3	Setting disabled

DM[1:0] – Sets the display operation mode. By setting DM[1:0] as follows, it is possible to switch between the internal clock operation mode and the external display interface mode. Do not switch between different external interface modes (RGB interface and VSYNC interface).

Table 31: DM[1:0] bits

DM	Display operation mode
0	Internal clock operation
1	RGB interface
2	VSYNC interface
3	Setting disabled

Notes:

1. Instructions are set only via the system interface.
2. Be sure that data transfer and dot clock input are performed in units of RGB dots in 6-bit RGB interface mode.

As the following table, the optimum interface for the state of display can be selected by setting the external display interface mode.

Table 32

Display State	Operation mode	RAM access (RM)	Display mode (DM)
Still pictures	Internal clock operation	System interface (RM = 0)	Internal clock operation (DM = 00)
Moving pictures	RGB interface (1)	RGB interface (RM = 0)	RGB interface (DM = 01)
Rewrite still picture area while display moving pictures	RGB interface (2)	RGB interface (RM = 0)	RGB interface (DM = 01)
Moving pictures	VSYNC interface	System interface (RM = 0)	VSYNC interface (DM = 10)

Notes:

1. Instructions are set only via the system interface.
2. The RGB-I/F and the VSYNC-I/F are not used simultaneously.
3. Do not make changes to the RGB-I/F mode setting (RIM) while the RGB I/F is in operation.
4. See the “External Display Interface” section for the flowcharts to follow when switching from one mode to another.

Internal clock operation mode

All display operations are synchronized with the signals generated from the internal operating clock in this mode. None of inputs via the external display interface are valid. The internal RAM is accessible only via the system interface.

RGB interface mode (1)

In RGB interface mode, display operations are synchronized with the frame synchronizing signal (VSYNC), the line synchronizing signal (HSYNC), and the dot clock (DOTCLK). These signals must be supplied through a display period using the RGB interface.

Display data are transferred in units of pixels via the DB[17:0] pins. All display data are stored in the internal RAM. The combined use of the high-speed RAM write mode and the widow address function enables not only displaying data in moving picture area and data in the internal RAM in other than the moving picture area at a time but also minimizing data transfer by transferring data only when rewriting screen.

The front porch (FP) and back porch (BP) periods, and the display duration period (NL) are automatically calculated inside the LGDP4524 by internally counting the number of line synchronizing signal clocks (HSYNC) from the falling edge of the frame synchronizing signal (VSYNC). Take this into consideration when transferring RGB data via the DB[17:0] pins.

RGB interface mode (2)

The LGDP4524 enables rewriting RAM data via the system interface while the RGB interface is selected for display operation. In this case, Be sure to write RAM data while display data are not being transferred via the RGB interface (ENABLE = High). To return to the display data transfer mode via the RGB interface, change the ENABLE bit first and then set a new address (AD[15:0]) in the AC and the index register to R22h.

VSYNC interface mode

In VSYNC interface mode, internal display operations are synchronized with the frame synchronizing signal (VSYNC). In this mode, a moving picture can be displayed via the system interface by writing data to the internal RAM at more than the minimum speed from the falling edge of frame synchronizing signal (VSYNC). In this case, there are constraints in the RAM writing speed and method. For details, see "External Display Interface".

No external signal input except VSYNC input is accepted in VSYNC interface mode.

The timings and durations of front porch (FP), back porch (BP) periods and display duration period (NL) are automatically calculated from the falling edge of the frame synchronization signal (VSYNC) according to the instructions set in the relevant registers.

Power Control 1 (R10h)

Power Control 2 (R11h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	SAP[2:0]			0	BT[2:0]			DUAL	AP[2:0]			STB	DK	SLP	DSTB
W	1	0	0	0	0	0	DC1[2:0]			0	DC0[2:0]			0	VC[2:0]		

SAP[2:0] – Adjusts the constant current in the operational amplifier circuit for the source driver. Setting a larger constant current stabilizes the operational amplifier circuit, but current consumption also increases. Adjust the constant current taking the trade-off between display quality and current consumption into account. During no display period, set SAP[2:0] = "000" to halt the operational amplifier circuit to reduce current consumption.

Table 33

SAP[2:0]	DC current of op-amp
0	Halt
1	Setting disable
2	0.5
3	0.75
4	1
5	1.25
6	1.5
7	1.75

Note: The DC current in the table is shown as the ratio to the DC current when SAP[2:0] = "100".

BT[2:0] – Changes the rate applied to the step-up circuit. Adjust the step-up rate according to the voltage in use. To reduce current consumption, set a smaller step-up rate.

Table 34

BT[2:0]	DDVDH	VCL	VGH	VGL	Capacitor connection pins
0	Vci1 x 2 [x2]	Vci1 x -1 [x-1]	DDVDH x 3 [x6]	(Vci1 + DDVDH x2) [x-5]	DDVDH, VGH, VGL, VCL, C11±, C13±, C21±, C22±
1	Vci1 x 2 [x2]	Vci1 x -1 [x-1]	DDVDH x 3 [x6]	(DDVDH x2) [x-4]	DDVDH, VGH, VGL, VCL, C11±, C13±, C21±, C22±
2	Vci1 x 2 [x2]	Vci1 x -1 [x-1]	DDVDH x 3 [x6]	(Vci1 + DDVDH) [x-3]	DDVDH, VGH, VGL, VCL, C11±, C13±, C21±, C22±
3	Vci1 x 2 [x2]	Vci1 x -1 [x-1]	Vci1 + DDVDH x 2 [x5]	(Vci1 + DDVDH x2) [x-5]	DDVDH, VGH, VGL, VCL, C11±, C13±, C21±, C22±
4	Vci1 x 2 [x2]	Vci1 x -1 [x-1]	Vci1 + DDVDH x 2 [x5]	(DDVDH x2) [x-4]	DDVDH, VGH, VGL, VCL, C11±, C13±, C21±, C22±
5	Vci1 x 2 [x2]	Vci1 x -1 [x-1]	Vci1 + DDVDH x 2 [x5]	(Vci1 + DDVDH) [x-3]	DDVDH, VGH, VGL, VCL, C11±, C13±, C21±, C22±
6	Vci1 x 2 [x2]	Vci1 x -1 [x-1]	DDVDH x 2 [x4]	(DDVDH x2) [x-4]	DDVDH, VGH, VGL, VCL, C11±, C13±, C21±, C22±
7	Vci1 x 2 [x2]	Vci1 x -1 [x-1]	DDVDH x 2 [x4]	(Vci1 + DDVDH) [x-3]	DDVDH, VGH, VGL, VCL, C11±, C13±, C21±

Notes:

1. The step-up rate from the Vci1 level is shown in the bracket [ ] in the above table.
2. When using the DDVDH, VCL, VGH and VGL voltage levels, connect a capacitor to each capacitor connection pin.
3. Set the following voltages within the limits: DDVDH = max 5.5V, VCL = min –3.3V, VGH = max 16.5V, VGL = min –16.5V.

DUAL – Controls the operation of the 2nd step-up circuit 1.This bit can be enabled in only condition DK=1 to prevent the 2nd step up circuit 1 from turning on even though the 1st step up circuit 1 is in off state. But this bit can be disabled regardless of DK bit condition. For details, see the “Power Supply Setting” section

AP[2:0] – Adjusts the constant current in the operational amplifier circuit in the LCD power supply circuit. Setting a larger constant current stabilizes the operational amplifier circuit, but current consumption increases. Adjust the constant current taking the trade-off between display quality and current consumption into account. During no display period, set AP[2:0] = “000” to halt the operational amplifier circuit and step-up circuits to reduce current consumption.

Table 35

AP[2:0]	DC current of op-amp
0	Halt
1	0.25
2	0.5
3	1
4	2
5	3
6	4
7	5

Note: The DC current in the table is shown as the ratio to the DC current when AP[2:0] = “011”.

STB – When STB = “1”, the LGDP4524 enters the standby mode. In standby mode, display operations are completely halted, and all internal operations including internal RC oscillation and reception of external clocks are halted. See the “Instruction Setting” section for the sequence. Only the instruction to exit the standby mode (STB = “0”) or that to start oscillators is accepted during standby mode. In standby mode, the GRAM data and the instruction sets before entering the standby mode are retained.

DK – Controls the operation of step-up circuit 1. In supplying power to the LGDP4524, stop generating DDVDH for a moment, and wait until the VGH level is stabilized. Then start generating the DDVDH level. For details, see the “Power Supply Setting” section.

Table 36

DK	Operation of step-up circuit 1
0	Operate
1	Halt

SLP – When SLP = "1", the LGDP4524 enters the sleep mode. In sleep mode, internal display operation except RC oscillation is halted to reduce current consumption. In sleep mode, only the following instructions, BT, DC0, DC1, AP, SLP, STB, VRH, VINIT, and VCM, are accepted. No changes to the GRAM data or other instruction sets are accepted. In sleep mode, the GRAM data and the instruction sets before entering the sleep mode are retained.

DSTB – When DSTB = "1", the LGDP4524 enters the deep standby mode. In deep standby mode, display operations are completely halted, with shutdown internal vcc regulator used as logic supply voltage and all internal operations including internal RC oscillation and reception of external clocks are halted. See the "Instruction Setting" section for the sequence. Only the sequence to exit the deep standby mode is hardware reset or 6 tmes CS pin low consecutively. GRAM data and instruction sets are susceptible to destruction and must be set again after exiting the deep standby mode

DC1[2:0] – Selects the operating frequency of the step-up circuit 2. A higher step-up operating frequency enhances the driving capacity of the step-up circuit and the quality of display. Adjust the frequency taking the trade-off between display quality and current consumption into account.

DC0[2:0] – Selects the operating frequency of the step-up circuit 1. A higher step-up operating frequency enhances the driving capacity of the step-up circuit and the quality of display. Adjust the frequency taking the trade-off between display quality and current consumption into account.

Note: Setting step-up cycles of step-up circuits 1/2, be sure the step-up cycle of the step-up circuit 1 is more than that of the step-up circuit 2 (step-up frequency 1 ≥ step-up frequency 2).

Table 37

DC1[2:0]	fDCDC2
0	Oscillation clock / 16
1	Oscillation clock / 32
2	Oscillation clock / 64
3	Oscillation clock / 128
4	Oscillation clock / 256
5	Oscillation clock / 512
6	Oscillation clock / 1024
7	Oscillation clock / 2048

Table 38

DC0[2:0]	fDCDC1
0	Oscillation clock / 8
1	Oscillation clock / 16
2	Oscillation clock / 32
3	Oscillation clock / 64
4	Oscillation clock / 128
5	Oscillation clock / 256
6	Oscillation clock / 512
7	Oscillation clock / 1024

Note: Be sure fDCDC1 ≥ fDCDC2 when setting DC0, DC1.

VC[2:0] – Sets the rate applied to Vci to generate the reference voltage for the VREG1OUT and Vci1 levels.

Table 39

VC[2:0]	Vci1 output voltage
0	Vci
1	0.93 x Vci
2	0.88 x Vci
3	0.82 x Vci
4	0.78 x Vci
5	0.74 x Vci
6	0.70 x Vci
7	Halt(Hi-z)

Power Control 3 (R12h)

Power Control 4 (R13h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	PON	VRH[3:0]			
W	1	0	0	VCOMG	VDV[4:0]					0	VCM[6:0]						

PON – Controls ON/OFF of VGL output. To stop VGL output, set PON to “0”. To start VGLoutput, set PON to “1”.

VRH[3:0] – Sets the amplifying rate (1.38 to 1.83) applied to REGP to output the VREG1OUT level, which is a reference level for the VCOM level and the grayscale voltage level.

Table 40: VRH

VRH[3:0]	VREG1OUT voltage
0 to 7	Halt
8	Vci1 x 1.38
9	Vci1 x 1.45
A	Vci1 x 1.53
B	Vci1 x 1.60
C	Vci1 x 1.68
D	Vci1 x 1.75
E	Vci1 x 1.83
F	Setting disable

VCOMG – When VCOMG = “1”, the LGDP4524 can output a negative voltage level for VcomL (1.0V to –Vci1+0.5V Max.). When VCOMG = “0”, the LGDP4524 halts the amplifier for negative voltage to save power. When VCOMG = “0”, the VDV bits are disabled. In this case, adjust the amplitude of Vcom AC voltage with the VCM bits (VcomH setting). Set PON to “1” before setting VCOMG to “1”.

VDV[4:0] – Sets the amplitude of Vcom AC voltage. The VDV bits can set the Vcom amplitude 0.6 to 1.23 times the VREG1OUT level. If VCOMG = “0”, the VDV bits are disabled.

Table 41

VDV[4:0]	Vcom amplitude	VDV[4:0]	Vcom amplitude
00h	VREG1OUT x 0.60	10h	VREG1OUT x 1.05
01h	VREG1OUT x 0.63	11h	VREG1OUT x 1.08
02h	VREG1OUT x 0.66	12h	VREG1OUT x 1.11
03h	VREG1OUT x 0.69	13h	VREG1OUT x 1.14
04h	VREG1OUT x 0.72	14h	VREG1OUT x 1.17
05h	VREG1OUT x 0.75	15h	VREG1OUT x 1.20
06h	VREG1OUT x 0.78	16h	VREG1OUT x 1.23
07h	VREG1OUT x 0.81	17h	Setting disabled
08h	VREG1OUT x 0.84	18h	Setting disabled
09h	VREG1OUT x 0.87	19h	Setting disabled
0Ah	VREG1OUT x 0.90	1Ah	Setting disabled
0Bh	VREG1OUT x 0.93	1Bh	Setting disabled
0Ch	VREG1OUT x 0.96	1Ch	Setting disabled
0Dh	VREG1OUT x 0.99	1Dh	Setting disabled
0Eh	VREG1OUT x 1.02	1Eh	Setting disabled
0Fh	Setting disabled	1Fh	Setting disabled

Notes:

1. Adjust VREG1OUT and VCM so that VcomH are set within the range 3.0 to (DDVDH – 0.5)V
2. Adjust VREG1OUT and VDV so that the amplitude of Vcom are set to 6.0V or less.

VCM[6:0] – Set the VcomH level (the high level of Vcom AC voltage). The VCM bits can set the VcomH level 0.4 to 0.98 times the VREG1OUT level. To stop adjusting VcomH with the internal volume and adjust it with an external resistor from VcomR, set VCM = “1111111”.

Table 42

VCM [6:0]	VcomH	VCM [6:0]	VcomH	VCM [6:0]	VcomH	VCM [6:0]	VcomH
00h	VREG1OUT x 0.400	20h	VREG1OUT x 0.560	40h	VREG1OUT x 0.720	60h	VREG1OUT x 0.880
01h	VREG1OUT x 0.405	21h	VREG1OUT x 0.565	41h	VREG1OUT x 0.725	61h	VREG1OUT x 0.885
02h	VREG1OUT x 0.410	22h	VREG1OUT x 0.570	42h	VREG1OUT x 0.730	62h	VREG1OUT x 0.890
03h	VREG1OUT x 0.415	23h	VREG1OUT x 0.575	43h	VREG1OUT x 0.735	63h	VREG1OUT x 0.895
04h	VREG1OUT x 0.420	24h	VREG1OUT x 0.580	44h	VREG1OUT x 0.740	64h	VREG1OUT x 0.900
05h	VREG1OUT x 0.425	25h	VREG1OUT x 0.585	45h	VREG1OUT x 0.745	65h	VREG1OUT x 0.905
06h	VREG1OUT x 0.430	26h	VREG1OUT x 0.590	46h	VREG1OUT x 0.750	66h	VREG1OUT x 0.910
07h	VREG1OUT x 0.435	27h	VREG1OUT x 0.595	47h	VREG1OUT x 0.755	67h	VREG1OUT x 0.915
08h	VREG1OUT x 0.440	28h	VREG1OUT x 0.600	48h	VREG1OUT x 0.760	68h	VREG1OUT x 0.920
09h	VREG1OUT x 0.445	29h	VREG1OUT x 0.606	49h	VREG1OUT x 0.765	69h	VREG1OUT x 0.925
0Ah	VREG1OUT x 0.450	2Ah	VREG1OUT x 0.610	4Ah	VREG1OUT x 0.770	6Ah	VREG1OUT x 0.930
0Bh	VREG1OUT x 0.455	2Bh	VREG1OUT x 0.615	4Bh	VREG1OUT x 0.775	6Bh	VREG1OUT x 0.935
0Ch	VREG1OUT x 0.460	2Ch	VREG1OUT x 0.620	4Ch	VREG1OUT x 0.780	6Ch	VREG1OUT x 0.940
0Dh	VREG1OUT x 0.465	2Dh	VREG1OUT x 0.625	4Dh	VREG1OUT x 0.785	6Dh	VREG1OUT x 0.945
0Eh	VREG1OUT x 0.470	2Eh	VREG1OUT x 0.630	4Eh	VREG1OUT x 0.790	6Eh	VREG1OUT x 0.950
0Fh	VREG1OUT x 0.475	2Fh	VREG1OUT x 0.635	4Fh	VREG1OUT x 0.795	6Fh	VREG1OUT x 0.955
10h	VREG1OUT x 0.480	30h	VREG1OUT x 0.640	50h	VREG1OUT x 0.800	70h	VREG1OUT x 0.960
11h	VREG1OUT x 0.485	31h	VREG1OUT x 0.645	51h	VREG1OUT x 0.805	71h	VREG1OUT x 0.965
12h	VREG1OUT x 0.490	32h	VREG1OUT x 0.650	52h	VREG1OUT x 0.810	72h	VREG1OUT x 0.970
13h	VREG1OUT x 0.495	33h	VREG1OUT x 0.655	53h	VREG1OUT x 0.815	73h	VREG1OUT x 0.975
14h	VREG1OUT x 0.500	34h	VREG1OUT x 0.660	54h	VREG1OUT x 0.820	74h	VREG1OUT x 0.980
15h	VREG1OUT x 0.505	35h	VREG1OUT x 0.665	55h	VREG1OUT x 0.825	75h	Setting disabled
16h	VREG1OUT x 0.510	36h	VREG1OUT x 0.670	56h	VREG1OUT x 0.830	76h	Setting disabled
17h	VREG1OUT x 0.515	37h	VREG1OUT x 0.675	57h	VREG1OUT x 0.835	77h	Setting disabled
18h	VREG1OUT x 0.520	38h	VREG1OUT x 0.680	58h	VREG1OUT x 0.840	78h	Setting disabled
19h	VREG1OUT x 0.525	39h	VREG1OUT x 0.685	59h	VREG1OUT x 0.845	79h	Setting disabled
1Ah	VREG1OUT x 0.530	3Ah	VREG1OUT x 0.690	5Ah	VREG1OUT x 0.850	7Ah	Setting disabled
1Bh	VREG1OUT x 0.535	3Bh	VREG1OUT x 0.695	5Bh	VREG1OUT x 0.855	7Bh	Setting disabled
1Ch	VREG1OUT x 0.540	3Ch	VREG1OUT x 0.700	5Ch	VREG1OUT x 0.860	7Ch	Setting disabled
1Dh	VREG1OUT x 0.545	3Dh	VREG1OUT x 0.705	5Dh	VREG1OUT x 0.865	7Dh	Setting disabled
1Eh	VREG1OUT x 0.550	3Eh	VREG1OUT x 0.710	5Eh	VREG1OUT x 0.870	7Eh	Setting disabled
1Fh	VREG1OUT x 0.555	3Fh	VREG1OUT x 0.715	5Fh	VREG1OUT x 0.875	7Fh	VCOMR setting

Power Control 5 (R14h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	RI[2:0]			0	RV[2:0]			0	0	LbiasEnb	

RI[2:0] – Adjusts the constant current in the operational amplifier circuit for the logic voltage regulator.

Table 43

RI[2:0]	DC current of op-amp
0	0.2
1	1
2	2
3	3
4	3
5	4
6	5
7	6

RV[2:0] – Set the logic voltage(VDDout) level. The RV bits can set the logic voltage(VDDout) level 0.45 to 0.80 times the Vcc level.

Table 44

RV[2:0]	VDDout voltage level
0	Vcc x 0.80
1	Vcc x 0.75
2	Vcc x 0.70
3	Vcc x 0.65
4	Vcc x 0.60
5	Vcc x 0.55
6	Vcc x 0.50
7	Vcc x 0.45

LbiasEnb – It enables bias circuit operate in minimum current consumption when standby mode is invoked. Default value of LbiasEnb is low which means enabling minimum current consumption.

RAM Address Set (R21h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	AD[15:0]															

AD[15:0] – Represents the GRAM address set in the AC (Address Counter) initially. The address in the AC is automatically updated in accordance with the AM, I/D bits as data are written to the internal GRAM so that data are written consecutively without resetting an address in the AC. The address is not automatically updated when reading data from the internal GRAM.

It is not possible to set an address in the AC when the LGDP4524 is in standby mode. Also be sure to set an address within the window address area.

Notes:

1. When the RGB interface is selected (RM = "1"), the address AD is set in the address counter every frame on the falling edge of VSYNC.
2. When the internal clock operation or the VSYNC interface mode is selected (RM = "0"), the address AD is set when executing an instruction.

Table 45: GRAM address range

AD[15:0]	GRAM setting
0000 – 00AF	Bitmap data for G1
0100 – 01AF	Bitmap data for G2
0200 – 02AF	Bitmap data for G3
0300 – 03AF	Bitmap data for G4
⋮	⋮
EC00 – ECAF	Bitmap data for G237
ED00 – EDAF	Bitmap data for G238
EE00 – EEAF	Bitmap data for G239
EF00 – EFAF	Bitmap data for G240

Write Data to GRAM (R22h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	WD[17:0]															

WD[17:0] – If data are less than 18 bits in unit, the LGDP4524 expands the data into 18 bits internally before written to the internal GRAM. How the data are expanded into 18 bits differs for each interface and data transfer mode.

The grayscale level is selected according to GRAM data. The GRAM address is automatically updated according to the AM and I/D bits as data are written to the internal GRAM. In standby mode, no access to the internal GRAM is allowed. When the 8 or 16 bit interface mode is selected, data are expanded into 18 bits internally by writing the MSBs of R and B dots to the LSBs of R and B dots respectively.

When writing data to the GRAM via a system interface while using the RGB interface, be sure there is no conflict between writing operations via respective interfaces (RGB and system interfaces). When the18-bit RGB interface is selected, 18-bit data are written via the DB[17:0] pins and 262,144 colors are available. When the 16-bit RGB interface is selected, the MSBs of R and B dots are also written to the LSBs of R and B dots respectively, and 65,536 colors are available.

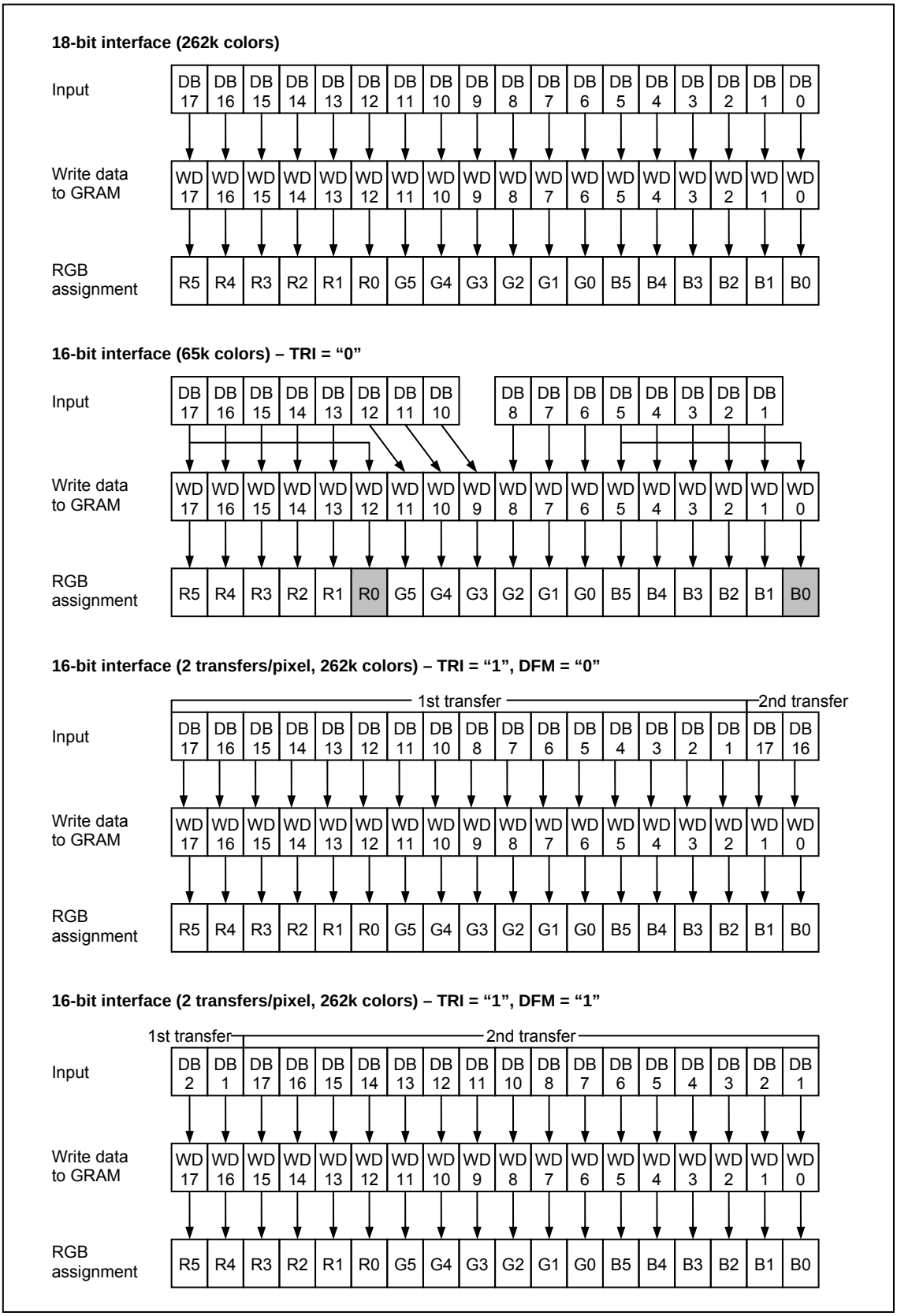


Figure 11: Write data to GRAM in 18-/16-bit interface mode

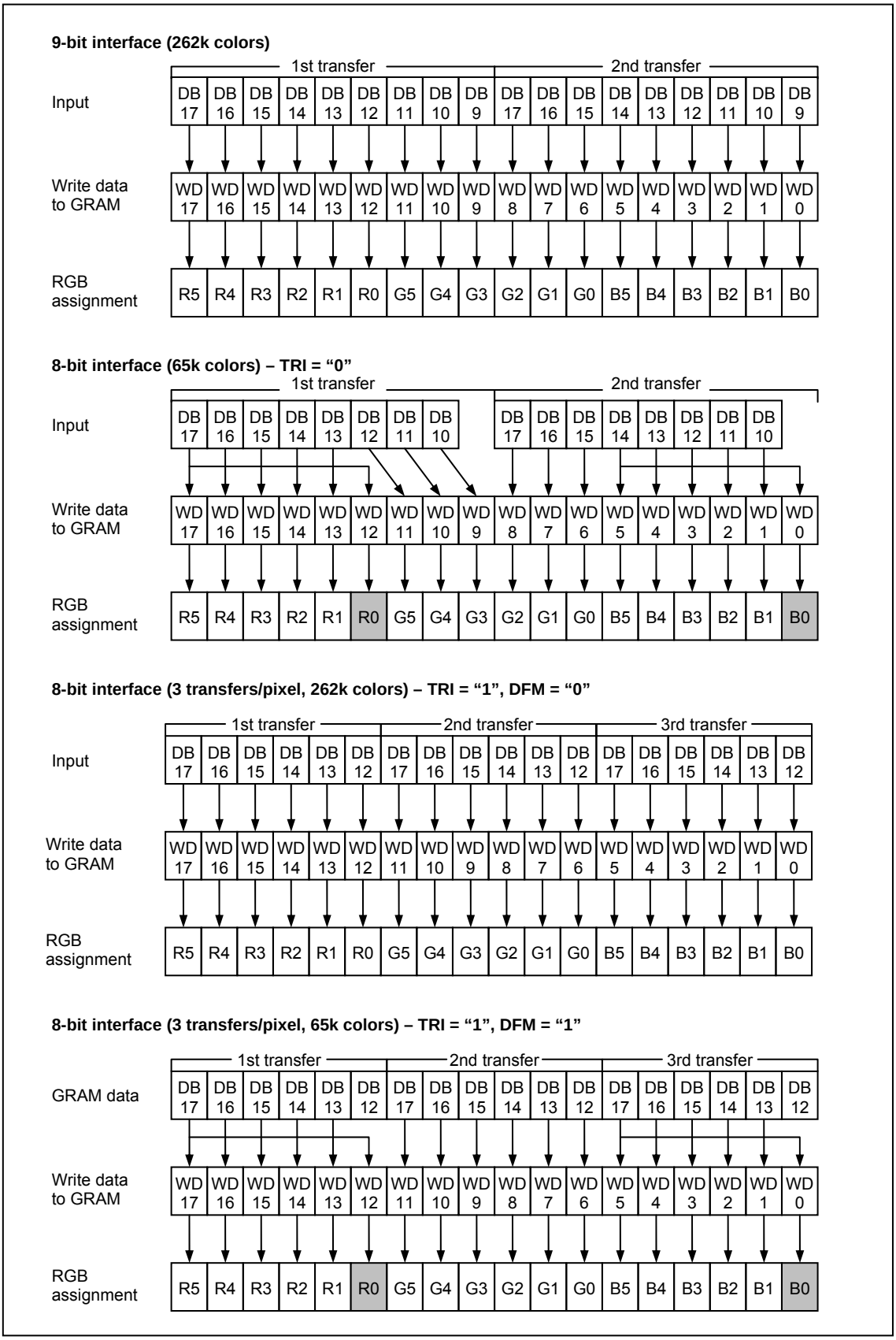


Figure 12: Write data to GRAM in 9-/8-bit interface mode

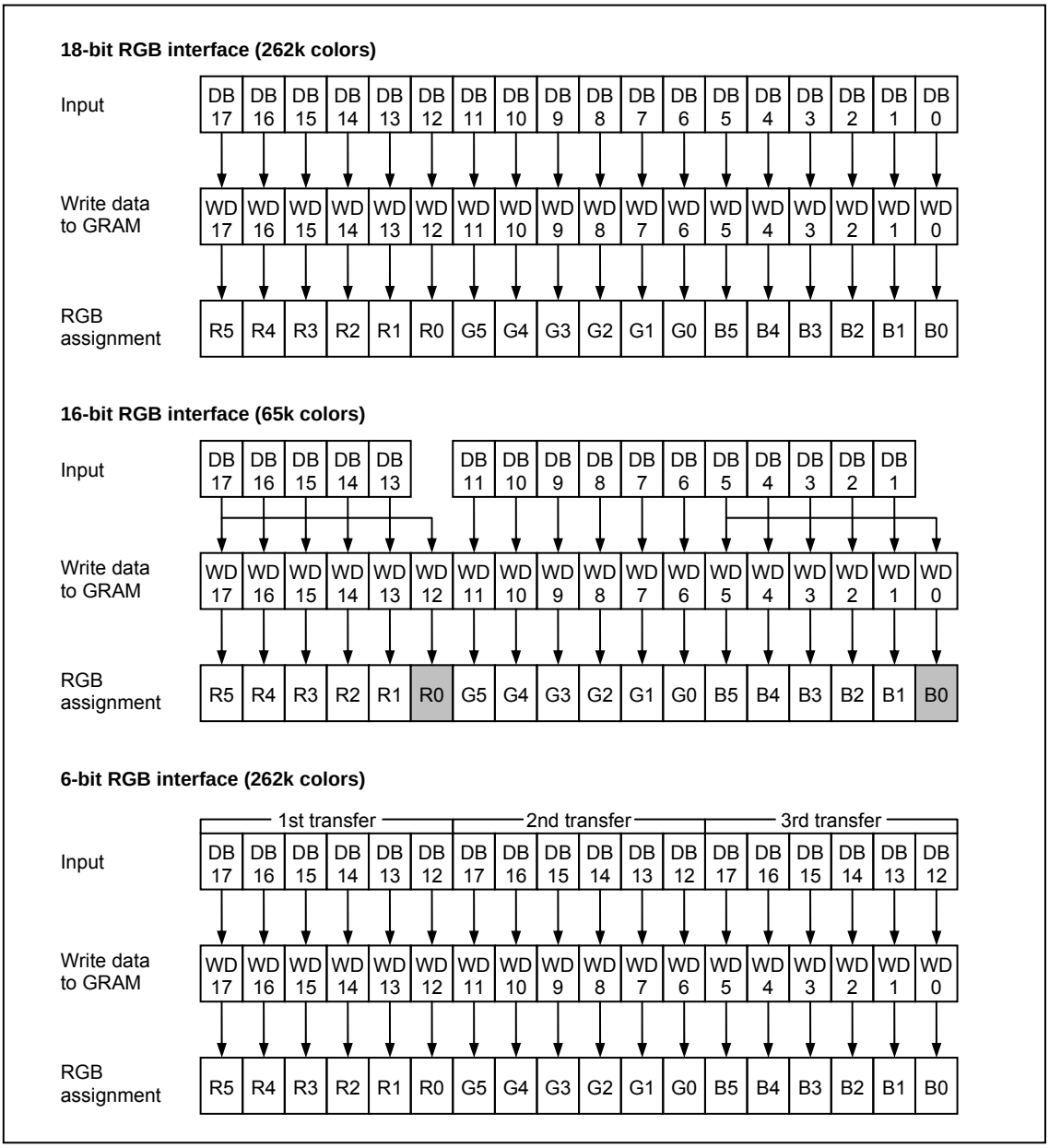


Figure 13: Write data to GRAM in 18-/16-/6-bit RGB interface mode

Table 46: GRAM data and LCD output level

GRAM data setting: RGB each	Grayscale	
	Negative	Positive
0	V0	V63
1	V1	V62
2	V2	V61
3	V3	V60
⋮	⋮	⋮
60	V60	V3
61	V61	V2
62	V62	V1
63	V63	V0

RAM Access via RGB I/F and System I/F

In RGB interface mode, the LGDP4524 stores all display data in the internal RAM, enabling transferring only moving picture data only when updating the frames of a moving picture. While the moving picture frames are not updated, it is possible to write data displayed in the area outside the moving picture area via the system interface.

In RGB interface mode, the LGDP4524 writes data to the internal RAM in synchronization with DOTCLK during ENABLE = “Low”. To access the internal RAM via the system interface while using the RGB interface for display operation, set ENABLE “High” to stop writing via the RGB interface. To start accessing the internal RAM via the RGB interface after accessing the RAM via the system interface, wait at least for a write/read bus cycle time. Data will not be written properly to the internal RAM when writing operations via both RGB and system interfaces are conflicting.

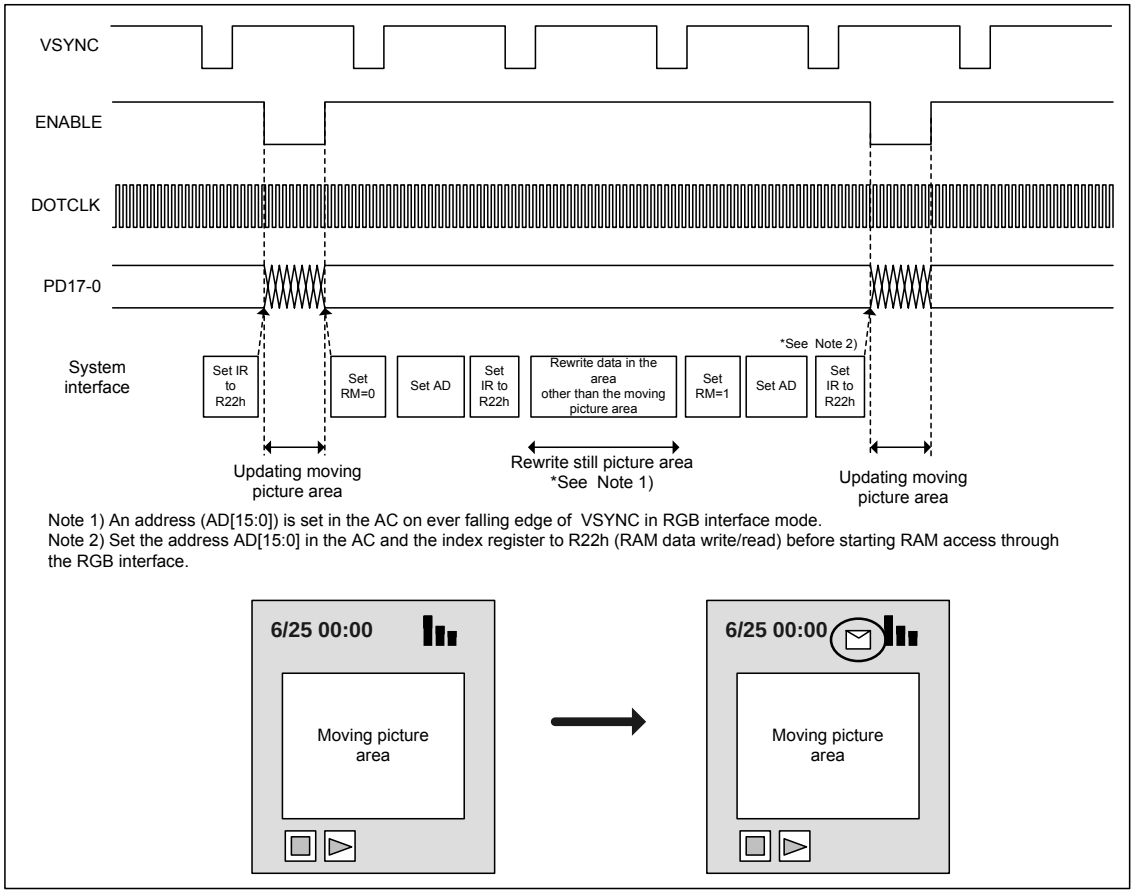


Figure 14 RAM Acess via RGB Interface and System Interface

Read Data Read from GRAM (R22h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R	1	RD[17:0]															

RD[17:0] – Reads 18-bit data from the GRAM. The bit assignment between the data read out from the GRAM and the DB[17:0] pins differs for each interface.

When data are read out from the GRAM to the microcomputer, the first word read immediately after executing RAM address set is taken in the internal read data latch and invalid data are sent to the data bus DB[17:0]. Valid data are sent to the data bus as the LGDP4524 reads out the second word data from the internal GRAM.

The 1st word data read into the internal read data latch are used for a bit operation (logical/compare operation) is performed inside the LGDP4524. Accordingly, the bit operation is processed with one read out operation. Note that the bit operation is performed on the data in units of 18 bits.

When the 8 or 16-bit interface is selected, the LSBs of R and B dots are not read out.

Note: This register is not available with the RGB interface.

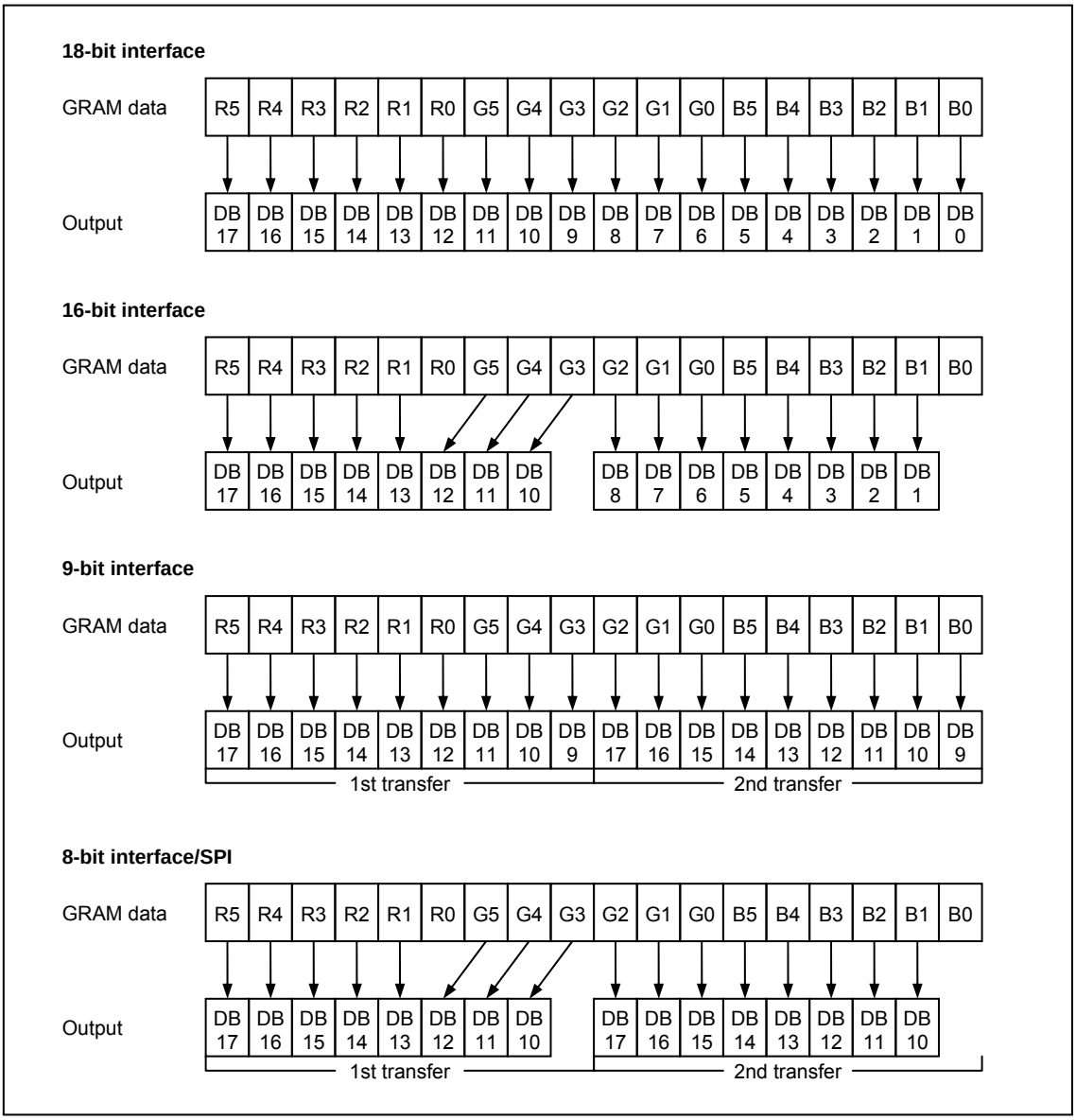


Figure 15: Read data from GRAM

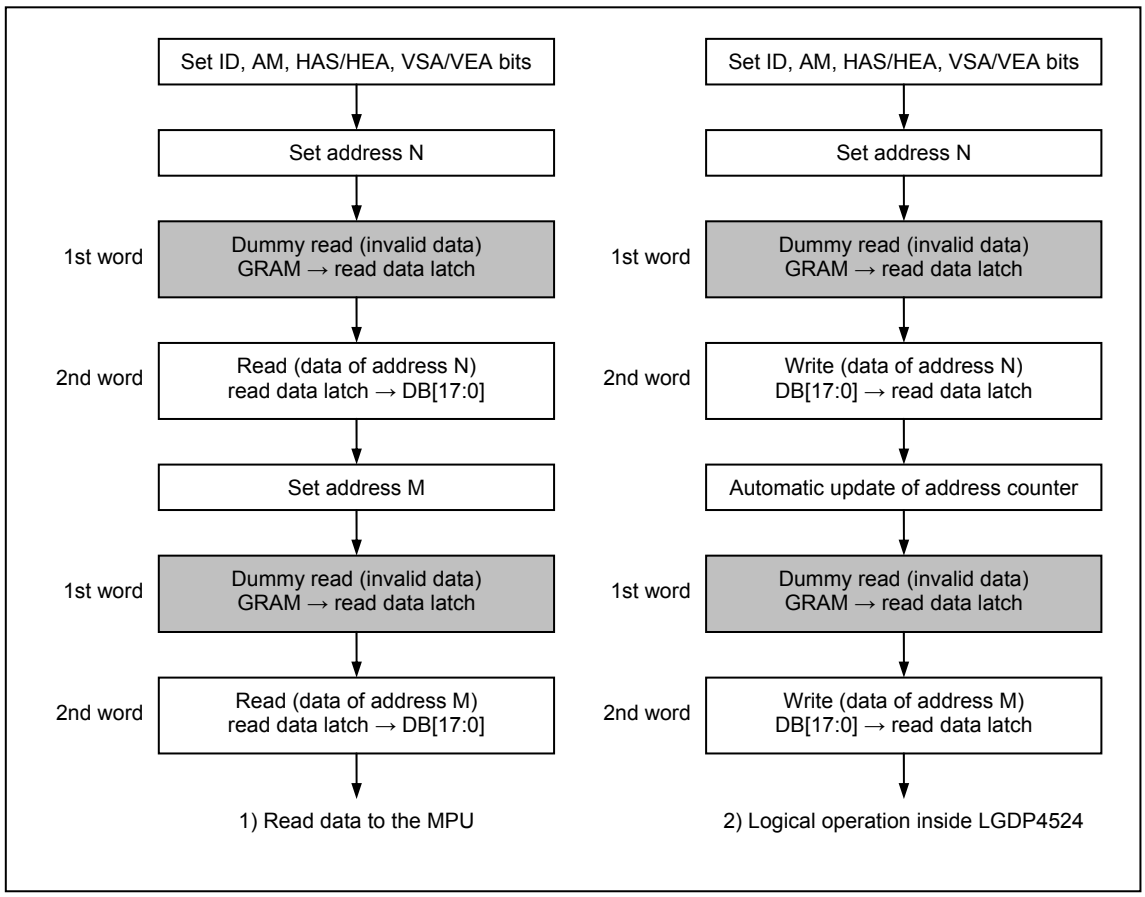


Figure 16: GRAM read sequence

γ Control (R30h to R3Fh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	PKP1[2:0]			0	0	0	0	0	PKP0[2:0]		
W	1	0	0	0	0	0	PKP3[2:0]			0	0	0	0	0	PKP2[2:0]		
W	1	0	0	0	0	0	PKP5[2:0]			0	0	0	0	0	PKP4[2:0]		
W	1	0	0	0	0	0	PRP1[2:0]			0	0	0	0	0	PRP0[2:0]		
W	1	0	0	0	0	0	PKN1[2:0]			0	0	0	0	0	PKN0[2:0]		
W	1	0	0	0	0	0	PKN3[2:0]			0	0	0	0	0	PKN2[2:0]		
W	1	0	0	0	0	0	PKN5[2:0]			0	0	0	0	0	PKN4[2:0]		
W	1	0	0	0	0	0	PRN1[2:0]			0	0	0	0	0	PRN0[2:0]		
W	1	0	0	0	VRP1[4:0]					0	0	0	VRP0[4:0]				
W	1	0	0	0	VRN1[4:0]					0	0	0	VRN0[4:0]				
W	1	0	0	0	0	0	PFP1[2:0]			0	0	0	0	0	PFP0[2:0]		
W	1	0	0	0	0	0	PFP3[2:0]			0	0	0	0	0	PFP2[2:0]		
W	1	0	0	0	0	0	PFN1[2:0]			0	0	0	0	0	PFN0[2:0]		
W	1	0	0	0	0	0	PFN3[2:0]			0	0	0	0	0	PFN2[2:0]		
W	1	0	0	0	0	0				0	0	0	0	0	PMP[2:0]		
W	1	0	0	0	0	0				0	0	0	0	0	PMN[2:0]		

PKP5-0[2:0] – γ fine adjustment register bits for positive polarity

PRP1-0[2:0] – γ gradient adjustment register bits for positive polarity

PKN5-0[2:0] – γ fine adjustment register bits for negative polarity

PRN1-0[2:0] – γ gradient adjustment register bits for negative polarity

VRP1-0[4:0] – amplitude adjustment register bits for positive polarity

VRN1-0[4:0] – amplitude average adjustment register bits for negative polarity

PFP3-0[2:0] – γ fine adjustment register bits for positive polarity

PFN3-0[2:0] – γ fine adjustment register bits for negative polarity

PMP[2:0] – γ fine adjustment register bits for positive polarity

PMN[2:0] – γ fine adjustment register bits for negative polarity

For details see "γ-Correction Function" section

Gate Scan Position (R40h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	SCN[4:0]				

SCN[4:0] – The LGDP4524 allows specifying the gate line from which the gate driver starts scan by setting the SCN4-0 bits.

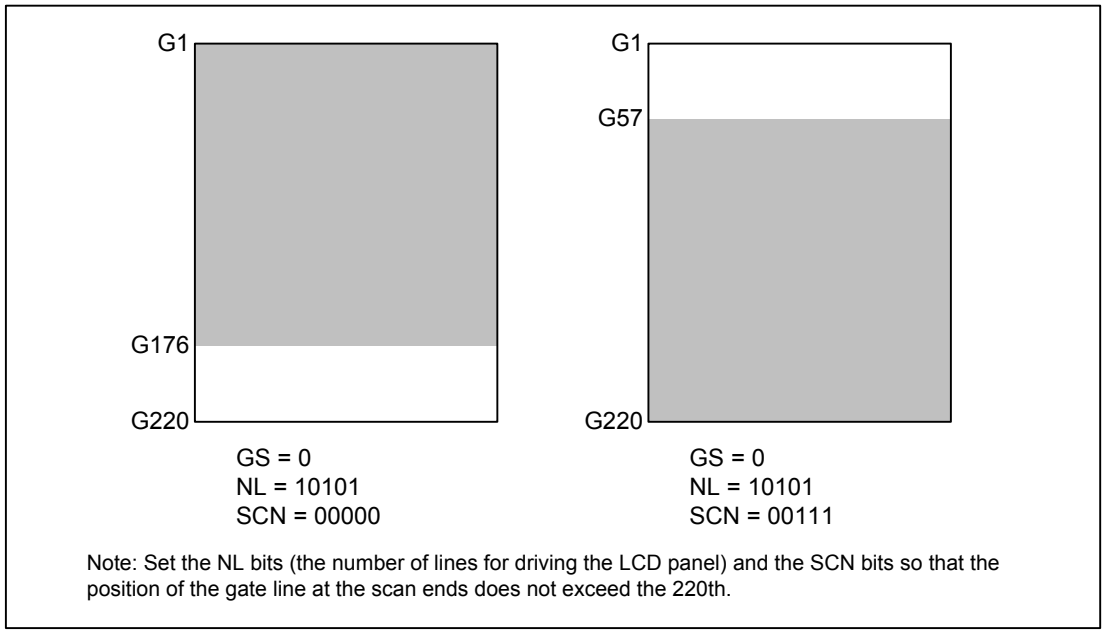


Figure 17 Example of Setting NL, GS & SCN

Table 47

SCN[4:0]	Scan start position (gate line)	
	GS = "0"	GS = "1"
00h	G1	G220
01h	G9	G212
02h	G17	G204
03h	G25	G196
04h	G33	G188
05h	G41	G180
06h	G49	G172
07h	G57	G164
08h	G65	G156
09h	G73	G148
0Ah	G81	G140
0Bh	G89	G132
0Ch	G97	G124
0Dh	G105	G116
0Eh	G113	G108
0Fh	G121	G100
10h	G129	G92
11h	G137	G84
12h	G145	G76
13h	G153	G68
14h	G161	G60
15h	G169	G52
16h	G177	G44
17h	G185	G36
18h	G193	G28
19h	G201	G20
1Ah	G209	G12
1Bh	G217	G4

Vertical Scroll Control (R41h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	VL[7:0]							

VL[7:0] – Sets the scrolling amount of an image on the screen in vertical direction. The scrolling amount can be set from 0 line to 220 lines. The start position for displaying the image is shifted vertically by the number of lines set with the VL bits. The part of the image, which is scrolled out from the end line (the 220th line) as a result of scrolling, is displayed from the 1st line of the physical display. The VL bits are enabled when either first display vertical scroll enable bit VLE[0] or the second display vertical scroll enable bit VLE[1] is set to "1". When VLE[1:0] = "00", the image on the screen is displayed at the position set with the SS and SE bits. The vertical scrolling function is not available with the external display interface.

Table 48

VL[7:0]	Scrolling lines
0	0 line
1	1 line
2	2 lines
⋮	⋮
218	218 line
219	219 lines

1st-Screen Drive Position (R42h)

2nd-Screen Drive Position (R43h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	SE1[7:0]								SS1[7:0]							
W	1	SE2[7:0]								SS2[7:0]							

SS1[7:0] – Sets the position of the start line from which the first display starts. The gate driver starts scan from the line of the number set with the SS1 bits + 1.

SE1[7:0] – Sets the position of the end line at which the first display ends. The gate driver ends scan at the line of the number set with the SE1 bits + 1. For instance, when SS1 = 07h and SE1 = 10h, the first display is shown on the gate lines from G8 to G17, and gate lines G1 to G7 and G18 thereafter are driven to show a blank screen. Be sure that SS1 ≤ SE1 ≤ EFh. For details, see the "Partial Display Function" section.

SS2[7:0] – Sets the position of the start line from which the second display starts. The gate driver starts scan from the line of the number set with the SS2 bits + 1. The second display is shown when SPT = "1".

SE2[7:0] – Sets the position of the end line at which the second display ends. The gate driver ends scan at the line of the number set with the SE2 bits + 1. For instance, when SPT = "1", and SS2 = 20h, SE2 = 4Fh, the second display is shown on the gate lines from G33 to G80.

Be sure that SS1 ≤ SE1 < SS2 ≤ SE2 ≤ EFh. For details, see the "Partial Display Function" section.

Horizontal RAM Address Position (R44h)

Vertical RAM Address Position (R45h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	HEA[7:0]								HSA[7:0]							
W	1	VEA[7:0]								VSA[7:0]							

HSA[7:0]/HEA[7:0] – HSA and HEA represent the respective addresses at the start and end of the window address area in horizontal direction. By setting HSA and HEA bits, it is possible to limit the area on the GRAM horizontally for writing data. The HSA and HEA bits must be set before starting RAM write operation. In setting these bits, be sure 00h ≤ HSA < HEA ≤ AFh.

VSA[7:0]/VEA[7:0] – VSA and VEA represent the respective addresses at the start and end of the window address area in vertical direction. By setting VAS and VEA bits, it is possible to limit the area on the GRAM vertically for writing data. The VSA and VEA bits must be set before starting RAM write operation. In setting, be sure 00h ≤ VSA < VEA ≤ EFh.

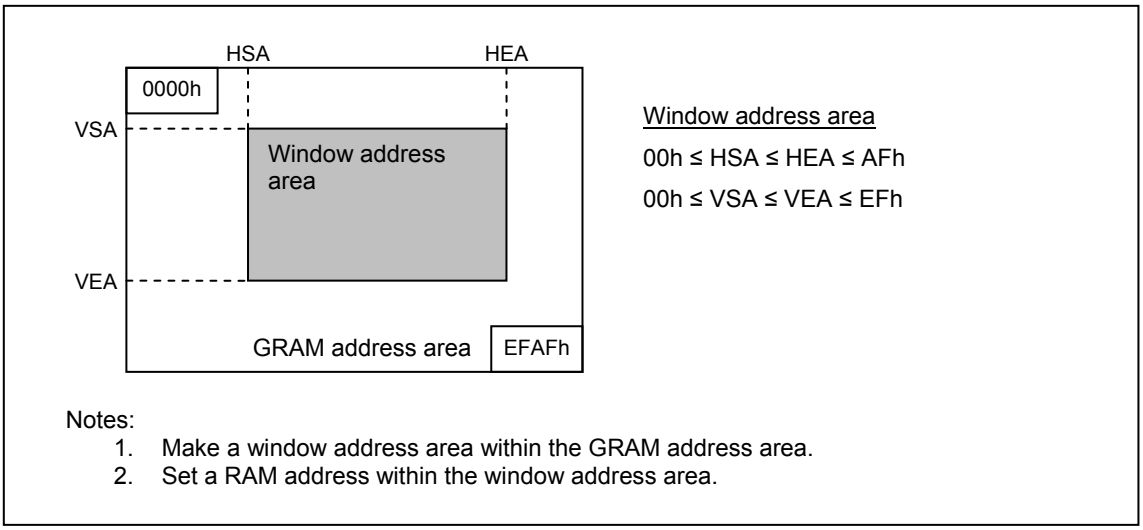


Figure 18: GRAM address and window address area

EPROM Control 1 (R60h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	POR	EVPP	PPROG	PWE	PA[1:0]		0	PDIN[6:0]						

EPROM programming control. See “EPROM Control” section.

Reading this instruction returns 8 bits data of a bank selected by RA[1:0] in R61h instruction.

POR – Power-on reset.

EVPP – Power switch control for the VPP pin of the embedded EPROM. When VPP = “1”, the internal VPP is set to 7.5V; otherwise it is set to 1.8V.

PPROG – Program mode enable.

PWE – Control Write enable.pin of embedded EPROM.

PA[1:0] – Program address input. This selects one of four banks of the EPROM.

PDIN[6:0] – Controls prgram data pins of EPROM. This corresponds to VCM[6:0] bits of R13h.

EPROM Control 2 (R61h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	AUTOWE	RA[1:0]		VCMSEL[1:0]	

EPROM read control. See “EPROM Control” section.

AUTOWE – Automatic Write Address Increment.

0:. While program operation, the write address of a bank increase automatically without setting PA[1:0] bits of R60h.

1 : While program operation, The write address of a bank can be selected by setting PA bits of R60h.

RA[1:0] – Read address input. This selects one of four banks of the EPROM.

Test Register 1 (R71h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	TDLY[1:0]		0	T8CL	TPOL[1:0]		0	TMEM	TOSC	TFN

TFN – Sets the chip to function test mode.

TOSC – Sets the pin FLM to output the internal oscillator signal instead of the frame head pulse signal

TMEM – Sets the pin FLM to output the internal memory A read enable signal instead of the frame head pulse signal.

TPOL[1:0] – When TPOL[1] = “1”, liquid crystal polarity is fixed to positive polarity if TPOL[0] = “0” or negative polarity if TPOL[0] = “1”. Affected are Vcom and source outputs. When TPOL[0] = “0”, field/line polarity inversion takes place.

T8CL – Set Power Saving for particular images. T8CL= “1”, that means it has a chance to reserve power and “0” means it operates normally when images are displayed.

TDLY[1:0] – Set the delay of arbiter logic,

Delay of TDLY[1:0] : 11 < 00 < 01 < 10

Test Register 2 (R72h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	REGULPD	0	0	0	**S_HIZ**	0	0	0	MVCOML	0	0	MVCI	0

MVCOML – Set Multiple Option for VCOM regulator.

S_HIZ – “0” Normal stepup2 operation

“1” Disable stepup2 and Hi-z stepup2 output for test mode.

REGULPD – Regulator Power Down

MVCI– Multiple Vci1 driving capability

Instruction List

Table 49

Index	Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
00	Start oscillation																1	-
01	Driver output control		VSPL	HSPL	DPL	EPL	SM	GS	SS				NL[4:0]					001B
02	LCD drive AC control					FLD[1:0]		B/C	EOR			NW[5:0]						0400
03	Entry mode	TRI	DFM		BGR							ID[1:0]		AM				0030
04	Resize control							RCV[1:0]				RCH[1:0]				RSZ[1:0]		0000
05	-																	
06	-																	
07	Display control 1			PTS[2:0]			VLE[1:0]		SPT			GON	DTE	CL	REV	D[1:0]		0000
08	Display control 2					FP[3:0]								BP[3:0]				0808
09	Display control 3											PTG[1:0]		ISC[3:0]				0000
0A	-																	
0B	Frame cycle adjustment	NO[1:0]		SDT[1:0]		EQ[1:0]		DIV[1:0]			RTN[6:1]							002C
0C	External display I/F ctrl								RM			DM[1:0]				RIM[1:0]		0000
10	Power control 1		SAP[2:0]				BT[2:0]			DUAL	AP[2:0]			STB	DK	SLP	DSTB	0004
11	Power control 2						DC1[2:0]				DC0[2:0]				VC[2:0]			0000
12	Power control 3												PON	VRH[3:0]				0000
13	Power control 4			VCOMG	VDV[4:0]						VCM[6:0]							0000
14	VDD regulator control						RI[2:0]				RV[2:0]					LbaisEn		0040
21	RAM address set	AD[15:0]																0000
22	RAM data R/W	RAM 18-bit R/W data																-
30	Gamma control 1						PKP1[2:0]								PKP0[2:0]			0000
31	Gamma control 2						PKP3[2:0]								PKP2[2:0]			0000
32	Gamma control 3						PKP5[2:0]								PKP4[2:0]			0000
33	Gamma control 4						PRP1[2:0]								PRP0[2:0]			0000
34	Gamma control 5						PKN1[2:0]								PKN0[2:0]			0000
35	Gamma control 6						PKN3[2:0]								PKN2[2:0]			0000
36	Gamma control 7						PKN5[2:0]								PKN4[2:0]			0000
37	Gamma control 8						PRN1[2:0]								PRN0[2:0]			0000
38	Gamma control 9				VRP1[4:0]									VRP0[3:0]				0000
39	Gamma control 10				VRN1[4:0]									VRN0[3:0]				0000
3A	Gamma control 11						PFP1[2:0]								PFP0[2:0]			0000
3B	Gamma control 12						PFP3[2:0]								PFP2[2:0]			0000
3C	Gamma control 13						PFN1[2:0]								PFN0[2:0]			0000
3D	Gamma control 14						PFN3[2:0]								PFN2[2:0]			0000
3E	Gamma control 15														PMP[2:0]			0000
3F	Gamma control 16														PMN[2:0]			0000
40	Gate scan start position												SCN[4:0]					0000
41	Vertical scroll control									VL[7:0]								0000
42	First screen position	SE1[7:0]								SS1[7:0]								FF00
43	Second screen position	SE2[7:0]								SS2[7:0]								FF00
44	Horizontal RAM address	HEA[7:0]								HSA[7:0]								AF00
45	Vertical RAM address	VEA[7:0]								VSA[7:0]								DB00
60	EPROM control 1			POR	VPP	PPROG	PWE	PA[1:0]		PDIN[7:0]								0000
61	EPROM control 2												AUTOWE	RA[1:0]		VCMSEL[1:0]		0000
71	Test register 1							TDLY[1:0]			T8CL	TPOL[1:0]			TMEM	TOSC	TFN	0000
72	Test register 2				REGULPD				S_HIZ				MVCOML			MVCI		0000

Interface Specifications

The LGDP4524 has the system interface for making instruction setting and other settings, and the external display interface for displaying a moving picture. The LGDP4524 allows selecting an optimum interface for the display (moving or still picture) in order to transfer data efficiently.

As the external display interface, the LGDP4524 has the RGB interface and the VSYNC interface, enabling data rewrite operation without flicker the moving picture on the screen.

In RGB interface mode, display operations are performed in synchronization with synchronizing signals VSYNC, HSYNC, and DOTCLK. Display data are written to the internal RAM according to the polarity of the data enable signal ENABLE via the moving picture display data bus DB[17:0] in synchronization with VSYNC, HSYNC, and DOTCLK. All display data are stored in the LGDP4524's GRAM to limit data transfer to only when switching the frames of a moving picture. By using the window address function, it is possible to limit the RAM area to be rewritten for displaying a moving picture and display both the moving picture and the data written on the RAM at a time.

In VSYNC interface mode, the internal display operations are synchronized with the frame synchronization signal VSYNC. The VSYNC interface enables a moving picture display via the system interface by writing data to the internal GRAM at more than the minimum speed in synchronization with the falling edge of VSYNC. In this case, there are constraints in speed and method for writing data to the internal RAM.

The LGDP4524 operates in one of the following 4 modes in line with the state of display. The mode for display operation is set in the external interface control register. When switching from one mode to another, refer to the sequences mentioned in the sections of RGB and VSYNC interfaces.

Table 50

Operation mode	RAM access setting (RM)	Display operation mode (DM)
Internal operating clock only: Displaying still pictures	System interface (RM = 0)	Internal operating clock (DM = 0)
RGB interface (1): Displaying moving pictures	RGB interface (RM = 1)	RGB interface (DM = 1)
RGB interface (2): Rewriting still pictures while displaying moving pictures	RGB interface (RM = 1)	RGB interface (DM = 1)
VSYNC interface: Displaying moving pictures	System interface (RM = 0)	VSYNC interface (DM = 2)

Notes:

1. Instructions are set only via the system interface.
2. The RGB I/F and the VSYNC I/F are not available simultaneously.
3. Do not make changes to the RGB I/F mode (RIM[1:0] bits) while an RGB I/F is in operation.
4. See the sections of RGB and VSYNC interfaces for the sequences to follow when switching from one mode to another.

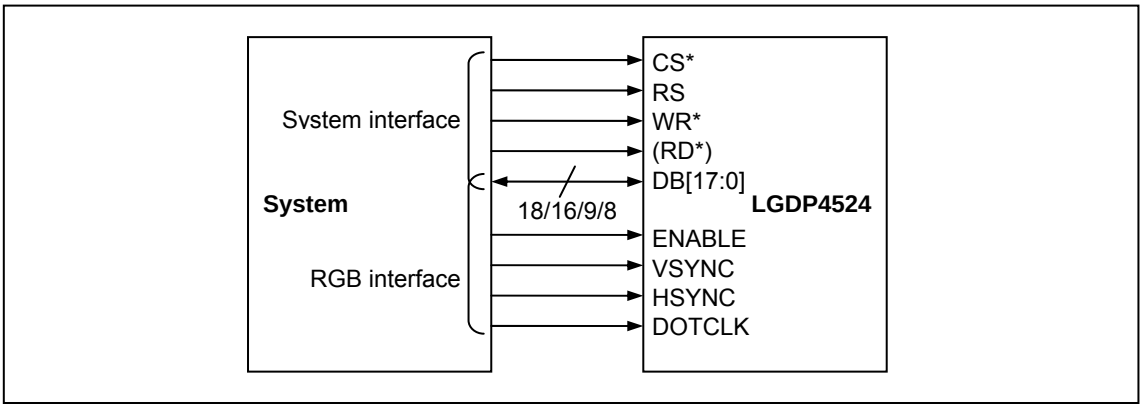


Figure 19: Interfaces between system and LGDP4524

System Interface

The following are the system interfaces available with the LGDP4524. The interface is selected by setting the IM[3:0] pins. The system interface is used for setting instructions and RAM access.

Table 51

IM[3:0]	MPU interface mode	DB pin in use
0000	68-system 16-bit interface	DB[17:10], DB[8:1]
0001	68-system 8-bit interface	DB[17:10]
0010	80-system 16-bit interface	DB[17:10], DB[8:1]
0011	80-system 8-bit interface	DB[17:10]
010*	Serial peripheral interface (SPI)	SDI, SDO
011*	Setting disabled	-
1000	68-system 18-bit interface	DB[17:0]
1001	68-system 9-bit interface	DB[17:9]
1010	80-system 18-bit interface	DB[17:0]
1011	80-system 9-bit interface	DB[17:9]
11**	Setting disabled	-

80-System 18-Bit Interface

The 80-system 18-bit parallel system interface is selected by setting the IM[3:0] pins to “1010”.

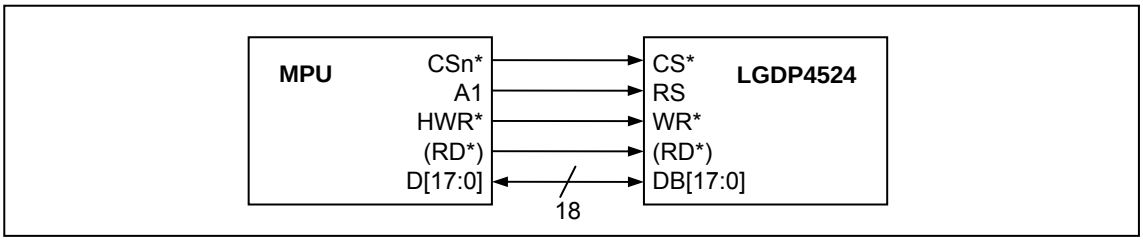


Figure 20: 18-bit microcomputer and LGDP4524

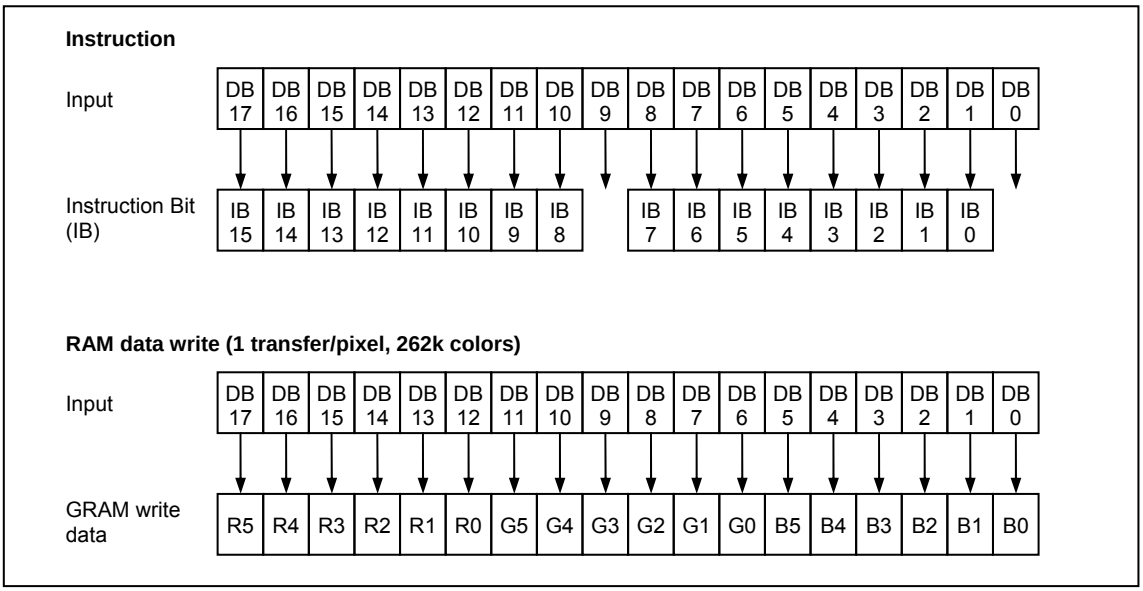


Figure 21: Data format for 18-bit interface

80-System 16-Bit Interface

The 80-system 16-bit parallel system interface is selected by setting the IM[3:0] pins to “0010”.

The unused pins, “DB[9] and DB[0] must be tied to GND.

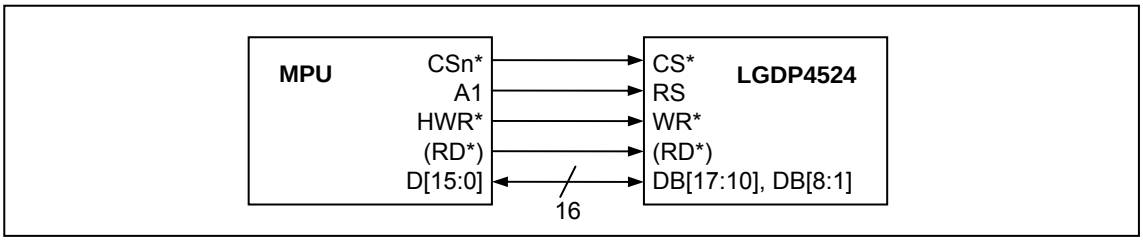


Figure 22: 16-bit microcomputer and LGDP4524

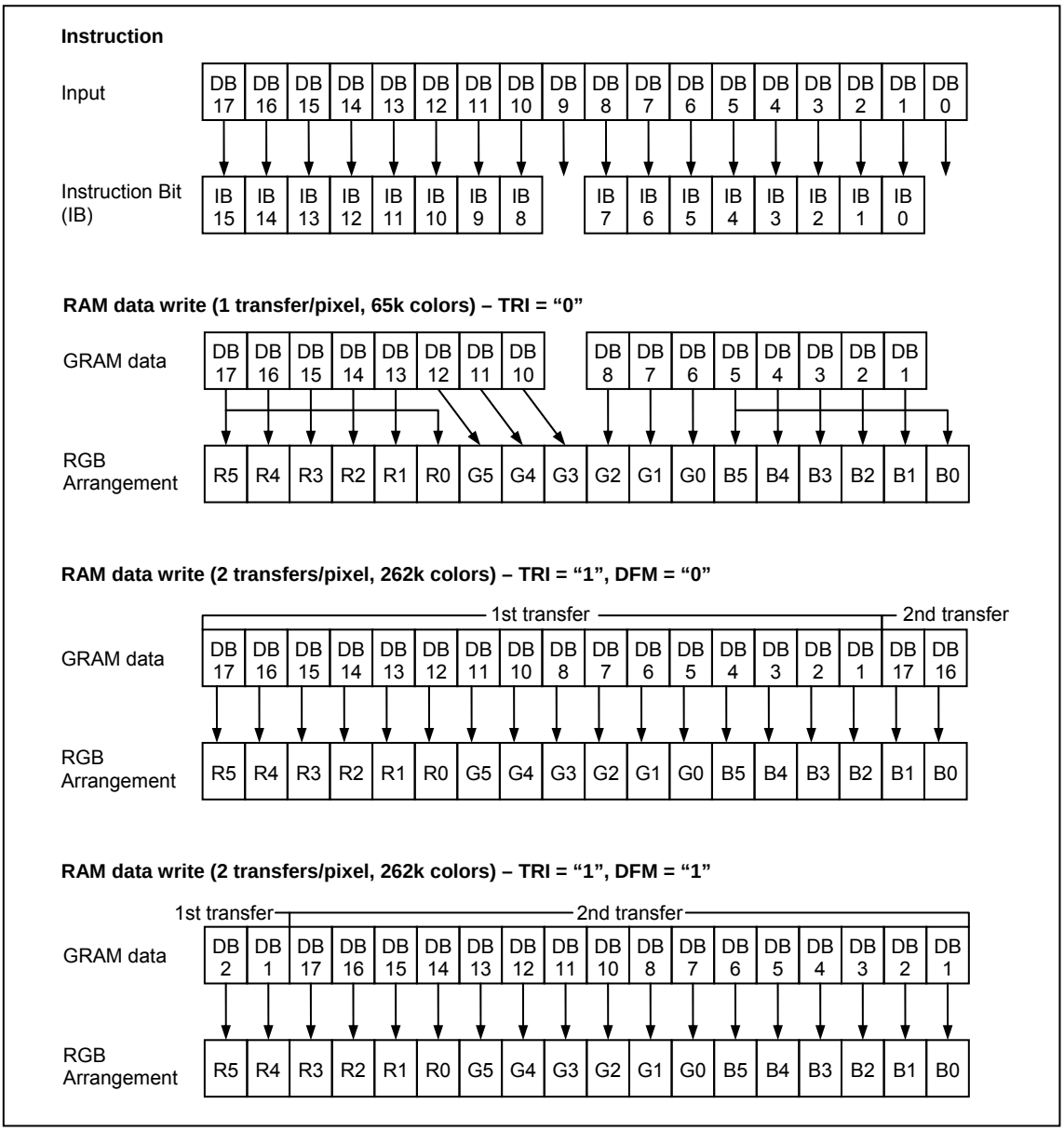


Figure 23: Data format for 16-bit interface

Data Transfer Synchronizing in 16-Bit Bus Interface Mode

The LGDP4524 supports a data transfer synchronization function, which resets the counter to count the numbers of upper 16/2-bit and lower 2/16-bit transfers in 16 bits x 2 transfer mode. When a mismatch occurs in data transfers due to noise and so on, the 000h instruction is written 4 times consecutively to reset the upper and lower counters to restart data transfers from the upper 2/16 bits. The synchronization function, when executed periodically, will prevent the runaway of the display system.

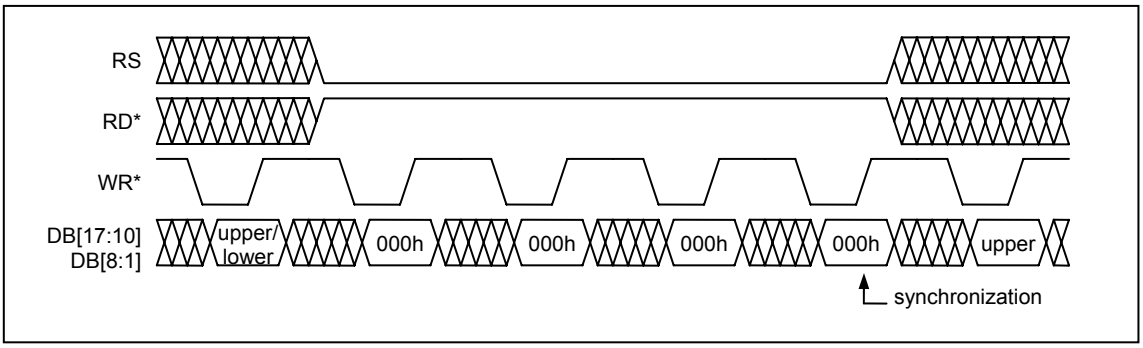


Figure 24: 16-bit data transfer synchronization

80-System 9-Bit Interface

The 80-system 9-bit parallel system interface using the DB17 to DB9 pins is selected by setting the IM[3:0] pins to “1011”. When transferring a 16-bit instruction, it is divided into upper and lower 8 bits (the LSB is not used), and the upper 8 bits are transferred first. The RAM write data are also divided into the upper and lower 9 bits, and the upper bits are transferred first. The unused DB[8:0] pins must be fixed at either Vcc or GND level. When writing the index register, the upper byte (8 bits) must be written.

The unused pins, “DB[8:0] must be tied to GND

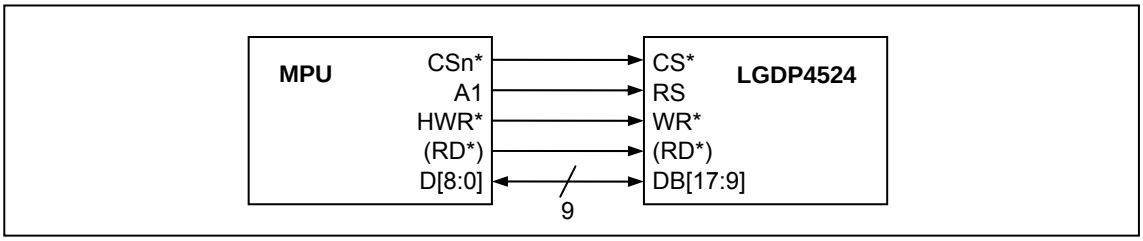


Figure 25: 9-bit microcomputer and LGDP4524

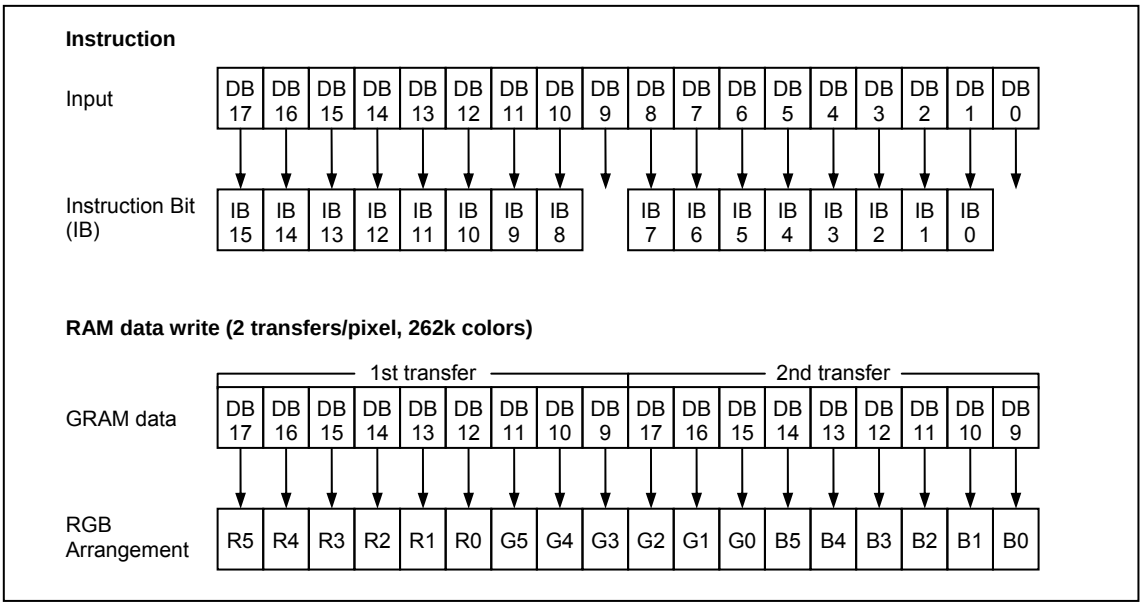


Figure 26: Data format for 9-bit interface

Data Transfer Synchronizing in 9-Bit Bus Interface Mode

The LGDP4524 supports a data transfer synchronization function to reset upper and lower counters counting the number of transfers of upper and lower 9 bits in 9-bit bus interface mode. If a mismatch arises in the numbers of transfers between the upper and lower 9 bit counters due to noise and so on, the 000h instruction is written 4 times consecutively to reset the upper and lower counters so that data transfer will restart with a transfer of upper 9 bits. This synchronization function, when executed periodically, can effectively prevent runaway of display system.

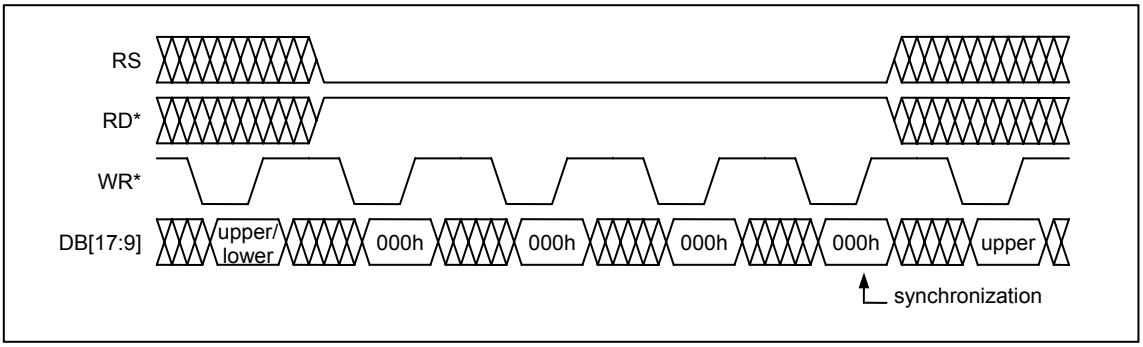


Figure 27: 9-bit data transfer synchronization

80-System 8-Bit Interface

The 80-system 8-bit parallel system interface using the DB17 to DB10 pins is selected by setting the IM[3:0] pins to “0011”. When transferring a 16-bit instruction, it is divided into upper and lower 8 bits and the upper 8 bits are transferred first. The RAM data is also divided into the upper and lower 8 bits, and the upper bits are transferred first. The RAM write data are expanded into 18 bits internally (see the figure below). The unused pins DB[9:0] must be fixed at either Vcc or GND level. When writing the index register, the upper byte (8 bits) must be written.

The unused pins, “DB[9:0] must be tied to GND

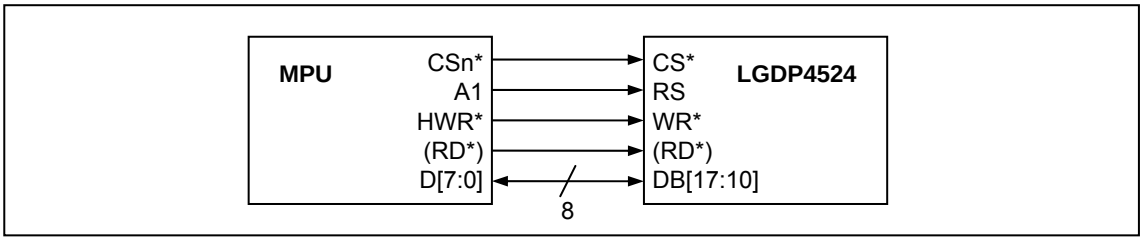


Figure 28: 8-bit microcomputer and LGDP4524

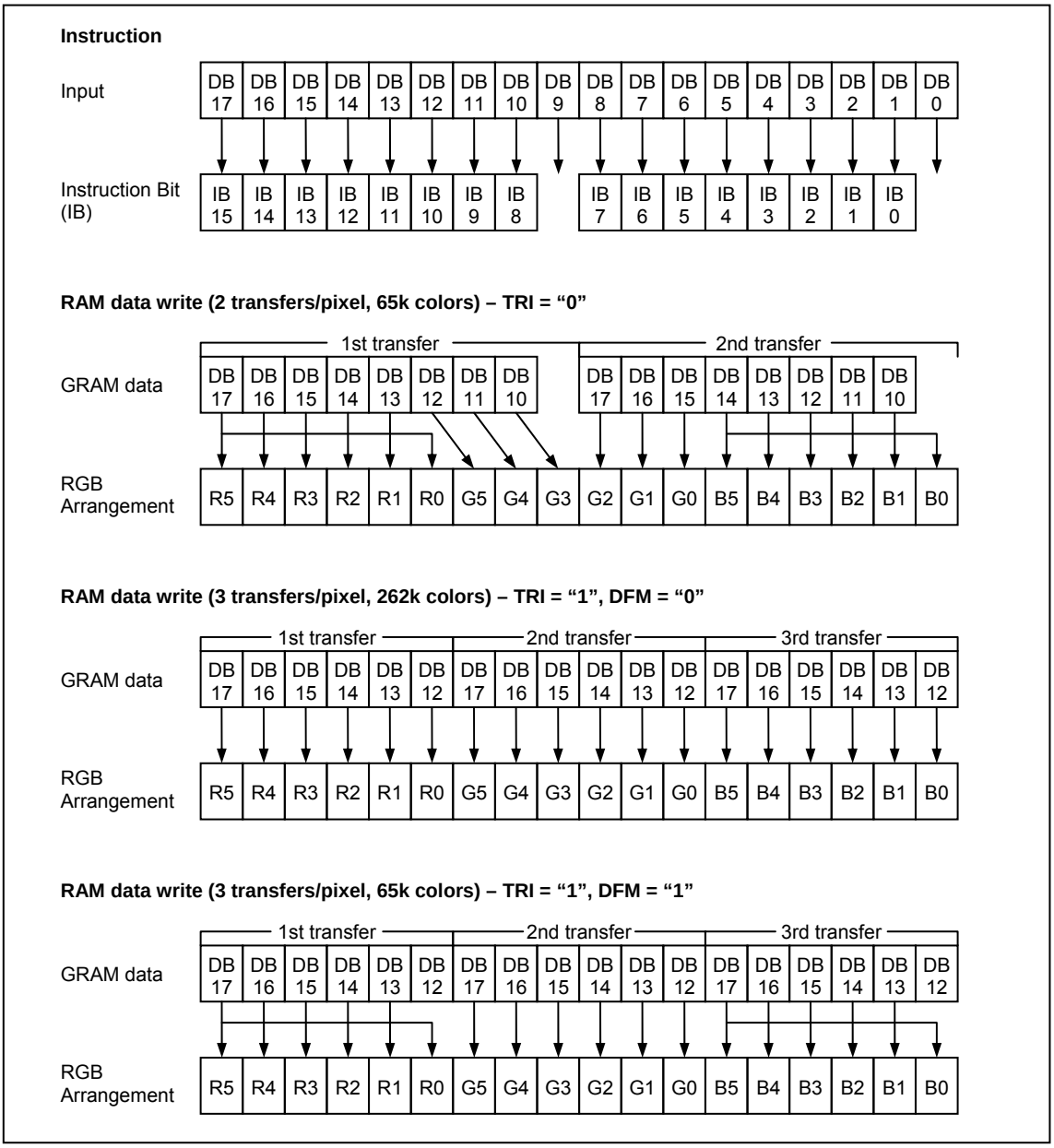


Figure 29: Data format for 8-bit interface

Data Transfer Synchronization in 8-Bit Bus Interface Mode

The LGDP4524 supports a data transfer synchronization function to reset upper and lower counters counting the number of transfers of upper and lower 8 bits in 8-bit bus interface mode. If a mismatch arises in the numbers of transfers between the upper and lower 8 bit counters due to noise and so on, the 00h instruction is written 4 times consecutively to reset the upper and lower counters so that data transfer will restart with a transfer of upper 8 bits. This synchronization function, when executed periodically, can effectively prevent runaway of display system.

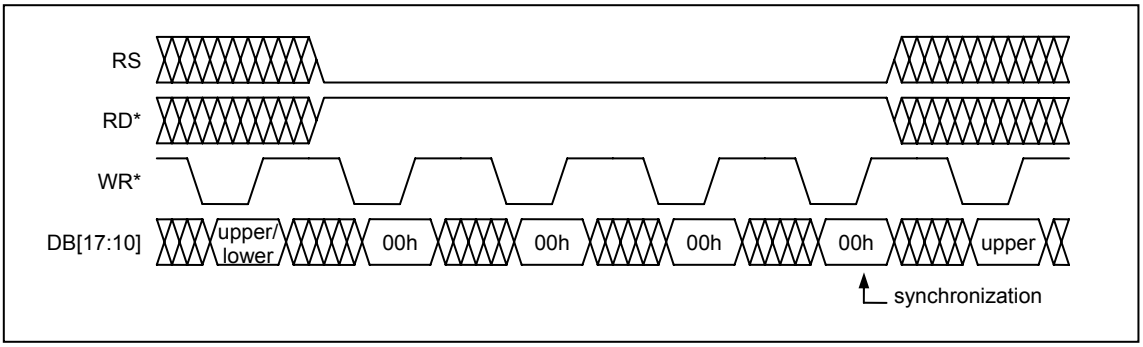


Figure 30: 8-bit data transfer synchronization

Serial Peripheral Interface (SPI)

The Serial Peripheral Interface (SPI) is selected by setting the IM[3:1] pins to “010”. The SPI is available via the chip select line (CS*), the serial transfer clock line (SCL), the serial data input (SDI), and the serial data output (SDO). In SPI mode, the IM0/ID pin functions as the ID pin and the DB[17:0] pins, which are not used, must be fixed at either IOVcc or GND level.

The LGDP4524 recognizes the start of data transfer on the falling edge of CS* input and transfers the start byte. It recognizes the end of data transfer on the rising edge of CS* input. The LGDP4524 is selected when the 6-bit chip address in the start byte transferred from the transmission unit and the 6-bit device identification code assigned to the LGDP4524 correspond as a result of comparison. When selected, the LGDP4524 starts taking subsequent data. The ID pin sets the least significant bit of the identification code. Send “01110” to the identification code, which is the five upper bits of the start byte. Two different chip addresses must be assigned to the LGDP4524 because the seventh bit of the start byte is assigned to the register select bit (RS). When RS = “0”, either index register write operation or status read operation is executed. When RS = “1”, either instruction write operation or RAM read/write operation is executed. The eighth bit of the start byte is to select either read or write operation (R/W bit). Data are received when the R/W bit is “0”, and are transferred when the R/W bit is “1”.

After receiving the start byte, the LGDP4524 starts transferring or receiving data in units of bytes. Data transfer is executed from the MSB. All instructions of the LGDP4524 take a 16-bit format and are executed internally after transferring two bytes (DB[15:0]) from the MSB. GRAM write data are internally expanded into 18 bits. After receiving the start byte, the LGDP4524 takes the first and the second byte as the upper and the lower eight bits of a 16-bit instruction, respectively.

In SPI mode, invalid data are sent to the data bus until 4-byte data are read out from the internal GRAM after the start byte. Valid data are read out as the LGDP4524 reads out the 5th byte data from the internal GRAM.

Table 52: Start byte format

Transferred bits	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**
Start byte format	Device ID code						RS	R/W
	0	1	1	1	0	ID		

Note: ID bit is selected by setting the IM0/ID pin.

Table 53

RS	**R/W**	**Function**
0	0	Set an index register
0	1	Read a status
1	0	Write an instruction or RAM data
1	1	Read an instruction or RAM data

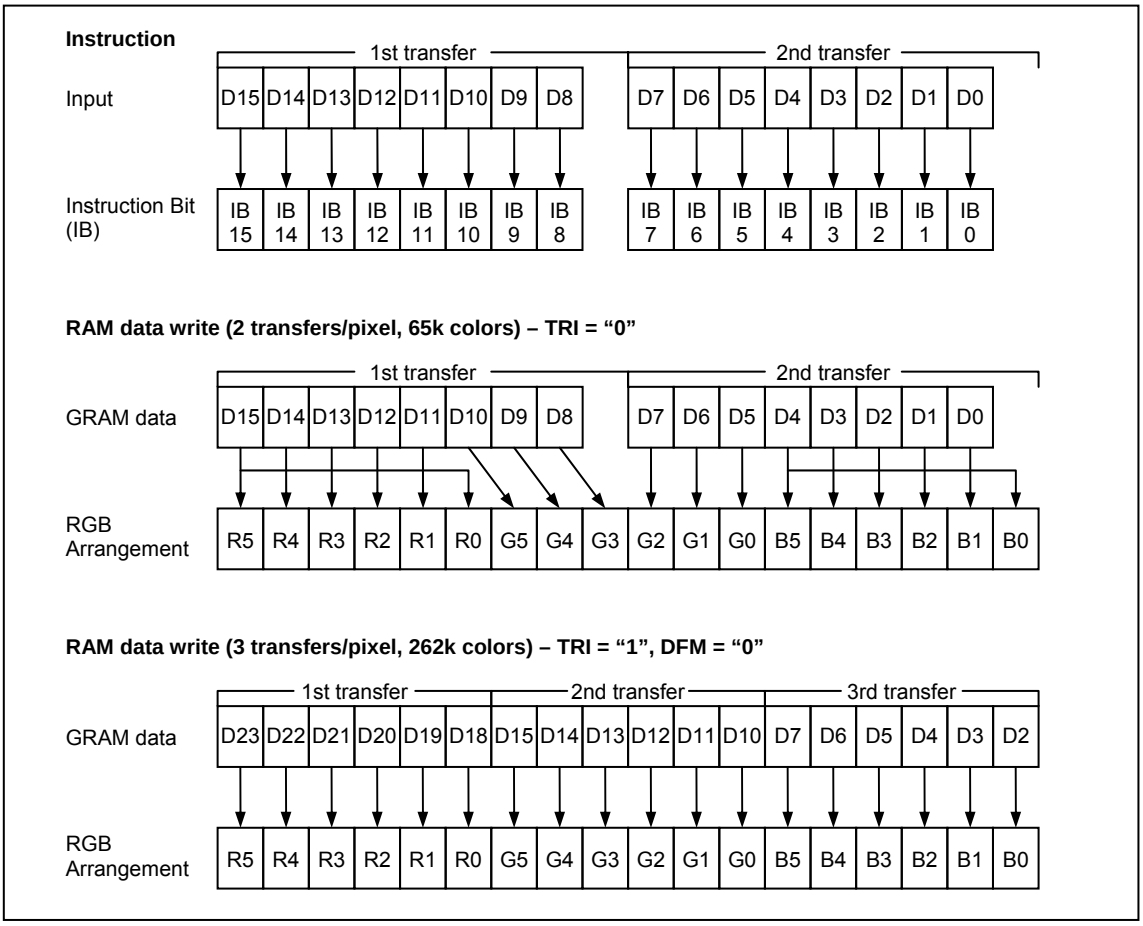


Figure 31: Data format for SPI

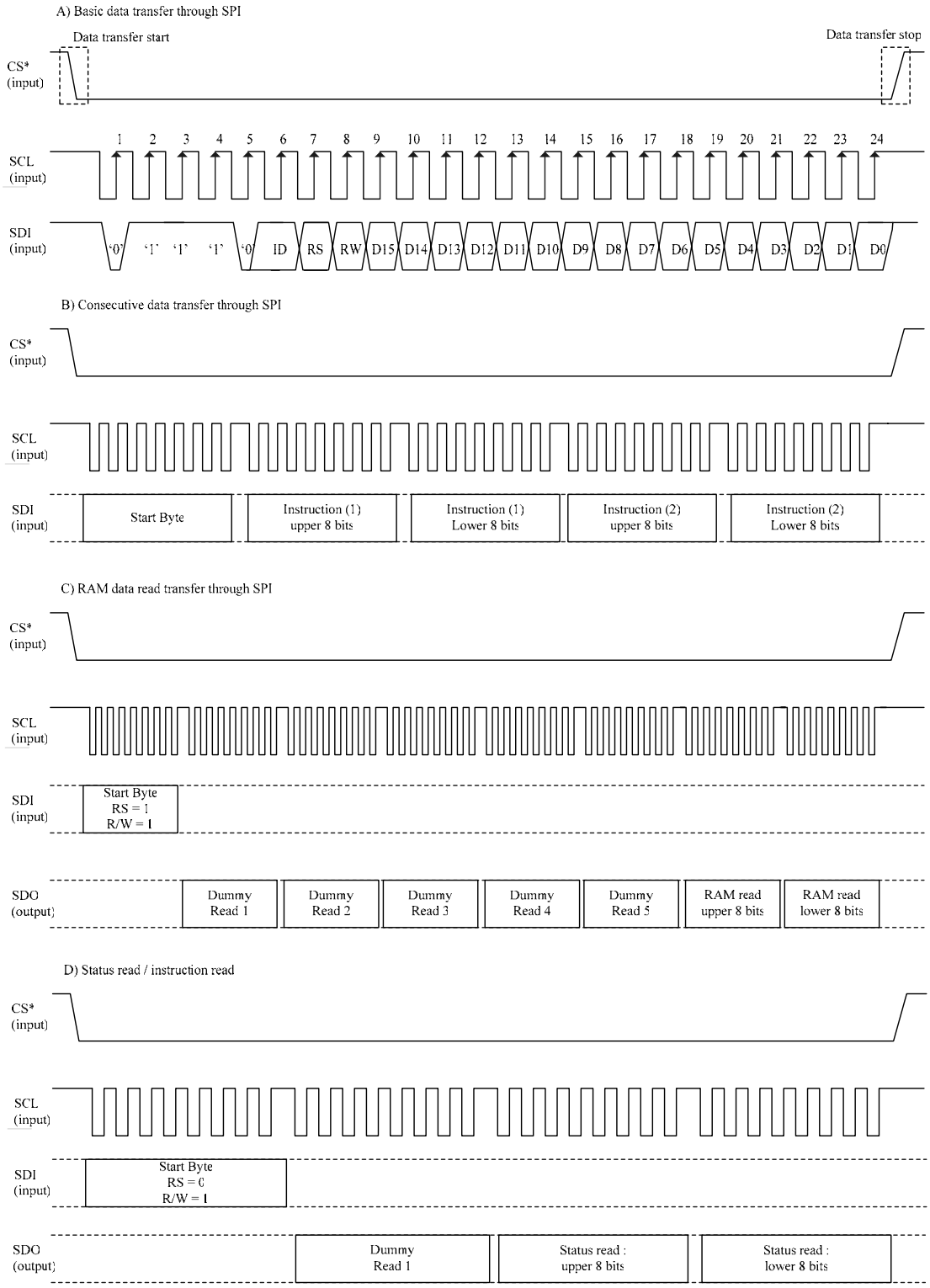


Figure 32: Data Transfer in Serial interface

VSYNC Interface

The LGDP4524 has the VSYNC interface, which enables moving picture display with the system interface in synchronization with the frame-synchronizing signal (VSYNC). The VSYNC interface enables the system interface to display a moving picture with minimum modification.

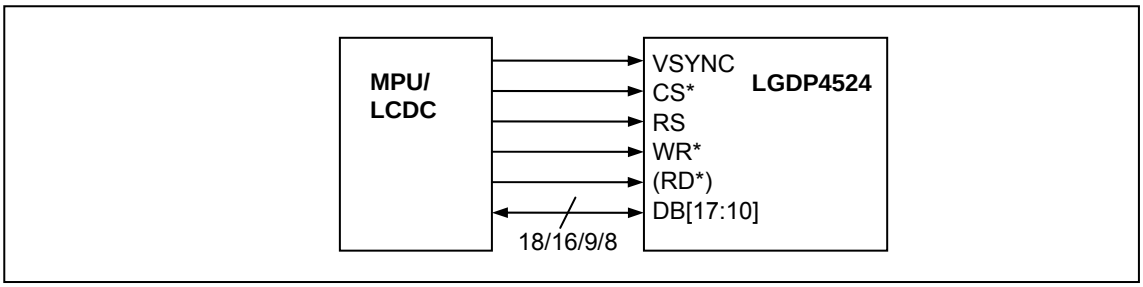


Figure 33: VSYNC interface

The VSYNC interface is selected by setting DM1-0 = “10” and RM = “0”. In VSYNC interface mode, the internal display operation is synchronized with the VSYNC signal. By writing data to the internal RAM via the system interface at a speed faster to a certain degree than that of internal display operation, the VSYNC interface enables moving picture display with the system interface and screen rewriting operation without flicker.

The display operation in VSYNC mode is executed in synchronization with the internal clock generated from internal oscillators and VSYNC input. All display data are stored in the internal RAM to limit the data to be transferred to those overwritten on the moving picture RAM area and minimize total data transfer required for moving picture display.

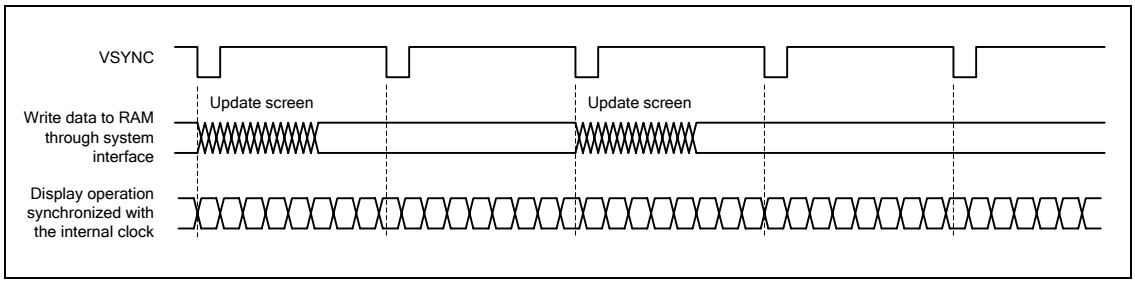


Figure 34: Moving picture data transfer via VSYNC interface

The VSYNC interface has the minimum speed of writing data to the internal RAM via the system interface and the minimum internal clock frequency, which are calculated from the following formulae.

Internal clock frequency (fclk)

$$= FrameFrequency \times (DisplayLines\ (NL) + FrontPorch\ (FP) + BackPorch\ (BP)) \times 44\ clocks \times variance$$

$$RAMWriteSpeed > \frac{176 \times DisplayLines\ (NL)}{(BackPorch\ (BP) + DisplayLines\ (NL) - margins) \times 44\ clocks \times \frac{1}{fclk}}$$

Note: When the RAM write operation does not start on the falling edge of VSYNC, the time from the falling edge of VSYNC until the start of RAM write operation must also be taken into account.

An example of minimum RAM writing speed and internal clock frequency in VSYNC interface mode is as follows.

[Example]	
Display size	176 RGB × 220 lines
Lines	220 lines (NL = 11001)

Back/front porch	14/2 lines (BP = 1110/FP = 0010)
Frame frequency	60 Hz

Internal clock frequency (fclk)
= 60 Hz × (220 + 2 + 14) lines × 44 Clocks × 1.1 / 0.9 = 760 kHz

When setting the internal clock frequency, possible causes of variances must also be taken into consideration. In this example, the calculated internal clock frequency with the above register setting allows for a margin of ±10% for variances and ensures to complete the display operation within one VSYNC cycle.

In this example, variances attributed to the fabrication process of LSI and room temperature are counted in. Other possible causes of variances, such as differences in external resistors or voltage changes are not in consideration. It is necessary to allow for an enough margin if these factors must be incorporated.

Minimum speed for RAM writing
> 176 × 220 / {((14 + 220 - 2) lines × 44 clock) / 760 kHz} = 2.88 MHz

The above theoretical value is calculated on the premise that the LGDP4524 starts writing data to the internal RAM on the falling edge of VSYNC. There must at least be a margin of 2 lines between the physical display line where display operation is performed and the RAM line address where data write operation is performed.

The RAM write speed of 2.88MHz or more on the falling edge of VSYNC will guarantee the completion of RAM write operation before the LGDP4524 starts displaying the RAM data on the screen, enabling rewriting the entire screen without flicker.

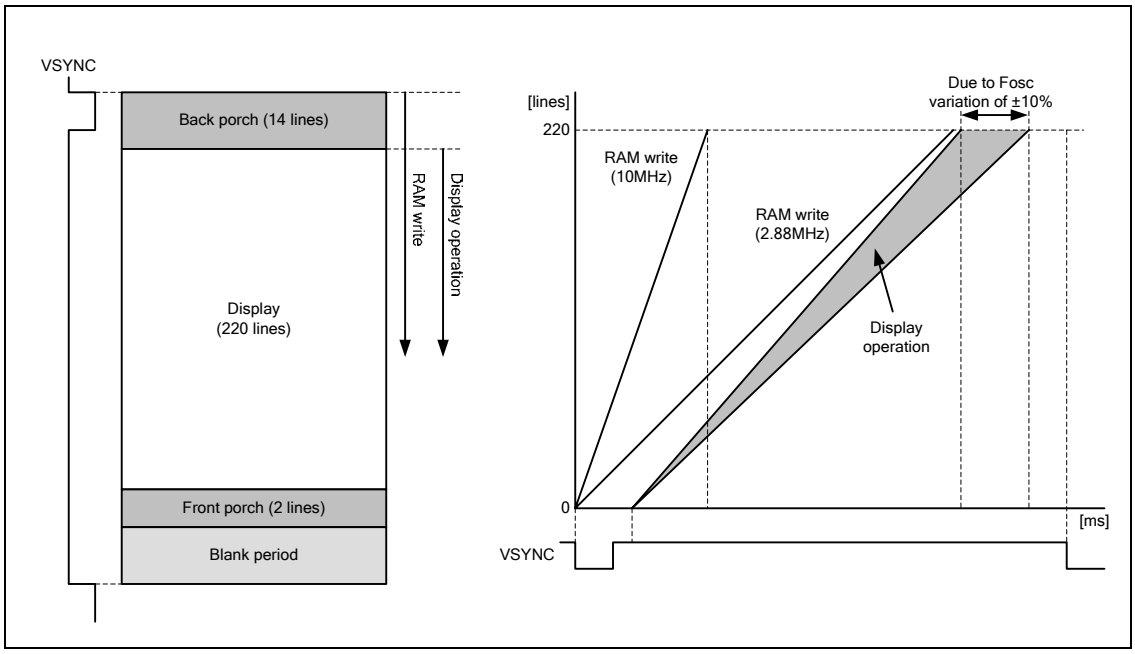


Figure 35: Write/display operation timing via VSYNC interface

Notes in Using the VSYNC Interface

1. The above example of calculation gives a theoretical value. In the actual setting, other possible causes of variances not counted in the above example such as differences in internal oscillators should also be taken into consideration. It is strongly recommended to allow for an enough margin in setting a RAM writing speed.

2. The above example of calculation gives a minimum value in case of rewriting the entire screen. If the moving picture display area is smaller than that, the range for setting a minimum RAM writing speed can have extra margins.
3. After drawing 1 frame, a front porch period continues until the next input of VSYNC is detected.
4. When switching from the internal clock operation mode (DM[1:0] = “00”) to the VSYNC interface mode, or the other way around, it is enabled from the next VSYNC cycle, i.e. after completing the display of the frame, which the LGDP4524 was internally processing when switching the modes.
5. The partial display, vertical scroll, and interlaced scan functions are not available in VSYNC interface mode.
6. In VSYNC interface mode, set the AM bit to “0” to transfer display data in the method mentioned above.

External Display Interface

The following are the external display interface (RGB interface) available with the LGDP4524. The interface is selected by setting the RIM1-0 bits as follows. The RGB interface is used to access RAM.

Table 54

RIM[1:0]	RGB interface	DB pins
00	18-bit RGB interface	DB[17:0]
01	16-bit RGB interface	DB[17:10], DB[8:1]
10	6-bit RGB interface	DB[17:12]
11	Setting disabled	

Note: Multiple RGB interfaces cannot be used simultaneously.

RGB Interface

The display operation via the RGB interface is synchronized with VSYNC, HSYNC, and DOTCLK. The RGB interface enables transferring minimum necessary data and rewriting the RAM area need to be overwritten with use of window address function. In RGB interface mode, it is necessary to set back and front porch periods before and after a display period, respectively.

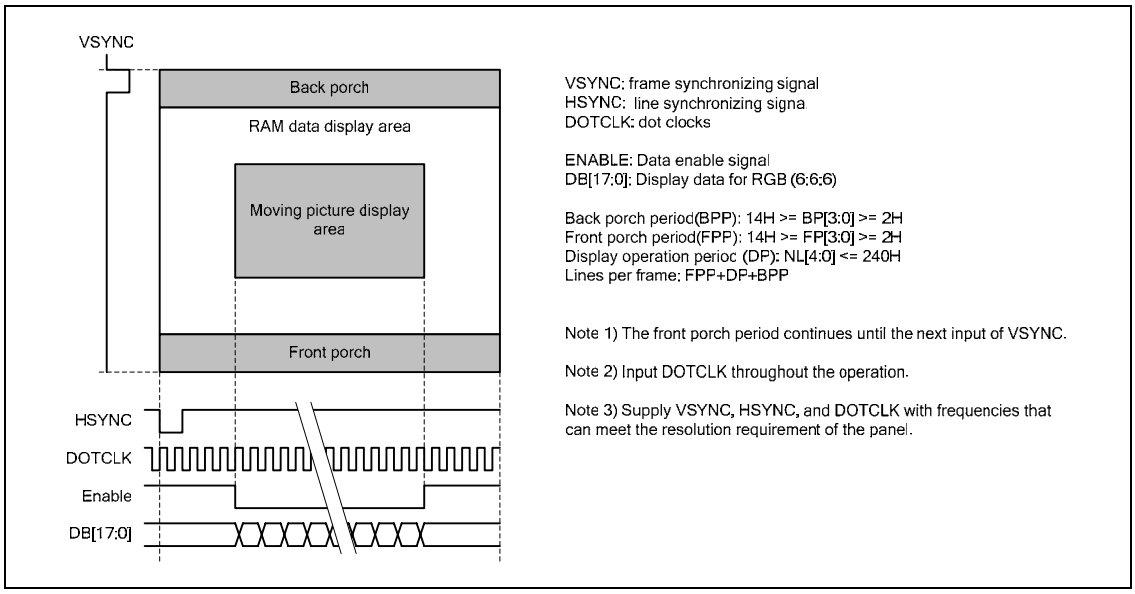


Figure 36: RGB interface

ENABLE Signal

The combinations of EPL and ENABLE bits and the functions are as follows. Note that it is necessary to set both EPL and ENABLE bits to automatically update RAM address in the AC when writing data to the internal RAM. The EPL bit inverts the polarity of ENABLE signal.

Table 55

EPL	ENABLE	RAM write	RAM address
0	0	Enabled	Updated
0	1	Disabled	Retained
1	0	Disabled	Retained
1	1	Enabled	Updated

RGB Interface Timing

The timing chart of signals in 16/18-bit RGB interface mode is as follows.

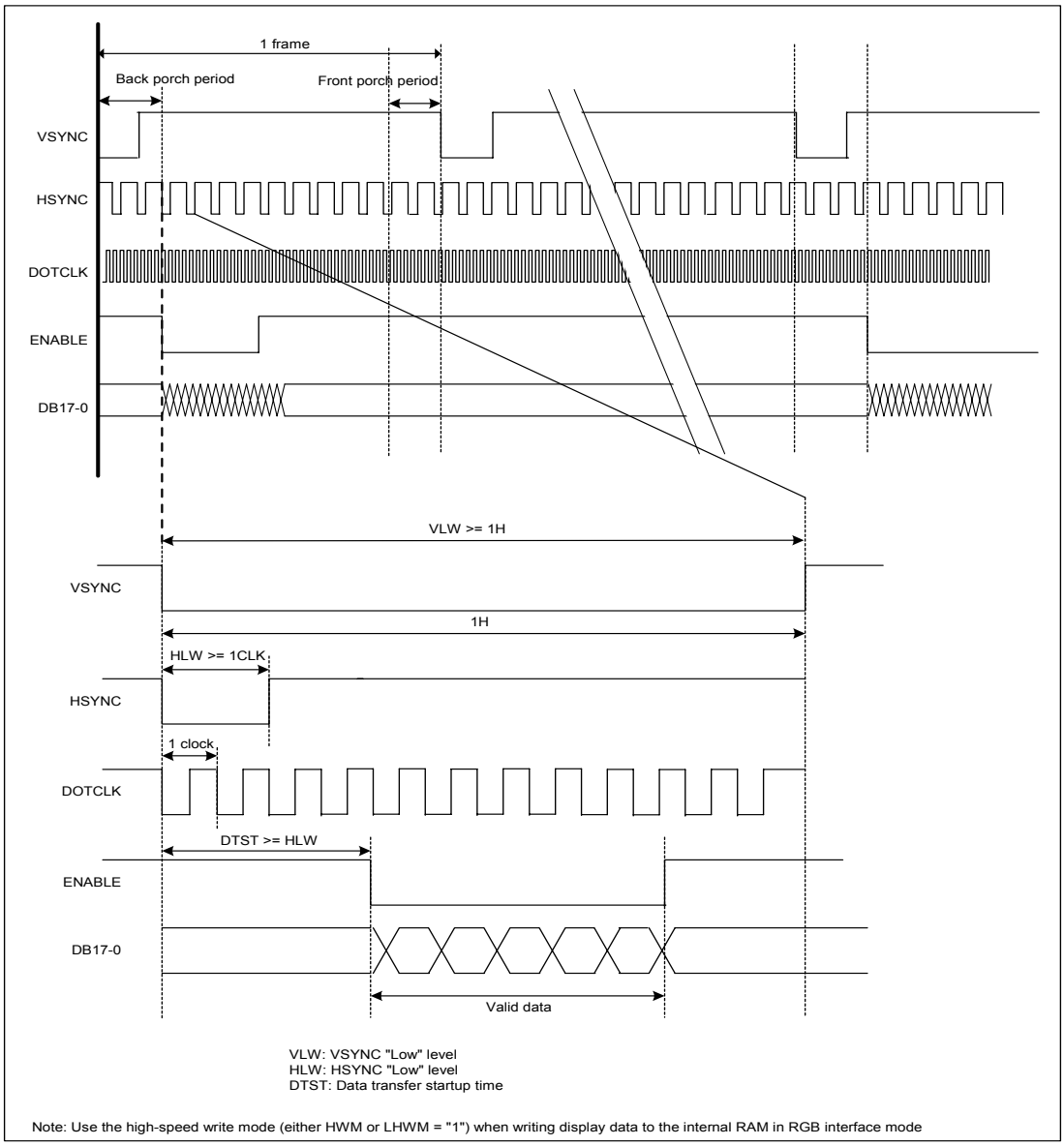


Figure 37: 16-/18-bit RGB Interface Timing

The timing chart of signals in 6-bit RGB interface mode is as follows.

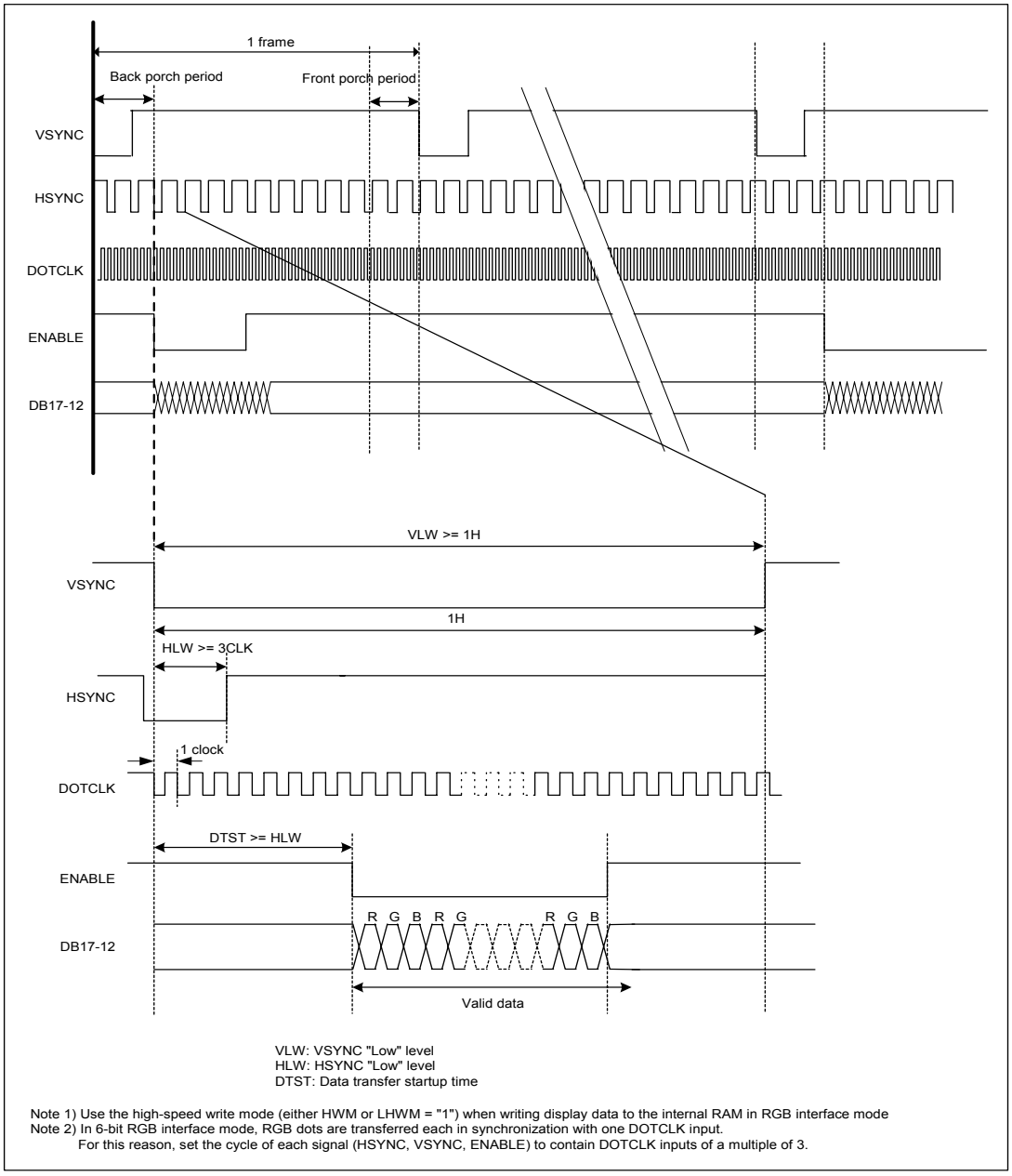


Figure 38: 6-bit RGB Interface Timing

Moving Picture Display

The LGDP4524 has the RGB interface for moving picture display and incorporates RAM for storing moving picture data, which has following merits in displaying a moving picture.

- The window address function enables transferring minimum necessary data to be written on the moving picture RAM area.
- Data are transferred only to the moving picture RAM area.
- The reduction in data transfer contributes to the reduction in power consumption by the entire system.
- Allowing the use of system interface to rewrite data, such as icons, in still picture RAM area while displaying a moving picture.

RAM Access via a System Interface in RGB-I/F Mode

The LGDP4524 allows RAM access via the system interface in RGB interface mode. In RGB interface mode, data are written to the internal RAM in synchronization with DOTCLK while ENABLE is “Low”. When writing data to the internal RAM via the system interface, set ENABLE high” to stop writing data via the RGB interface. Then set RM = “0” to make RAM accessible via the system interface. When restarting RAM access in RGB interface mode, wait a time for one read/write bus cycle. Then, set RM = “1” and the index register to R22h to start accessing RAM via the RGB interface. If RAM accesses via two interfaces conflicts, there is no guarantee that data are written to the internal RAM.

The following figure illustrates the operation of the LGDP4524 when displaying a moving picture via the RGB interface and rewriting data in the still picture RAM area via the system interface.

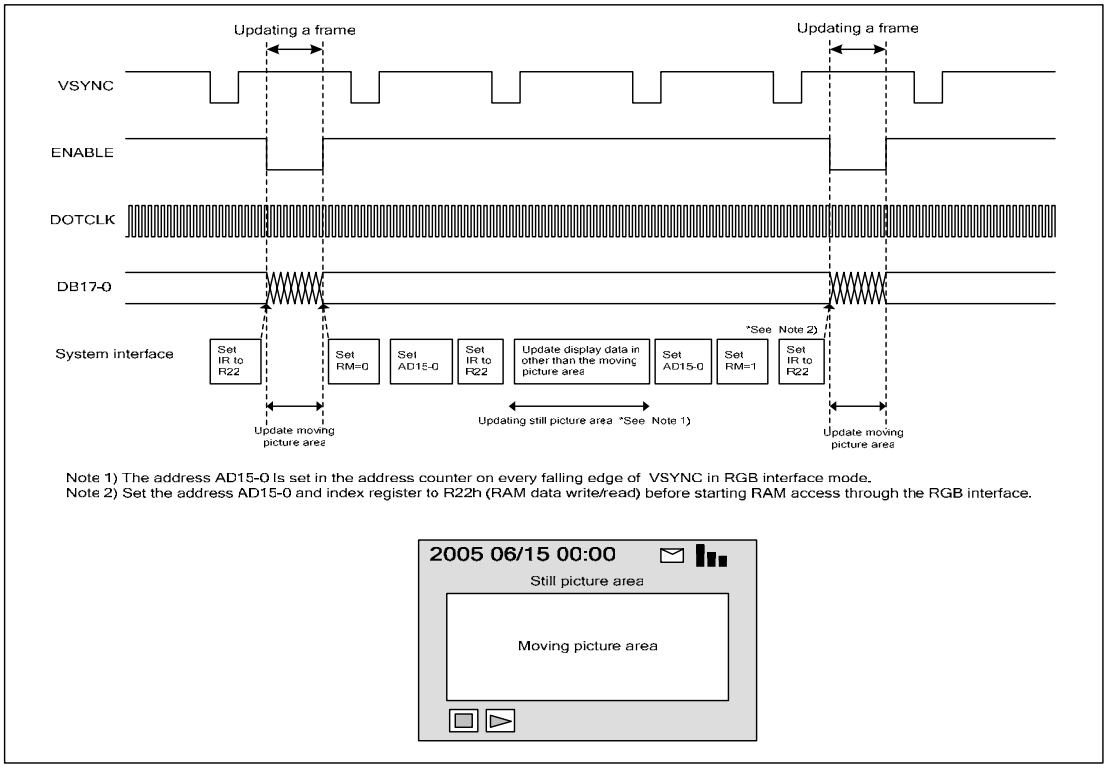


Figure 39 RAM Access via a system interface and RGB interface

6-Bit RGB Interface

The 6-bit RGB interface is selected by setting the RIM[1:0] bits to “10”. The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. Display data are transferred to the internal RAM in synchronization with the display operation via 6-bit RGB data bus (DB[17:12]) according to the data enable signal (ENABLE). Unused pins (DB[11:0]) must be fixed at either IOVcc or GND level.

Instructions are set only via the system interface.

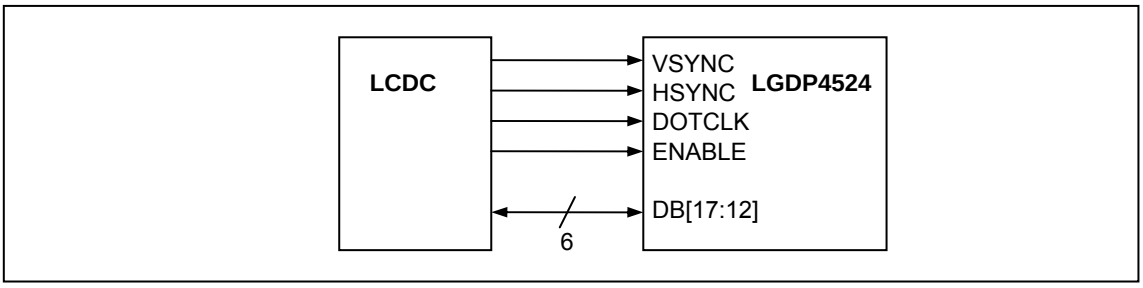


Figure 40: 6-bit RGB interface

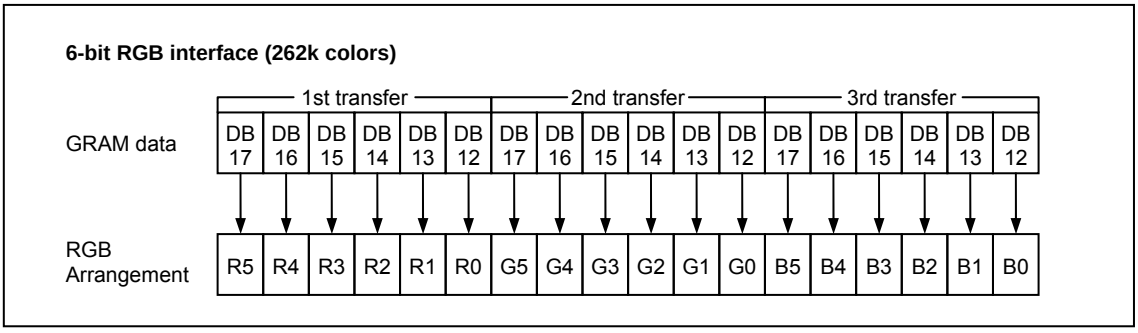


Figure 41: Data format for 6-bit interface

Data Transfer Synchronization in 6-Bit RGB Interface Mode

The LGDP4524 has data transfer counters for counting the first, second, third data transfers in 6-bit RGB interface mode. The transfer counters are always reset to the state of first data transfer on the falling edge of VSYNC. If a mismatch arises in the number of each data transfer, the counters are reset to the state of first data transfer at the start of the frame (i.e. on the falling edge of VSYNC) to restart data transfer in the correct order from the next frame. This function is expedient for moving picture display, which requires consecutive data transfer in light of minimizing effects from failed data transfer and enabling the system to return to a normal state.

Note that internal display operation is performed in units of pixels (RGB: taking 3 inputs of DOTCLK). Accordingly, the number of DOTCLK inputs in one frame period must be a multiple of 3 to complete data transfer correctly. Otherwise it will affect the display of that frame as well as the next frame.

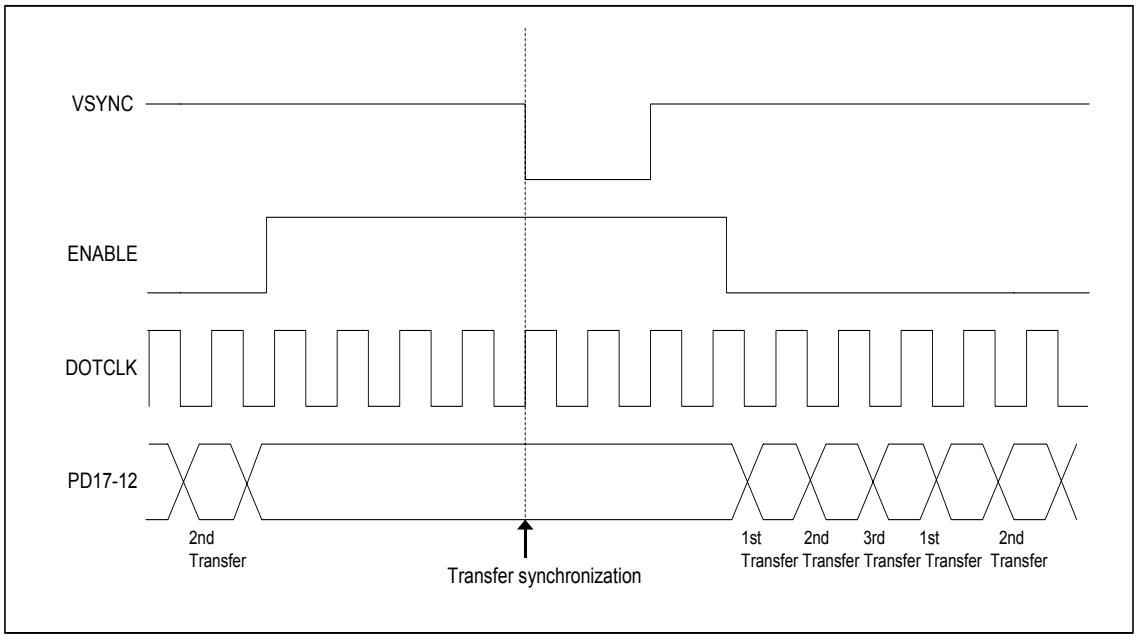


Figure 42: 6-bit data transmission synchronization

16-Bit RGB Interface

The 16-bit RGB interface is selected by setting the RIM1-0 bits to “01”. The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. Display data are transferred to the internal RAM in synchronization with the display operation via 16-bit RGB data bus (DB17-10, DB8-1) according to the data enable signal (ENABLE).

Instructions are set only via the system interface.

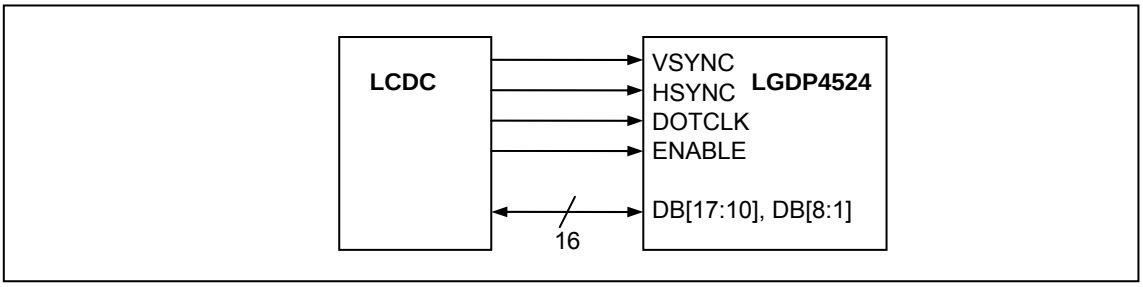


Figure 43: 16-bit RGB interface

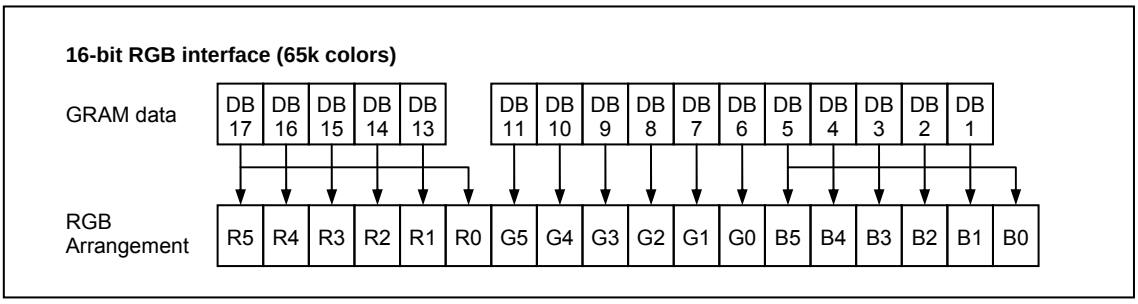


Figure 44: Data format for 16-bit interface

18-Bit RGB Interface

The 18-bit RGB interface is selected by setting the RIM1-0 bits to “00”. The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. Display data are transferred to the internal RAM in synchronization with the display operation via 18-bit RGB data bus (DB[17:0]) according to the data enable signal (ENABLE).

Instructions are set only via the system interface.

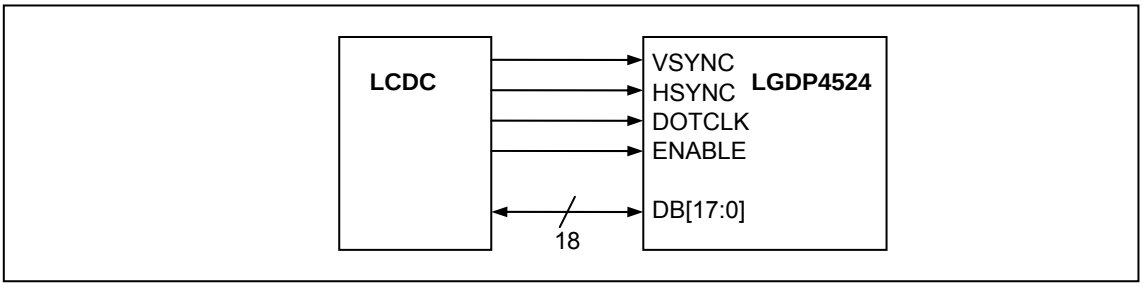


Figure 45: 18-bit RGB interface

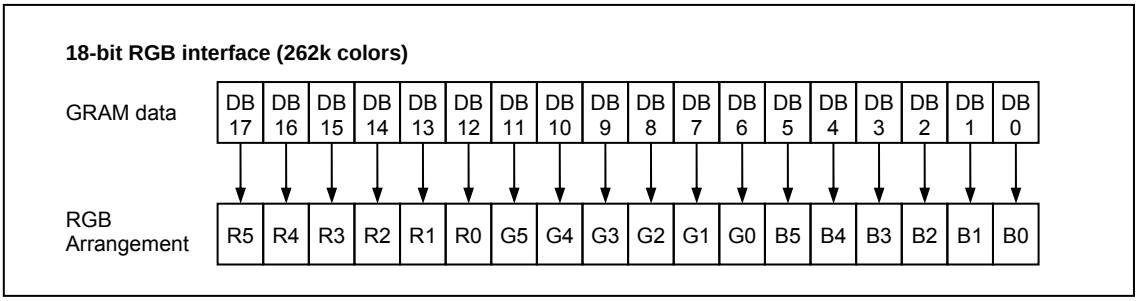


Figure 46: Data format for 18-bit interface

Notes in Using the External Display Interface

1. The following are the functions not available in external display interface mode.

Table 56

Function	External display interface	Internal display operation
Partial display	Not available	Available
Scroll function	Not available	Available
Interlaced scan	Not available	Available
Graphics operation function	Not available	Available

2. VSYNC, HSYNC, and DOTCLK signals must be supplied throughout a display operation period.
3. The periods set with the NO1-0 bits (gate output non-overlap period), STD1-0 bits (source output delay period) and EQ1-0 bits (equalization period) are not based on the internal clock but based on DOTCLK in RGB interface mode.
4. In 6-bit RGB interface mode, each of RGB dots is transferred in synchronization with a DOTCLK input. In other words, it takes 3 DOTCLK inputs to transfer one pixel. Be sure to complete data transfer in units of 3 DOTCLK inputs in 6-bit RGB interface mode.
5. In 6-bit RGB interface mode, data of one pixel, which consists of RGB dots, are transferred in units of 3 DOTCLK. Accordingly, set the cycle of each signal in 6-bit interface mode (VSYNC, HSYNC ENABLE, DB[17:0]) to contain DOTCLK inputs of a multiple of 3 to complete data transfer in units of pixels.
6. When switching from the internal operation mode to the external display interface mode, or the other way around, follow the sequence below.
7. In RGB interface mode, the front porch period continues until the next VSYNC input is detected after drawing one frame.
8. In RGB interface mode, a RAM address (AD15-0) is set in the address counter every frame on the falling edge of VSYNC.

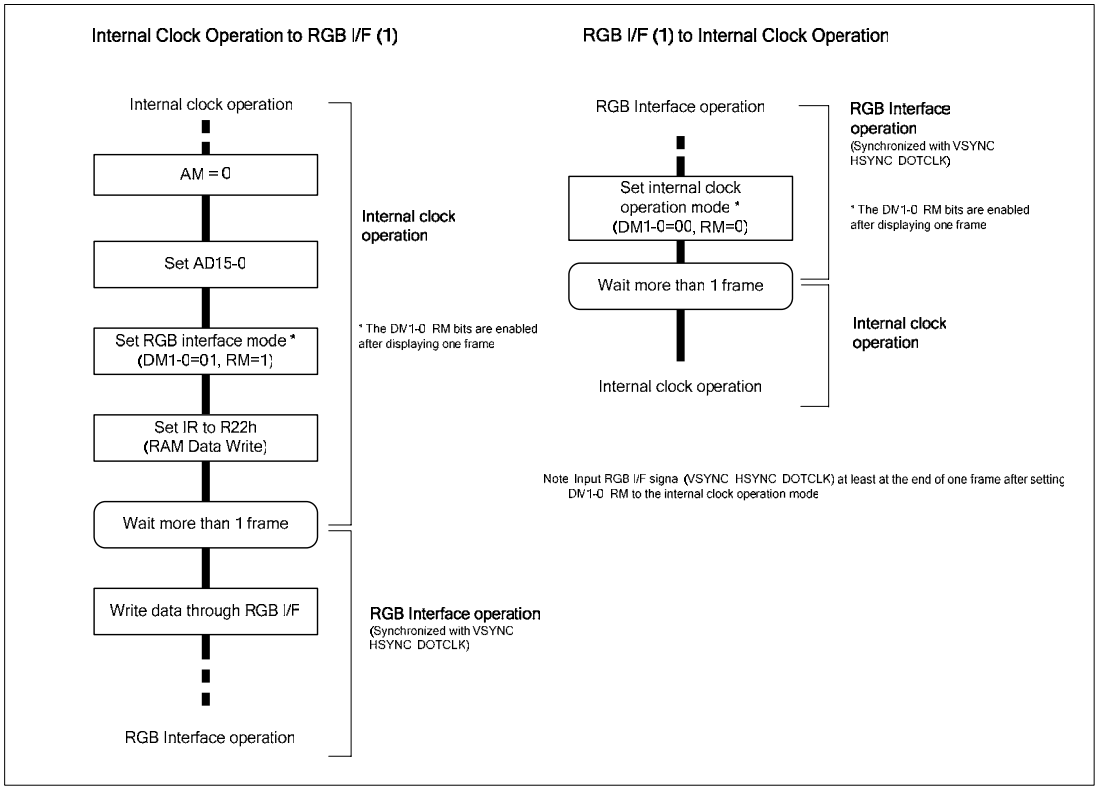


Figure 47: Internal clock operation/RGB interface mode switching sequence

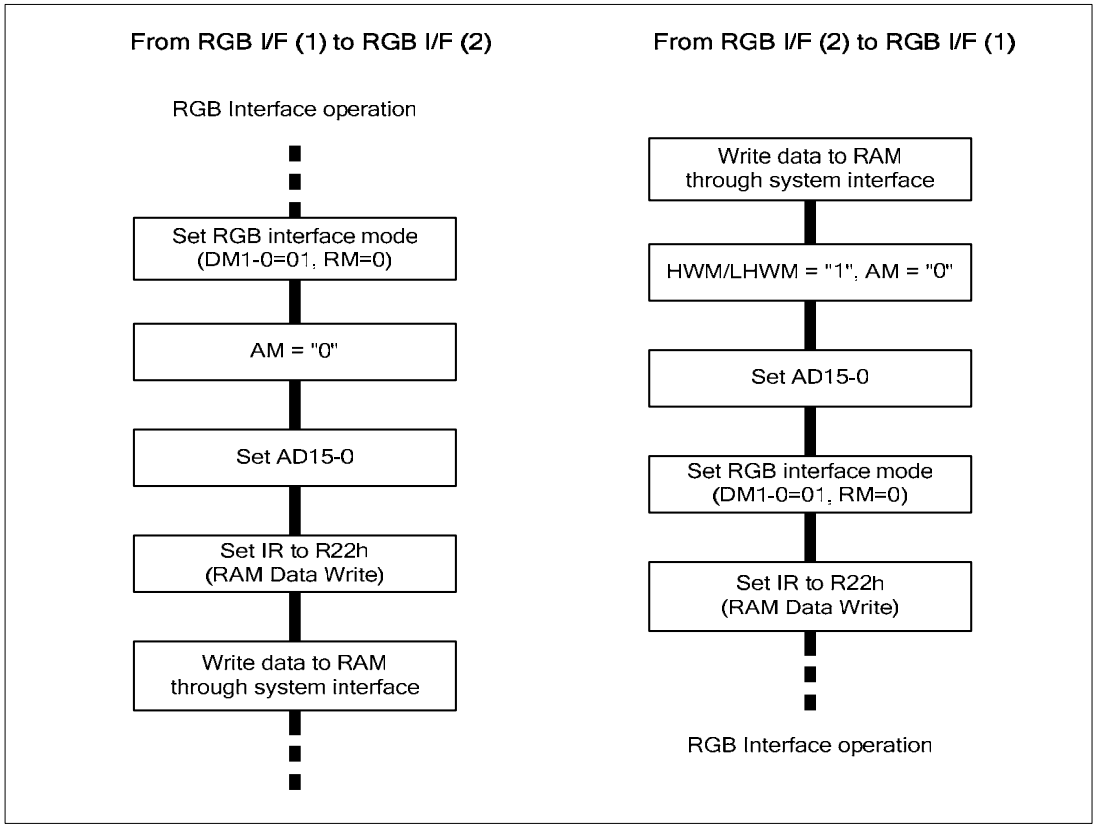


Figure 48: Switching RAM access modes (between system interface and RGB interface modes)

Interfacing Timing with LCD Panel

The following are diagrams of interfacing timing with LCD panel control signals in internal operation and RGB interface modes.

RGB I/F Mode

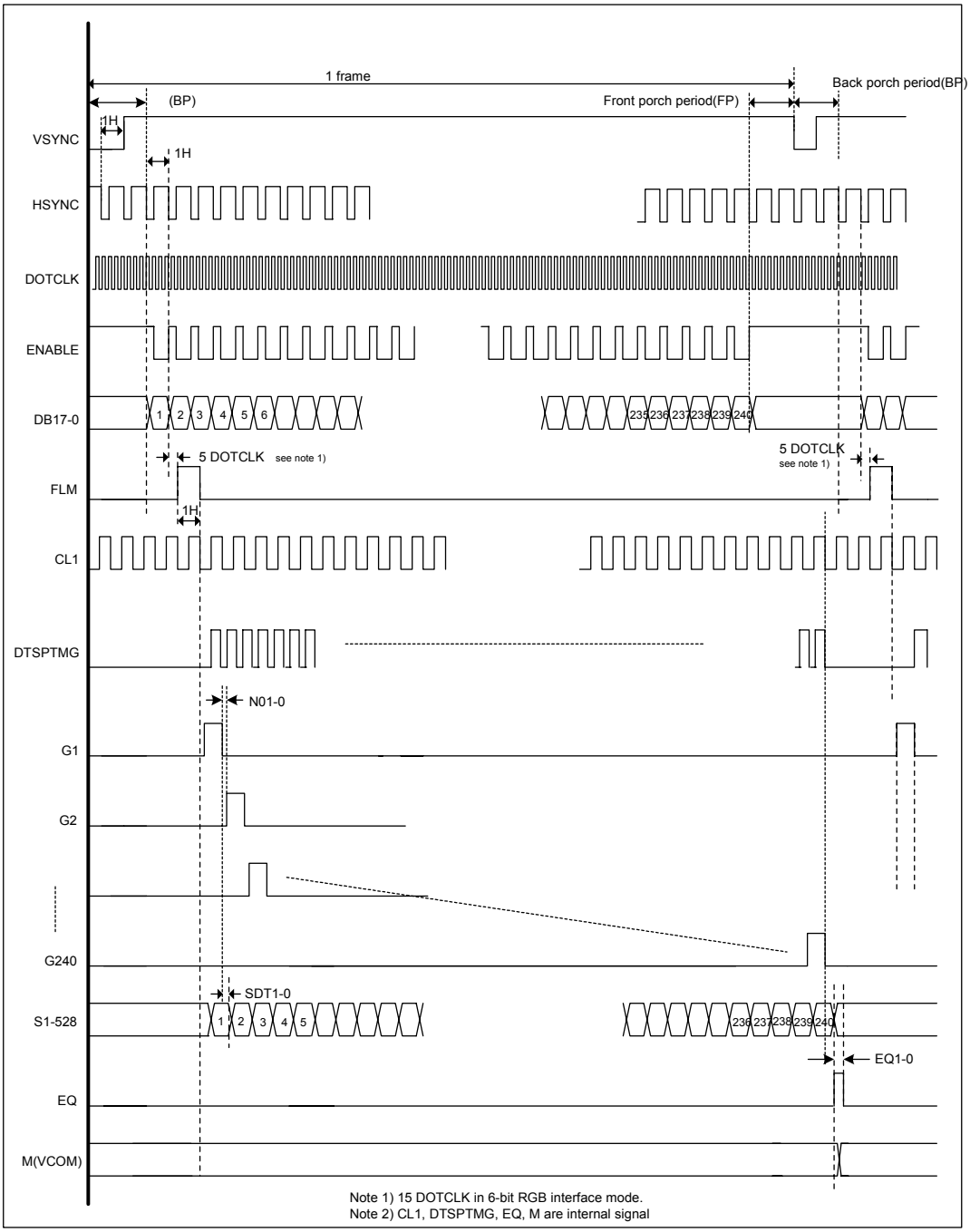


Figure 49 RGB Inteface Timing Diagram

Internal Clock Operation Mode

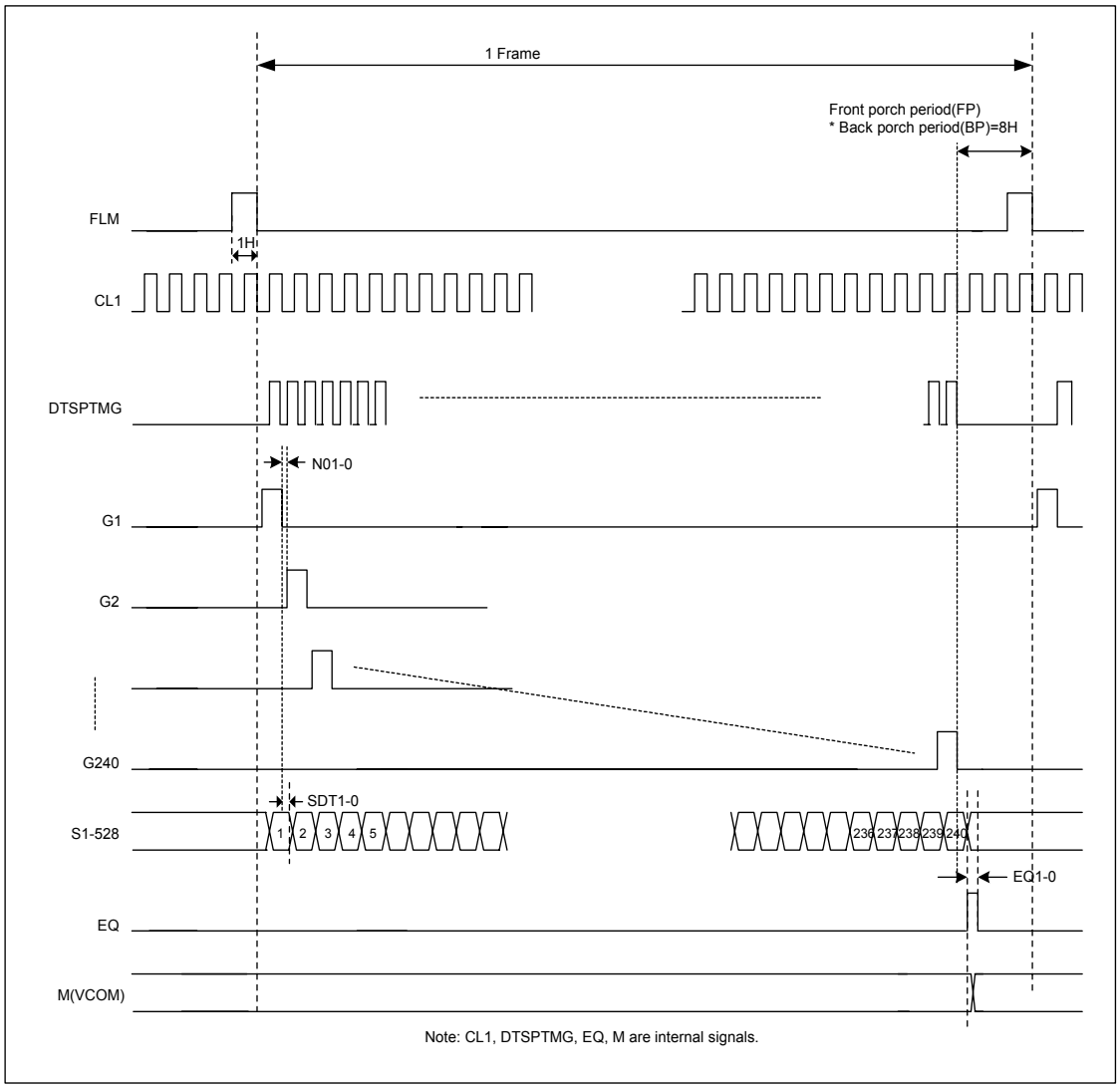


Figure 50 : Internal Clock Operation Timing diagram

Scan Mode Setting

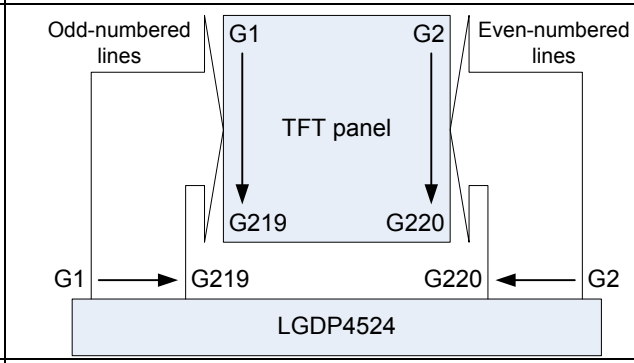
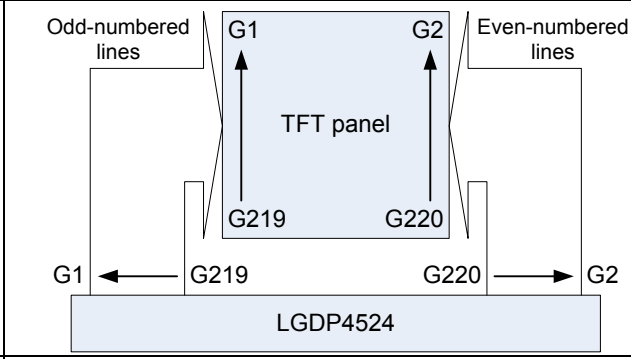
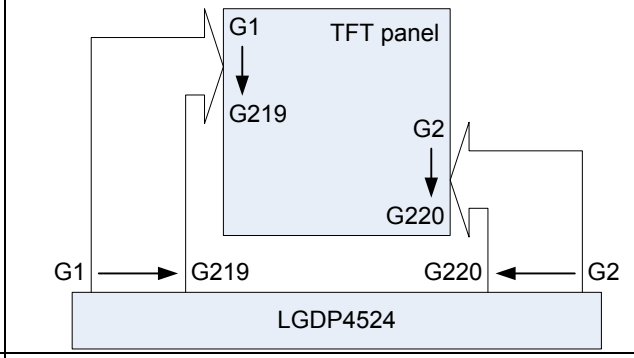
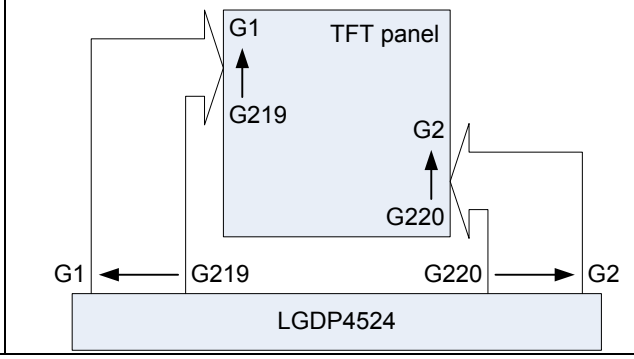
SM	GS	Scan direction	
0	0		G1, G2, G3, G4, …, G218, G219, G220
0	1		G220, G219, G218, …, G4, G3, G2, G1
1	0		G1, G3, G5, …, G217, G219, G2, G4, G6, …, G218, G220
1	1		G220, G218, G216, …, G6, G4, G2, G219, G217, G215, …, G5, G3, G1

Figure 51

γ-Correction Function

The LGDP4524 has the γ-correction function to display in 262,144 colors simultaneously. The γ-correction is performed with 3 groups of registers determining eight reference grayscale levels, which are gradient adjustment, amplitude adjustment and fine-adjustment registers. Each register groups further consists of register groups of positive and negative polarities. Each register group is set independently to other register groups, making the LGDP4524 available with liquid crystal panels of various characteristics.

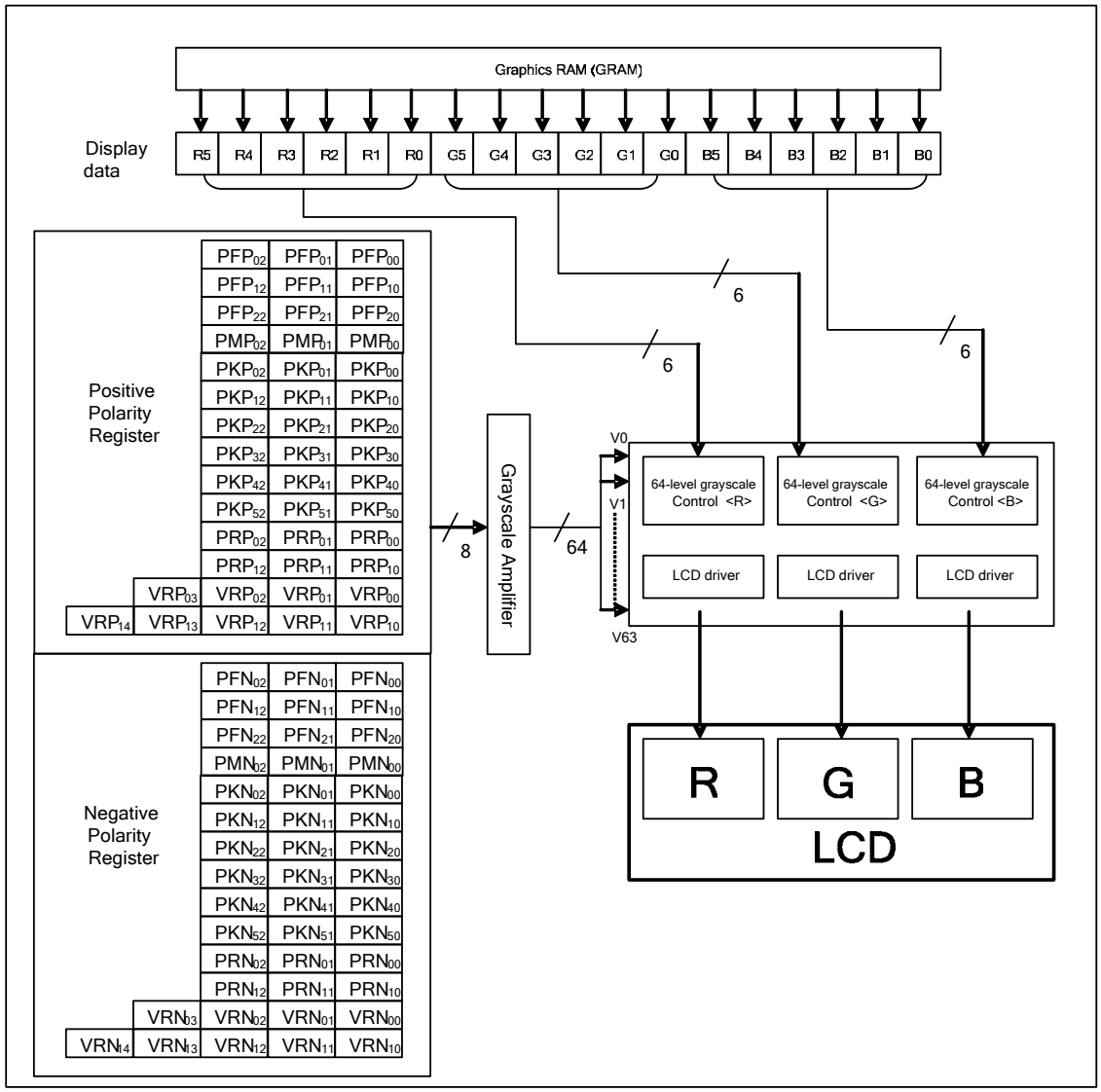


Figure 52

Grayscale Amplifier Unit Configuration

The following figure illustrates the grayscale amplifier unit of the LGDP4524.

To generate 64 grayscale voltages (V0 to V63), the LGDP4524 first generates eight reference grayscale voltages (VINP0-7/VINN0-7). The grayscale amplifier unit then divides eight reference grayscale voltages with the ladder resistors incorporated therein.

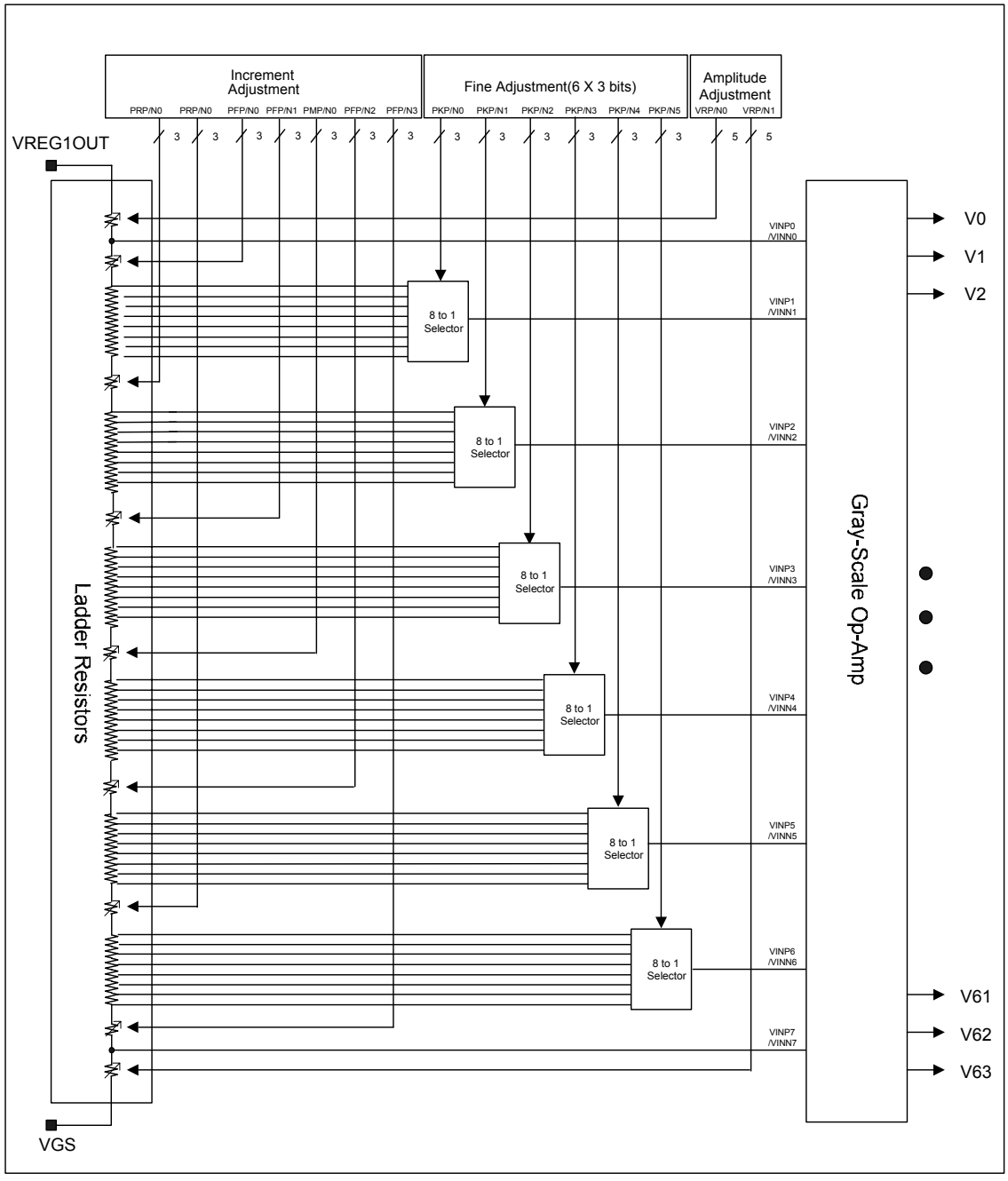


Figure 53: Grayscale amplifier unit

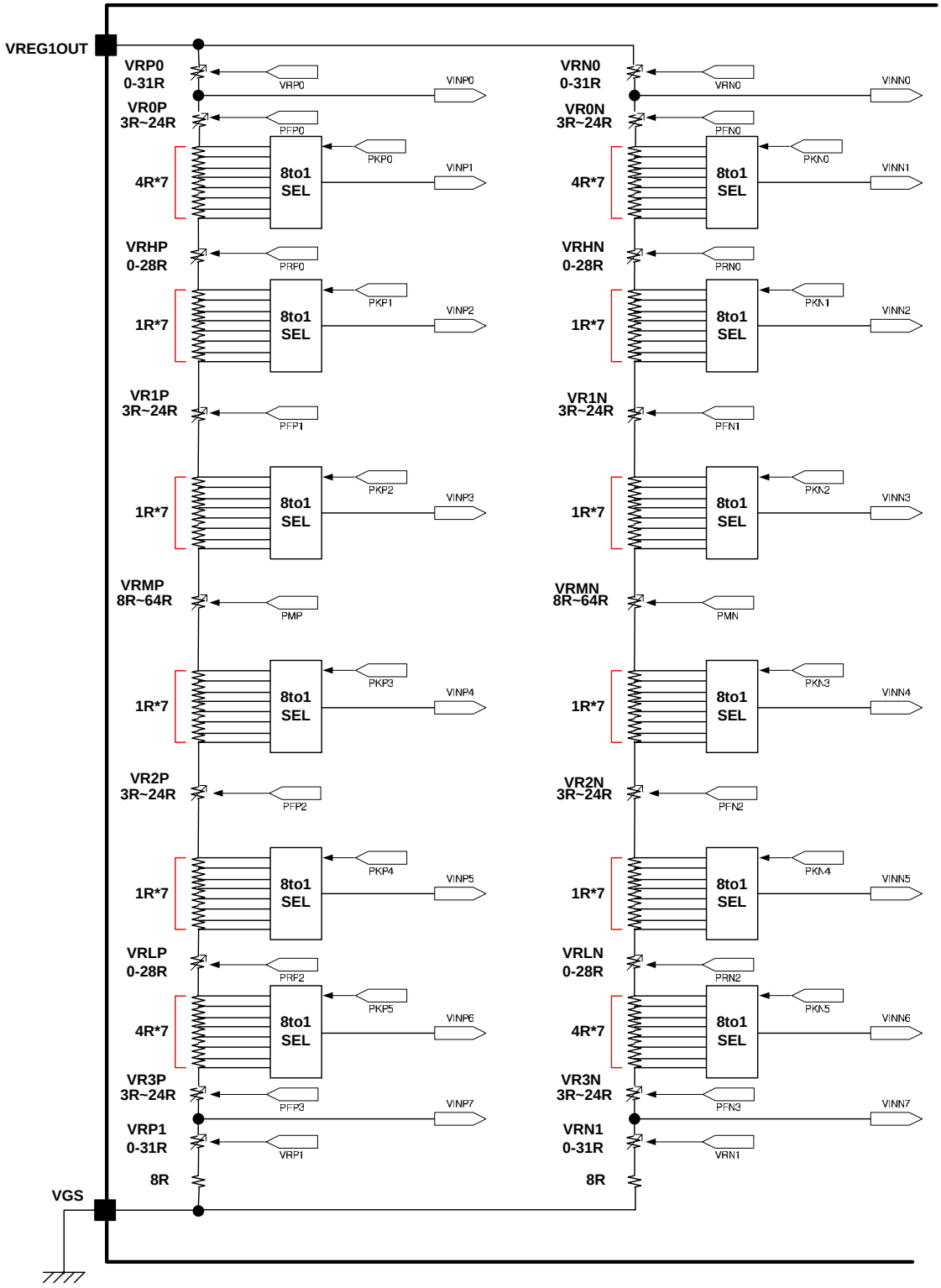


Figure 54: Ladder resistor units and 8-to-1 selectors

γ-Correction Register

The γ-correction registers of the LGDP4524 consist of gradient adjustment, amplitude adjustment, and fine adjustment registers, each of which has registers of positive and negative polarities. Each different register group can be set independently to others, enabling adjustment of grayscale voltage levels in relation to grayscales set optimally for γ-characteristics of a liquid crystal panel. These γ-correction register settings and the reference levels of the 64 grayscales to which the three kinds of adjustments are made (bold lines in the following figure) are common to all RGB dots.

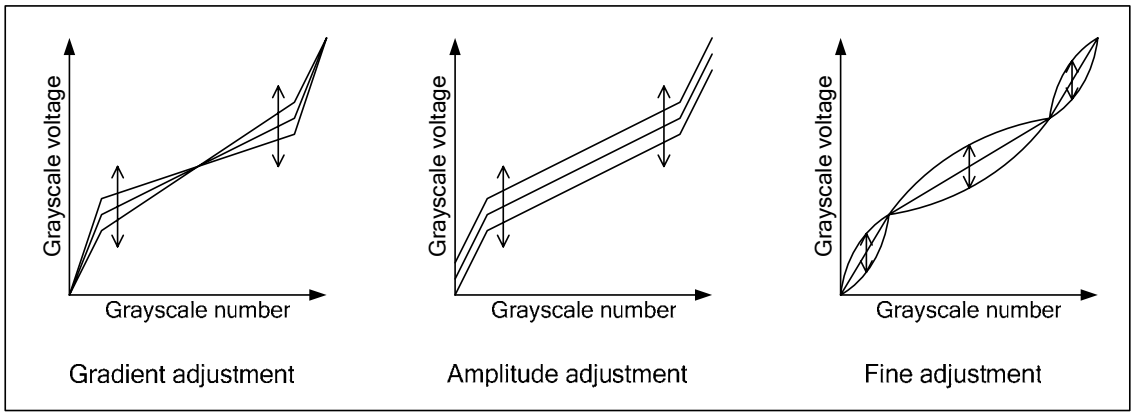


Figure 55

1. Gradient adjustment registers

The gradient adjustment registers are used to adjust the gradient of the curve representing the relationship between the grayscale and the grayscale voltage level around middle grayscales without changing the dynamic range. To adjust the gradient, the resistance values of grayscale reference voltage generating variable resistors (VRHP(N)/VRLP(N)) in the middle of the ladder resistor unit are adjusted. The registers consist of positive and negative polarity registers, allowing asymmetric drive.

2. Amplitude adjustment registers

The amplitude adjustment registers are used to adjust the amplitude of grayscale voltages. To adjust the amplitude, the resistance values of the grayscale voltage generating variable resistors (VRP(N)1/0) at the top and bottom of the ladder resistor unit are adjusted. Same with the gradient registers, the amplitude adjustment registers consist of positive and negative polarity registers.

3. Fine adjustment registers

The fine adjustment registers are used to fine-adjust grayscale voltage levels. To fine-adjust grayscale voltage levels, fine adjustment registers adjust the reference voltage levels, 8 levels for each register generated from the ladder resistor unit, in respective 8-to-1 selectors. Same with other registers, the fine adjustment registers consist of positive and negative polarity registers.

Table 57

Register Groups	Positive Polarity	Negative Polarity	Description
Gradient adjustment	PRP0[2:0]	PRN0[2:0]	Variable resistor VRHP(N)
	PRP1[2:0]	PRN1[2:0]	Variable resistor VRHP(N)
	PFP0[2:0]	PFN0[2:0]	Variable resistor VR0P(N)
	PFP1[2:0]	PFN1[2:0]	Variable resistor VR1P(N)
	PFP2[2:0]	PFN2[2:0]	Variable resistor VR2P(N)
	PFP3[2:0]	PFN3[2:0]	Variable resistor VR3P(N)
	PMP[2:0]	PMN[2:0]	Variable resistor VRMP(N)
Amplitude adjustment	VRP0[3:0]	VRN0[3:0]	Variable resistor VRP(N)0
	VRP1[4:0]	VRN1[4:0]	Variable resistor VRP(N)1
Fine adjustment	PKP0[2:0]	PKN0[2:0]	8-to-1 selector (voltage level of grayscale 1)
	PKP1[2:0]	PKN1[2:0]	8-to-1 selector (voltage level of grayscale 8)
	PKP2[2:0]	PKN2[2:0]	8-to-1 selector (voltage level of grayscale 20)
	PKP3[2:0]	PKN3[2:0]	8-to-1 selector (voltage level of grayscale 43)
	PKP4[2:0]	PKN4[2:0]	8-to-1 selector (voltage level of grayscale 55)
	PKP5[2:0]	PKN5[2:0]	8-to-1 selector (voltage level of grayscale 62)

Ladder Resistors and 8-to-1 Selector

Block Configuration

The reference voltage generating unit as illustrated in page 100 consists of two ladder resistor units including variable resistors and 8-to-1 selectors. Each 8-to-1 selector selects one of the 8 voltage levels generated from the ladder resistor unit to output as a grayscale reference voltage. Both variable resistors and 8-to-1 selectors are controlled according to the γ correction registers. This unit has pins to connect a volume resistor externally to compensate differences in various characteristics of panels.

Variable Resistors

The LGDP4524 uses variable resistors of the following three purposes: gradient adjustment (VRHP(N)/VRLP(N)); amplitude adjustment (1) (VRP(N)0); and the amplitude adjustment (2) (VRP(N)1). The resistance values of these variable resistors are set by gradient adjustment registers and amplitude adjustment registers as follows.

Table 58:

Gradient adjustment(1)

Contents of register PRP(N)0/1[2:0]	Resistance VRHP(N) VRLP(N)
000	0R
001	4R
010	8R
011	12R
100	16R
101	20R
110	24R
111	28R

Gradient adjustment(2)

Contents of register PFP0/1/2/3(N)	Resistance VR0/1P(N) VR2/3P(N)
000	3R
001	6R
010	9R
011	12R
100	15R
101	18R
110	21R
111	24R

Gradient adjustment(3)

Contents of register VRP(N)1[4:0]	Resistance VRMP(N)
000	8R
001	16R
010	24R
011	32R
100	40R
101	48R
110	56R
111	64R

Table 59:

Amplitude adjustment

Contents of register VRP(N)0[4:0]	Resistance VRP(N)0 VRP(N)1
00000	0R
00001	1R
00010	2R
:	:
:	:
11101	29R
11110	30R
11111	31R

8-to-1 Selectors

The 8-to-1 selector selects one of eight voltage levels generated from the ladder resistor unit according to the fine adjustment register, and output the selected voltage level as a reference grayscale voltage (VINP(N)1~ VINP(N 6). The table below shows the setting in the fine adjustment register and the selected voltage levels for respective reference grayscale voltages

Table 60: Fine adjustment registers and selected voltage

PKP(N)[2:0]	Selected Voltage					
	VINP(N)1	**VINP(N)2**	**VINP(N3**	**VINP(N)4**	**VINP(N)5**	**VINP(N)6**
0	KVP(N)1	KVP(N)9	KVP(N)17	KVP(N)25	KVP(N)33	KVP(N)41
1	KVP(N)2	KVP(N)10	KVP(N)18	KVP(N)26	KVP(N)34	KVP(N)42
2	KVP(N)3	KVP(N)11	KVP(N)19	KVP(N)27	KVP(N)35	KVP(N)43
3	KVP(N)4	KVP(N)12	KVP(N)20	KVP(N)28	KVP(N)36	KVP(N)44
4	KVP(N)5	KVP(N)13	KVP(N)21	KVP(N)29	KVP(N)37	KVP(N)45
5	KVP(N)6	KVP(N)14	KVP(N)22	KVP(N)30	KVP(N)38	KVP(N)46
6	KVP(N)7	KVP(N)15	KVP(N)23	KVP(N)31	KVP(N)39	KVP(N)47
7	KVP(N)8	KVP(N)16	KVP(N)24	KVP(N)32	KVP(N)40	KVP(N)48

The grayscale voltage levels for V0~V63 grayscales are calculated from the following formulae.

Table 61: Formulae for calculating voltage (1)

Pin	Formula	Fine adjustment register value	Reference voltage
KVP0	VREG1OUT - ΔV*VRP0/SUMRP	-	VINP0
KVP1	VREG1OUT - ΔV*(VRP0+VR0P+0R)/SUMRP	PKP0= 0	VINP1
KVP2	VREG1OUT - ΔV*(VRP0+VR0P+4R)/SUMRP	PKP0= 1	
KVP3	VREG1OUT - ΔV*(VRP0+VR0P+8R)/SUMRP	PKP0= 2	
KVP4	VREG1OUT - ΔV*(VRP0+VR0P+12R)/SUMRP	PKP0= 3	
KVP5	VREG1OUT - ΔV*(VRP0+VR0P+16R)/SUMRP	PKP0= 4	
KVP6	VREG1OUT - ΔV*(VRP0+VR0P+20R)/SUMRP	PKP0= 5	
KVP7	VREG1OUT - ΔV*(VRP0+VR0P+24R)/SUMRP	PKP0= 6	
KVP8	VREG1OUT - ΔV*(VRP0+VR0P+28R)/SUMRP	PKP0= 7	
KVP9	VREG1OUT - ΔV*(VRP0+VR0P+28R+VRHP)/SUMRP	PKP1= 0	VINP2
KVP10	VREG1OUT - ΔV*(VRP0+VR0P+29R+VRHP)/SUMRP	PKP1= 1	
KVP11	VREG1OUT - ΔV*(VRP0+VR0P+30R+VRHP)/SUMRP	PKP1= 2	
KVP12	VREG1OUT - ΔV*(VRP0+VR0P+31R+VRHP)/SUMRP	PKP1= 3	
KVP13	VREG1OUT - ΔV*(VRP0+VR0P+32R+VRHP)/SUMRP	PKP1= 4	
KVP14	VREG1OUT - ΔV*(VRP0+VR0P+33R+VRHP)/SUMRP	PKP1= 5	
KVP15	VREG1OUT - ΔV*(VRP0+VR0P+34R+VRHP)/SUMRP	PKP1= 6	
KVP16	VREG1OUT - ΔV*(VRP0+VR0P+35R+VRHP)/SUMRP	PKP1= 7	
KVP17	VREG1OUT - ΔV*(VRP0+VR0/1P+35R+VRHP)/SUMRP	PKP2= 0	VINP3
KVP18	VREG1OUT - ΔV*(VRP0+VR0/1P+36R+VRHP)/SUMRP	PKP2= 1	
KVP19	VREG1OUT - ΔV*(VRP0+VR0/1P+37R+VRHP)/SUMRP	PKP2= 2	
KVP20	VREG1OUT - ΔV*(VRP0+VR0/1P+38R+VRHP)/SUMRP	PKP2= 3	
KVP21	VREG1OUT - ΔV*(VRP0+VR0/1P+39R+VRHP)/SUMRP	PKP2= 4	
KVP22	VREG1OUT - ΔV*(VRP0+VR0/1P+40R+VRHP)/SUMRP	PKP2= 5	
KVP23	VREG1OUT - ΔV*(VRP0+VR0/1P+41R+VRHP)/SUMRP	PKP2= 6	
KVP24	VREG1OUT - ΔV*(VRP0+VR0/1P+42R+VRHP)/SUMRP	PKP2= 7	
KVP25	VREG1OUT - ΔV*(VRP0+VR0/1P+42R+VRHP +VRMP)/SUMRP	PKP3= 0	VINP4
KVP26	VREG1OUT - ΔV*(VRP0+VR0/1P+43R+VRHP +VRMP)/SUMRP	PKP3= 1	
KVP27	VREG1OUT - ΔV*(VRP0+VR0/1P+44R+VRHP +VRMP)/SUMRP	PKP3= 2	
KVP28	VREG1OUT - ΔV*(VRP0+VR0/1P+45R+VRHP +VRMP)/SUMRP	PKP3= 3	
KVP29	VREG1OUT - ΔV*(VRP0+VR0/1P+46R+VRHP +VRMP)/SUMRP	PKP3= 4	
KVP30	VREG1OUT - ΔV*(VRP0+VR0/1P+47R+VRHP +VRMP)/SUMRP	PKP3= 5	
KVP31	VREG1OUT - ΔV*(VRP0+VR0/1P+48R+VRHP +VRMP)/SUMRP	PKP3= 6	
KVP32	VREG1OUT - ΔV*(VRP0+VR0/1P+49R+VRHP +VRMP)/SUMRP	PKP3= 7	
KVP33	VREG1OUT - ΔV*(VRP0+VR0/1/2P+49R+VRHP +VRMP)/SUMRP	PKP4= 0	VINP5
KVP34	VREG1OUT - ΔV*(VRP0+VR0/1/2P+50R+VRHP +VRMP)/SUMRP	PKP4= 1	
KVP35	VREG1OUT - ΔV*(VRP0+VR0/1/2P+51R+VRHP +VRMP)/SUMRP	PKP4= 2	
KVP36	VREG1OUT - ΔV*(VRP0+VR0/1/2P+52R+VRHP +VRMP)/SUMRP	PKP4= 3	
KVP37	VREG1OUT - ΔV*(VRP0+VR0/1/2P+53R+VRHP +VRMP)/SUMRP	PKP4= 4	
KVP38	VREG1OUT - ΔV*(VRP0+VR0/1/2P+54+VRHP +VRMP)/SUMRP	PKP4= 5	
KVP39	VREG1OUT - ΔV*(VRP0+VR0/1/2P+55R+VRHP +VRMP)/SUMRP	PKP4= 6	
KVP40	VREG1OUT - ΔV*(VRP0+VR0/1/2P+56R+VRHP +VRMP)/SUMRP	PKP4= 7	
KVP41	VREG1OUT - ΔV*(VRP0+VR0/1/2P+56R+VRHP +VRMP+VRLP)/SUMRP	PKP5= 0	VINP6
KVP42	VREG1OUT - ΔV*(VRP0+VR0/1/2P+60R+VRHP +VRMP+VRLP)/SUMRP	PKP5= 1	
KVP43	VREG1OUT - ΔV*(VRP0+VR0/1/2P+64R+VRHP +VRMP+VRLP)/SUMRP	PKP5= 2	
KVP44	VREG1OUT - ΔV*(VRP0+VR0/1/2P+68R+VRHP +VRMP+VRLP)/SUMRP	PKP5= 3	
KVP45	VREG1OUT - ΔV*(VRP0+VR0/1/2P+72R+VRHP +VRMP+VRLP)/SUMRP	PKP5= 4	
KVP46	VREG1OUT - ΔV*(VRP0+VR0/1/2P+76R+VRHP+VRMP +VRLP)/SUMRP	PKP5= 5	
KVP47	VREG1OUT - ΔV*(VRP0+VR0/1/2P+80R+VRHP+VRMP +VRLP)/SUMRP	PKP5= 6	
KVP48	VREG1OUT - ΔV*(VRP0+VR0/1/2P+84R+VRHP+VRMP +VRLP)/SUMRP	PKP5= 7	
KVP49	VREG1OUT - ΔV*(VRP0+VR0/1/2/3P+84R+VRHP+VRMP +VRLP)/SUMRP	-	VINP7

SUMRP: Sum of positive ladder resistors = 92R+VRHP+VRLP+VRP0+VRP1+VR0P+VR1P+VR2P +VR3P+VRMP

ΔV : Difference in electrical potential between VDH and VGS

Table 62: Formulae for calculating voltage (2)

Grayscale voltage	Formula
V0	VINP0
V1	VINP1
V2	VINP2+(VINP1-VINP2)*(30/48)
V3	VINP2+(VINP1-VINP2)*(23/48)
V4	VINP2+(VINP1-VINP2)*(16/48)
V5	VINP2+(VINP1-VINP2)*(12/48)
V6	VINP2+(VINP1-VINP2)*(8/48)
V7	VINP2+(VINP1-VINP2)*(4/48)
V8	VINP2
V9	VINP3+(VINP2-VINP3)*(22/24)
V10	VINP3+(VINP2-VINP3)*(20/24)
V11	VINP3+(VINP2-VINP3)*(18/24)
V12	VINP3+(VINP2-VINP3)*(16/24)
V13	VINP3+(VINP2-VINP3)*(14/24)
V14	VINP3+(VINP2-VINP3)*(12/24)
V15	VINP3+(VINP2-VINP3)*(10/24)
V16	VINP3+(VINP2-VINP3)*(8/24)
V17	VINP3+(VINP2-VINP3)*(6/24)
V18	VINP3+(VINP2-VINP3)*(4/24)
V19	VINP3+(VINP2-VINP3)*(2/24)
V20	VINP3
V21	VINP4+(VINP3-VINP4)*(22/23)
V22	VINP4+(VINP3-VINP4)*(21/23)
V23	VINP4+(VINP3-VINP4)*(20/23)
V24	VINP4+(VINP3-VINP4)*(19/23)
V25	VINP4+(VINP3-VINP4)*(18/23)
V26	VINP4+(VINP3-VINP4)*(17/23)
V27	VINP4+(VINP3-VINP4)*(16/23)
V28	VINP4+(VINP3-VINP4)*(15/23)
V29	VINP4+(VINP3-VINP4)*(14/23)
V30	VINP4+(VINP3-VINP4)*(13/23)
V31	VINP4+(VINP3-VINP4)*(12/23)

Grayscale voltage	Formula
V32	VINP4+(VINP3-VINP4)*(11/23)
V33	VINP4+(VINP3-VINP4)*(10/23)
V34	VINP4+(VINP3-VINP4)*(9/23)
V35	VINP4+(VINP3-VINP4)*(8/23)
V36	VINP4+(VINP3-VINP4)*(7/23)
V37	VINP4+(VINP3-VINP4)*(6/23)
V38	VINP4+(VINP3-VINP4)*(5/23)
V39	VINP4+(VINP3-VINP4)*(4/23)
V40	VINP4+(VINP3-VINP4)*(3/23)
V41	VINP4+(VINP3-VINP4)*(2/23)
V42	VINP4+(VINP3-VINP4)*(1/23)
V43	VINP4
V44	VINP5+(VINP4-VINP5)*(22/24)
V45	VINP5+(VINP4-VINP5)*(20/24)
V46	VINP5+(VINP4-VINP5)*(18/24)
V47	VINP5+(VINP4-VINP5)*(16/24)
V48	VINP5+(VINP4-VINP5)*(14/24)
V49	VINP5+(VINP4-VINP5)*(12/24)
V50	VINP5+(VINP4-VINP5)*(10/24)
V51	VINP5+(VINP4-VINP5)*(8/24)
V52	VINP5+(VINP4-VINP5)*(6/24)
V53	VINP5+(VINP4-VINP5)*(4/24)
V54	VINP5+(VINP4-VINP5)*(2/24)
V55	VINP5
V56	VINP6+(VINP5-VINP6)*(44/48)
V57	VINP6+(VINP5-VINP6)*(40/48)
V58	VINP6+(VINP5-VINP6)*(36/48)
V59	VINP6+(VINP5-VINP6)*(32/48)
V60	VINP6+(VINP5-VINP6)*(25/48)
V61	VINP6+(VINP5-VINP6)*(18/48)
V62	VINP6
V63	VINP7

Note: Make sure DDVDH-V0 > 0.5V

Relationship between RAM Data and Voltage Output Levels

The relationship between RAM data and source output voltage levels is as follows. See also Table 46: GRAM data and LCD output level.

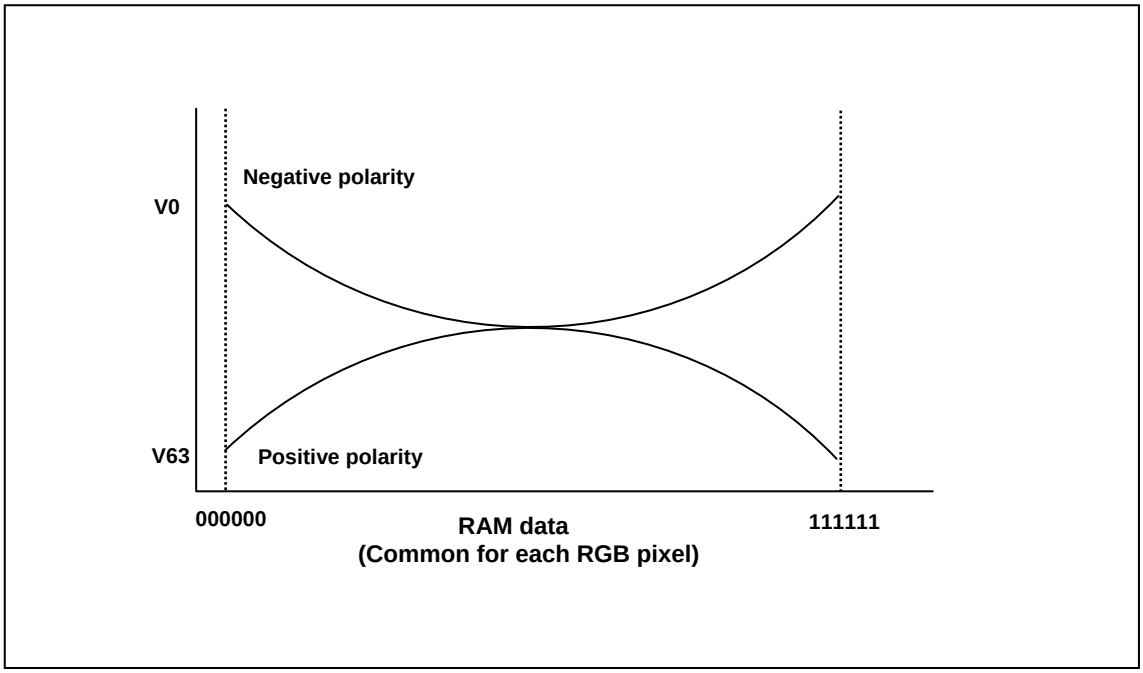


Figure 56: RAM data and the output voltage (REV = "0")

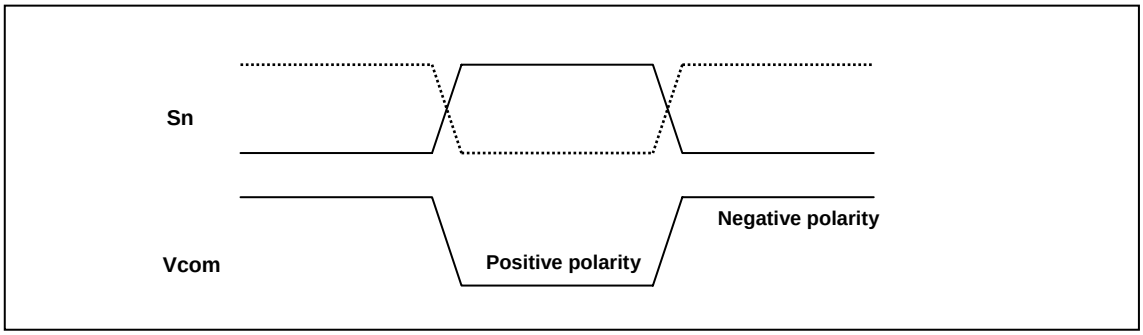


Figure 57: Source output and Vcom

8-Color Display Mode

The LGDP4524 has a function to display in 8colors. In 8-color mode, available grayscale levels are V0 and V63, and the power supplies of other grayscales (V1 to V62) are halted to reduce power consumption.

In 8-color display mode, the MSBs of the respective dot data (R5, G5, B5) are written to the rest of the dot data in order to display in 8 colors without rewriting the RAM data.

The γ- correction registers, PKP0-PKP5 and PKN0-PKN5, are disabled in 8-color display mode.

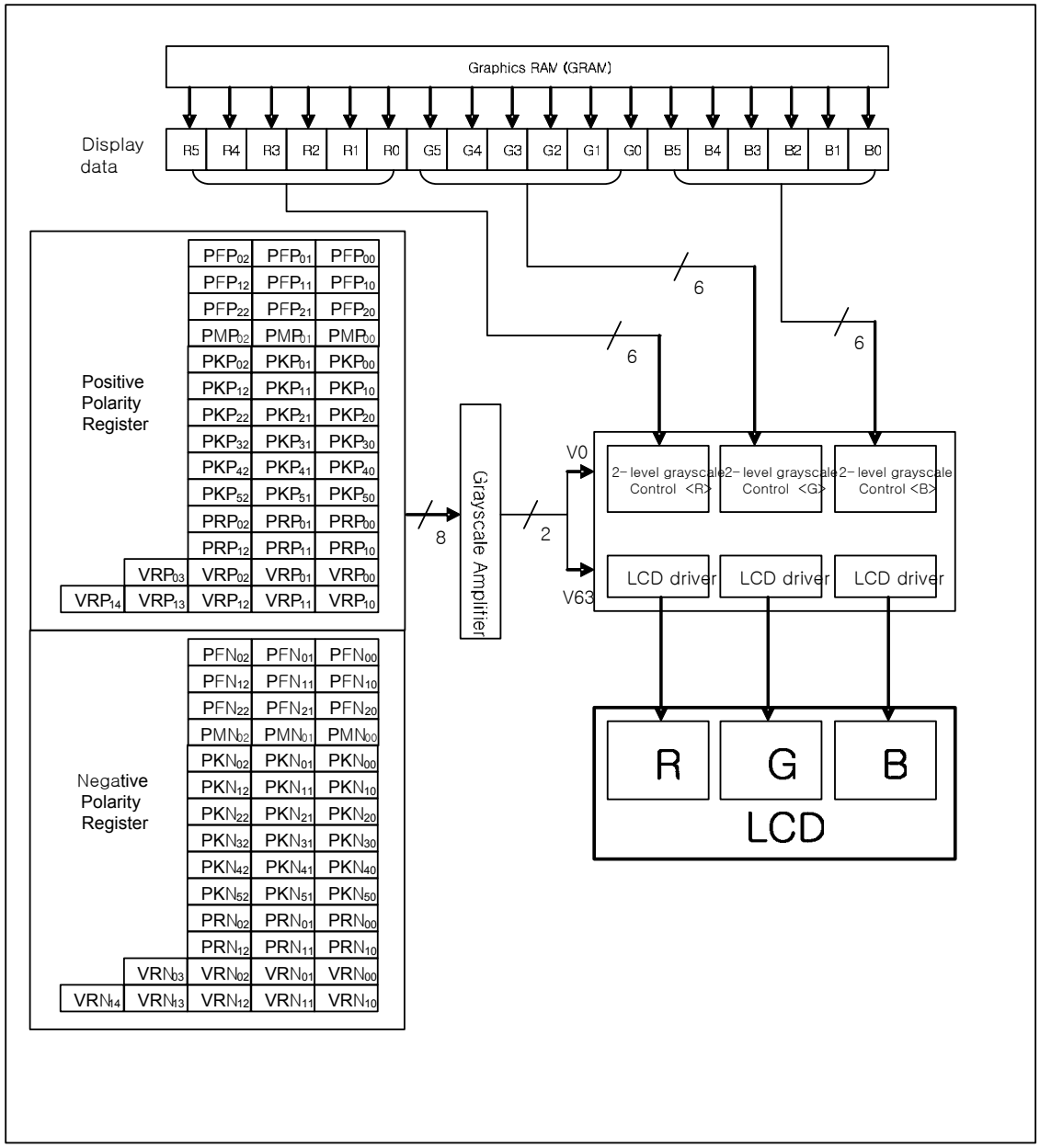


Figure 58

To switch between the 262,144-color mode and 8-color mode, follow the sequence below.

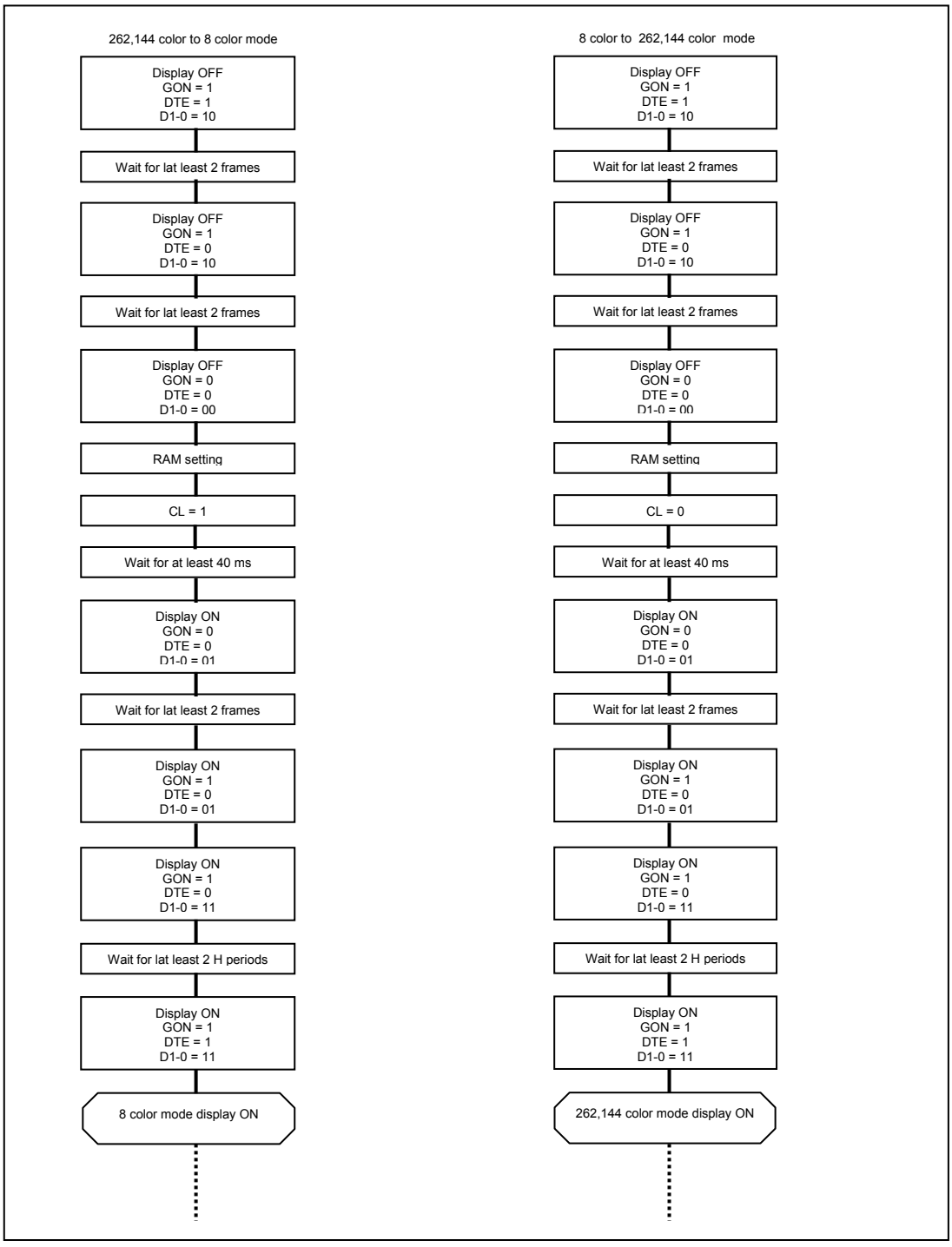


Figure 59

Configuration of Power Supply Circuit

The follow are the configuration of power supply circuit to generate liquid crystal panel drive levels.

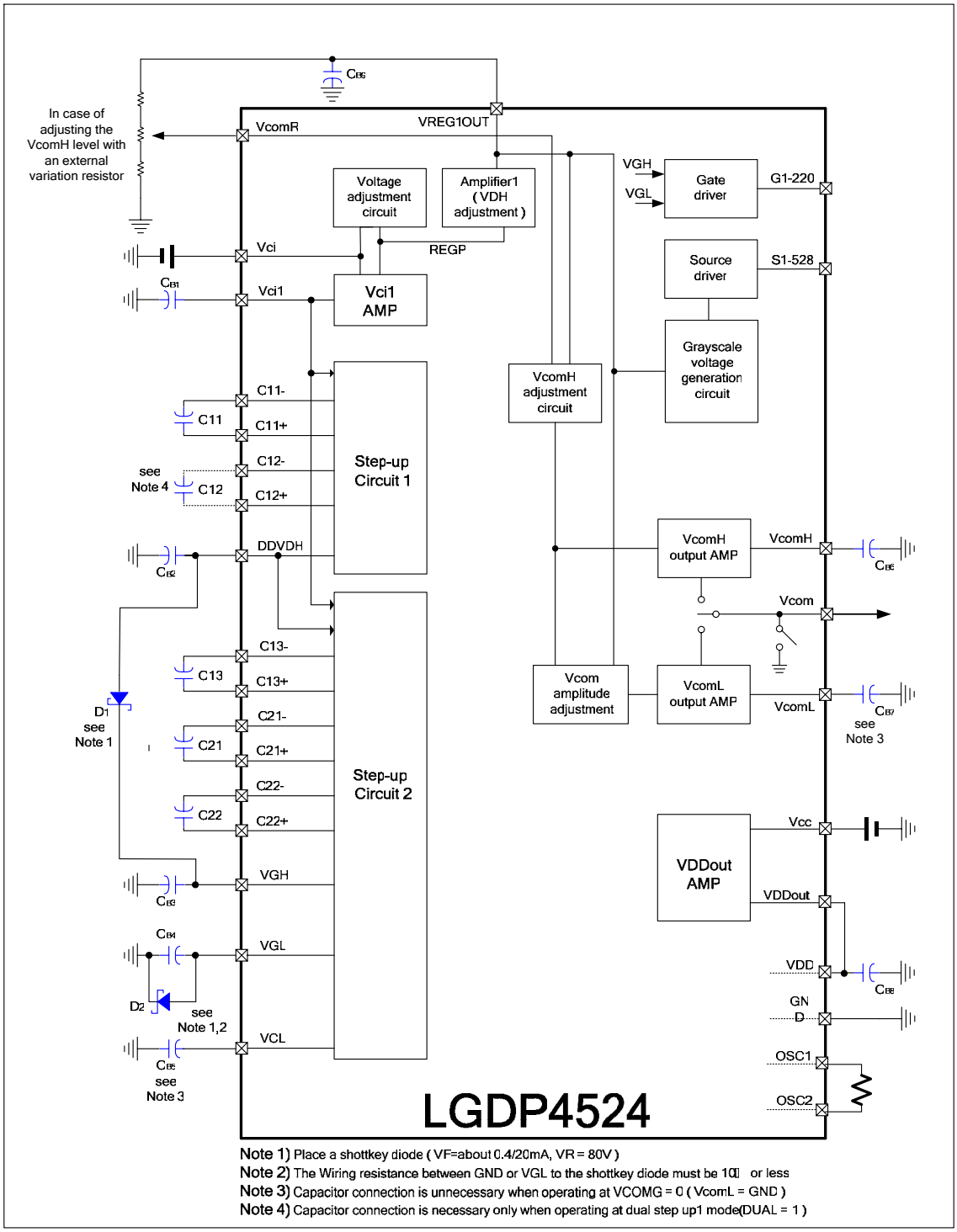


Figure 60

Specification of External Elements Connected to LGDP4524 Power Supply

The follow table shows specifications of external element connected to the LGDP4524's power supply circuit.

Table 63: Capacitor

Capacity	Recommended voltage	Pin connection
1uF (B characteristics)	6V	Vci1, C11+/- , C12+/-, C13+/-, VCL(see note), VcomL (see note), VDD
	10V	VREG1OUT, VcomH, DDVDH, C21+/- , C22+/-
	25V	VGH, VGL

Note: Capacitor connection is not necessary in some operation modes.

Table 64: Schottky diode

Feature	Pin connection
VF < 0.4V/20mA at 25°C , VR>30V	GND – VGL DDVDH – VGH

Table 65: Variable resistor

Feature	Pin connection
> 200kΩ	VcomR

Instruction Setting

When setting the following instructions, follow respective sequences below.

Display On/Off

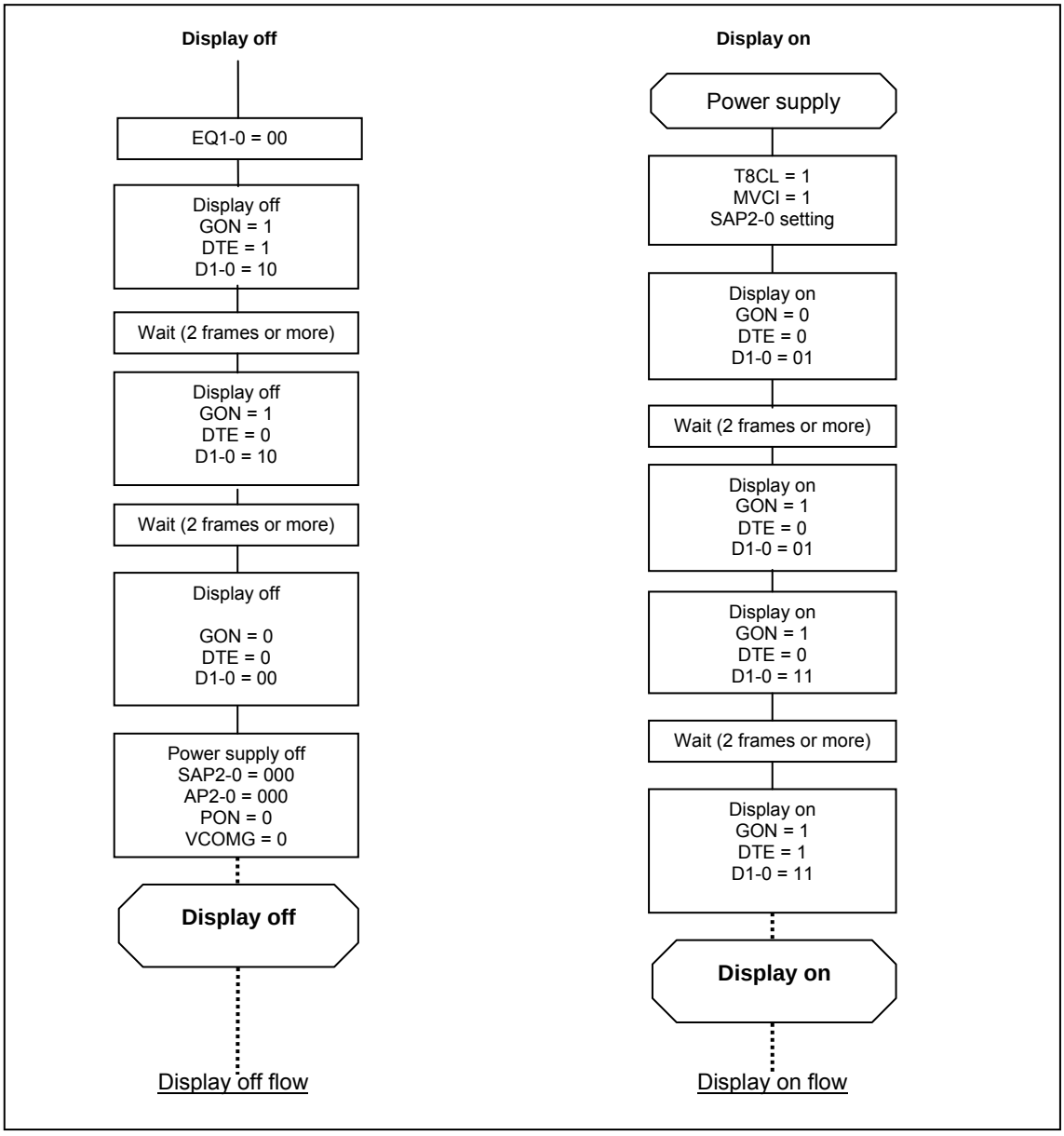


Figure 61

Standby and Sleep Modes

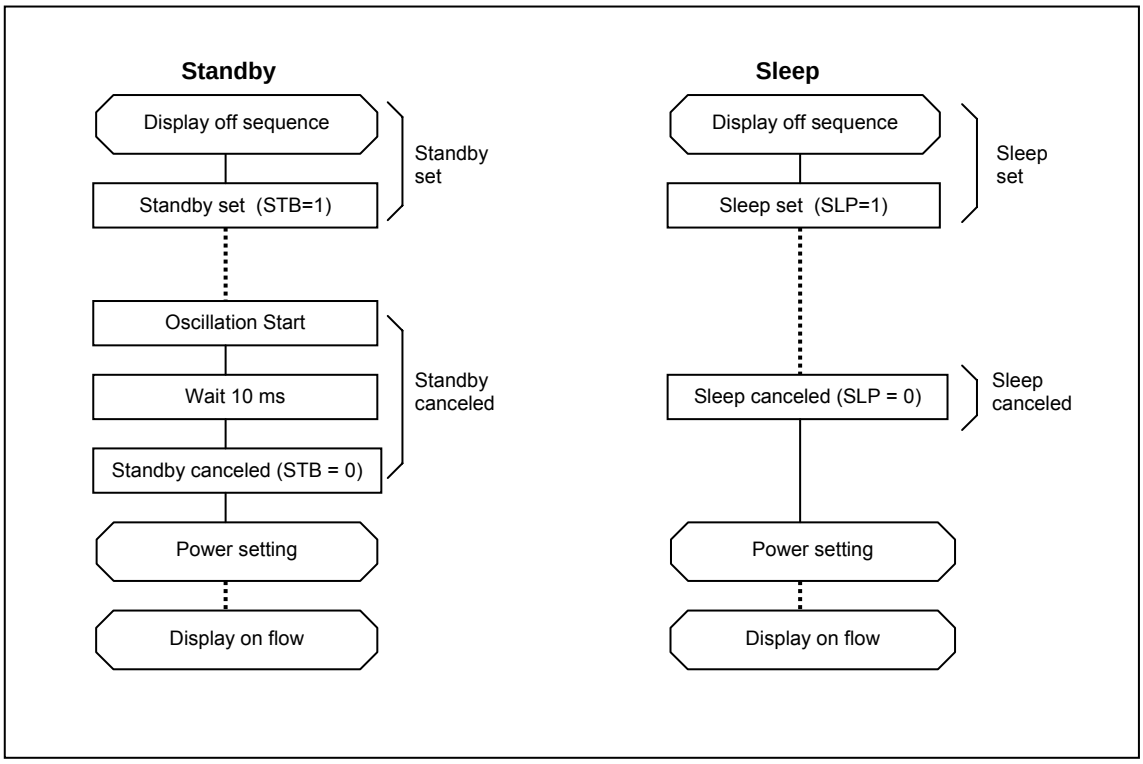


Figure 62

Deep Standby Mode

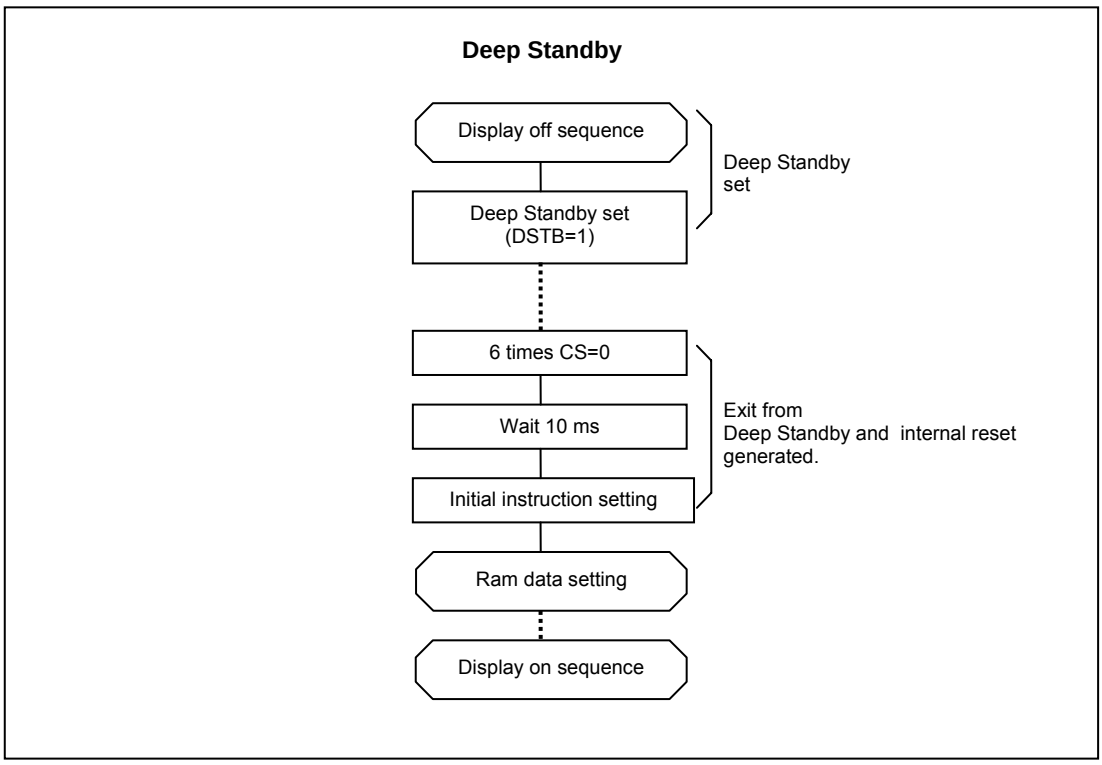


Figure 63

Power Supply Setting

When supplying and cutting off power, follow the sequence below. The setting time for oscillators, step-up circuits and operational amplifiers depends on external resistance and capacitance.

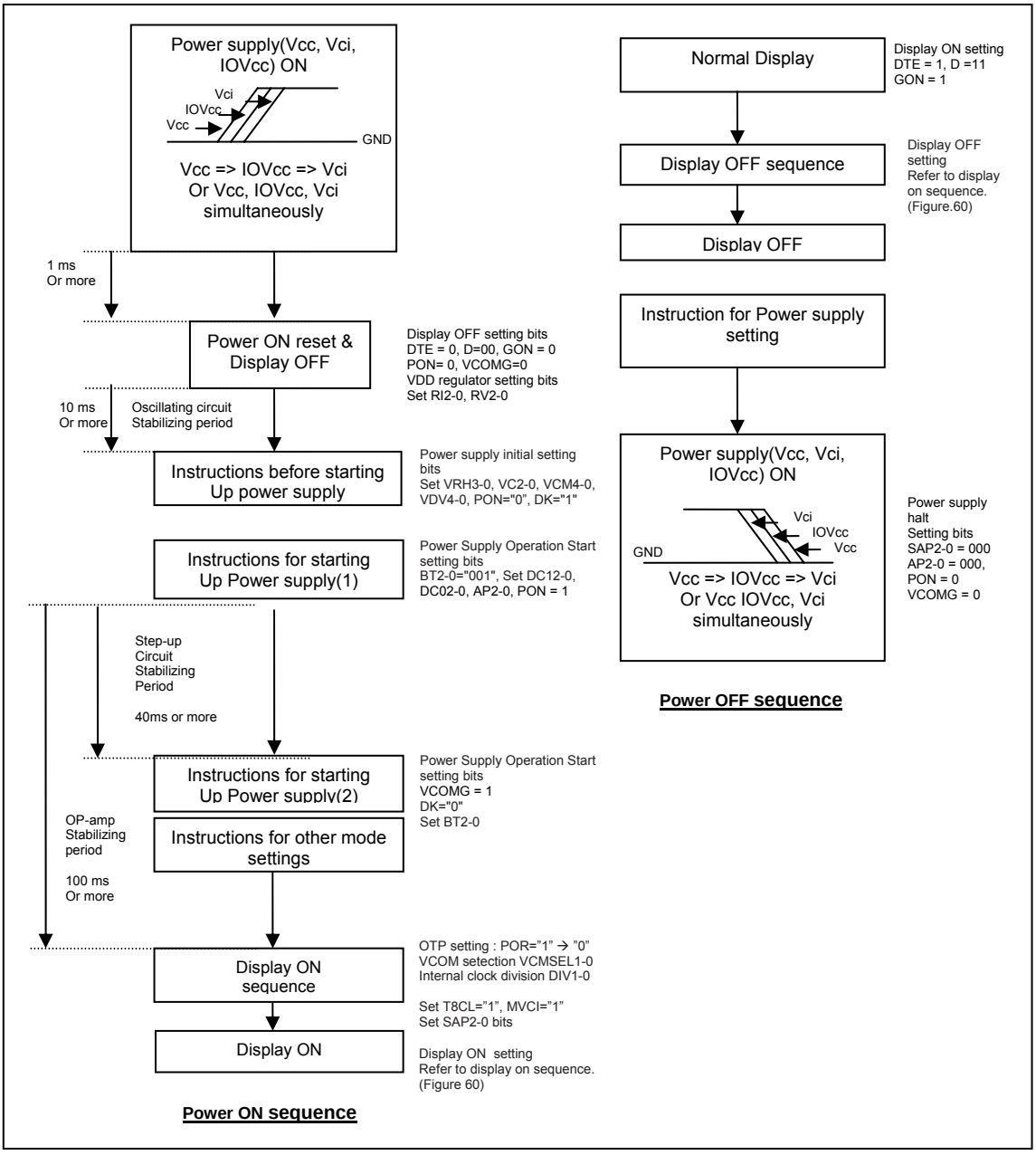


Figure 64

Pattern Diagram for Voltage Setting

The pattern diagram for the voltages and the waveforms of the voltages of the LGDP4524 are as follows.

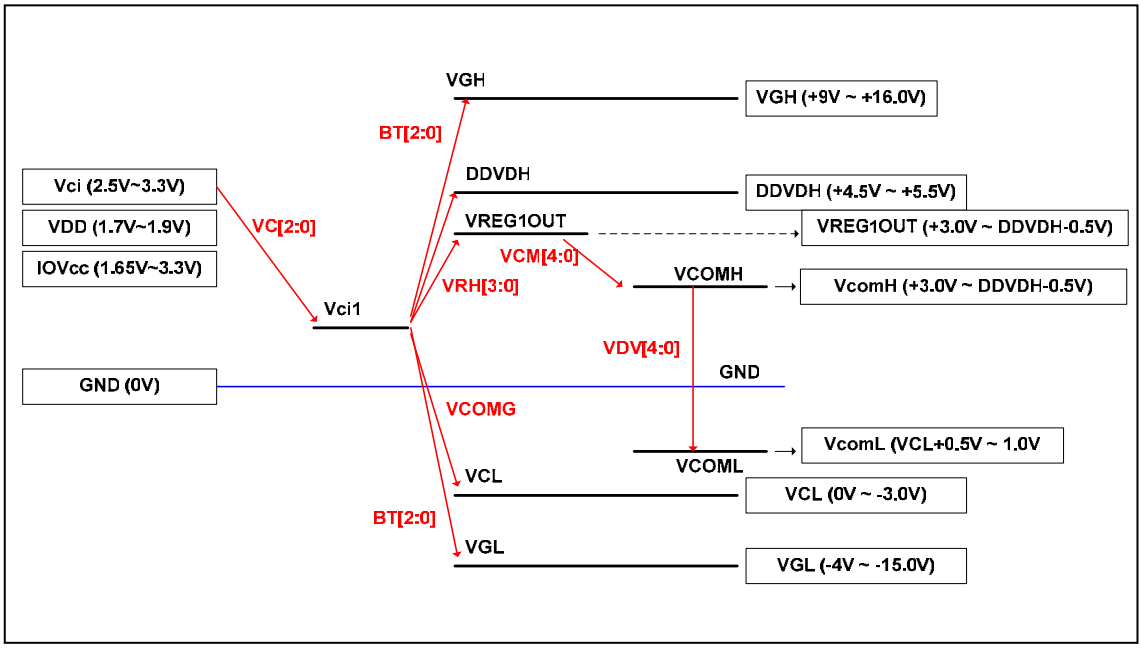


Figure 65

Note: The DDVDH, VGH, VGL, and VCL output voltage levels are lower than their theoretical levels (ideal voltage levels) due to current consumption at respective output. The voltage levels in the following relationships (DDVDH – VREG1OUT) > 0.5V, (VcomL – VCL) > 0.5V are the actual voltage levels. When the alternating cycles of Vcom are set high (e.g. the polarity inverts every line cycle), current consumption is large. In this case, check the voltage before use.

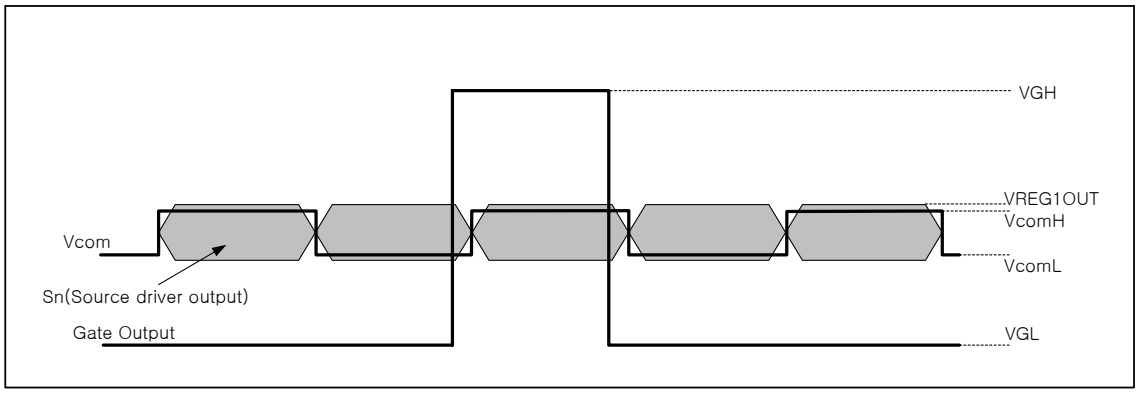


Figure 66: Applied voltage to the TFT display

Oscillator

The LGDP4524 generates oscillation with the LGDP4524's internal RC oscillators by placing an external oscillation resistor between the OSC1 and OSC2 pins. The oscillation frequency varies due to resistance value of external resistor, wiring distance, and operating supply voltage. For example, placing an Rf resistor of a larger resistance value, or lowering the supply voltage level brings down the oscillation frequency. See the "Notes to Electrical Characteristics" section for the relationship between resistance value of Rf resistor and oscillation frequency.

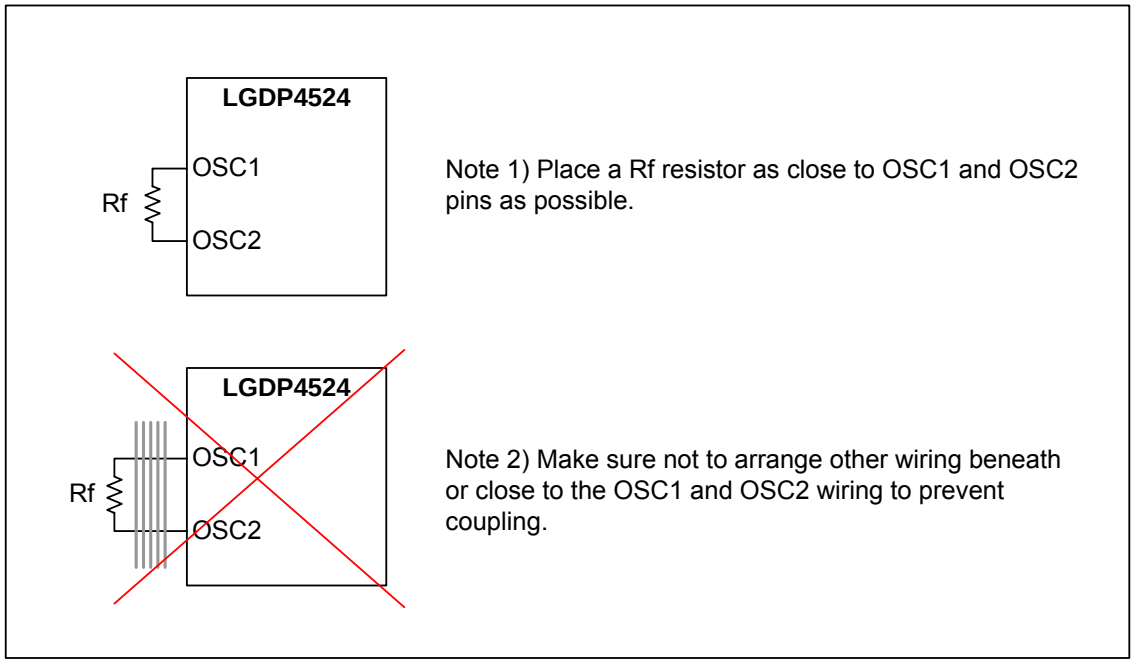


Figure 67

n-Line Inversion AC Drive

The LGDP4524, in addition to the frame-inversion liquid crystal AC drive, supports the n-line inversion AC drive, in which the polarity of liquid crystal is inverted in units of n lines, where n takes a number from 1 to 64. The quality of display will be improved by using n-line inversion AC drive.

In determining n (the value set with the NW bits +1), which represents the number of lines that determines the timing of liquid crystal polarity inversion, check the quality of display on the liquid crystal panel in use. Note that setting a smaller number of lines will raise the frequency of liquid crystal polarity inversion and increase charging/discharging current on liquid crystal cells.

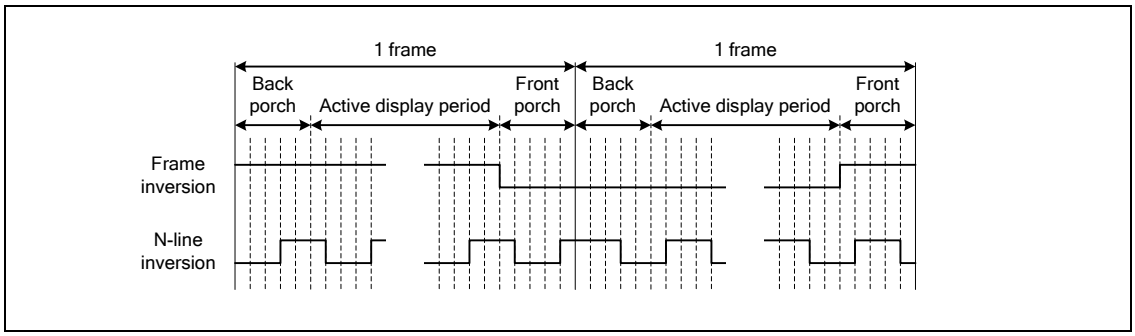


Figure 68

Interlaced Scan

The LGDP4524 supports interlaced scan for driving a frame by splitting it into n fields in order to prevent flicker.

To determine the number of fields (n: value set with the FLD bits), check the quality of display on the liquid crystal panel in use. The following table shows the scanned (gate) lines in each field. When FLD[1:0] = “01”, the number of fields in one frame is one. When FLD[1:0] = “11”, the number of fields in one frame is three. The figure illustrates the output waveforms of 3-field interlaced scan.

Table 66: Interlaced scan (GS = “0”)

FLD[1:0]	01	11		
Field / Gate	-	1	2	3
G1	*	*		
G2	*		*	
G3	*			*
G4	*	*		
G5	*		*	
G6	*			*
G7	*	*		
G8	*		*	
:				
G217	*	*		
G218	*		*	
G219	*			*
G220	*	*		

Table 67: Interlaced scan (GS = “1”)

FLD[1:0]	01	11		
Field / Gate	-	1	2	3
G220	*	*		
G219	*		*	
G218	*			*
G217	*	*		
G216	*		*	
G215	*			*
G214	*	*		
G213	*		*	
:				
G4	*	*		
G3	*		*	
G2	*			*
G1	*	*		

*: scanned gate lines

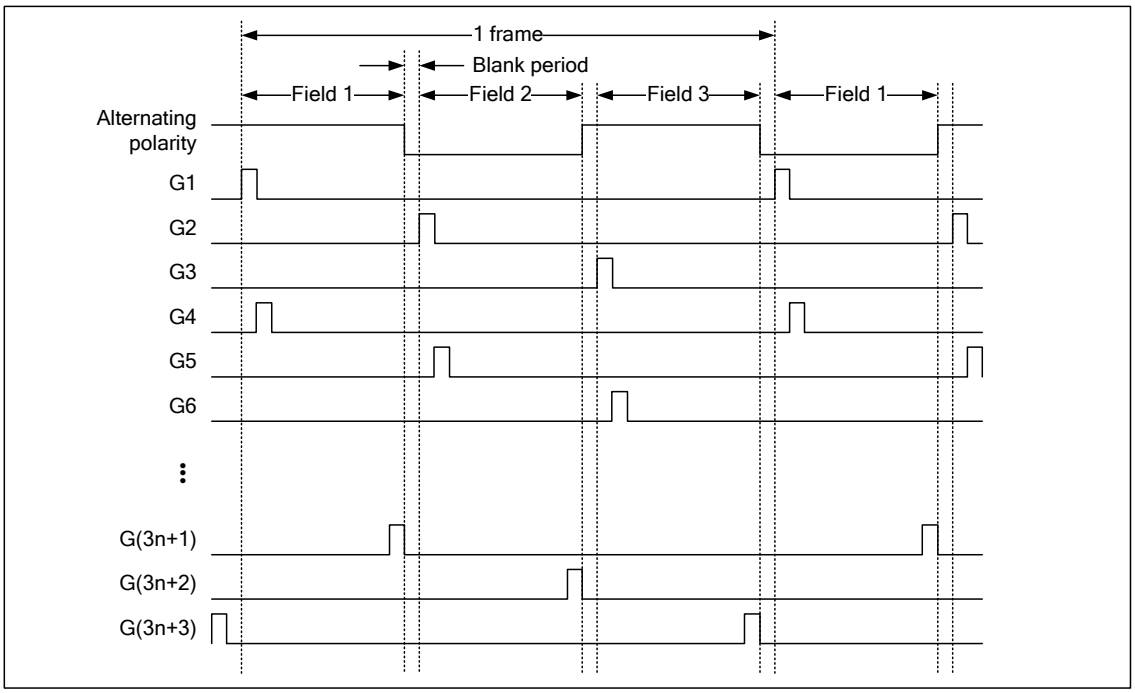


Figure 69: Gate output timing of 3-field interlaced scan

Alternating Timing

The following figure illustrates the timing of liquid crystal polarity inversion in different driving formulae. In case of frame-inversion AC drive, the polarity is inverted after drawing one frame, followed by a blank period lasting for a 16H period, where all outputs from the gate lines become the VGL level. In case of 3-field interlaced scan, polarity is inverted after drawing one field, followed by blank periods that add up to a 16H period in one frame. In case of n-line inversion AC drive, polarity is inverted as drawing n lines, and a blank period lasting for a 16H period is inserted after drawing one frame.

In the interlaced scan, be sure to set the numbers of back and front porches as follows: BP = 3, FP = 5.

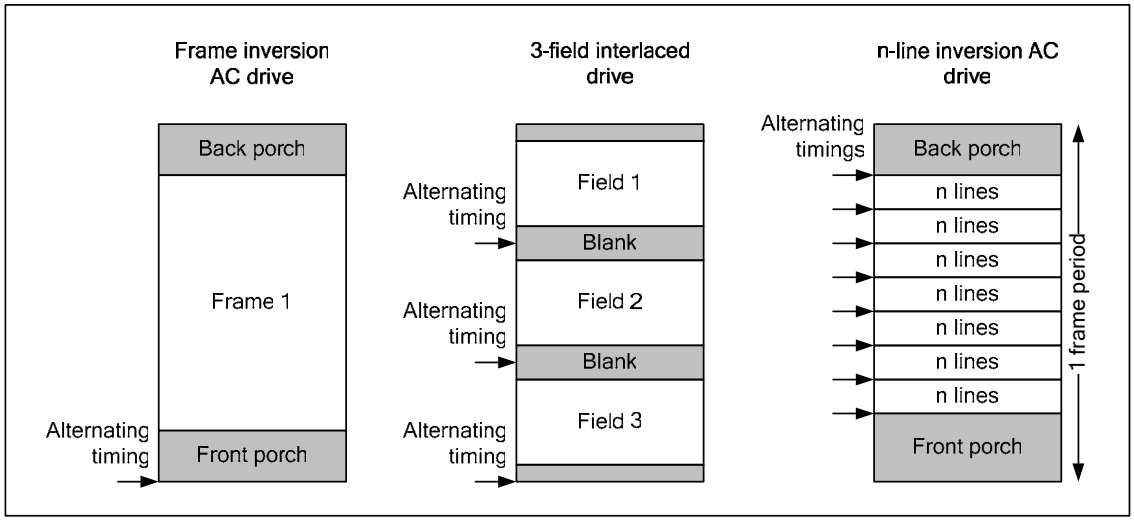


Figure 70

Frame Frequency Adjustment Function

The LGDP4524 has a frame frequency adjustment function. The frame frequency for driving LCDs can be adjusted by instructions (using the DIV, RTN bits) without changing the oscillation frequency.

To switch frame frequencies between when displaying a moving picture and when displaying a still picture, set a high oscillation frequency in advance. By doing so, it becomes possible to set a low frame frequency when displaying a still picture for saving power consumption and to set a high frame frequency when displaying a moving picture.

Relationship between Liquid Crystal Drive Duty and Frame Frequency

The relationship between the liquid crystal drive duty and the frame frequency is calculated from the following formula. The frame frequency is adjusted by instruction using the 1H period adjustment bits (RTN bits) and the operation clock division bits (DIV bits).

$$frame\ frequency = \frac{fosc}{clock\ cycles\ per\ line * division\ ratio * (Line + BP + FP)}$$

where

fosc = RC oscillation frequency,
Line = number of lines to drive the LCD (NL bits),
clock cycle per line = RTN bits,
division ratio: DIV bits,
FP = number of lines for front porch and
BP = number of lines for back porch.

Example of Calculation: when maximum frame frequency = 60 Hz

Number of lines to drive the LCD: 220 lines
1H period: 44 clock cycle (RTN[6:0] = 2Ch)
Operational clock division ratio: 2/1

$$fosc = 60\ Hz \times (0 + 44)\ clocks \times 2/1 \times (220 + 16)\ lines = 1{,}246\ kHz$$

In this case, the target RC oscillation frequency is 1,246 kHz. Adjust the external resistor of the RC oscillator to 1,246 kHz.

Partial Display Function

The LGDP4524 allows selectively driving two images on the screen at arbitrary positions set in the screen drive position registers (R42h and R43h). Only the lines for displaying two images are selectively driven in order to reduce current consumption.

The first display drive position register (R42h) includes the start line setting bits (SS1) and the end line setting bits (SE1) for displaying the first image. The second display drive position register (R43h) includes the start line setting bits (SS2) and the end line setting bits (SE2) for displaying the second image. The second display control is effective when the SPT bit is set to “1”. The total number of lines driven for displaying the first and second display must be less than the number of lines set with the NL bits.

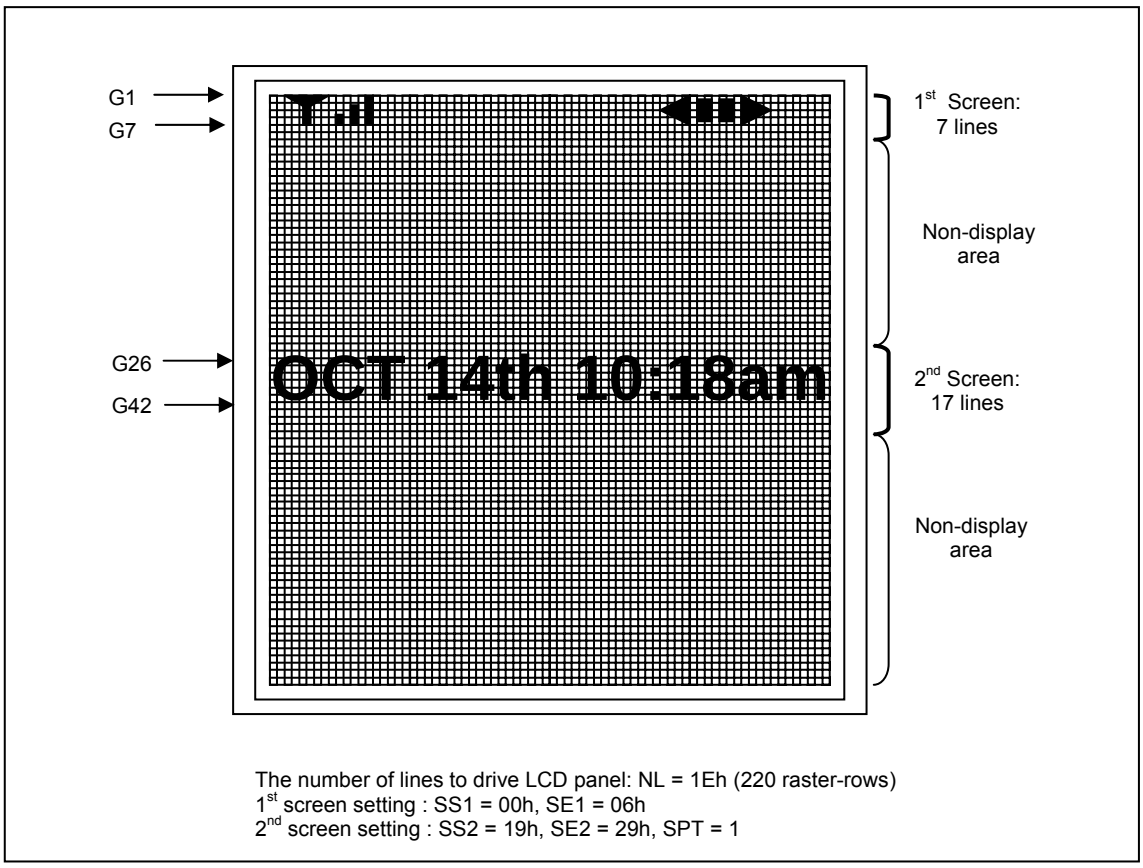


Figure 71

Constraints in Setting the 1st/2nd Screen Drive Position Registers

When setting the start line setting bits (SS1[7:0]) and the end line setting bits (SE1[7:0]) of the first display drive position register (R42h), and the start line setting bits (SS2[7:0]) and the end line setting bits (SE2[7:0]) of the second display drive position register (R43h), it is necessary to satisfy the following conditions to display screens correctly.

Table 68: One screen drive (SPT = "0")

Register Settings	Display Operation
(SE1 – SS1) = NL	Full screen display The area of (SE1 – SS1) is normally displayed.
(SE1 – SS1) < NL	Partial screen display The area of (SE1 – SS1) is normally displayed. The rest of the area is a white display irrespective of data in RAM.
(SE1 – SS1) > NL	Setting disabled

Table 69: Two screen drive (SPT = "1")

Register Settings	Display Operation
((SE1 – SS1) + (SE2 – SS2)) = NL	Full screen display The area of (SE2 – SS1) is normally displayed.
((SE1 – SS1) + (SE2 – SS2)) < NL	Partial screen display The area of (SE2 – SS1) is normally displayed. The rest of the area is a white display irrespective of data in RAM.
((SE1 – SS1) + (SE2 – SS2)) > NL	Setting disabled

Note 1) Be sure that SS1 ≤ SE1 ≤ SS2 ≤ SE2 ≤ EFh.
Note 2) Be sure that (SE2 – SS1) ≤ NL.

The outputs from the source driver in non-display areas of the partial display can be changed as follows. Select the appropriate kind of source outputs according to the characteristics of the display panel.

Table 70

PTS	Source output in non-display area		Operating grayscale amplifier in non-display area
	Positive polarity	Negative polarity	
000	V63	V0	V0 to V63
001	Setting disabled	Setting disabled	-
010	GND	GND	V0 to V63
011	High impedance	High impedance	V0 to V63
100	V63	V0	V0, V63
101	Setting disabled	Setting disabled	-
110	GND	GND	V0, V63
111	High impedance	High impedance	V0, V63

Table 71

PTG	Gate outputs in non-display area
00	Normal scan
01	VGL (fixed)
10	Interval scan
11	Setting disabled

Follow the sequences below when using the partial display function.

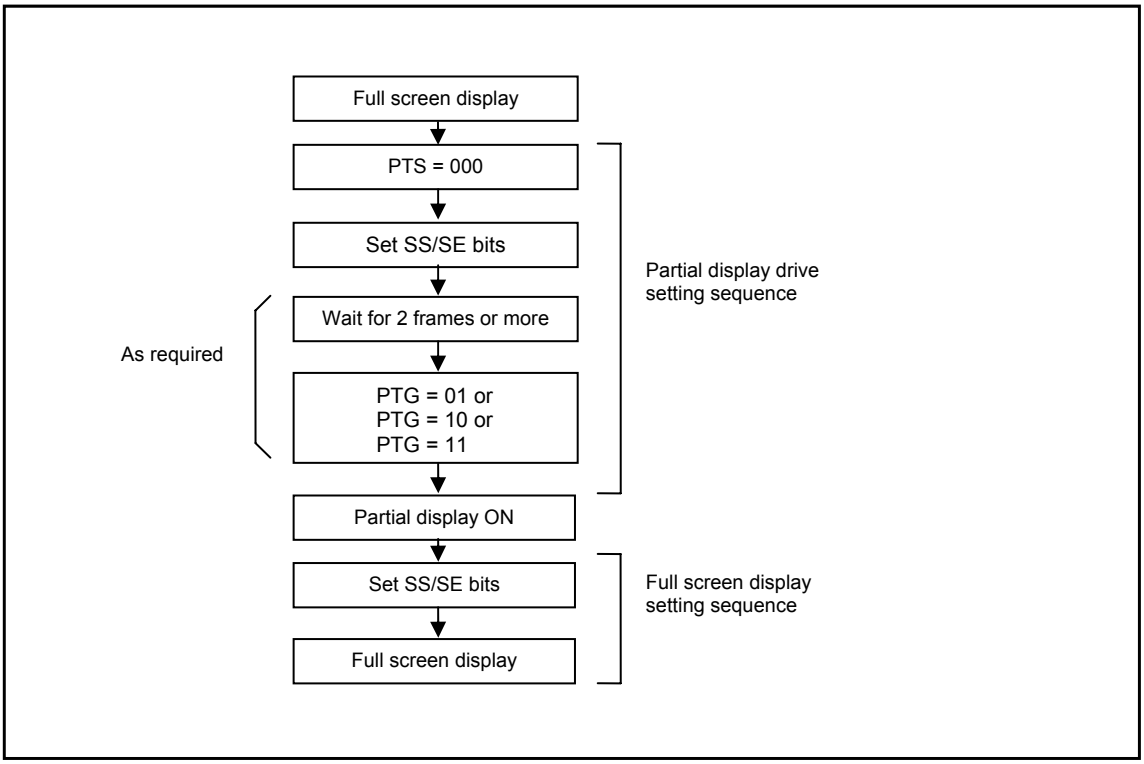

Full screen display
PTS = 000
Set SS/SE bits
Wait for 2 frames or more
PTG = 01 or
PTG = 10 or
PTG = 11
Partial display ON
Set SS/SE bits
Full screen display
As required
Partial display drive
setting sequence
Full screen display
setting sequence

Figure 72

EPROM Control

LGDP4524 has an embedded EPROM which is consisted of a 32-bit one-time programmable EPROM. 32 bits are separated into 4 banks. One bank has 1 bit for flag bit and 7 bits for data which can be used to set VcomH level . The initial data of EPROM is a logic high. Only UV light can erase OTP cells in EPROM.

The EPROM usage for setting VcomH level is shown as following.

Organization of EPROM

Bank3	Flag3	6	5	4	3	2	1	0	PD[31:24]
Bank2	Flag2	6	5	4	3	2	1	0	PD[23:16]
Bank1	Flag1	6	5	4	3	2	1	0	PD[15:8]
Bank0	Flag0	6	5	4	3	2	1	0	PD[7:0]

VcomH level can be set by VCM[6:0] of R13h or EPROM data. The VCMSEL[1:0] of R61h selects one of VCM[6:0] and EPROM data to set VcomH level. If VCMSEL[1:0] =00, EPROM data sets VcomH level if EPROM has data. If EPROM data has no data, VcomH level is set by VCM[6:0] even though VCMSEL[1:0]=00. Otherwise, in condition of VCMSEL[1:0]=10, VcomH level is set by only VCM[6:0] of R13h.

Each 7 bits of each bank is assigned to set VcomH level like VCM[6:0] in R13h.

If one of bank is written to set VcomH level in condition of VCMSEL[1:0] =00, correspond flag bit should be written as logic low level. Internal logic checks first 4 flag bits with priority from 3 to 0 and see if there is logic low bit. If it exists, the corresponding 7 bits are selected and used to set VcomH level.

VcomH Level Setting flow in condition of VCMSEL[1:0]=00

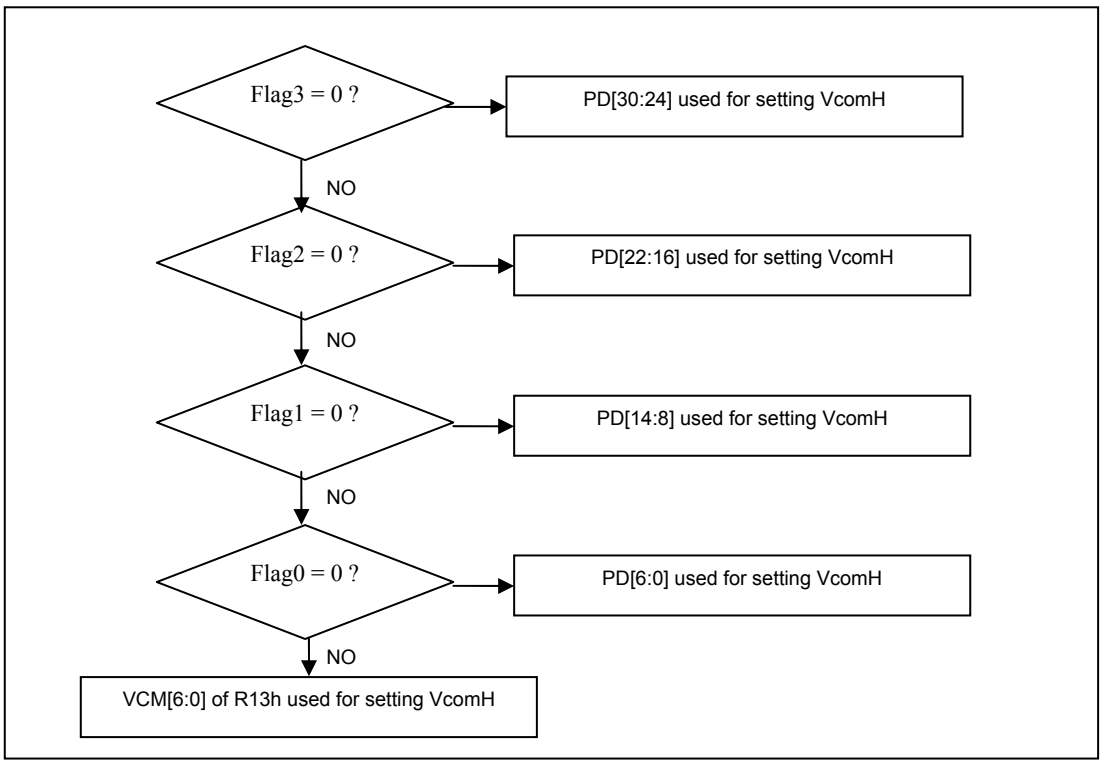


Figure 73

The pins of the embedded EPROM can be controlled using the EPROM control 1 (R60h) register as shown below.

Table 72: Pin mapping

EO01X32KCV6	Bit fields of register R60h
POR = 0V/1.8V	POR = 0/1
VPP = 1.8V/7.5V	VPP = 0/1
PPROG = 0V/1.8V	PPROG = 0/1
PWE = 0V/1.8V	PWE = 0/1
PA[1:0] = 0V/1.8V	PA[1:0] = 0/1
PDIN[6:0] = 0V/1.8V	PDIN[6:0] = 0/1

ERPOM Program and Read Flow

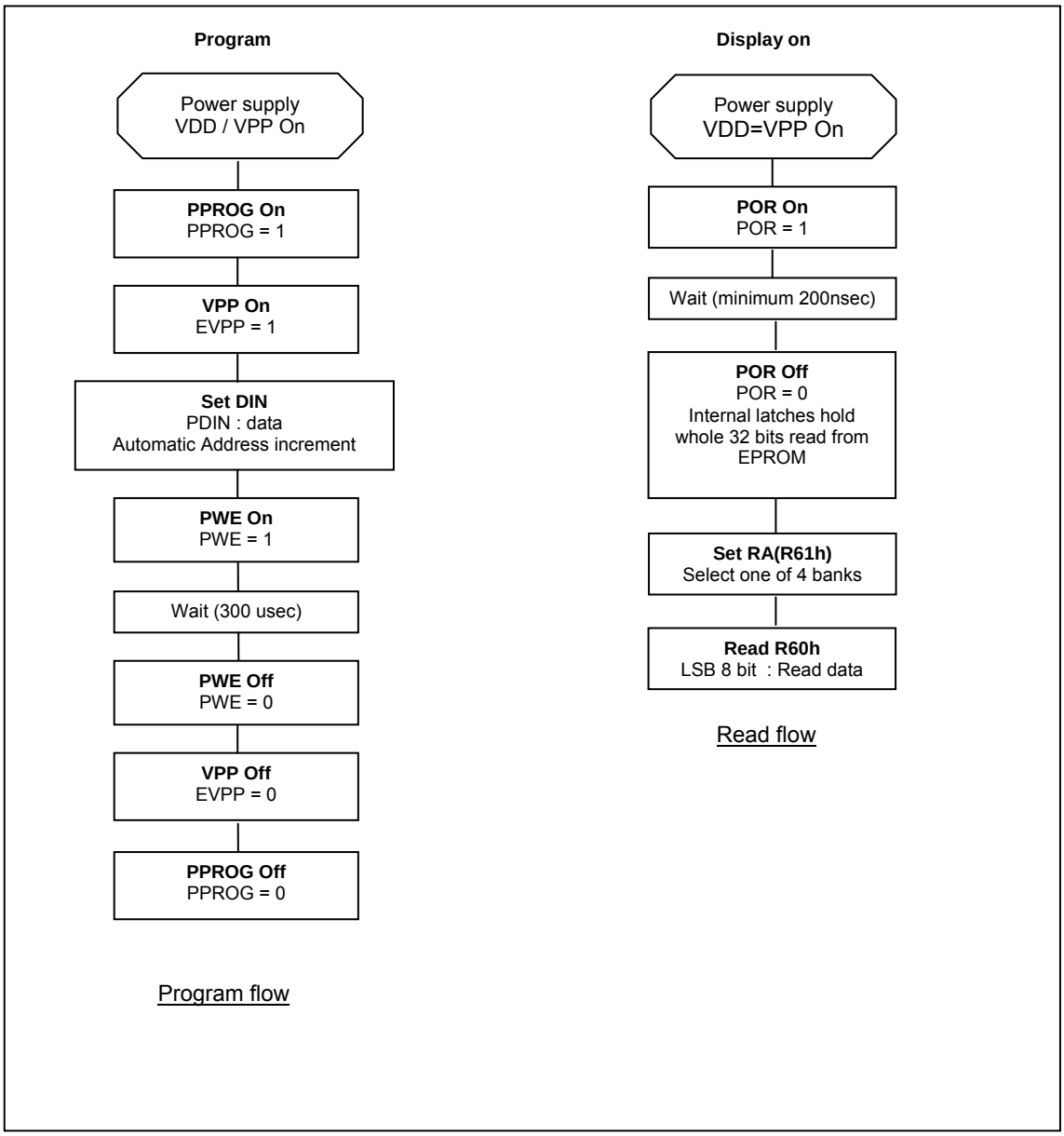


Figure 74

If AUTOWE of R61h is logic high, while program flow, automatic address increment function disabled and PA[1:0] of R60h must be specified to set address of EPROM at the same time with setting PDIN.

The RA[1:0] of register R61h selects one of four EPROM bytes after read cycle.

Accessing EPROM control registers, follow the timing requirements of read and program cycles.

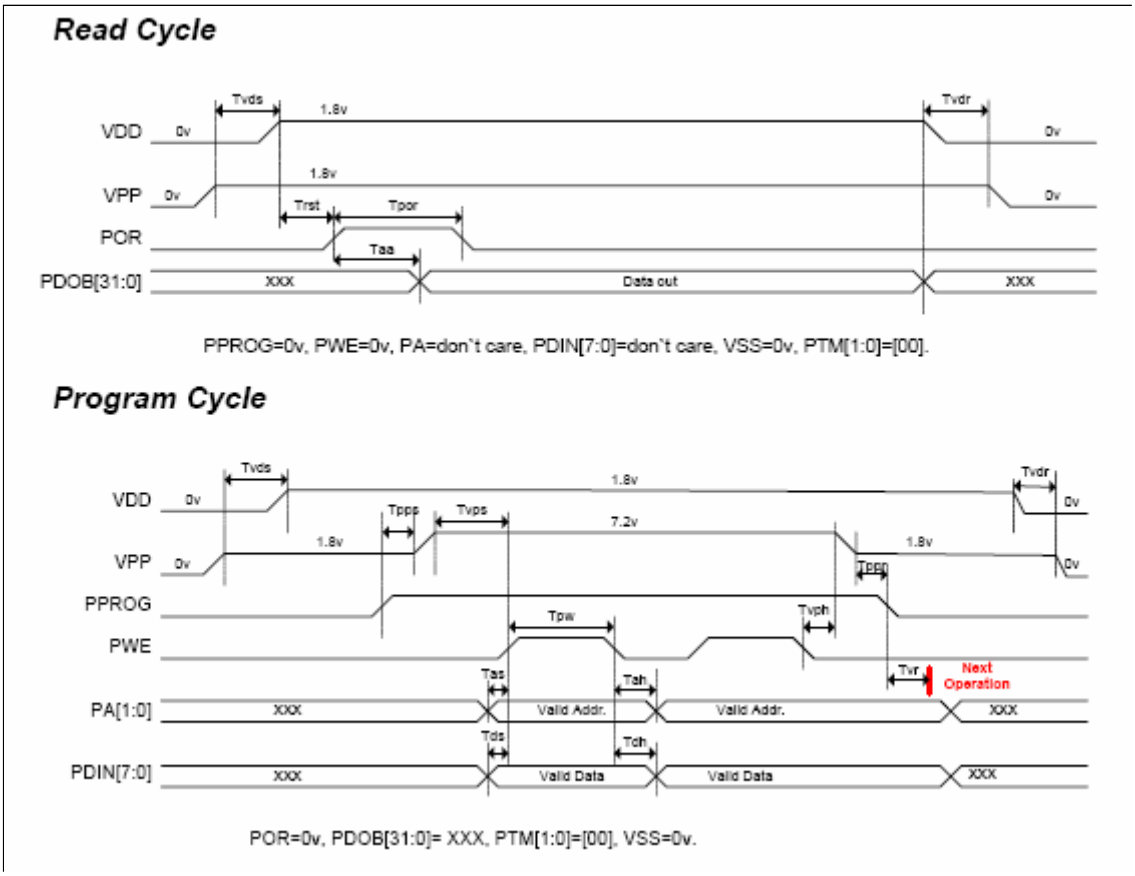


Figure 75: EPROM timings

Table 73

Parameter	Symbol	EPROM		Unit
		Min	Max	
Rising Time / Falling Time	T_r / T_f	-	1	nS
Data Access Time	T_{aa}	-	70	nS
Power-on Pulse Width Time	T_{por}	200	-	nS
Address / Data Setup Time	T_{as} / T_{ds}	4	-	nS
Address / Data Hold Time	T_{ah} / T_{dh}	9	-	nS
External VPP Setup Time	T_{vps}	0	-	nS
External VPP Hold Time	T_{vph}	0	-	nS
Program Recovery Time	T_{vr}	10	-	uS
Program Pulse Width	T_{pw}	300	350	uS
VDD Setup Time	T_{vds}	0	-	mS
VDD Recovery Time	T_{vdr}	0	-	mS
PPROG Setup Time	T_{pps}	10	-	nS
PPROG Recovery Time	T_{ppr}	10	-	nS

Absolute Maximum Ratings

Item	Symbol	Unit	value	Notes
Power supply voltage (1)	Vcc, IOVcc	V	-0.3 ~ +4.2	1, 2
Power supply voltage (2)	Vci – GND	V	-0.3 ~ +4.2	1, 3
Power supply voltage (3)	DDVDH – GND	V	-0.3 ~ +7.7	1, 4
Power supply voltage (4)	GND – VCL	V	-0.3 ~ +4.2	1
Power supply voltage (5)	Vci –VCL	V	-0.3 ~ +7.7	1, 5
Power supply voltage (6)	VGH – GND	V	-0.3 ~ +18	1, 6
Power supply voltage (7)	GND – VGL	V	-0.3 ~ +18	1, 7
Input voltage	Vt	V	-0.3 ~ +4.2	1
Operating temperature	Topr	˚C	-40 ~ +85	1, 8
Storage temperature	Tstg	˚C	-55 ~ +125	1

Notes :

1. If used beyond the absolute maximum ratings, the LSI may permanently be damaged. It is strongly recommended to use the LSI at a condition within the electrical characteristics for normal operation. Exposure to a condition not within the electrical characteristics may affect device reliability.
2. Make sure (High) Vcc ≥ GND (Low), (High) IOVcc ≥ GND (Low).
3. Make sure (High) Vci ≥ GND (Low).
4. Make sure (High) DDVDH ≥ GND (Low).
5. Make sure (High) Vci ≥ VCL (Low).
6. Make sure (High) VGH ≥ GND (Low).
7. Make sure (High) GND ≥ VGL (Low).
8. The DC/AC characteristics of die and wafer products is guaranteed at 85 ℃.

Electrical Characteristics

DC Characteristics

Table 74: DC Characteristics

Item	Symbol	Unit	Test Condition	Min.	Typ.	Max	Notes
Input high-level voltage	V_{IH}	V	IOVcc=1.65~3.3	0.8IOVcc	-	IOVcc	2 ,3
Input low-level voltage	V_{IL}	V	IOVcc=1.65~3.3	-0.3	-	0.2IOVcc	2 ,3
Output high-level voltage(1) (DB17-0, SDO, FLM)	V_{OH1}	V	IOVcc=1.65~3.3 I_{OH} =0.1mA	0.8IOVcc	-	-	2
Output high-level voltage(2) (DB17-0, SDO, FLM)	V_{OL1}	V	IOVcc=1.65~3.3 I_{OL} =0.1mA	-	-	0.2IOVcc	2
I/O leakage current	I_{Li}	uA	Vin=0~IOVcc	-1	-	1	4
Current consumption: Standby mode (IOVcc-GND) +(Vcc-GND)	I_{ST}	uA	IOVcc=Vcc=Vci= 2.8V Ta=25℃	-	1.4	10	5

80-System Bus Interface Timing Characteristics (18/16-Bit Bus)

Table 75 (Condition: IOVcc = 1.65 to 3.30V,Vcc = 2.50 to 3.30V, VDD = 1.7 to 1.9V)

Item			Symbol	Unit	Min	Typ	Max
Bus cycle time		Write	t_{CYCW}	ns	100	-	-
		Read	t_{CYCR}		250	-	-
Write “Low” level pulse width		Write	PW_{LW}	ns	40	-	-
Read “Low” level pulse width		Read	PW_{LR}		150	-	-
Write “High” level pulse width		Write	PW_{HW}	ns	30	-	-
Read “High” level pulse width		Read	PW_{HR}		100	-	-
Write/Read rise/fall time			t_{WRr}, t_{WRf}	ns	-	-	25
Setup time	Write (RS to CS*/WR*)		t_{AS}	ns	0	-	-
	Read (RS to CS*/RD*)				10	-	-
Address hold time			t_{AH}	ns	2	-	-
Write data setup time			t_{DSW}	ns	25	-	-
Write data hold time			t_{H}	ns	2	-	-
Read data delay time			t_{DDR}	ns	-	-	100
Read data hold time			t_{DHR}	ns	5	-	-

80-System Bus Interface Timing Characteristics (8/9-Bit Bus)

Table 76 (Condition: IOVcc = 1.65 to 3.30V,Vcc = 2.50 to 3.30V, VDD = 1.7 to 1.9V)

Item			Symbol	Unit	Min	Typ	Max
Bus cycle time		Write	t_{CYCW}	ns	100	-	-
		Read	t_{CYCR}		250	-	-
Write "Low" level pulse width		Write	PW_{LW}	ns	40	-	-
Read "Low" level pulse width		Read	PW_{LR}		150	-	-
Write "High" level pulse width		Write	PW_{HW}	ns	30	-	-
Read "High" level pulse width		Read	PW_{HR}		100	-	-
Write/Read rise/fall time			t_{WRr}, t_{WRf}	ns	-	-	25
Setup time	Write (RS to CS*/WR*)		t_{AS}	ns	0	-	-
	Read (RS to CS*/RD*)				10	-	-
Address hold time			t_{AH}	ns	2	-	-
Write data setup time			t_{DSW}	ns	25	-	-
Write data hold time			t_{H}	ns	2	-	-
Read data delay time			t_{DDR}	ns	-	-	100
Read data hold time			t_{DHR}	ns	5	-	-

Serial Peripheral Interface Timing Characteristics

Table 77 (Condition: IOVcc = 1.65 to 3.30V,Vcc = 2.50 to 3.30V, VDD = 1.7 to 1.9V)

Item		Symbol	Unit	Min	Typ	Max
Serial clock cycle time	Write (received)	t_{SCYC}	ns	100	-	20000
	Read (transmitted)			350	-	20000
Serial clock "High" level pulse width	Write (received)	t_{SCH}	ns	40	-	-
	Read (transmitted)			150	-	-
Serial clock "Low" level pulse width	Write (received)	t_{SCL}	ns	40	-	-
	Read (transmitted)			150	-	-
Serial clock rise/fall time		t_{scr}, t_{scf}	ns	-	-	20
Chip select setup time		t_{CSU}	ns	20	-	-
Chip select hold time		t_{CH}	ns	60	-	-
Serial input data setup time		t_{SISU}	ns	30	-	-
Serial input data hold time		t_{SIH}	ns	30	-	-
Serial output data setup time		t_{SOD}	ns	-	-	100
Serial output data hold time		t_{SOH}	ns	5	-	-

Reset Timing Characteristics

Table 78 (Condition: IOVcc = 1.65 to 3.30V,Vcc = 2.50 to 3.30V, VDD = 1.7 to 1.9V)

Item	Symbol	Unit	Min	Typ	Max
Reset "Low" level width	t_{RES}	ms	1	-	-
Reset rise time	t_{rRES}	us	-	-	10

RGB Interface Timing Characteristics

Table 79 (18/16-bit I/F, IOVcc = 1.65 to 3.30V, Vcc = 2.50 to 3.30V, VDD = 1.7 to 1.9V)

Item	Symbol	Unit	Min	Typ	Max
VSYNC/HSYNC setup time	tSYNCS	ns	0		
ENABLE setup time	tENS	ns	10		
ENABLE hold time	tENH	ns	20		
DOTCLK “Low” level pulse width	PW_{DL}	ns	40		
DOTCLK “High” level pulse width	PW_{DH}	ns	40		
DOTCLK cycle time	tCYCD	ns	100		
Data setup time	tPDS	ns	10		
Date hold time	tPDH	ns	40		
DOTCLK, VSYNC, HSYNC rise/fall time	trgbr, trgbf	ns			25

Table 80 (6-bit I/F, IOVcc = 1.65 to 3.30V, Vcc = 2.50 to 3.30V, VDD = 1.7 to 1.9V)

Item	Symbol	Unit	Min	Typ	Max
VSYNC/HSYNC setup time	tSYNCS	ns	0		
ENABLE setup time	tENS	ns	10		
ENABLE hold time	tENH	ns	20		
DOTCLK “Low” level pulse width	PW_{DL}	ns	30		
DOTCLK “High” level pulse width	PW_{DH}	ns	30		
DOTCLK cycle time	tCYCD	ns	100		
Data setup time	tPDS	ns	10		
Date hold time	tPDH	ns	40		
DOTCLK, VSYNC, HSYNC rise/fall time	trgbr, trgbf	ns			25

Notes to Electrical Characteristics

1. The DC/AC electrical characteristics of bare die and wafer products are guaranteed at 85°C.
2. The following are the configurations of I pin, I/O pin, and O pin.

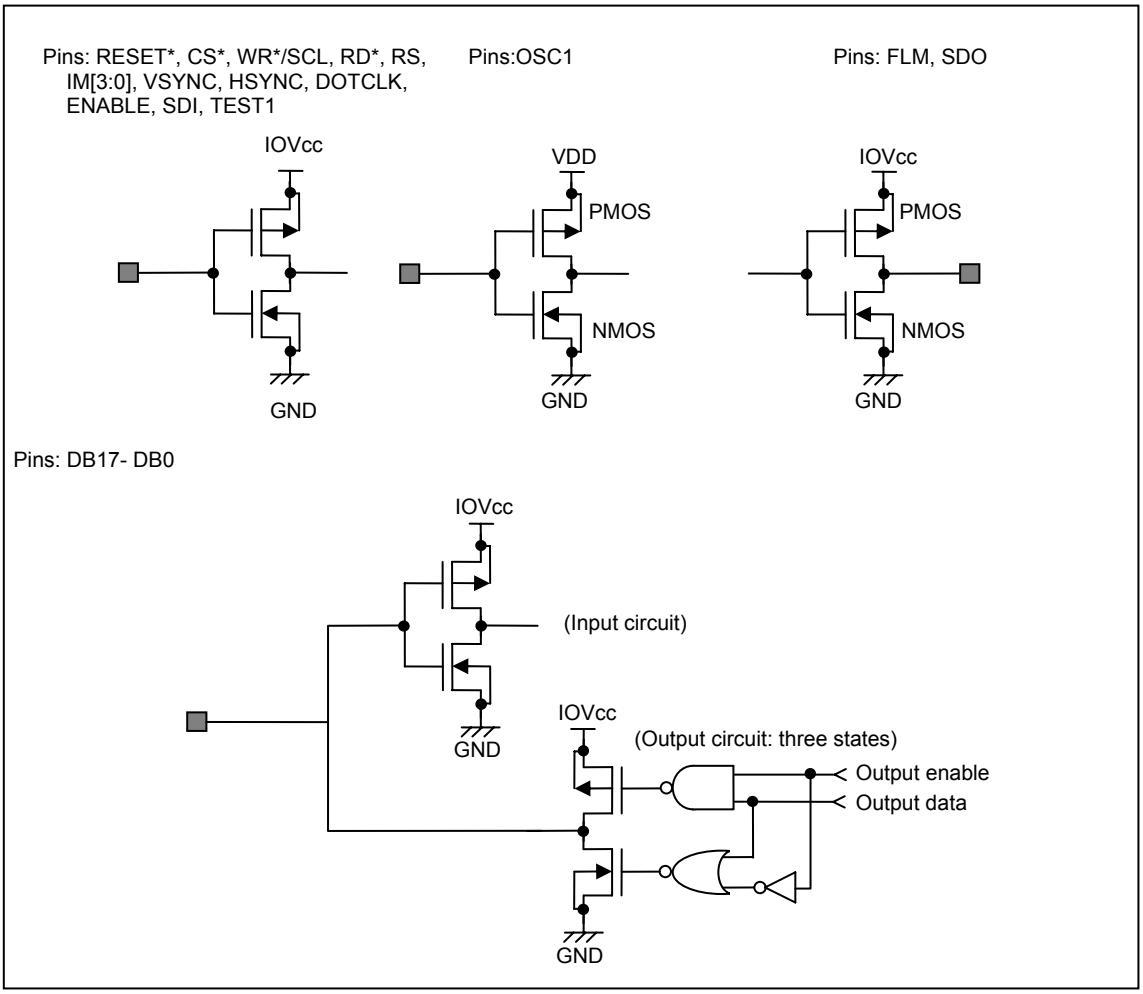


Figure 76

3. The TEST1 pin must be grounded (GND). The IM[3:0] pins must be fixed at either GND or the IOVcc level.
4. This excludes current though the output drive MOS.
5. This excludes current flowing through input/output units. Be sure that input levels are fixed to prevent increase in the transient current in input units when a CMOS input level takes medium range. While not accessing via interface pins, current consumption will not change whether the CS* pin is set to “High” or “Low”.
6. This is the case when an external oscillation resistor Rf is used.

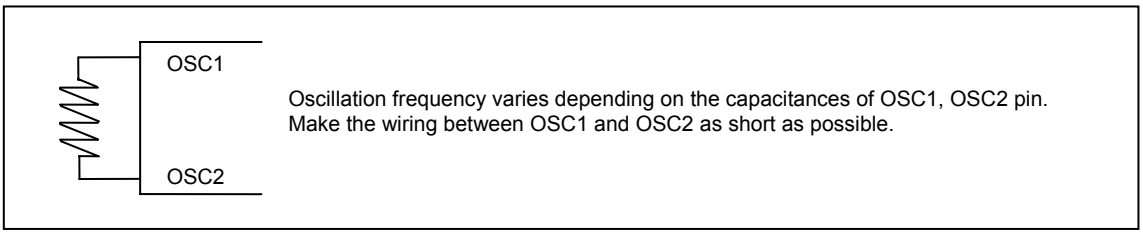


Figure 77

Table 81: Reference Data, Ta=25°C

Oscillation Resistance (kΩ)	RC Oscillation Frequency: fosc (kHz)
	@ VDD = 1.8V
24	2,150
27	1,940
30	1,760
33	1,620
36	1,490
39	1,390
43	1,270
47	1,170
51	1,080
56	991
62	899
68	825
75	750
82	688
91	624
100	570
120	477
130	441
150	384
160	361
180	322

Timing Characteristics Diagram

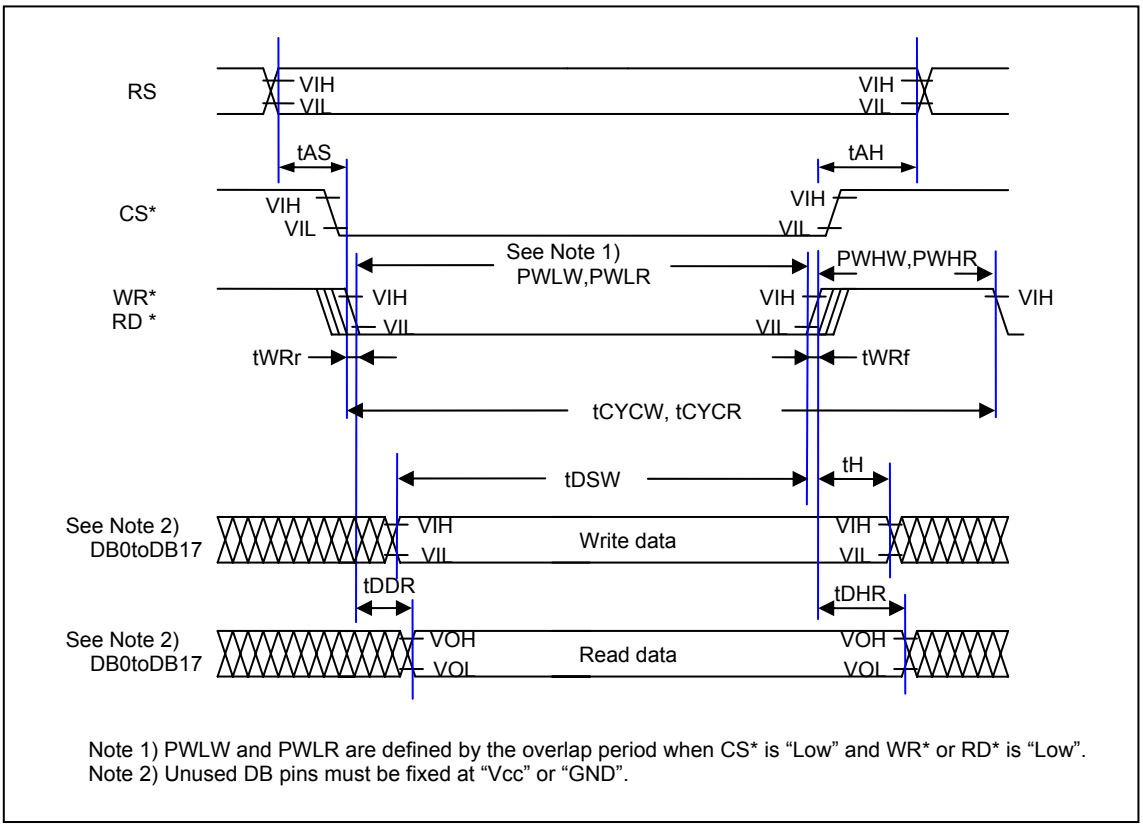


Figure 78: 80-system bus interface operation

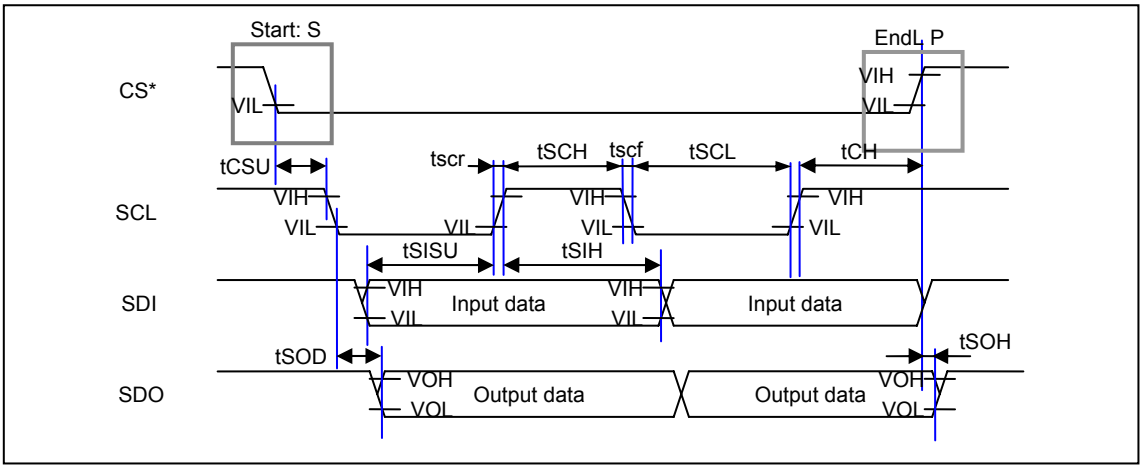


Figure 79: Serial peripheral interface operation

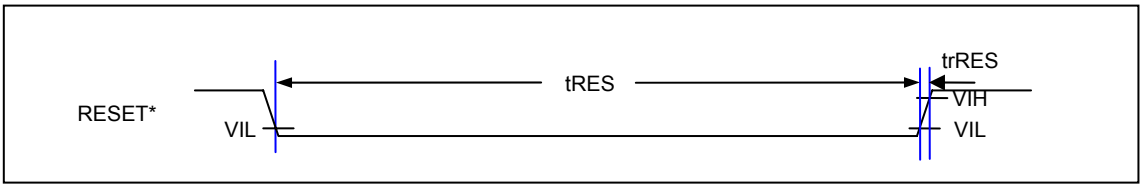


Figure 80: Reset operation

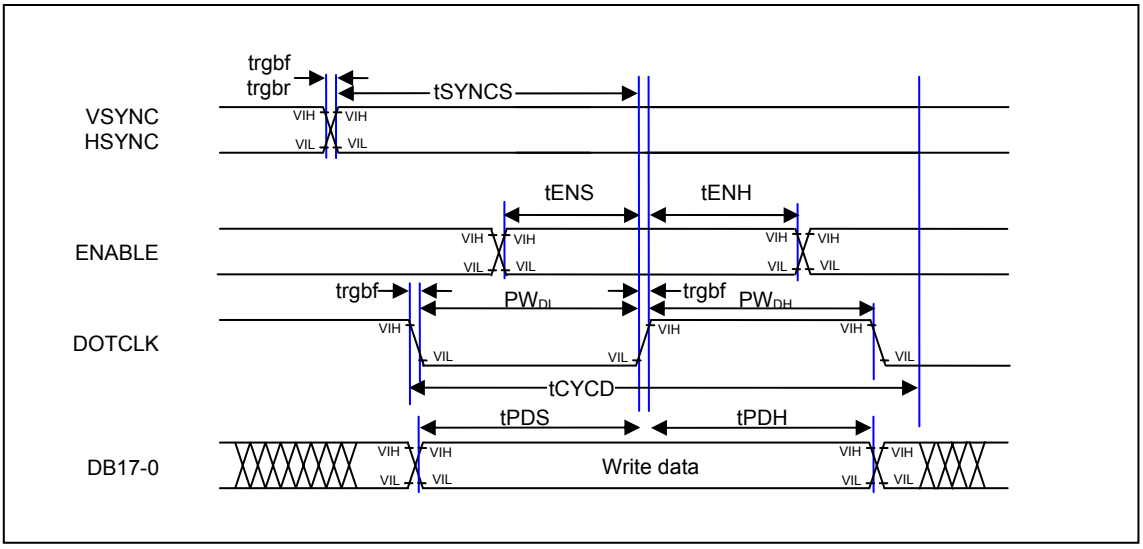


Figure 81 RGB interface