DATA SHEET

(DOC No. HX5116-A-DS)

HX5116-A

160CH Single Chip Driver for LTPS AMOLED

Preliminary version 03 July, 2007

Himax Technologies, Inc.
http://www.himax.com.tw

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1. General Description

HX5116-A is a timing controller and driver LSI that integrated the power circuit. It can drive the 320RGBx240, 320RGBx480, 480RGBx272, 480RGBx234 and 240RGBx400 graphics on LTPS AMOLED panel displays in 16,777,216 colors.
HX5116-A has a low-voltage operation, 1.5V min. In addition, HX5116-A is equipped with a DC-DC converter control circuit that generates the supply voltage for source and gate drivers with minimum external components. A common voltage generation circuit is included to drive the LTPS AMOLED display counter electrode. An integrated gamma control circuit is also included that can be adjusted by software commands to provide maximum flexibility and optimal display quality.

2. Features

- Single chip solution to drive an AMOLED panel.
- Panel resolution: QVGA 320RGBx240, QVGA+ 320RGBx480, WQVGA 480RGBx272, WQVGA- 480RGBx234, QVGA- 240RGBx400
- Input: 8-bit serial RGB, 24-bit parallel RGB, 8-bit RGBDummy, CCIR601 and CCIR656 input interface.
- Support NTSC and PAL mode.
- Support SYNC mode and DE mode.
- Support delta and stripe types of color arrange.
- 3-wire (SPI) register control for display and function selection.
- 8-bit resolution 256 gray scales with 8-bit DAC.
- Three independent adjustable gammas for RGB color outputs.
- Build-in contrast, brightness and gamma modulation.
- Build-in DC-DC charge pump circuits :
  - VDDD/VCI1OUT/DDVDH/VGH/VGL/ARREF
- Build-in OTP (one-time programming) memory for initial register setting (for gamma adjustment)
- Output: 160 channels (MUX6:1 for QVGA/QVGA+,MUX 9:1 for WQVGA/WQVGA-)
  120 channels (MUX 6:1 for QVGA-)
- Support power saving mode
- Digital power VCC : 1.5V~3.6V
- Analog power VCI : 2.7V~3.6V
- COG package

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3. Block Diagram

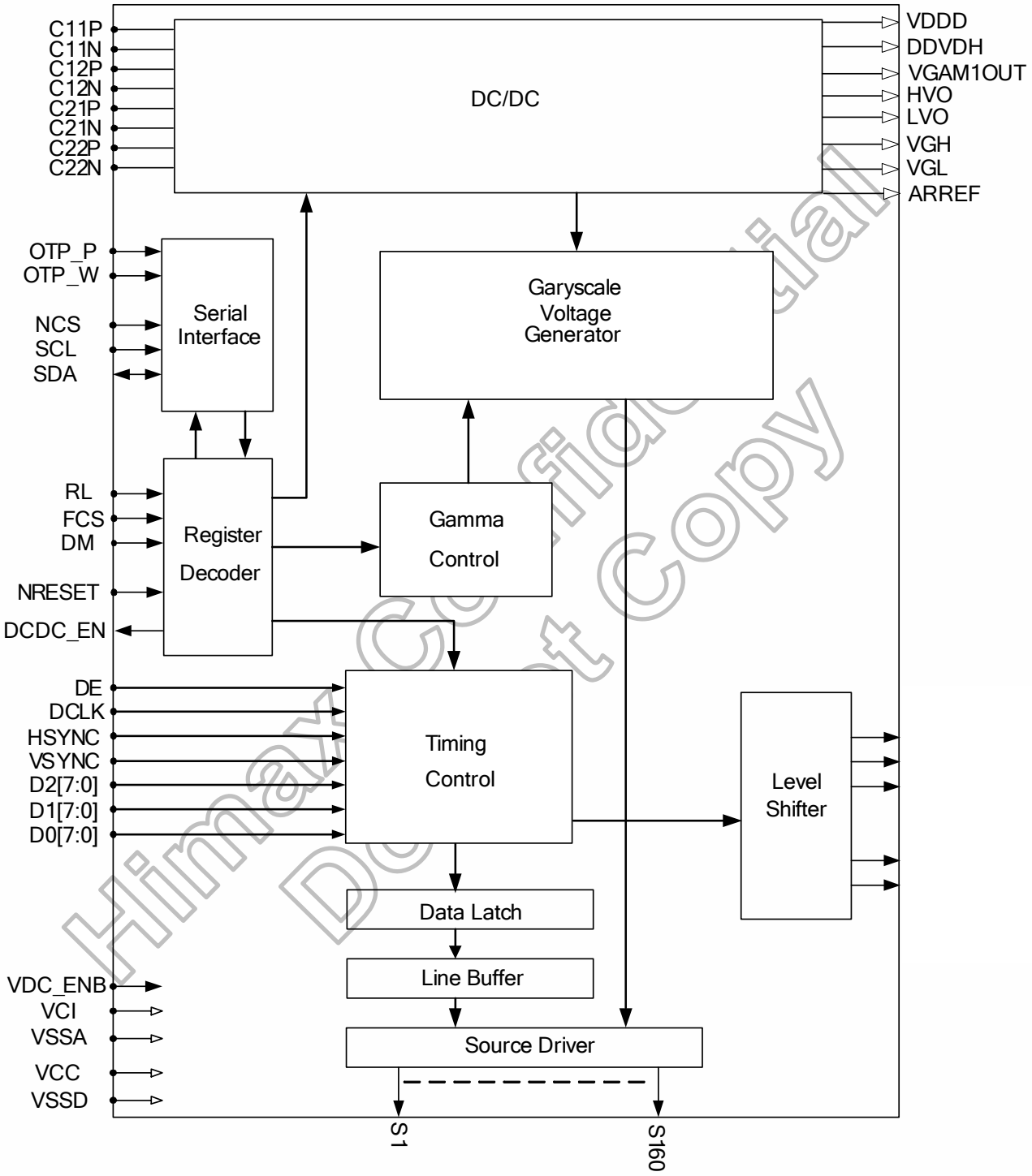


Figure 3. 1 HX5116-A block diagram description

4. Pin Description

Input Parts			
Signals	**I/O**	**Connected with**	**Description**
VSYNC	I	MPU	Frame synchronizing signal. If VSPL=0: Active low. If VSPL=1: Active high.
HSYNC	I	MPU	Line synchronizing signal. If HSPL=0: Active low. If HSPL=1: Active high.
DCLK	I	MPU	Dot clock signal. If DPL=0: Data are input on the rising edge of DOTCLK. If DPL=1: Data are input on the falling edge of DOTCLK.
DE	I	MPU	Data enable: When VSYNC+HSYNC+DE mode, DE=H: Data enable, DE=L: Data disable (Black). **(Normally pull low)**
D27 ~ D20 D17 ~ D10 D07 ~ D00	I	MPU	Digital data input. DX0 is LSB and DX7 is MSB. **(Normally pull low)** 1. If parallel RGB input mode is used, D0X, D1X, and D2X indicate R, G, and B data in turn. 2. If serial RGB or RGBD or CCIR601 or CCIR656 input mode is selected, only D07~D00 are used, and others short to GND. DX7~DX0 has 8-bit width, respectively to compose 16,777,216 color and 256 gray scale of 1 pixel.
NRESET	I	MPU	Reset pin. Setting either pin low initializes the LSI. Must be reset after power is supplied. **(Normally pull high)**
DM	I	MPU	Display mode setting pins **(Normally pull low)** Normal display mode and Stand by mode. If DM=0: Stand by mode. If DM=1: Normal display mode.
FCS	I	MPU	This pin can select control signal. (RL, DM) **(Normally pull high)** FCS=H: IC accepts the values of internal register. FCS=L: IC accepts the value of external input pads.
RL	I	MPU	This pin can select shift direction of source output. **(Normally pull high)** RL=H: S1 (1st data) → S160 RL=L: S160 (1st data) → S1
OTP_W	I	MPU	When OTP_W =L, writing/programming OTP memory disable. (Normal operation) **(Normally pull low)** When OTP_W =H, writing/programming OTP memory enable.
SCL	I	MPU	Serial Interface clock input pin. **(Normally pull high)**
NCS	I	MPU	Serial Interface chip enable pin. **(Normally pull high)**
SDA	I/O	MPU	Serial Interface data line. **(Normally pull high)**
VDC_ENB	I	Input pin	If VDC_ENB=0: VDC is Enable, VDDD is output; **(Normally pull low)** If VDC_ENB=1: VDC is Disable, VDDD is input.

Power Part			
Signals	**I/O**	**Connected with**	**Description**
VCI	P	Power supply	A power supply for the Analog circuit. (2.7V~3.6V)
VSSA	P	Power supply	Analog ground pin. It must connect to external ground.
VSSP	P	Power supply	Charge pump ground pin. It must connect to external ground.
VCC	P	Power supply	A power supply for the Digital circuit. (1.5V~3.6V)
VSSD	P	Power supply	Digital ground pin. It must connect to external ground.
OTP_P	P	Power supply	Voltage applied during OTP programming. (7.5V)
VDDD	I/O	Capacitor	Internal logic voltage input or output pin VDC_ENB=0, VDDD is output, please connect to 1uF capacitor. VDC0 / VDDD / Status: 0 / 1.8V / Normal display; 1 / 2.5V / OTP program VDC_ENB=1, VDDD is input. (Input range = 1.6V~2.75V)
DDVDH	I/O	Capacitor	Output voltage of the booster1. (5.1V/6.0V)
VGAM1OUT	I/O	Capacitor	Output voltage of the VGAM1OUT regulator and used positive power of source driver. (4.8V/5.8V)
HVO	I/O	Capacitor	Positive output voltage of the booster2. (8.5V)
LVO	I/O	Capacitor	Negative output voltage of the booster2. (-8.5V)
VGH	I/O	Capacitor	High Voltage output of regulator VGH or external input voltage. (+3V~+8V)
VGL	I/O	Capacitor	Low Voltage output of regulator VGL or external input voltage. (-3V~-8V)
ARREF	I/O	Capacitor	Panel refers voltage of the regulator ARREF or external input voltage. (-8V~+8V)
C11P, C11N C12P, C12N	I/O	Step-up Capacitor	Connect to the step-up circuit, 4capacitors according to the step-up factor. Leave this pin open if the internal step-up circuit is not used.
C21P, C21N C22P, C22N	I/O	Step-up Capacitor	Connect to the step-up circuit, 4capacitors according to the step-up factor. Leave this pin open if the internal step-up circuit is not used.

Other Part			
Signals	**I/O**	**Connected with**	**Description**
S1_DMY	O	-	S1 output test pin.
S160_DMY	O	-	S160 output test pin.
TESTS	O	-	These pins are test pin, and must be open.
TESTB	O	-	These pins are test pin, and must be open.
VMONI	O	-	These pins are test pin, and must be open.
VTESTOUT	O	-	These pins are test pin, and must be open.
TESTO[3:0]	O	-	These pins are test pin, and must be open.

5. Function Description

5.1 Interface

5.1.1 Serial Interface

The HX5116-A offers 3-wire serial interface to display initialization setting and to selecting display function.

The clock synchronized serial peripheral interface (SPI) using the chip select line (NCS), serial transfer clock line (SCL), serial input/output data (SDA). The SPI read or write is decision by R/W bit. If the R/W control bit is high, the data byte D7~D0 will be read from HX5116-A. If it is low, the data byte D7~D0 will be a write to HX5116-A.

The HX5116-A starts serial data transfer at the falling edge of NCS input and it ends serial data transfer at the rising edge of NCS input. In serial bus interface, the data is transferred with the MSB first. On write mode, it needs to input 16 valid data to SPA. Under 16 or over 16 data, HX5116-A will judge as invalid data and ignore this command.

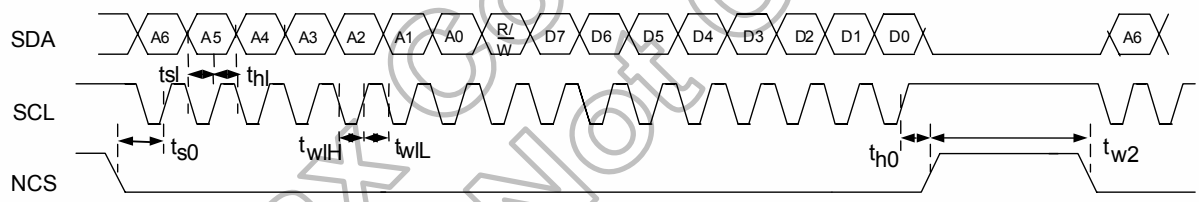


Figure 5. 1 3 wire SPI Timing

Parameter	Symbol	Min.	Typ.	Max.	Unit
Time from NCS to SCL	Ts0	40	-	-	ns
Time from SCL to NCS	Th0	60	-	-	ns
SCL low time	TwlH	-	Tcyc/2	-	ns
SCL high time	TwlL	-	Tcyc/2	-	ns
Setup time of SDI	Tsl	40	-	-	ns
Hold time of SDI	Thl	40	-	-	ns
NCS high pulse width	Tw2	500			ns
Serial Clock Cycle Time	Tcyc	100	500	-	ns

Table 5. 1 SPI timing diagram

5.1.2 Data Interface

The HX5116-A supports several kinds of data interface. It can selected 8-bit serial RGB, 24-bit parallel RGB, 8-bit RGBDummy, CCIR601 or CCIR656 data input by register IFS[3:0] setting.

IFS[3:0]	Interface Format Select
0000	8-bit serial RGB (SYNC)
0001	8-bit serial RGB (DE)
0010	24-bit parallel RGB (SYNC)
0011	24-bit parallel RGB (DE)
0100	8-bit RGBDummy 24.54MHz
0101	8-bit RGBDummy 27MHz
0110	CCIR601 mode A 24.54MHz
0111	CCIR601 mode B 24.54MHz
1000	CCIR601 mode A 27MHz
1001	CCIR601 mode B 27MHz
1010	CCIR656 mode A 27MHz
1011	CCIR656 mode B 27MHz

Table 5. 2 Data Interface Format Select

For digital RGB input data format, both SYNC mode and DE mode are supported. When DE mode selected, display operations is executed in synchronization with the frame synchronizing signal (VSYNC), line synchronizing signal (HSYNC) and dot clock (DCLK). The display data are transferred in pixel unit via Data bus(D27~D20、D17~D10、D07~D00) and according to the signal of data enable(DE). When SYNC mode is selected, display operations is executed in synchronization with only VSYNC, HSYNC and DCLK.

5.2 Delta or Stripe Color Arrange

The HX5116-A supports the Delta or Stripe types color filter. It can be selected by register SW[1:0].

5.2.1 Delta color arrange types

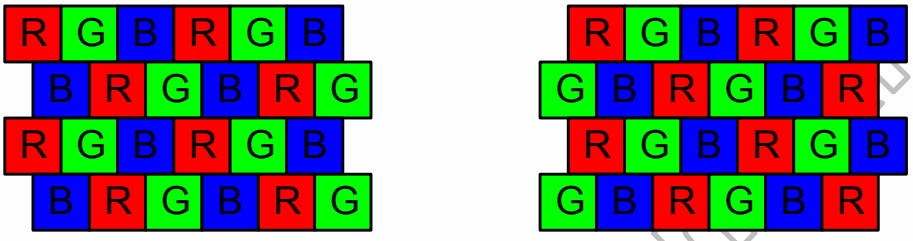


Figure 5. 2 Supported two types of delta color arrange

5.2.2 Stripe color arrange types

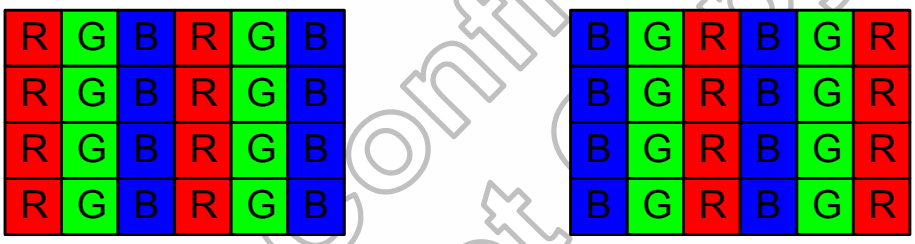


Figure 5. 3 Supported two types of stripe color arrange

SW1	SW0	Color arrange
0	0	Delta RGB/BRG
0	1	Delta RGB/GBR
1	0	Stripe RGB
1	1	Stripe BGR

Table 5. 3 Color arrange type Select

5.3 Input sequence

5.3.1 Data input sequence

HX5116-A supports serial RGB、parallel RGB、RGBD、CCIR601 and CCIR656 input data formats. When serial RGB data format, the data sequence is decided by RL setting, and others data format does not.

IFS[3:0]	SW[1:0]	Odd/Even line	RL=H	RL=L	Note
0000 0001	00	odd	RGB	BGR	Input sequence = color arrange
		even	BRG	GRB	
	01	odd	RGB	BGR	
		even	GBR	RBG	
	10	Odd/Even	RGB	BGR	
	11	Odd/Even	BRG	RGB	
0010 0011	00 01 10 11	Odd/Even	RGB		Input sequence is fixed
0100 0101		Odd/Even	RGBD		
0110 0111 1000 1001		Odd/Even	Cb,Y,Cr,Y…		
1010 1011		Odd/Even	Cb,Y,Cr,Y…		

Table 5. 4 Input data sequence vs. Interface Format

5.4 Display function

5.4.1 Resolution setting

HX5116-A supports QVGA、QVGA+、WQVGA、WQVGA- resolutions. Each resolution can be supported by different interface format. Each resolution displays on different source channels. Please reference to following table.

Resolution		SD CH	Bank	Interface	NTSC/PAL
QVGA	320x240	160ch	1:6	S-RGB/P-RGB/RGBD/ CCIR601/CCIR656	Yes
WQVGA-	480x234	160ch	1:9	S-RGB/P-RGB/ CCIR601/CCIR656	Yes
WQVGA	480x272	160ch	1:9	S-RGB/P-RGB	No
QVGA+	320x480	160ch	1:6	S-RGB/P-RGB	No
QVGA-	240x400	120ch	1:6	S-RGB/P-RGB	No

5.4.2 Display Mode Setting

The HX5116-A output display sequence can set by external input pin (RL) or internal register DISPLAY_MODE3(0x05). When FCS=L, we can set RL input pin to select output scan sequence. If FCS=H, the register DISPLAY_MODE3(0x05) will decision output scan sequence.

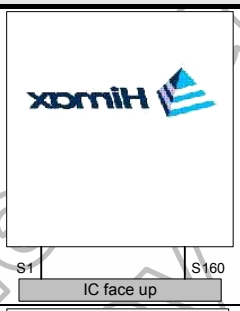
RL / DISPLAY_MODE2(0x05) [0]	Scan direction
0	
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Figure 5. 4 SCAN Mode Setting

5.4.3 Relationship between input data and output channels

The relationship between input data and output channels depends on the resolution and scan sequence setting. User can reference to the following table to find out them. The data of the table is meaning the dot data, or divide 3 as the pixel data.

Resolution	CH	Bank	RL	S1	S2	…	S60	S61	…	S100	S101	…	S159	S160
QVGA 320x240 QVGA+ 320x480	160ch	6	H	D1~ D6	D7~ D12	→	D355~ D360	D361~ D366	→	D595~ D600	D601~ D606	→	D948~ D954	D955~ D960
			L	D955~ D960	D948~ D954	←	D601~ D606	D595~ D600	←	D361~ D366	D355~ D360	←	D7~ D12	D1~ D6
WQVGA 480x272 WQVGA- 480x234	160ch	9	H	D1~ D9	D10~ D18	→	D532~ D540	D541~ D549	→	D892~ D900	D901~ D909	→	D1423~ D1431	D1432~ D1440
			L	D1432~ D1440	D1423~ D1431	←	D901~ D909	D892~ D900	←	D541~ D549	D532~ D540	←	D10~ D18	D1~ D9
QVGA- 240x400	120ch	6	H	D1~ D6	D7~ D12	→	D355~ D360	x	x	x	D361~ D366	→	D709~ D714	D715~ D720
			L	D715~ D720	D709~ D714	←	D361~ D366	x	x	x	D355~ D360	←	D7~ D12	D1~ D6

Table 5. 5 Relationship between input and output channels

5.5 Data Transfer Format

YUV_601/656 to RGB conversion :

Y = 0.257*R + 0.504*G + 0.098*B + 16
Cb(U) = -0.148*R – 0.291*G + 0.439*B + 128
Cr(V) = 0.439*R – 0.368*G – 0.071*B + 128

R = 1.164*(Y-16) + 1.596*(Cr -128)
G = 1.164*(Y-16) - 0.813*(Cr -128) - 0.392*(Cb -128);
B = 1.164*(Y-16) + 2.017*(Cb-128)

Note : Y= 16~235, Cr/Cb=16~240

5.6 Gamma/Grayscale Voltage Generator

The HX5116-A incorporates gamma adjustment function for the 16,777,216-color display (256 grayscale for each R, G, B color). Gamma adjustment operation is implemented by deciding the 8 grayscale levels firstly in gamma adjustment control registers to match the AMOLED panel. Then total 256 grayscale levels are generated in grayscale voltage generator. These registers are available for both polarities.

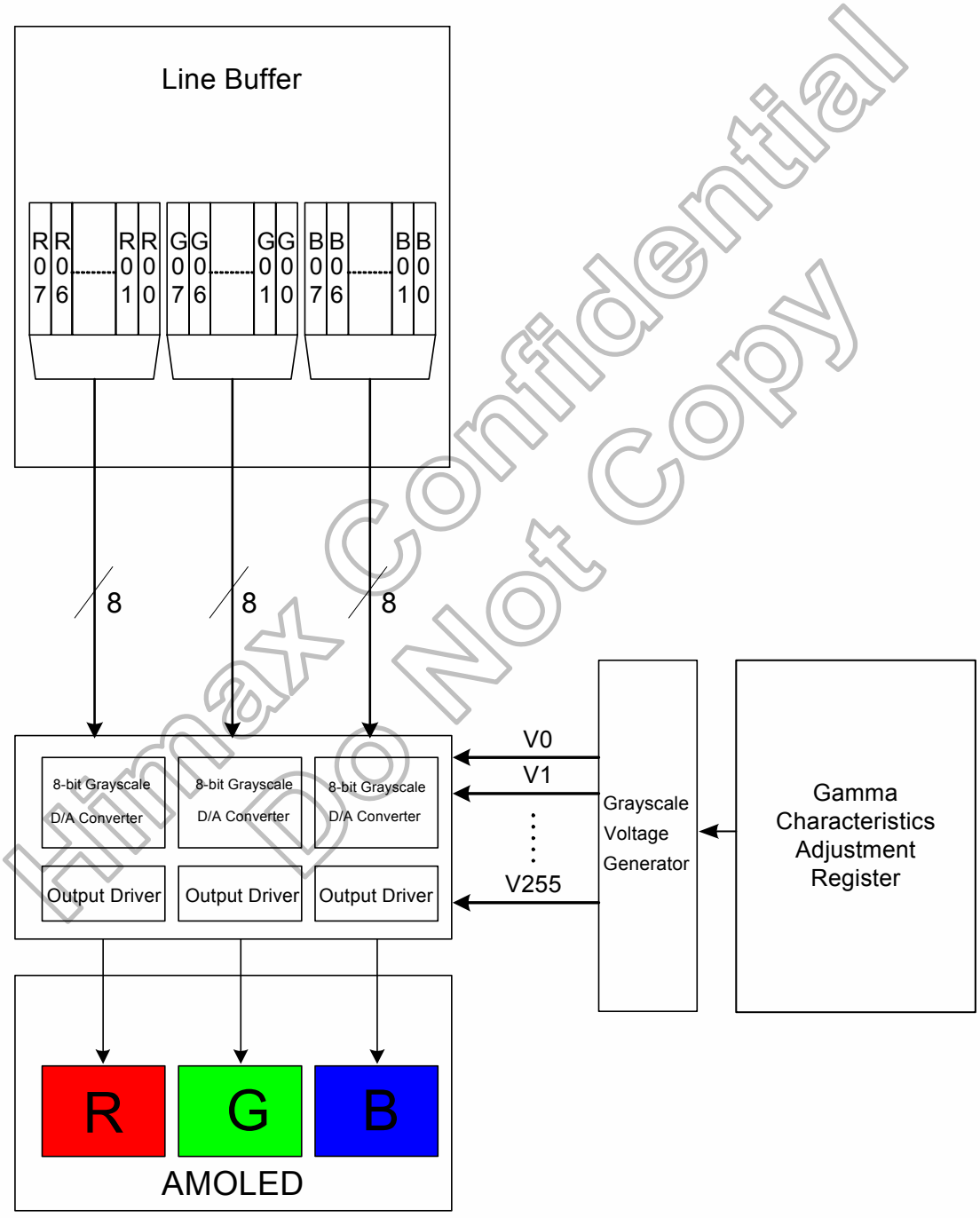


Figure 5. 5 Gamma/Grayscale Voltage Generator

5.6.3 Structure of Grayscale Voltage Generator

Ten reference gamma voltages (V0, V10, V36, V80, V124, V168, V212, V255) are specified by the center adjustment, the micro adjustment and the offset adjustment registers firstly. With those eight voltage injected into specified node of grayscale voltage generator, total 256 grayscale voltages (V0-V255) can be generated from grayscale amplifier for AMOLED panel used.

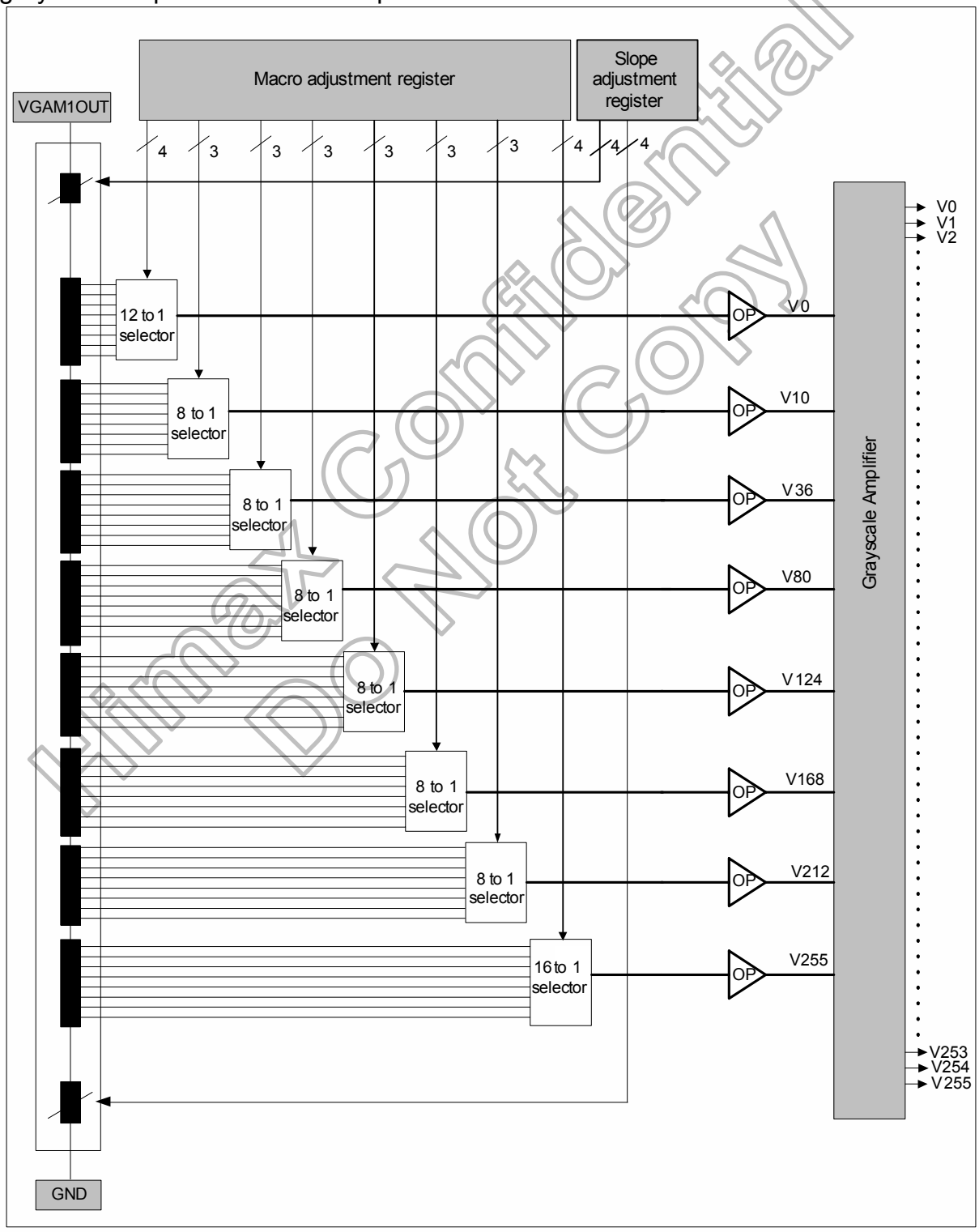


Figure 5. 6 Structure of Grayscale Voltage Generator

5.6.4 Gamma-Characteristics Adjustment Register

This HX5116-A has register groups for specifying a series grayscale voltage that meets the Gamma-characteristics for the AMOLED panel used. These registers are divided into two groups, which correspond to the gradient, amplitude, and macro adjustment of the voltage for the grayscale characteristics.

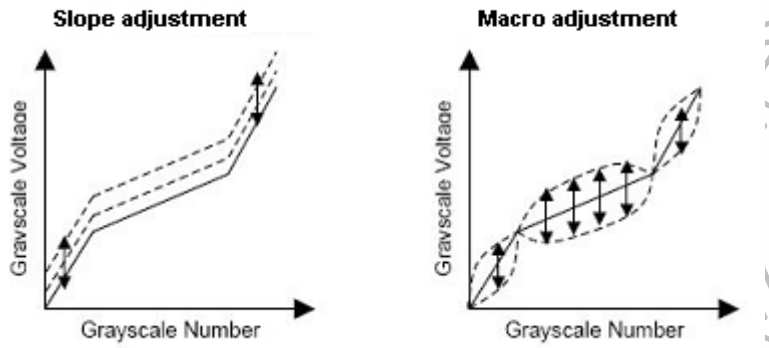


Figure 5. 7 Gamma-Characteristics Adjustment function

5.6.4.1 Slope adjustment registers

The slope adjustment variable registers are used to adjust the amplitude of the grayscale voltage. This function is implemented by controlling these variable resisters in the top and bottom of the gamma resister stream for reference gamma voltage generation.

5.6.4.2 Macro adjustment registers

The gamma macro adjustment registers can be used for fine adjustment of the reference gamma voltage. This function is implemented by controlling the N-to-1 selectors (Gamma0[3:0], Gamma10[2:0], Gamma36[2:0], Gamma80[2:0], Gamma124[2:0], Gamma168[2:0], Gamma212[2:0] , Gamma255[3:0]), each of which has N inputs and generate one reference voltage output (V0, V10, V36, V80, V124, V168, V212, V255). These registers are available for both positive and negative polarities.

Register Groups	Register name	Description
Slope Adjustment	SLOPE1 3-0	Variable resistor for offset adjustment
	SLOPE2 3-0	Variable resistor for offset adjustment
Macro Adjustment	Gamma0 3-0	12-to-1 selector (voltage level of grayscale 0)
	Gamma10 2-0	8-to-1 selector (voltage level of grayscale 10)
	Gamma36 2-0	8-to-1 selector (voltage level of grayscale 36)
	Gamma80 2-0	8-to-1 selector (voltage level of grayscale 80)
	Gamma124 2-0	8-to-1 selector (voltage level of grayscale 124)
	Gamma168 2-0	8-to-1 selector (voltage level of grayscale 168)
	Gamma212 2-0	8-to-1 selector (voltage level of grayscale 212)
	Gamma255 3-0	16-to-1 selector (voltage level of grayscale 255)

Table 5. 6 Gamma-Adjustment Registers

5.6.4.3 Ladder Resistor

This block outputs the reference voltage of the grayscale voltage. There are one ladder resistors including the variable resistor, the N to 1 selector selecting voltage generated by the ladder resistor. The gamma registers control the variable resistors and N to 1 selector resistors.

5.6.4.4 Variable Resistor

There are 3 types of the variable resistors that are for the gradient and amplitude adjustment. The resistance is set by the register R_SLOPE1, G_SLOPE1 and B_SLOPE1 and R_SLOPE2, G_SLOPE2, B_SLOPE2 as below.

VGAM1OUT=5.8V (GAMV=1)				VGAM1OUT=4.8V (GAM1=0)			
Register X_SLOPE1[3:0]	R	G	B	Register X_SLOPE1[3:0]	R	G	B
0000	154R	154R	154R	0000	68R	68R	68R
0001	145R	145R	145R	0001	58R	58R	58R
0010	136R	136R	136R	0010	48R	48R	48R
0011	127R	127R	127R	0011	38R	38R	38R
0100	118R	118R	118R	0100	28R	28R	28R
0101	108R	108R	108R	0101	18R	18R	18R
0110	98R	98R	98R	0110	9R	9R	9R
0111	88R	88R	88R	0111	0R	0R	0R
1000	78R	78R	78R	1000	0R	0R	0R
1001	68R	68R	68R	1001	0R	0R	0R
1010	58R	58R	58R	1010	0R	0R	0R
1011	48R	48R	48R	1011	0R	0R	0R
1100	38R	38R	38R	1100	0R	0R	0R
1101	28R	28R	28R	1101	0R	0R	0R
1110	18R	18R	18R	1110	0R	0R	0R
1111	9R	9R	9R	1111	0R	0R	0R

Table 5. 7 SPOLE1 Register Select of VGAM1OUT – V0 (code0) Resistance

Register X_SLOPE2[3:0]	R	G	B
0000	0R	20.1R	1.5R
0001	9R	29.1R	10.5R
0010	18R	38.1R	19.5R
0011	27R	47.1R	28.5R
0100	37R	57.1R	38.5R
0101	47R	67.1R	48.5R
0110	57R	77.1R	58.5R
0111	67R	87.1R	68.5R
1000	77R	97.1R	78.5R
1001	87R	107.1R	88.5R
1010	97R	117.1R	98.5R
1011	117R	137.1R	118.5R
1100	157R	177.1R	158.5R
1101	177R	197.1R	178.5R
1110	197R	217.1R	198.5R
1111	217R	237.1R	218.5R

Table 5. 8 SPOLE2 Register Select of V255 (code15) – VSS Resistance

5.6.4.5 N to 1 selector

In the N to 1 selector, a reference voltage can be selected from the levels which are generated by the ladder resistors. There are eight types of reference voltage (V0, V10, V36, V80, V124, V168, V212, V255) and totally 76 divided voltages can be selected in one ladder resistor. Following figure explains the relationship between the micro adjusting register and the selecting voltage.

Reference Voltage								
Register GAMMAXXX[X:0]	Selected voltage							
	V0	V10	V36	V80	V124	V168	V212	V255
0000	KV1	KV13	KV21	KV29	KV37	KV45	KV53	KV61
0001	KV2	KV14	KV22	KV30	KV38	KV46	KV54	KV62
0010	KV3	KV15	KV23	KV31	KV39	KV47	KV55	KV63
0011	KV4	KV16	KV24	KV32	KV40	KV48	KV56	KV64
0100	KV5	KV17	KV25	KV33	KV41	KV49	KV57	KV65
0101	KV6	KV18	KV26	KV34	KV42	KV50	KV58	KV66
0110	KV7	KV19	KV27	KV35	KV43	KV51	KV59	KV67
1111	KV8	KV20	KV28	KV36	KV44	KV52	KV60	KV68
1000	KV9	-	-	-	-	-	-	KV69
1001	KV10	-	-	-	-	-	-	KV70
1010	KV11	-	-	-	-	-	-	KV71
1011	KV12	-	-	-	-	-	-	KV72
1100	-	-	-	-	-	-	-	KV73
1101	-	-	-	-	-	-	-	KV74
1110	-	-	-	-	-	-	-	KV75
1111	-	-	-	-	-	-	-	KV76
Step level	50mV	50mV	50mV	50mV	50mV	50mV	50mV	25mV

Table 5. 9 GAMMAXXX Register Select

Register GAMMAXXX[X:0]	Code		R	G	B
gamma0[3:0]	0000	KV1	5.0R	5.0R	5.0R
	0001	KV2	5.0R	5.0R	5.0R
	0010	KV3	5.0R	5.0R	5.0R
	0011	KV4	5.0R	5.0R	5.0R
	0100	KV5	5.0R	5.0R	5.0R
	0101	KV6	5.0R	5.0R	5.0R
	0110	KV7	5.0R	5.0R	5.0R
	0111	KV8	5.0R	5.0R	5.0R
	1000	KV9	5.0R	5.0R	5.0R
	1001	KV10	5.0R	5.0R	5.0R
	1010	KV11	5.0R	5.0R	5.0R
	1011	KV12	38.8R	33.7R	40.1R
gamma10[2:0]	000	KV13	5.0R	5.0R	5.0R
	001	KV14	5.0R	5.0R	5.0R
	010	KV15	5.0R	5.0R	5.0R
	011	KV16	5.0R	5.0R	5.0R
	100	KV17	5.0R	5.0R	5.0R
	101	KV18	5.0R	5.0R	5.0R
	110	KV19	5.0R	5.0R	5.0R
	111	KV20	27.7R	26.9R	26.1R

gamma36[2:0]	000	KV21	5.0R	5.0R	5.0R
	001	KV22	5.0R	5.0R	5.0R
	010	KV23	5.0R	5.0R	5.0R
	011	KV24	5.0R	5.0R	5.0R
	100	KV25	5.0R	5.0R	5.0R
	101	KV26	5.0R	5.0R	5.0R
	110	KV27	5.0R	5.0R	5.0R
	111	KV28	33.4R	27.7R	31.7R
gamma80[2:0]	000	KV29	5.0R	5.0R	5.0R
	001	KV30	5.0R	5.0R	5.0R
	010	KV31	5.0R	5.0R	5.0R
	011	KV32	5.0R	5.0R	5.0R
	100	KV33	5.0R	5.0R	5.0R
	101	KV34	5.0R	5.0R	5.0R
	110	KV35	5.0R	5.0R	5.0R
	111	KV36	16.1R	13.0R	15.3R
gamma124[2:0]	000	KV37	5.0R	5.0R	5.0R
	001	KV38	5.0R	5.0R	5.0R
	010	KV39	5.0R	5.0R	5.0R
	011	KV40	5.0R	5.0R	5.0R
	100	KV41	5.0R	5.0R	5.0R
	101	KV42	5.0R	5.0R	5.0R
	110	KV43	5.0R	5.0R	5.0R
	111	KV44	8.8R	5.7R	9.5R
gamma168[2:0]	000	KV45	5.0R	5.0R	5.0R
	001	KV46	5.0R	5.0R	5.0R
	010	KV47	5.0R	5.0R	5.0R
	011	KV48	5.0R	5.0R	5.0R
	100	KV49	5.0R	5.0R	5.0R
	101	KV50	5.0R	5.0R	5.0R
	110	KV51	5.0R	5.0R	5.0R
	111	KV52	5.1R	2.1R	4.3R
gamma212[2:0]	000	KV53	5.0R	5.0R	5.0R
	001	KV54	5.0R	5.0R	5.0R
	010	KV55	5.0R	5.0R	5.0R
	011	KV56	5.0R	5.0R	5.0R
	100	KV57	5.0R	5.0R	5.0R
	101	KV58	5.0R	5.0R	5.0R
	110	KV59	5.0R	5.0R	5.0R
	111	KV60	2.6R	3.3R	4.0R
gamma255[3:0]	0000	KV61	2.5R	2.5R	2.5R
	0001	KV62	2.5R	2.5R	2.5R
	0010	KV63	2.5R	2.5R	2.5R
	0011	KV64	2.5R	2.5R	2.5R
	0100	KV65	2.5R	2.5R	2.5R
	0101	KV66	2.5R	2.5R	2.5R
	0110	KV67	2.5R	2.5R	2.5R
	0111	KV68	2.5R	2.5R	2.5R
	1000	KV69	2.5R	2.5R	2.5R
	1001	KV70	2.5R	2.5R	2.5R
	1010	KV71	2.5R	2.5R	2.5R
	1011	KV72	2.5R	2.5R	2.5R
	1100	KV73	2.5R	2.5R	2.5R
	1101	KV74	2.5R	2.5R	2.5R
	1110	KV75	2.5R	2.5R	2.5R
	1111	KV76			
		Total	435.0R	414.9R	433.5R

5.7 Power Generation

5.7.1 Power circuit relationship

The voltage setting pattern diagram of the HX5116-A illustrates as following Figure. The outputs of DVDDH, VGAM1OUT, VGH, VGL, and ARREF are sensitive to the voltage drop that set from the idea setting voltage in virtue of current consumption.

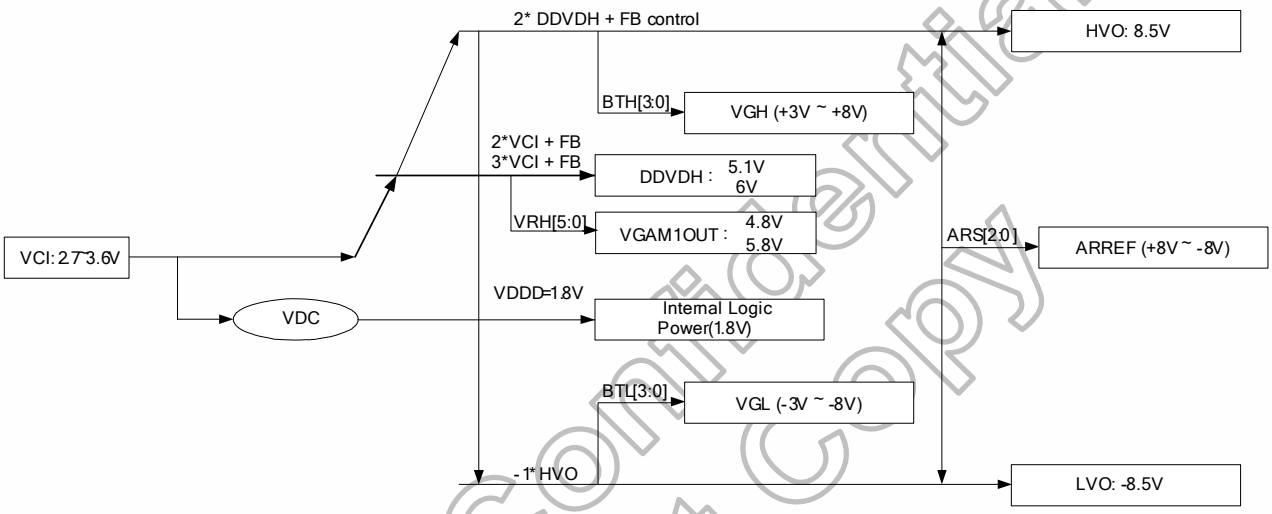


Figure 5. 8 Power relationship

5.7.2 Specification

The specification of power supply circuit and pins connection are shown as following table:

Pins connection	Recommended voltage	Capacity	Resistance of wire (Ω)
C11P/N, C12P/N, DDVDH	10V	1 μF	< 10
VGAM1OUT	10V	1 μF	< 15
C21P/N, C22P/N	10V	1 μF	< 10
HVO, LVO	16V	1 μF	< 10
VGH, VGL,ARREF	16V	1 μF	< 15
VDDD	10V	1uF	< 10
VCI, VSSD, VSSA, VSSP	-	-	< 5

Table 5. 10 Adoptability of Capacitor

Pins connection	Feature
VCI – HVO, VCI – DDVDH, LVO – VSSA	VF < 0.4V / 20mA at 25°C, VR ≥30V (Recommended diode: HSC226)

Table 5. 11 Adoptability of Schottkey diode

5.7.3 Power Circuit

The power circuit of HX5116-A presides over generating supply voltages to drive an OLED panel.

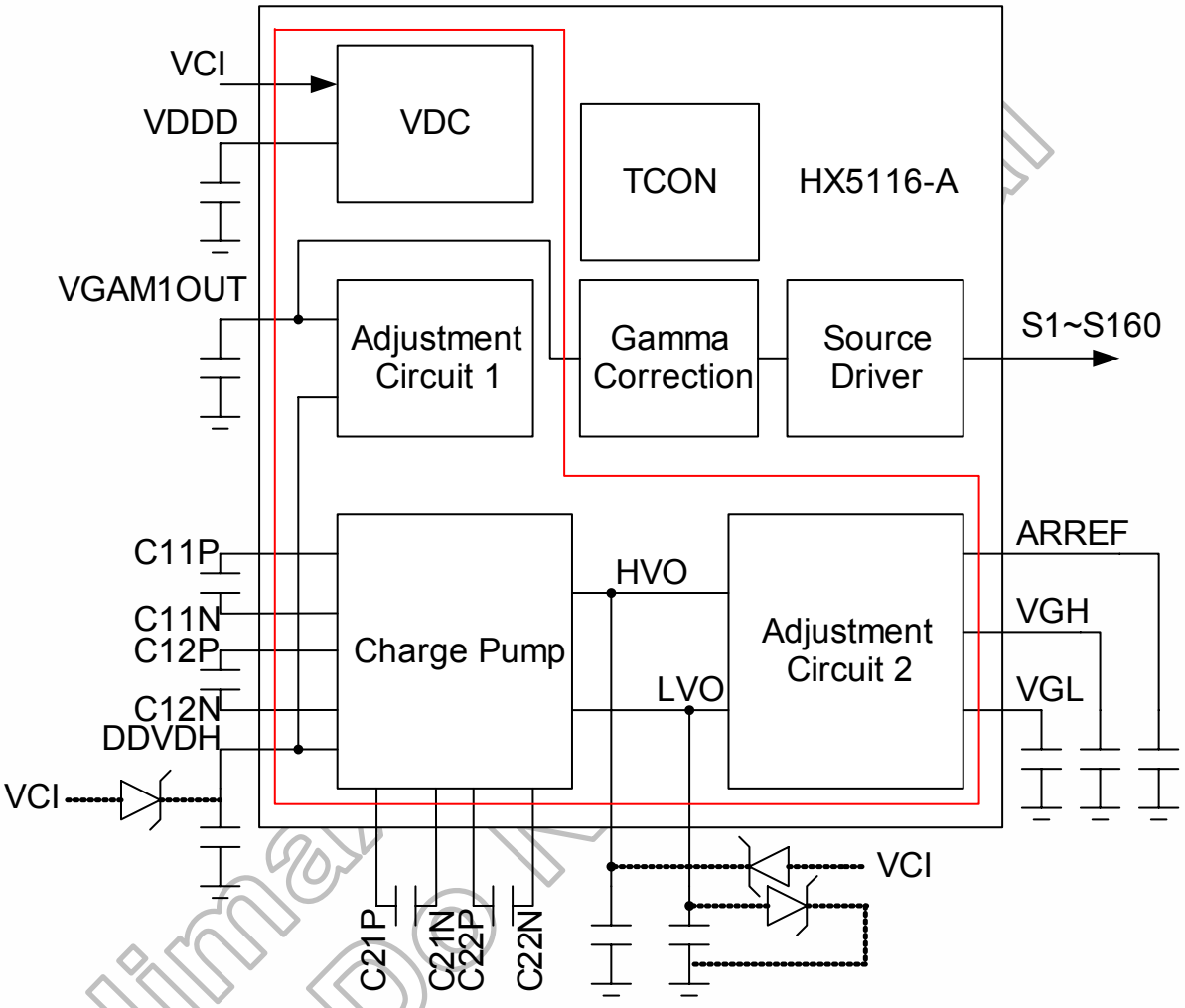


Figure 5. 9 Block Diagram of Power Circuit

5.8 Reset Circuit

This block is integrated into the Interface Logic which includes Power on Reset circuitry and the hardware reset pin, NRESET. Both of these having the same reset function. Once the NRESET pin receives a negative reset pulse, all internal circuitry will start to initialize and output pin will normal operating after the next VSYNC falling edge. The NRESET minimum pulse width for completing the reset sequence is 10us.

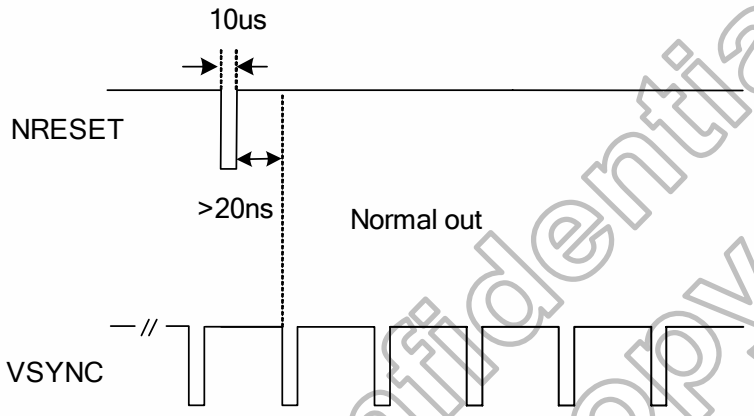


Figure 5. 10 RESET signal setting

5.9 Power on/off sequence

When power on/off HX5116-A, please follow the sequence:

Power ON: VCI/VCC -> NRESET -> Normal mode

Power OFF: Standby mode -> wait A+B stage -> power off VCI/VCC

Then HX5116-A will automatically power on/off the charge pump, source output and the gate signals like the following sequence. User can adjust the A stage, B stage, C stage by register POW_SEQ1(0x0C).

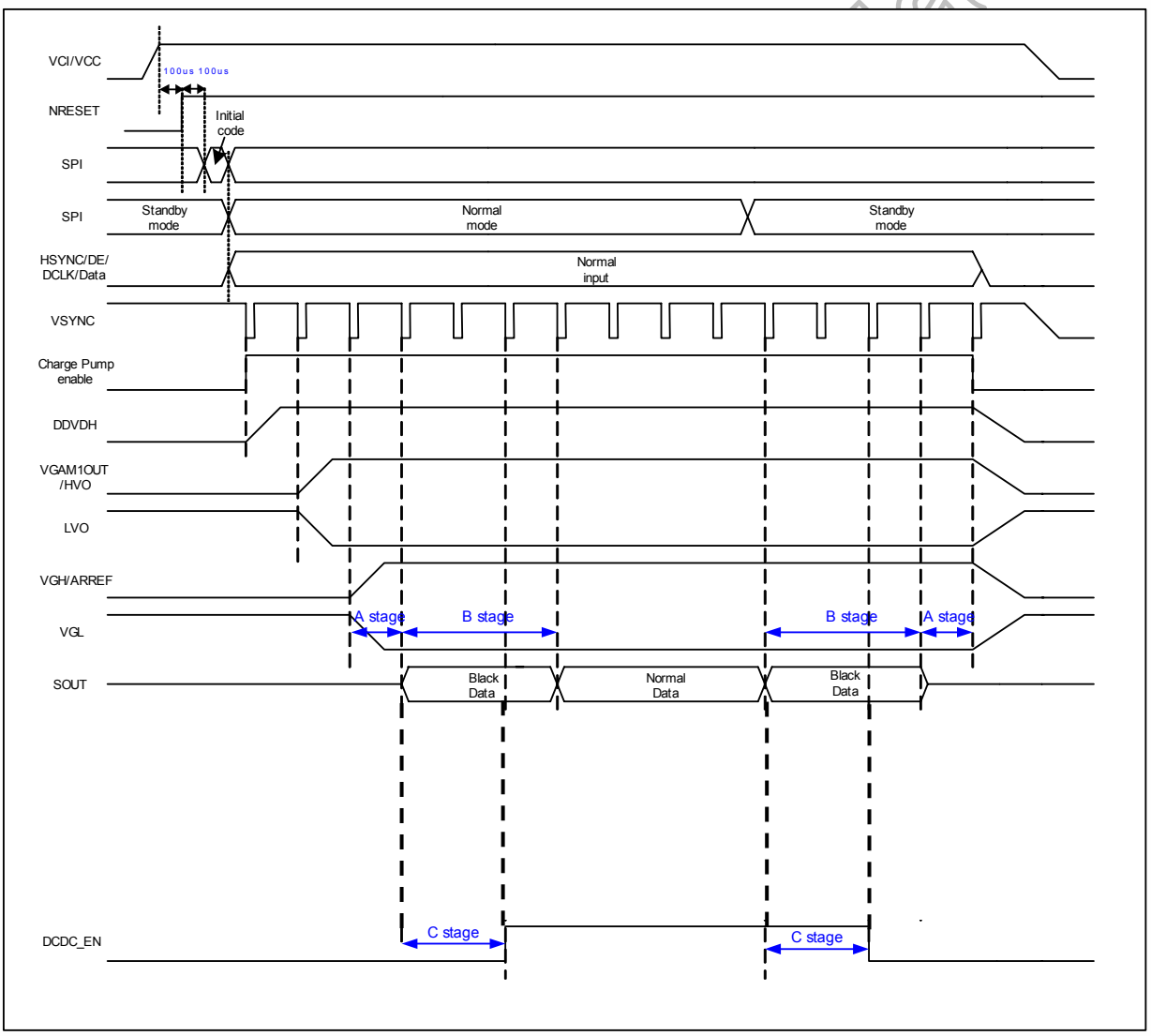


Figure 5. 11 Power (Standby) on/off sequence

If user want to control DCDC_EN by manual mode, please set register POW_SEQ2(0x0D) [3] to “1”, then user can control the DCDC_EN on/off by set register POW_SEQ1[2] (DCEN). The DCDC_EN polarity can be selected by register POW_SEQ[1].

Source output data in B stage can select black or white data for customer needed. Please set register POW_SEQ2[0] to choose the B stage data.

5.10 OTP function

The variation of EL characteristics may cause shifting of white point panel by panel. Here fore, OTP function is required in this IC to recover the EL process variations. In the following, we describe our requirement.

(1) At first, the VGAM1OUT must be precisely adjusted by OTP trimming.
(2) Then, we will use regular register to choose the best data for the RGB gamma slope. (OTP_W = L, OTP_ENABLE register = 01)
(3) Next, let OTP_W = H and write the best data (from step 2) for the RGB gamma slope to OTP through SPI.
(4) For normal operation (OTP_W = L), the values of RGB gamma slopes are read from OTP memory data (OTP_ENABLE register = 11).

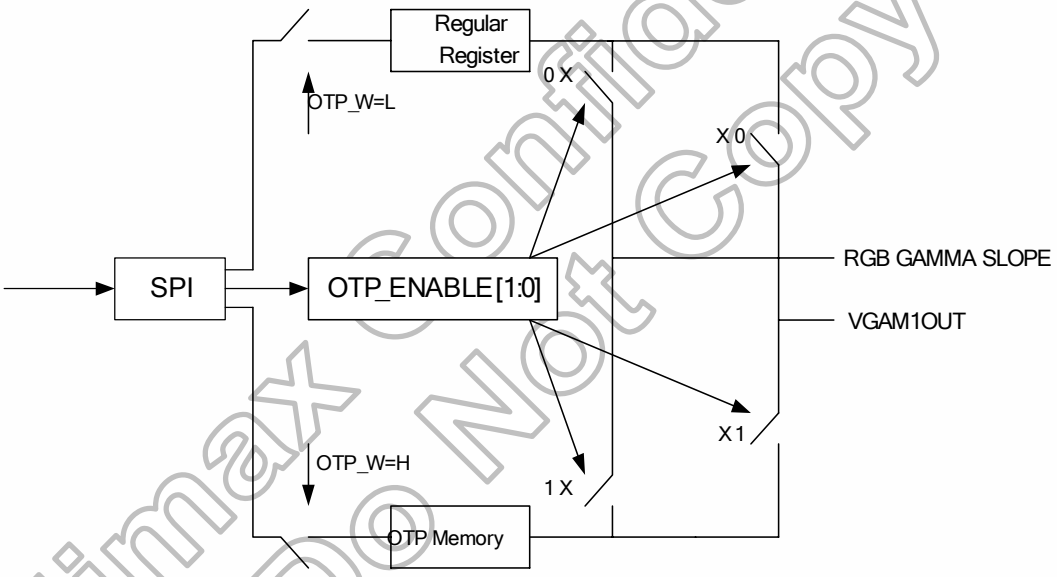


Figure 5. 12 Block diagram of OTP Function

5.10.1 OTP Programming

The HX5116-A OTP memory can write one time data by SPI interface.

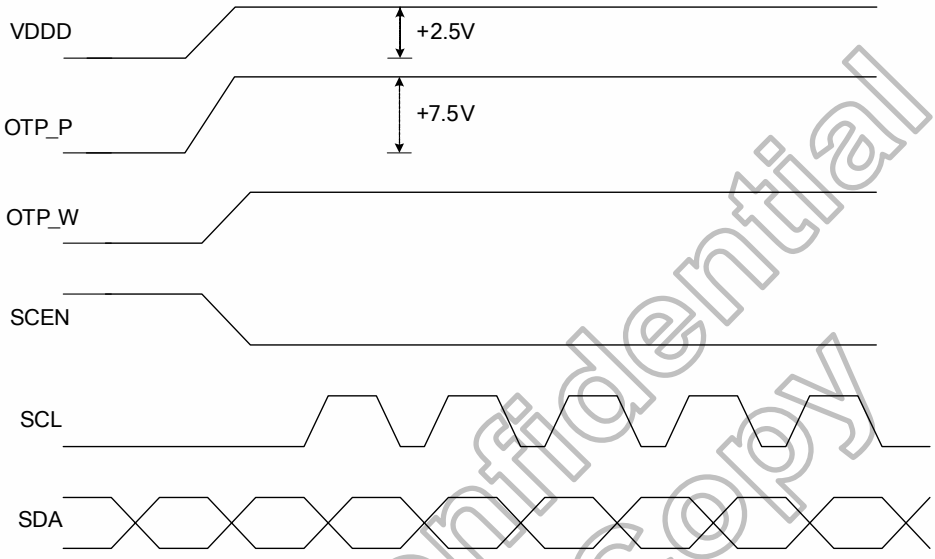


Figure 5. 13 OTP programming timing

6. Command Table

Display function control register				
Register Address	**Register name**	**Default**	**Read/Write**	**Description**
0x01	CHIP_ID0x	00	R	**[7:4]: Chip ID** **[3:0]: Chip version**
0x02	OTP_ENABLE	0x00	R/W	**[1]: RGB GAMMA SLOPEs** 0: Read from input regular register setting **(default)** 1: Read from OTP memory **[0]: VGAM1OUT_LEVEL** 0: Read from input regular register setting **(default)** 1: Read from OTP memory
0x03	DISPLAY_ MODE1	0x02	R/W	**[3]: VSYNC polarity** 0: Low pulse **(default)** 1: High pulse **[2]: HSYNC polarity** 0: Low pulse **(default)** 1: High pulse **[1]: DE polarity** 0: Low pulse 1: High pulse **(default)** **[0]: Input clock latch data edge** 0: Positive edge **(default)** 1: Negative edge
0x04	DISPLAY_ MODE2	0x01	R/W	**[6:4]: RESL[2:0]** Resolution select **RESL[2:0]** / **Resolution** 000 QVGA 320RGBx240 **(default)** 001 WQVGA- 480RGBx234 010 WQVGA 480RGBx272 011 QVGA+ 320RGBx480 100 QVGA- 240RGBx400 **[3:0]: IFS3-0** Input Data Format select **IFS[3:0]** / **Interface Format Select** 0000 8-bit serial RGB (SYNC) 0001 8-bit serial RGB (DE) **(default)** 0010 24-bit parallel RGB (SYNC) 0011 24-bit parallel RGB (DE) 0100 8-bit RGBDummy 24.54MHz 0101 8-bit RGBDummy 27MHz 0110 CCIR601 mode A 24.54MHz 0111 CCIR601 mode B 24.54MHz 1000 CCIR601 mode A 27MHz 1001 CCIR601 mode B 27MHz 1010 CCIR656 mode A 27MHz 1011 CCIR656 mode B 27MHz

<table>
<tr>
<td>0x05</td>
<td>DISPLAY_MODE3</td>
<td>0x42</td>
<td>R/W</td>
<td>
[7:6]: SW[1:0] Resolution select
<table>
<tr><th>SW[1:0]</th><th>Color arrange</th></tr>
<tr><td>00</td><td>Delta RGB/BRG</td></tr>
<tr><td>01</td><td>Delta RGB/GBR (default)</td></tr>
<tr><td>10</td><td>Stripe RGB</td></tr>
<tr><td>11</td><td>Stripe BGR</td></tr>
</table>
[5]: NTSC/PAL selection
0: NTSC mode (default)
1: PAL mode
[4]: PAL mode selection (only available when PAL mode)
0: Input data format is PAL 1/6,8 (280 active line) (default)
1: Input data format is PAL 1/6 (288 active line)
[1]: Horizontal Reverse (SS): (when FCS=H)
0: source output is in ascending order S160 → S1
1: source output is in descending order S1 →S160 (default)
</td>
</tr>
</table>

<table>
<tr><th colspan="5">Power control register</th></tr>
<tr><th>Register Address</th><th>Register name</th><th>Default</th><th>Read/Write</th><th>Description</th></tr>
<tr><td>0x06</td><td>POWER_CTRL1</td><td>0x02</td><td>R/W</td><td>[2]: Reserved (set default value = 0)

[1]: Globe reset
0: reset the whole chip.
1: normal operation. (default)

[0]: Power management (when FCS=H)
0: Stand by mode (default)
1: Normal display mode</td></tr>
<tr><td>0x07</td><td>DRIVER_CAPABULITY</td><td>0x00</td><td>R/W</td><td>[3:2]: GMTBA1–0 Adjust the amount of fixed current from the fixed current source for the operational amplifier in the Gamma circuit.
<table>
<tr><th>GMTBA1</th><th>GMTBA0</th><th>Constant Current of Operational Amplifier</th></tr>
<tr><td>0</td><td>0</td><td>0.25 (default)</td></tr>
<tr><td>0</td><td>1</td><td>0.50</td></tr>
<tr><td>1</td><td>0</td><td>0.75</td></tr>
<tr><td>1</td><td>1</td><td>1</td></tr>
</table>
[1:0]: DRI_CAPA1–0 DRIVER_CAPABULITY select.
<table>
<tr><th>DRI_CAPA1</th><th>DRI_CAPA0</th><th>DRIVER CAPABULITY</th></tr>
<tr><td>0</td><td>0</td><td>50 % (default)</td></tr>
<tr><td>0</td><td>1</td><td>67 %</td></tr>
<tr><td>1</td><td>0</td><td>83 %</td></tr>
<tr><td>1</td><td>1</td><td>100 %</td></tr>
</table></td></tr>
<tr><td>0x08</td><td>POWER_CTRL2</td><td>0x00</td><td>R/W</td><td>[7]: Set CP1 disable.
0: CP1 enable. (default)
1: CP1 disable.

[6]: Set CP2 disable.
0: CP2 enable. (default)
1: CP2 disable.

[5]: Set VGAM1OUT generation enable or disable.
0: VGAM1OUT generation enable. (default)
1: VGAM1OUT generation disable, VGAM1OUT could be external input.

[4]: Set VGH generation enable or disable.
0: VGH generation enable. (default)
1: VGH generation disable, VGH could be external input.

[3]: Set VGL generation enable or disable.
0: VGL generation enable. (default)
1: VGL generation disable, VGL could be external input.

[2]: Set ARREF generation enable or disable.
0: ARREF generation enable. (default)
1: ARREF generation disable, ARS could be external input.

[1:0]: VDC1-0 Set the VDDD output voltage.
<table>
<tr><th>VDC1</th><th>VDC0</th><th>VDDD</th></tr>
<tr><td>0</td><td>0</td><td>1.8V (default)</td></tr>
<tr><td>0</td><td>1</td><td>2.5V</td></tr>
<tr><td>1</td><td>0</td><td>1.6V (not open)</td></tr>
<tr><td>1</td><td>1</td><td>1.5V (not open)</td></tr>
</table></td></tr>
</table>

<table>
<tr><td>0x09</td><td>POWER_CTRL3</td><td>0x20</td><td>R/W</td><td>
[5:0]: VRH5-0 Set the magnification of amplification for VGAM1OUT voltage. (reference voltage for grayscale voltage)

If GAMV = 0 :

000000: 4.8V * (1-0.5%*32) V
100000: 4.8 V * 1 (default)
111111: 4.8V * (1+0.5%*31) V
Unit : 0.5%

When VCI≧3.0V, please set VRH to VGAM1OUT=4.8V.
When VCI< 3.0V, please set VRH to VGAM1OUT =4.6V.

If GAMV = 1 :

000000: 5.8V * (1-0.5%*32) V
100000: 5.8V * 1 (default)
111111: 5.8V * (1+0.5%*31) V
Unit : 0.5%

Set VRH to VGAM1OUT = 5.8V.

When want to read VRH5-0 from SPI 0x09, set
OTP_enable = 0 : from SPI memory
OTP_enable = 1 : from OTP memory
</td></tr>
<tr><td>0x0A</td><td>POWER_CTRL4</td><td>0x66</td><td>R/W</td><td>
[7:4]: BTH3–0 Set the VGH output voltage.
[3:0]: BTL3–0 Set the VGL output voltage.
<table>
<tr><th>BTH3-0</th><th>VGH Output(V)</th><th>BTL3-0</th><th>VGL Output(V)</th></tr>
<tr><td>0000</td><td>3</td><td>0000</td><td>-3</td></tr>
<tr><td>0001</td><td>3.5</td><td>0001</td><td>-3.5</td></tr>
<tr><td>0010</td><td>4</td><td>0010</td><td>-4</td></tr>
<tr><td>0011</td><td>4.4</td><td>0011</td><td>-4.4</td></tr>
<tr><td>0100</td><td>4.6</td><td>0100</td><td>-4.6</td></tr>
<tr><td>0101</td><td>4.8</td><td>0101</td><td>-4.8</td></tr>
<tr><td>0110</td><td>5 (default)</td><td>0110</td><td>-5 (default)</td></tr>
<tr><td>0111</td><td>5.2</td><td>0111</td><td>-5.2</td></tr>
<tr><td>1000</td><td>5.4</td><td>1000</td><td>-5.4</td></tr>
<tr><td>1001</td><td>5.6</td><td>1001</td><td>-5.6</td></tr>
<tr><td>1010</td><td>5.8</td><td>1010</td><td>-5.8</td></tr>
<tr><td>1011</td><td>6</td><td>1011</td><td>-6</td></tr>
<tr><td>1100</td><td>6.5</td><td>1100</td><td>-6.5</td></tr>
<tr><td>1101</td><td>7</td><td>1101</td><td>-7</td></tr>
<tr><td>1110</td><td>7.5</td><td>1110</td><td>-7.5</td></tr>
<tr><td>1111</td><td>8</td><td>1111</td><td>-8</td></tr>
</table>
</td></tr>
<tr><td>0x0B</td><td>POWER_CTRL5</td><td>0x04</td><td>R/W</td><td>
[2:0]: ARS Set the ARREF output voltage.
<table>
<tr><th>ARS2</th><th>ATS1</th><th>ARS0</th><th>ARREF</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>+8V</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>+7V</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>+6V</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>+5V</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>-5V (default)</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>-6V</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>-7V</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>-8V</td></tr>
</table>
</td></tr>
</table>

<table>
<tr>
<td>0x0C</td>
<td>POWER_CTRL6</td>
<td>0x21</td>
<td>R/W</td>
<td>
[7]: CP1X : Set-up circuit 1 selection.
0: Set-up circuit 1 pump ratio = 2X. (default)
1: Set-up circuit 1 pump ratio = 3X.

[6]: GAMV : DDVDH and VGAM1OUT selection.
0: VDDA = 5.1V, VGAM1OUT=4.8V (default)
1: VDDA=6.0V, VGAM1OUT=5.8V

[5:3]: DC1: Set the operating frequency for the step-up circuit 2. When using the higher frequency, the driving ability of the step-up circuit and the display quality are high, but the current consumption is increased. The tradeoff is between the display quality and the current consumption.
<table>
<tr><th>DC1[2]</th><th>DC1[1]</th><th>DC1[0]</th><th>Operation Frequency of Step-up Circuit 2</th></tr>
<tr><td>1</td><td>1</td><td>1</td><td>6*frequency of hsync</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>4*frequency of hsync</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>2*frequency of hsync</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1*frequency of hsync(default)</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0.5*frequency of hsync</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0.25*frequency of hsync</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0.125*frequency of hsync</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0.0625*frequency of hsync</td></tr>
</table>
Note:
Ensure that the operation frequency of step-up circuit 1 ≧ step-up circuit 2.

[2:0]: DC0 Set the operating frequency for the step-up circuit 1. When using the higher frequency, the driving ability of the step-up circuit and the display quality are high, but the current consumption is increased. The tradeoff is between the display quality and the current consumption.
<table>
<tr><th>DC0[2]</th><th>DC0[1]</th><th>DC0[0]</th><th>Operation Frequency of Step-up Circuit 1</th></tr>
<tr><td>1</td><td>1</td><td>1</td><td>8*frequency of hsync</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>7*frequency of hsync</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>6*frequency of hsync</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>5*frequency of hsync</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>4*frequency of hsync</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>3*frequency of hsync</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>2*frequency of hsync(default)</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1*frequency of hsync</td></tr>
</table>
</td>
</tr>
</table>

0x0D	POWER_SEQ1	0x09	R/W	**[5:4]: A_STAGE** 00: 1 frame **(default)** 01: 2 frame 10: 3 frame 11: 4 frame **[3:2]: B_STAGE** 00: 1 frame 01: 2 frame 10: 3 frame **(default)** 11: 4 frame **[1:0]: C_STAGE** 00: 1 frame 01: 2 frame **(default)** 10: 3 frame 11: 4 frame
0x0E	POWER_SEQ2	0x00	R/W	**[3]: DCDC_EN control selection** 0: Auto mode, DCDC controlled by C_STAGE. **(default)** 1: Manual mode, DCDC controlled by DCEN. **[2]: DCEN:** DCDC manual mode on/off control 0: DCDC turn off **(default)** 1: DCDC turn on **[1]: DCDC_EN polarity** 0: DCDC_EN H level is turn on mode **(default)** 1: DCDC_EN L level is turn on mode **[0]: B_STAGE data** 0: Black data **(default)** 1: White data

Gamma correction control register				
Register Address	**Register name**	**Default**	**Read/Write**	**Description**
0x10	R_SLOPE	0x43	R/W	**[7:4] Red color GAMMA slope 1 correction** 0000: VR0 - 6% 0001: VR0 - 4.5% ……. 0100: VR0 + 0% **(default)** ……. 1110: VR0 + 18% 1111: VR0 + 20% **[3:0] Red color GAMMA slope 2 correction** 0000: VR255 - 54% 0001: VR255 - 36% ……. 0011: VR255+ 0% **(default)** ……. 1110: VR255 + 181% 1111: VR255 + 195% When want to read R_SLOPE from SPI 0x10, set OTP_enable = 0 : from SPI memory OTP_enable = 1 : from OTP memory
0x11	G_SLOPE	0x43	R/W	**[7:4] Red color GAMMA slope 1 correction** 0000: VG0 - 6% 0001: VG0- 4.5% ……. 0100: VG0 + 0% **(default)** ……. 1110: VG0 + 18% 1111: VG0 + 20% **[3:0] Red color GAMMA slope 2 correction** 0000: VG255 - 54% 0001: VG255 - 36% ……. 0011: VG255 + 0% **(default)** ……. 1110: VG255 + 181% 1111: VG255 + 195% When want to read G_SLPOE from SPI 0x11, set OTP_enable = 0 : from SPI memory OTP_enable = 1 : from OTP memory
0x12	B_SLOPE	0x43	R/W	**[7:4] Red color GAMMA slope 1 correction** 0000: VB0 - 6% 0001: VB0 - 4.5% ……. 0100: VB0 + 0% **(default)** ……. 1110: VB0 + 18% 1111: VB0 + 20% **[3:0] Red color GAMMA slope 2 correction** 0000: VB255 - 54% 0001: VB255 - 36% ……. 0011: VB255 + 0% **(default)** ……. 1110: VB255 + 181% 1111: VB255 + 195% When want to read B_SLOPE from SPI 0x12, set OTP_enable = 0 : from SPI memory OTP_enable = 1 : from OTP memory

0x13	R_GAMMA0	0x02	R/W	**Red GAMMA0 [3:0] of gamma correction.** 0000:KV1 (R) 0010:KV3 (R) **(default)** 1011:KV12 (R) Step unit : 50mV
0x14	R_GAMMA10	0x04	R/W	**Red GAMMA10 [2:0] of gamma correction.** 000:KV13 (R) 100:KV17 (R) **(default)** 111:KV20 (R) Step unit : 50mV
0x15	R_GAMMA36	0x04	R/W	**Red GAMMA36 [2:0] of gamma correction.** 000:KV21 (R) 100:KV25 (R) **(default)** 111:KV28 (R) Step unit : 50mV
0x16	R_GAMMA80	0x04	R/W	**Red GAMMA80 [2:0] of gamma correction.** 000:KV29 (R) 100:KV33 (R) **(default)** 111:KV36 (R) Step unit : 50mV
0x17	R_GAMMA124	0x04	R/W	**Red GAMMA124 [2:0] of gamma correction.** 000:KV37 (R) 100:KV41 (R) **(default)** 111:KV44 (R) Step unit : 50mV
0x18	R_GAMMA168	0x04	R/W	**Red GAMMA168 [2:0] of gamma correction.** 000:KV45 (R) 100:KV49 (R) **(default)** 111:KV52 (R) Step unit : 50mV
0x19	R_GAMMA212	0x04	R/W	**Red GAMMA212 [2:0] of gamma correction.** 000:KV53 (R) 100:KV57 (R) **(default)** 111:KV60 (R) Step unit : 50mV
0x1A	R_GAMMA255	0x08	R/W	**Red GAMMA255 [3:0] of gamma correction.** 0000:KV61 (R) 1000:KV69 (R) **(default)** 1111:KV76 (R) Step unit : 25mV
0x1B	G_GAMMA0	0x02	R/W	**Green GAMMA0 [3:0] of gamma correction.** 0000:KV1 (G) 0010:KV3 (G) **(default)** 1011:KV12 (G) Step unit : 50mV
0x1C	G_GAMMA10	0x04	R/W	**Green GAMMA10 [2:0] of gamma correction.** 000:KV13 (G) 100:KV17 (G) **(default)** 111:KV20 (G) Step unit : 50mV
0x1D	G_GAMMA36	0x04	R/W	**Green GAMMA36 [2:0] of gamma correction.** 000:KV21 (G) 100:KV25 (G) **(default)** 111:KV28 (G) Step unit : 50mV
0x1E	G_GAMMA80	0x04	R/W	**Green GAMMA80 [2:0] of gamma correction.** 000:KV29 (G) 100:KV33 (G) **(default)** 111:KV36 (G) Step unit : 50mV
0x1F	G_GAMMA124	0x04	R/W	**Green GAMMA124 [2:0] of gamma correction.** 000:KV37 (G) 100:KV41 (G) **(default)** 111:KV44 (G) Step unit : 50mV

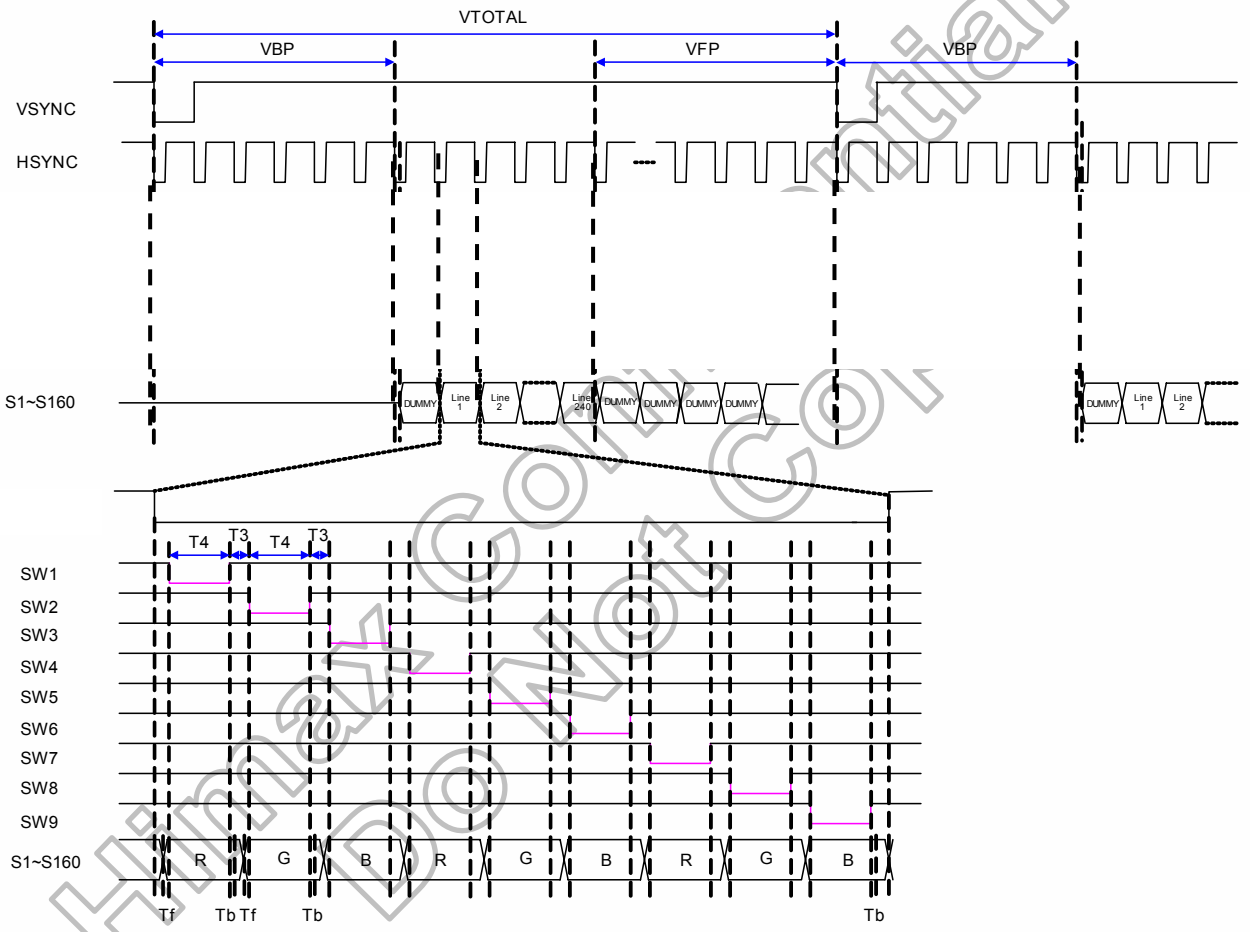
0x20	G_GAMMA168	0x04	R/W	**Green GAMMA168 [2:0] of gamma correction.** 000:KV45 (G) 100:KV49 (G) **(default)** 111:KV52 (G) Step unit : 50mV
0x21	G_GAMMA212	0x04	R/W	**Green GAMMA212 [2:0] of gamma correction.** 000:KV53 (G) 100:KV57 (G) **(default)** 111:KV60 (G) Step unit : 50mV
0x22	G_GAMMA255	0x08	R/W	**Green GAMMA255 [3:0] of gamma correction.** 0000:KV61 (G) 1000:KV69 (G) **(default)** 1111:KV76 (G) Step unit : 25mV
0x23	B_GAMMA0	0x02	R/W	**Blue GAMMA0 [3:0] of gamma correction.** 0000:KV1 (B) 0010:KV3 (B) **(default)** 1011:KV12 (B) Step unit : 50mV
0x24	B_GAMMA10	0x04	R/W	**Blue GAMMA10 [2:0] of gamma correction.** 000:KV13 (B) 100:KV17 (B) **(default)** 111:KV20 (B) Step unit : 50mV
0x25	B_GAMMA36	0x04	R/W	**Blue GAMMA36 [2:0] of gamma correction.** 000:KV21 (B) 100:KV25 (B) **(default)** 111:KV28 (B) Step unit : 50mV
0x26	B_GAMMA80	0x04	R/W	**Blue GAMMA80 [2:0] of gamma correction.** 000:KV29 (B) 100:KV33 (B) **(default)** 111:KV36 (B) Step unit : 50mV
0x27	B_GAMMA124	0x04	R/W	**Blue GAMMA124 [2:0] of gamma correction.** 000:KV37 (B) 100:KV41 (B) **(default)** 111:KV44 (B) Step unit : 50mV
0x28	B_GAMMA168	0x04	R/W	**Blue GAMMA168 [2:0] of gamma correction.** 000:KV45 (B) 100:KV49 (B) **(default)** 111:KV52 (B) Step unit : 50mV
0x29	B_GAMMA212	0x04	R/W	**Blue GAMMA212 [2:0] of gamma correction.** 000:KV53 (B) 100:KV57 (B) **(default)** 111:KV60 (B) Step unit : 50mV
0x2A	B_GAMMA255	0x08	R/W	**Blue GAMMA255 [3:0] of gamma correction.** 0000:KV61 (B) 1000:KV69 (B) **(default)** 1111:KV76 (B) Step unit : 25mV

<table>
<tr><th colspan="5">Panel control register</th></tr>
<tr><th>Register Address</th><th>Register name</th><th>Default</th><th>Read/Write</th><th>Description</th></tr>
<tr><td>0x34</td><td>T3</td><td>0x1E</td><td>R/W</td><td>[6:0]: Switch non-overlap period.
0x00: Reserved
0x01: 1 DCLK
0x02: 2 DCLK
……
0x1E: 30 DCLK (default)
……
0x8E: 126 DCLK
0x8F: 127 DCLK</td></tr>
<tr><td>0x35</td><td>T4</td><td>0x60</td><td>R/W</td><td>[7:0]: Switch turn on time.
0x00: Reserved
0x01: 1 DCLK
0x02: 2 DCLK
0x03: 3 DCLK
……
……
0x60: 96 DCLK (default)
……
……
0xFD: 253 DCLK
0xFE: 254 DCLK
0xFF: 255 DCLK</td></tr>
<tr><td>0x36</td><td>TF</td><td>0x05</td><td>R/W</td><td>[5:0]: SOUT turn on to SW turn on time
0x00: Reserved
0x01: 1 DCLK
……
0x05: 5 DCLK (default)
……
0x4E: 62 DCLK
0x4F: 63 DCLK</td></tr>
<tr><td>0x37</td><td>TB</td><td>0x0F</td><td>R/W</td><td>[5:0]: SW turn off to SOUT turn off time
0x00: Reserved
0x01: 1 DCLK
……
0x0F: 15 DCLK (default)
……
0x4E: 62 DCLK
0x4F: 63 DCLK</td></tr>
<tr><td>0x38</td><td>VSTS</td><td>0x10</td><td>R/W</td><td>[6:5]: Odd frame or Even frame advance control
<table>
<tr><th>[6:5]</th><th>Advance Frame</th><th>Notes</th></tr>
<tr><td>00</td><td>Default</td><td>Odd/Even frame VBP are the same</td></tr>
<tr><td>01</td><td>Odd frame</td><td>Even frame VBP = VSTS setting + 1H</td></tr>
<tr><td>10</td><td>Even frame</td><td>Odd frame VBP = VSTS setting + 1H</td></tr>
<tr><td>11</td><td>Reserve</td><td>Reserve</td></tr>
</table>
Note:
Please set the [5:4]=01 when CCIR601 NTSC/PAL、CCIR656 PAL mode；set the [5:4]=00 when CCIR656 NTSC mode for video decoder SAA7114。(Please refer the input timing of the “8.1.3 Data input format for CCIR601 Mode”)

[4:0]: Vertical valid data start time select (VBP)
0x00 = -16 HSYNC
0x01 = -15 HSYNC
……
0x0F = -1 HSYNC
0x10 = 0 HSYNC (default)
0x11 = +1 HSYNC
……
0x1E = +14 HSYNC
0x1F =+15 HSYNC</td></tr>
</table>

0x39	HSTS	0x20	R/W	**[5:0]: Horizontal valid data start time select (HBP)** 0x00 = -32DCLK 0x01 = -31DCLK …… 0x1F = -1 DCLK 0x20 = +0 DCLK **(default)** 0x21 = +1 DCLK …… 0x3E = +30 DCLK 0x3F = +31 DCLK

Scan output timing



VTOTAL = VBP + VACTIVE + VFP
VFP > 4H

T1 = 0.5H
T2 =1H
T2= 9xT4 + 10xT3
TF + TB ≦T3 - 1

Color enhance control register				
Register Address	**Register name**	**Default**	**Read/Write**	**Description**
0x3A	RGB_CONTRAST	0x20	R/W	**[5:0]: RGB contrast totally adjustment** 000000: Input Digital Data * (0/32) 100000: Input Digital Data * (32/32) **(default)** 111111: Input Digital Data * (63/32)
0x3B	R_CONTRAST	0x20	R/W	**[5:0]: R contrast totally adjustment** 000000: Input Digital Data * (0/32) 100000: Input Digital Data * (32/32) **(default)** 111111: Input Digital Data * (63/32)
0x3C	G_CONTRAST	0x20	R/W	**[5:0]: G contrast totally adjustment** 000000: Input Digital Data * (0/32) 100000: Input Digital Data * (32/32) **(default)** 111111: Input Digital Data * (63/32)
0x3D	B_CONTRAST	0x20	R/W	**[5:0]: B contrast totally adjustment** 000000: Input Digital Data * (0/32) 100000: Input Digital Data * (32/32) **(default)** 111111: Input Digital Data * (63/32)
0x3E	BRIGHT_OFFSET	0x80	R/W	**[8:0]: brightness offset adjustment** 00000000: Input Digital Data - 128 10000000: Input Digital Data + 0 **(default)** 11111111: Input Digital Data + 127
Note: $D_{CONSTRAST} = D_{IN}$ * Gain, $D_{BRIGHTNESS} = D_{CONSTRAST}$ + Brightness Offset Contrast Adjustment Sequence: RGB_CONTRAST → R_CONTRAST → G_CONTRAST → B_CONTRAST				

OTP register				
Register Address	Register name	Default	Read/Write	Description
0x00	R_SLOPE	0x43	R/W	**[7:4] Red color GAMMA slope 1 correction** 0000: VR0 - 6% ……. 0100: VR0 + 0% **(default)** ……. 1111: VR0 + 20% **[3:0] Red color GAMMA slope 2 correction** 0000: VR255 - 54% ……. 0011: VR255+ 0% **(default)** ……. 1111: VR255 + 195%
0x01	G_SLOPE	0x43	R/W	**[7:4] Red color GAMMA slope 1 correction** 0000: VG0 - 6% ……. 0100: VG0 + 0% **(default)** ……. 1111: VG0 + 20% **[3:0] Red color GAMMA slope 2 correction** 0000: VG255 - 54% ……. 0011: VG255 + 0% **(default)** ……. 1111: VG255 + 195%
0x02	B_SLOPE	0x43	R/W	**[7:4] Red color GAMMA slope 1 correction** 0000: VB0 - 6% ……. 0100: VB0 + 0% **(default)** ……. 1111: VB0 + 20% **[3:0] Red color GAMMA slope 2 correction** 0000: VB255 - 54% ……. 0011: VB255 + 0% **(default)** ……. 1111: VB255 + 195%
0x03	VGAM1_LEVEL	0x00	R/W	**[5:0]: VRH5-0** Set the magnification of amplification for VGAM1OUT voltage. (reference voltage for grayscale voltage) If GAMV = 0 : 000000: 4.8V * (1-0.5%*32) V 100000: 4.8 V * 1 (default) 111111: 4.8V * (1+0.5%*31) V Unit : 0.5% When VCI≧3.0V, please set VRH to VGAM1OUT=4.8V. When VCI< 3.0V, please set VRH to VGAM1OUT =4.6V. If GAMV = 1 : 000000: 5.8V * (1-0.5%*32) V 100000: 5.8V * 1 (default) 111111: 5.8V * (1+0.5%*31) V Unit : 0.5% Set VRH to VGAM1OUT = 5.8V.

7. Electrical Characteristic

7.1 Maximum Rating

Symbol	Parameter	Value	Unit
VCC	Logic Supply Voltage	-0.3 to +3.6	V
VCI	Analog Supply Voltage	-0.3 to +3.6	V
TA	Operating Temperature	-30 to +70	℃
Tstg	Storage Temperature	-55 to +125	℃

Table 7. 1 Maximum ratings

Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section.
Unused outputs must be left open. This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

7.2 DC Characteristics

DC Characteristics

(Unless otherwise specified, Voltage Referenced to VSS = 0V, VCC = 1.5 to 3.6V, T_A = -20 to 70C)

Parameter	Symbol	Test condition	Min.	Typ.	Max.	Unit
System power supply pins of the logic block	VCC	-	1.5	-	3.6	V
Booster Reference Supply Voltage Range	VCI	-	2.7	-	3.6	V
DDVDH Output Voltage 1	DDVDH	Set GAMV=0	4.9	5.1	5.3	V
DDVDH Output Voltage 2	DDVDH	Set GAMV=1	5.8	6.0	6.2	V
VGAM1OUT Output Voltage 1	VGAM1OUT	Set GAMV=0	4.7	4.8	4.9	V
VGAM1OUT Output Voltage 2	VGAM1OUT	Set GAMV=1	5.7	5.8	5.9	V
Gate driver High Output Voltage	VGH	-	+3	-	+8	V
Gate driver Low Output Voltage	VGL	-	-8	-	-3	V
OLED Diode Refer Voltage	ARREF	-	-8	-	+8	V
Logic High Output Voltage	VOH	Iout=-400μA	0.8 * VCC	-	VCC	V
Logic Low Output Voltage	VOL	Iout=400μA	0	-	0.2 * VCC	V
Logic High Input voltage	VIH	-	0.8 * VCC	-	VCC	V
Logic Low Input voltage	VIL		0	-	0.2 * VCC	V
Logic Input Current	IIL/IIH	No pull up or pull low	-1	-	1	μA
Pull high resistance	RH	Pull up pins	600	900	1200	KΩ
Pull low resistance	RL	Pull low pins	600	900	1200	KΩ
High Output Current	IOH	S1~S107, Vo=4.9V vs. 4V	50	-	-	μA
Low Output Current	IOL	S1~S107, Vo=0.1V vs. 1V	-	-	-50	μA
Output leakage Current	IOZ	-	-1	-	1	μA
Output voltage offset	VOS	S1~S107, Vo=0.1V~DDVDH-0.1V		±10		mV
Output voltage deviation	VOD	S1~S107, Vo=0.1V~DDVDH-0.1V		±10		mV
Analog standby current	ISTB	VCI=3.0V, Stand by mode		-	10	uA
Analog operating current	IVCI	VCI=3.0V, S1~S160 no load		TBD		mV
Analog operating current	IVCI	VCI=3.0V, S1~S160 no load		TBD		mV
Logic Pins Input Capacitance	CIN	-	-	5	7.5	pF

Table 7. 2 DC characteristics

7.3 AC Characteristics

7.3.1 AC Electrical Characteristics

PARAMETER	Symbol	Min.	Typ.	Max.	Unit
HSYNC setup time	T_{hst}	10	-	-	ns
HSYNC hold time	T_{hhd}	10	-	-	ns
VSYNC setup time	T_{vst}	10	-	-	ns
VSYNC hold time	T_{vhd}	10	-	-	ns
Data setup time	T_{dsu}	10	-	-	ns
Data hold time	T_{dhd}	10	-	-	ns
DE setup time	T_{esu}	10	-	-	ns
VSYNC falling to HSYNC falling time on odd field @ RGB mode	T_{HV_O}	-4	0	+4	T_{CPH}
VSYNC falling to HSYNC falling time on even field @ RGB mode	T_{HV_E}	0.4	0.5	0.6	T_H
Source output settling time	T_{ST}	-	3	-	µs
Gate signals settling time (90%)	T_{GL}	-	0.5	-	µs
SW signals settling time (90%)	T_{SW}	-	0.6	-	µs

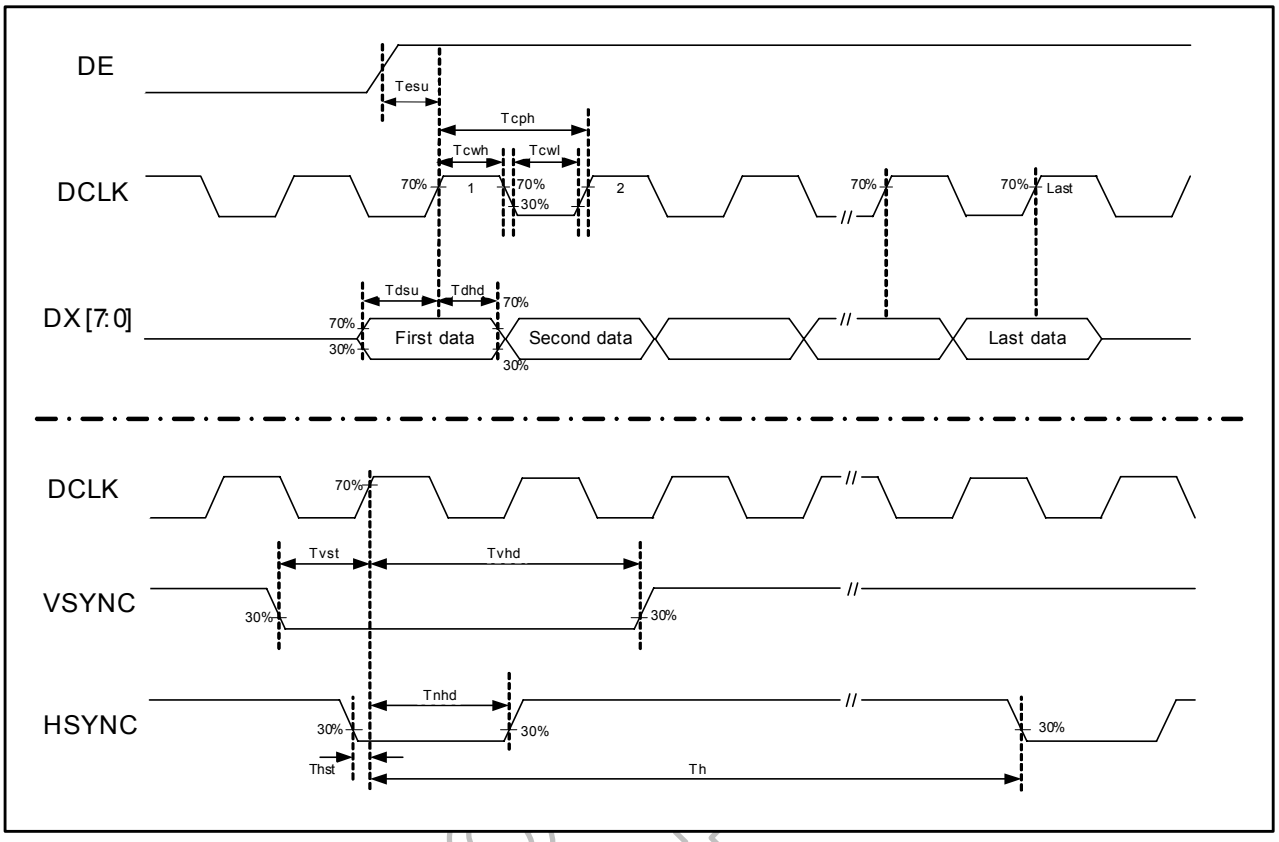


Figure 7. 1 Clock and Data input waveforms

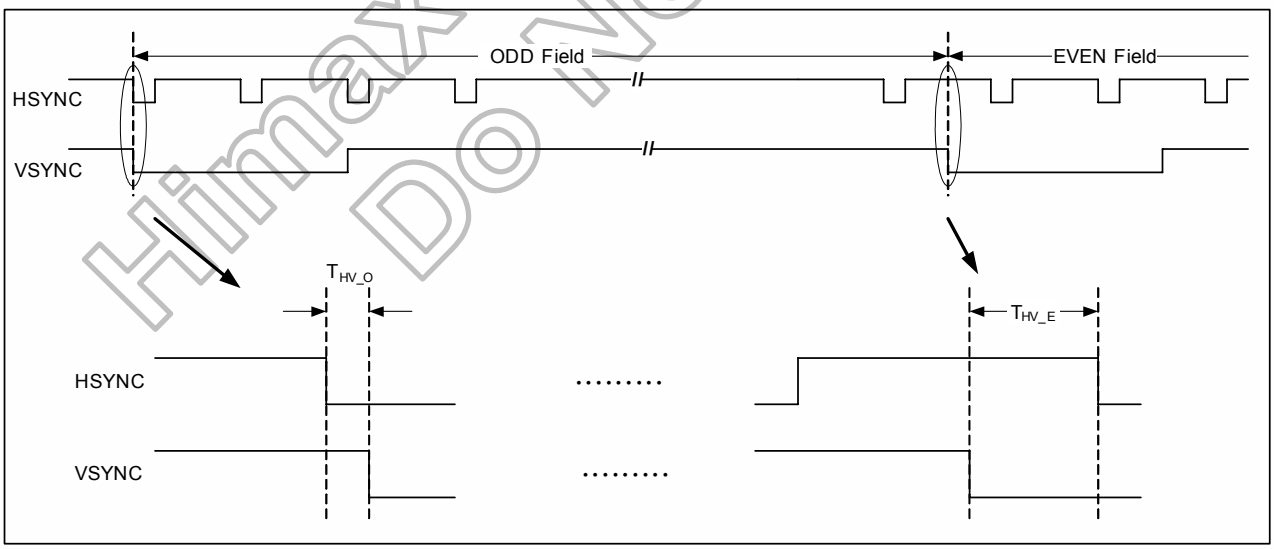


Figure 7. 2 Define the HSYNC to VSYNC timing for RGB mode

7.3.2 Digital Serial RGB interface (320RGBx240 resolution)

PARAMETER		Symbol	Min.	Typ.	Max.	Unit
DCLK frequency		F_{CPH}	-	19.28	-	MHz
DCLK period		T_{CPH}	-	51.87	-	ns
DCLK pulse duty		T_{CWH}	40	50	60	%
HSYNC period		T_H	-	1224	-	T_{CPH}
HSYNC pulse width		T_{WH}	5	90	-	T_{CPH}
HSYNC-first horizontal data time		T_{HBP}	172	204	235	T_{CPH}
DE pulse width		T_{EP}	-	960	-	T_{CPH}
VSYNC pulse width		T_{WV}	1	3	5	T_H
VSYNC-1st Data input (DE) time		T_{VBP}	4	18	-	T_H
VSYNC period	NTSC	T_V	-	262.5 / 262	-	T_H
	PAL	T_V	-	312.5 / 312	-	T_H

PARAMETER	Symbol	Min.	Typ.	Max.	Unit
SW pulse width	T_4	-	96	-	T_{CPH}
SW-SW non-overlap time	T_3	-	30	-	T_{CPH}
SOUT-SW front time	T_F	-	5	-	T_{CPH}
SW-SOUT back time	T_B	-	15	-	T_{CPH}

7.3.3 Digital Parallel RGB interface (320RGBx240 resolution)

PARAMETER		Symbol	Min.	Typ.	Max.	Unit
DCLK frequency		F_{CPH}	-	6.42	-	MHz
DCLK period		T_{CPH}	-	155.6	-	ns
DCLK pulse duty		T_{CWH}	40	50	60	%
HSYNC period		T_H	-	408	-	T_{CPH}
HSYNC pulse width		T_{WH}	5	30	-	T_{CPH}
HSYNC-first horizontal data time		T_{HBP}	36	68	99	T_{CPH}
DE pulse width		T_{EP}	-	320	-	T_{CPH}
VSYNC pulse width		T_{WV}	1	3	5	T_H
VSYNC-1st Data input (DE) time		T_{VBP}	4	18	-	T_H
VSYNC period	NTSC	T_V	-	262.5 / 262	-	T_H
	PAL	T_V	-	312.5 / 312	-	T_H

PARAMETER	Symbol	Min.	Typ.	Max.	Unit
SW pulse width	T_4	-	32	-	T_{CPH}
SW-SW non-overlap time	T_3	-	10	-	T_{CPH}
SOUT-SW front time	T_F	-	2	-	T_{CPH}
SW-SOUT back time	T_B	-	6	-	T_{CPH}

7.3.4 Serial RGB interface (480RGBx234 resolution)

PARAMETER		Symbol	Min.	Typ.	Max.	Unit
DCLK frequency		F_{CPH}	-	28.92	-	MHz
DCLK period		T_{CPH}	-	34.58	-	ns
DCLK pulse duty		T_{CWH}	40	50	60	%
HSYNC period		T_H	-	1836	-	T_{CPH}
HSYNC pulse width		T_{WH}	5	90	-	T_{CPH}
HSYNC-first horizontal data time		T_{HBP}	274	306	337	T_{CPH}
DE pulse width		T_{EP}	-	1440	-	T_{CPH}
VSYNC pulse width		T_{WV}	1	3	5	T_H
VSYNC-1st Data input (DE) time		T_{VBP}	4	18	-	T_H
VSYNC period	NTSC	T_V	-	262.5 / 262	-	T_H
	PAL	T_V	-	312.5 / 312	-	T_H

PARAMETER	Symbol	Min.	Typ.	Max.	Unit
SW pulse width	T_4	-	144	-	T_{CPH}
SW-SW non-overlap time	T_3	-	45	-	T_{CPH}
SOUT-SW front time	T_F	-	6	-	T_{CPH}
SW-SOUT back time	T_B	-	24	-	T_{CPH}

7.3.5 Parallel RGB interface (480RGBx234 resolution)

PARAMETER		Symbol	Min.	Typ.	Max.	Unit
DCLK frequency		F_{CPH}	-	9.64	-	MHz
DCLK period		T_{CPH}	-	103.7	-	ns
DCLK pulse duty		T_{CWH}	40	50	60	%
HSYNC period		T_H	-	612	-	T_{CPH}
HSYNC pulse width		T_{WH}	5	30	-	T_{CPH}
HSYNC-first horizontal data time		T_{HBP}	70	102	133	T_{CPH}
DE pulse width		T_{EP}	-	480	-	T_{CPH}
VSYNC pulse width		T_{WV}	1	3	5	T_H
VSYNC-1st Data input (DE) time		T_{VBP}	4	18	-	T_H
VSYNC period	NTSC	T_V	-	262.5 / 262	-	T_H
	PAL	T_V	-	312.5 / 312	-	T_H

PARAMETER	Symbol	Min.	Typ.	Max.	Unit
SW pulse width	T_4	-	48	-	T_{CPH}
SW-SW non-overlap time	T_3	-	15	-	T_{CPH}
SOUT-SW front time	T_F	-	2	-	T_{CPH}
SW-SOUT back time	T_B	-	8	-	T_{CPH}

7.3.6 Serial RGB interface (480RGBx272 resolution)

PARAMETER	Symbol	Min.	Typ.	Max.	Unit
DCLK frequency	F_{CPH}	33.3	-	-	MHz
DCLK period	T_{CPH}	-	-	30	ns
DCLK pulse duty	T_{CWH}	40	50	60	%
HSYNC period	T_H	-	1836	-	T_{CPH}
HSYNC pulse width	T_{WH}	5	90	-	T_{CPH}
HSYNC-first horizontal data time	T_{HBP}	274	306	337	T_{CPH}
DE pulse width	T_{EP}	-	1440	-	T_{CPH}
VSYNC pulse width	T_{WV}	1	3	5	T_H
VSYNC-1st Data input (DE) time	T_{VBP}	4	20	35	T_H
VSYNC period	T_V	302	-	-	T_H

PARAMETER	Symbol	Min.	Typ.	Max.	Unit
SW pulse width	T_4	-	-	150	T_{CPH}
SW-SW non-overlap time	T_3	-	-	40	T_{CPH}
SOUT-SW front time	T_F	-	-	6	T_{CPH}
SW-SOUT back time	T_B	-	-	20	T_{CPH}

7.3.7 Parallel RGB interface (480RGBx272 resolution)

PARAMETER	Symbol	Min.	Typ.	Max.	Unit
DCLK frequency	F_{CPH}	11.1	-	-	MHz
DCLK period	T_{CPH}	-	-	90	ns
DCLK pulse duty	T_{CWH}	40	50	60	%
HSYNC period	T_H	-	612	-	T_{CPH}
HSYNC pulse width	T_{WH}	5	30	-	T_{CPH}
HSYNC-first horizontal data time	T_{HBP}	70	102	133	T_{CPH}
DE pulse width	T_{EP}	-	480	-	T_{CPH}
VSYNC pulse width	T_{WV}	1	3	5	T_H
VSYNC-1st Data input (DE) time	T_{VBP}	4	20	35	T_H
VSYNC period	T_V	302	-	-	T_H

PARAMETER	Symbol	Min.	Typ.	Max.	Unit
SW pulse width	T_4	-	-	50	T_{CPH}
SW-SW non-overlap time	T_3	-	-	13	T_{CPH}
SOUT-SW front time	T_F	-	-	2	T_{CPH}
SW-SOUT back time	T_B	-	-	6	T_{CPH}

7.3.8 Serial RGB interface (320RGBx480 resolution)

PARAMETER	Symbol	Min.	Typ.	Max.	Unit
DCLK frequency	F_{CPH}	37.45	-	-	MHz
DCLK period	T_{CPH}	-	-	26.7	ns
DCLK pulse duty	T_{CWH}	40	50	60	%
HSYNC period	T_H	-	1224	-	T_{CPH}
HSYNC pulse width	T_{WH}	5	90	-	T_{CPH}
HSYNC-first horizontal data time	T_{HBP}	172	204	235	T_{CPH}
DE pulse width	T_{EP}	-	960	-	T_{CPH}
VSYNC pulse width	T_{WV}	1	3	5	T_H
VSYNC-1st Data input (DE) time	T_{VBP}	4	20	35	T_H
VSYNC period	T_V	510	-	-	T_H

PARAMETER	Symbol	Min.	Typ.	Max.	Unit
SW pulse width	T_4	-	-	150	T_{CPH}
SW-SW non-overlap time	T_3	-	-	38	T_{CPH}
SOUT-SW front time	T_F	-	-	6	T_{CPH}
SW-SOUT back time	T_B	-	-	20	T_{CPH}

7.3.9 Parallel RGB interface (320RGBx480 resolution)

PARAMETER	Symbol	Min.	Typ.	Max.	Unit
DCLK frequency	F_{CPH}	12.48	-	-	MHz
DCLK period	T_{CPH}	-	-	80.1	ns
DCLK pulse duty	T_{CWH}	40	50	60	%
HSYNC period	T_H	-	408	-	T_{CPH}
HSYNC pulse width	T_{WH}	5	30	-	T_{CPH}
HSYNC-first horizontal data time	T_{HBP}	36	68	99	T_{CPH}
DE pulse width	T_{EP}	-	320	-	T_{CPH}
VSYNC pulse width	T_{WV}	1	3	5	T_H
VSYNC-1st Data input (DE) time	T_{VBP}	4	20	35	T_H
VSYNC period	T_V	510	-	-	T_H

PARAMETER	Symbol	Min.	Typ.	Max.	Unit
SW pulse width	T_4	-	-	50	T_{CPH}
SW-SW non-overlap time	T_3	-	-	13	T_{CPH}
SOUT-SW front time	T_F	-	-	2	T_{CPH}
SW-SOUT back time	T_B	-	-	6	T_{CPH}

7.3.10 Serial RGB interface (240RGBx400 resolution)

PARAMETER	Symbol	Min.	Typ.	Max.	Unit
DCLK frequency	F_{CPH}	28	-	-	MHz
DCLK period	T_{CPH}	-	-	35.6	ns
DCLK pulse duty	T_{CWH}	40	50	60	%
HSYNC period	T_H	-	918	-	T_{CPH}
HSYNC pulse width	T_{WH}	5	90	-	T_{CPH}
HSYNC-first horizontal data time	T_{HBP}	121	153	184	T_{CPH}
DE pulse width	T_{EP}	-	720	-	T_{CPH}
VSYNC pulse width	T_{WV}	1	3	5	T_H
VSYNC-1st Data input (DE) time	T_{VBP}	4	20	35	T_H
VSYNC period	T_V	510	-	-	T_H

PARAMETER	Symbol	Min.	Typ.	Max.	Unit
SW pulse width	T_4	-	-	111	T_{CPH}
SW-SW non-overlap time	T_3	-	-	27	T_{CPH}
SOUT-SW front time	T_F	-	-	4	T_{CPH}
SW-SOUT back time	T_B	-	-	14	T_{CPH}

7.3.11 Parallel RGB interface (240RGBx400 resolution)

PARAMETER	Symbol	Min.	Typ.	Max.	Unit
DCLK frequency	F_{CPH}	9.36	-	-	MHz
DCLK period	T_{CPH}	-	-	106.8	ns
DCLK pulse duty	T_{CWH}	40	50	60	%
HSYNC period	T_H	-	306	-	T_{CPH}
HSYNC pulse width	T_{WH}	5	30	-	T_{CPH}
HSYNC-first horizontal data time	T_{HBP}	19	51	82	T_{CPH}
DE pulse width	T_{EP}	-	240	-	T_{CPH}
VSYNC pulse width	T_{WV}	1	3	5	T_H
VSYNC-1st Data input (DE) time	T_{VBP}	4	20	35	T_H
VSYNC period	T_V	510	-	-	T_H

PARAMETER	Symbol	Min.	Typ.	Max.	Unit
SW pulse width	T_4	-	-	37	T_{CPH}
SW-SW non-overlap time	T_3	-	-	9	T_{CPH}
SOUT-SW front time	T_F	-	-	2	T_{CPH}
SW-SOUT back time	T_B	-	-	4	T_{CPH}

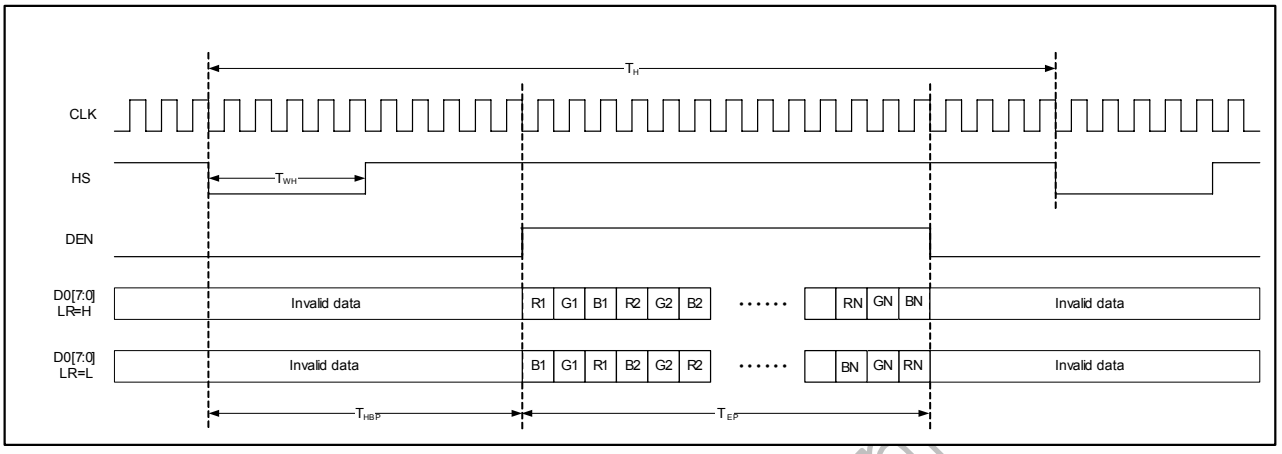


Figure 7. 3 Serial RGB Horizontal Data Format

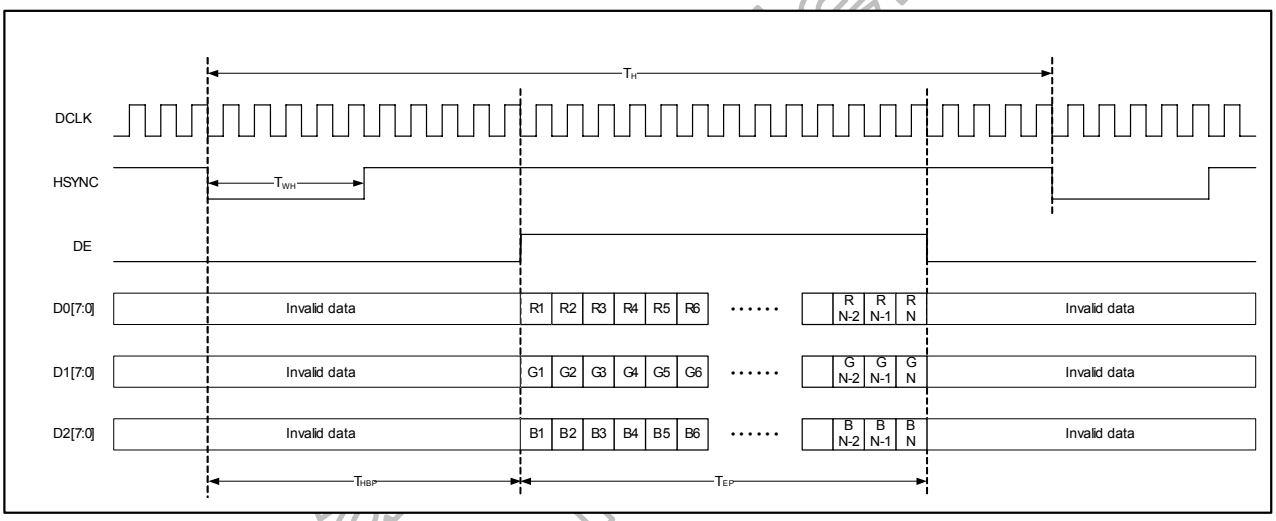


Figure 7. 4 Parallel RGB Horizontal Data Format

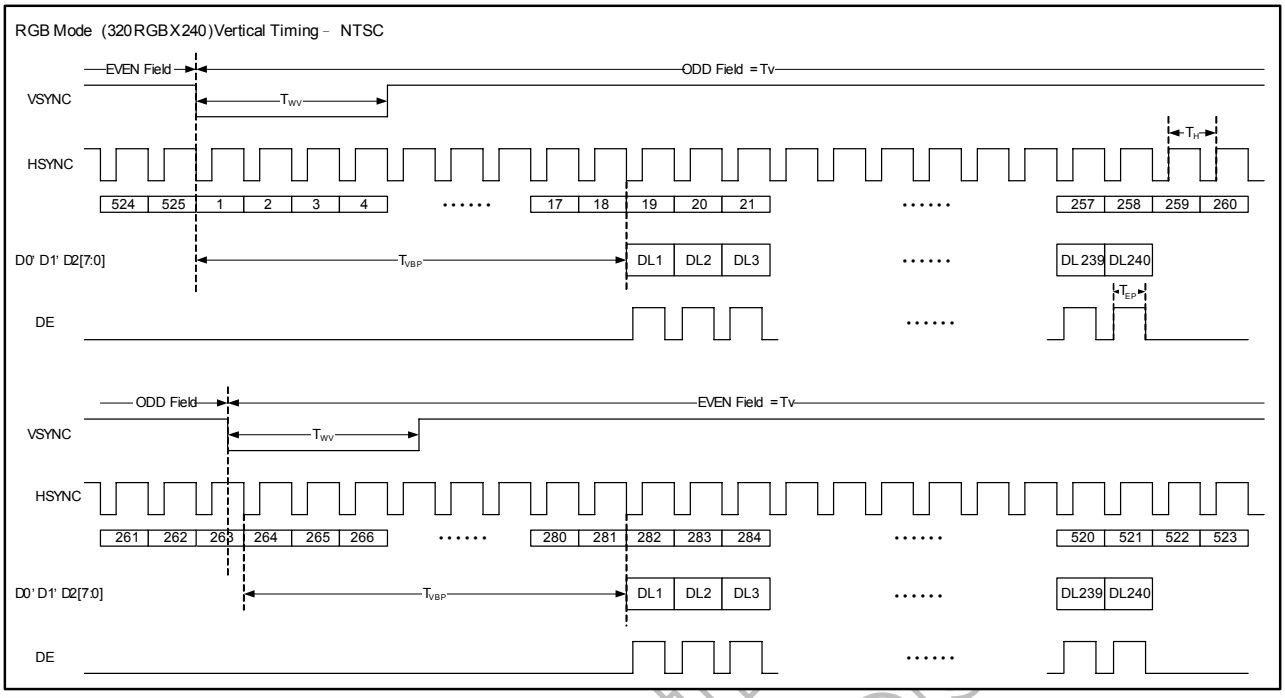


Figure 7. 5 Digital RGB NTSC mode Vertical Data Format for 262.5T_H

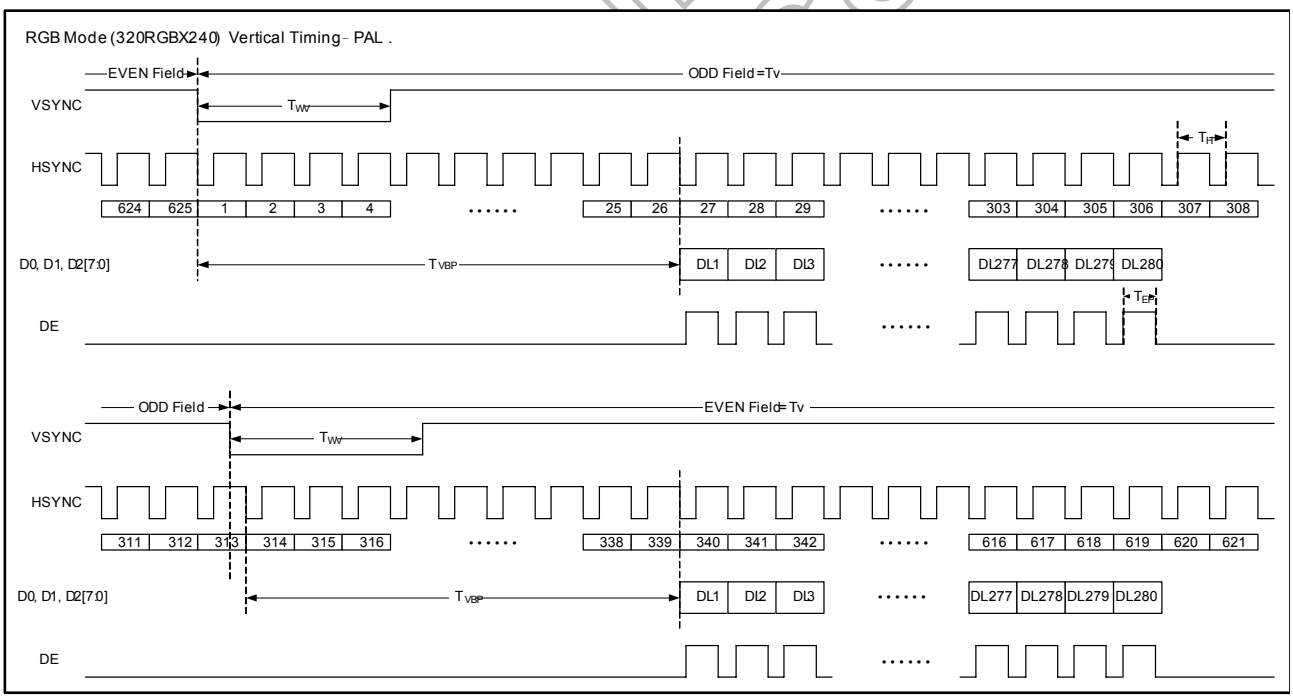


Figure 7. 6 Digital RGB PAL mode Vertical Data Format for 312.5T_H

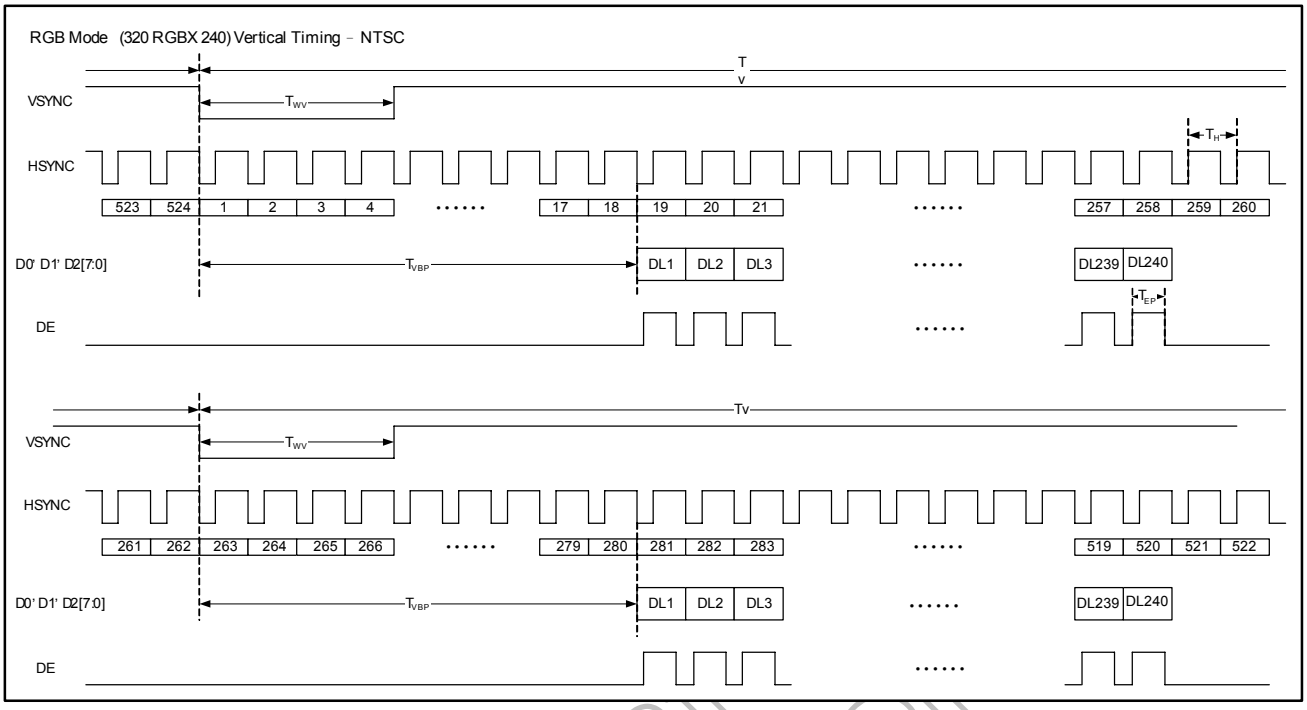


Figure 7. 7 Digital RGB NTSC mode Vertical Data Format for 262T_H

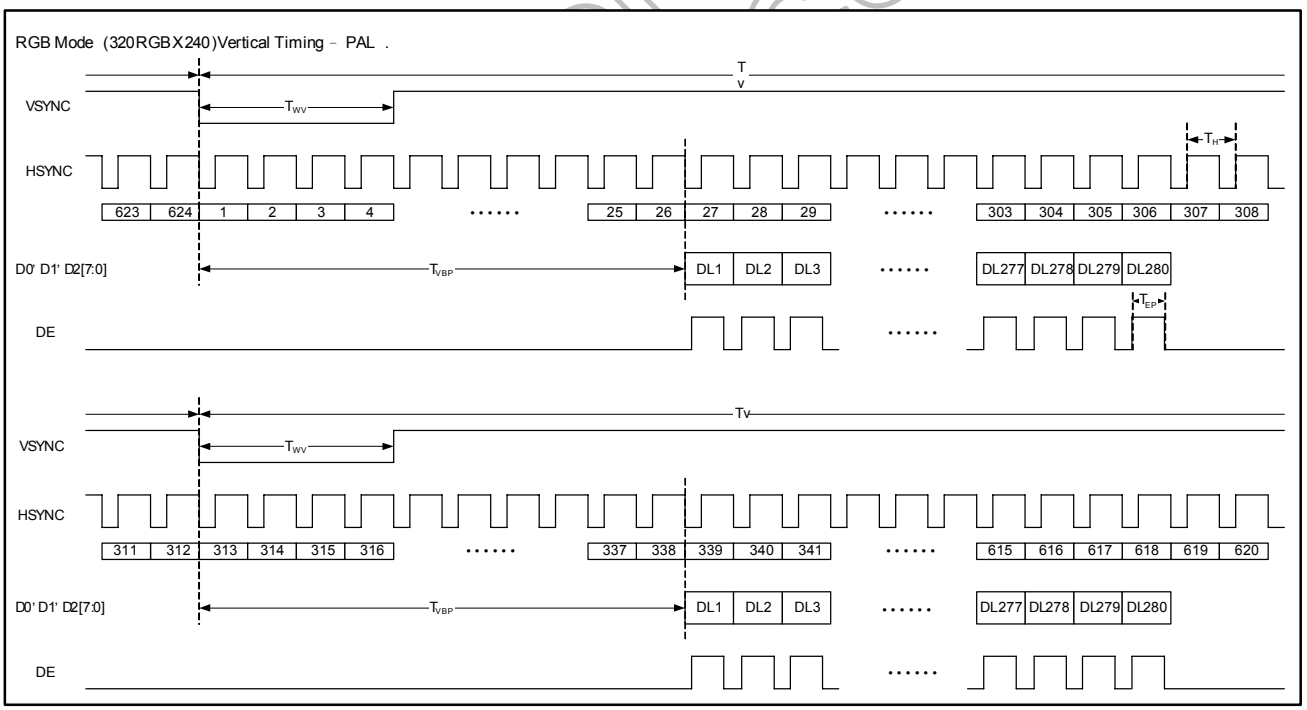


Figure 7. 8 Digital RGB PAL mode Vertical Data Format for 312T_H

7.3.12 Serial RGB Dummy interface (320RGBx240 resolution)

(For 24.54MHz, NTSC mode)

PARAMETER	Symbol	Min.	Typ.	Max.	Unit
DCLK frequency	F_{CPH}	-	24.54	-	MHz
DCLK period	T_{CPH}	-	40.7	-	ns
DCLK pulse duty	T_{CWH}	40	50	60	%
HSYNC period	T_H	-	1560	-	T_{CPH}
Horizontal active data area	T_{HA}	-	1280	-	T_{CPH}
VSYNC pulse width	T_{WV}		1.5		T_H
VSYNC-1st Data input time	T_{VBP}	4	17	-	T_H
VSYNC period	T_V	-	262.5	-	T_H

PARAMETER	Symbol	Min.	Typ.	Max.	Unit
SW pulse width	T_4	-	123	-	T_{CPH}
SW-SW non-overlap time	T_3	-	37	-	T_{CPH}
SOUT-SW front time	T_F	-	6	-	T_{CPH}
SW-SOUT back time	T_B	-	18	-	T_{CPH}

(For 27MHz)

PARAMETER		Symbol	Min.	Typ.	Max.	Unit
DCLK frequency		F_{cph}	-	27	-	MHz
DCLK period		T_{cph}	-	37	-	ns
DCLK pulse duty		T_{CWH}	40	50	60	%
HSYNC period	NTSC	T_H	-	1716	-	T_{CPH}
	PAL	T_H	-	1728	-	T_{CPH}
Horizontal active data area		T_{HA}	-	1440	-	T_{CPH}
VSYNC pulse width		T_{WV}		1.5		T_H
VSYNC-1st Data input time		T_{VBP}	4	17	-	T_H
VSYNC period	NTSC	T_V	-	262.5	-	T_H
	PAL	T_V	-	312.5	-	T_H

PARAMETER	Symbol	Min.	Typ.	Max.	Unit
SW pulse width	T_4	-	135	-	T_{CPH}
SW-SW non-overlap time	T_3	-	40	-	T_{CPH}
SOUT-SW front time	T_F	-	6	-	T_{CPH}
SW-SOUT back time	T_B	-	20	-	T_{CPH}

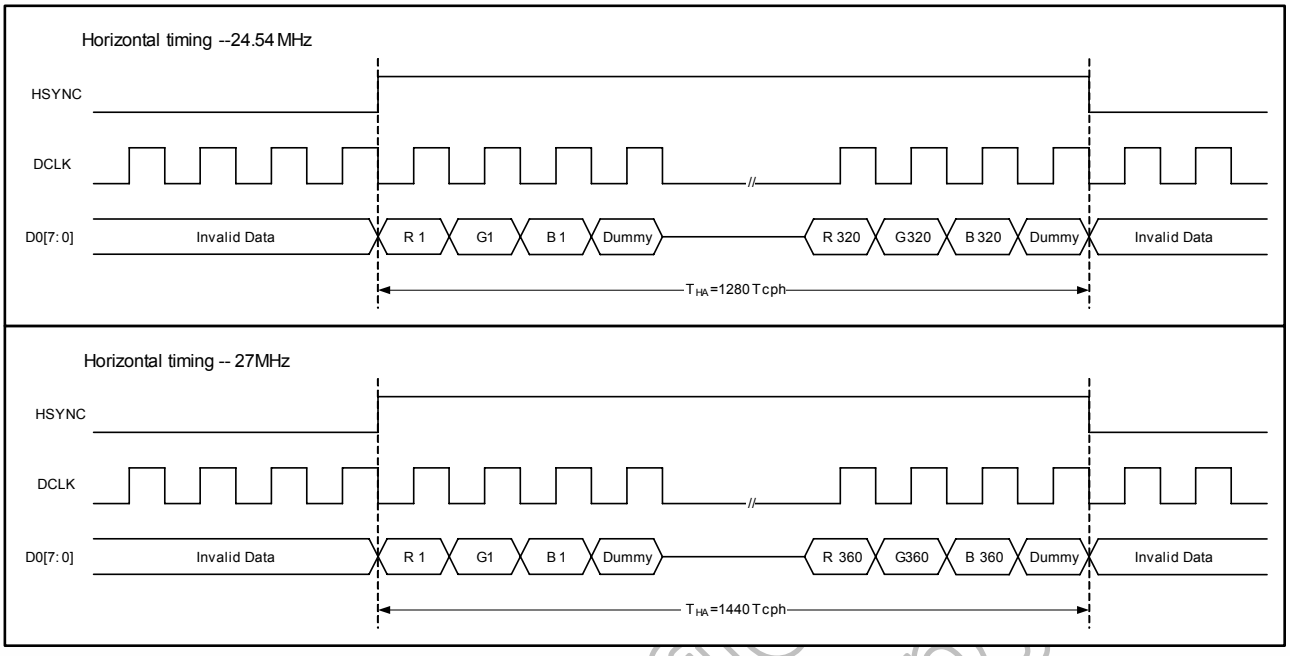


Figure 7. 9 RGB Dummy Horizontal Data Format

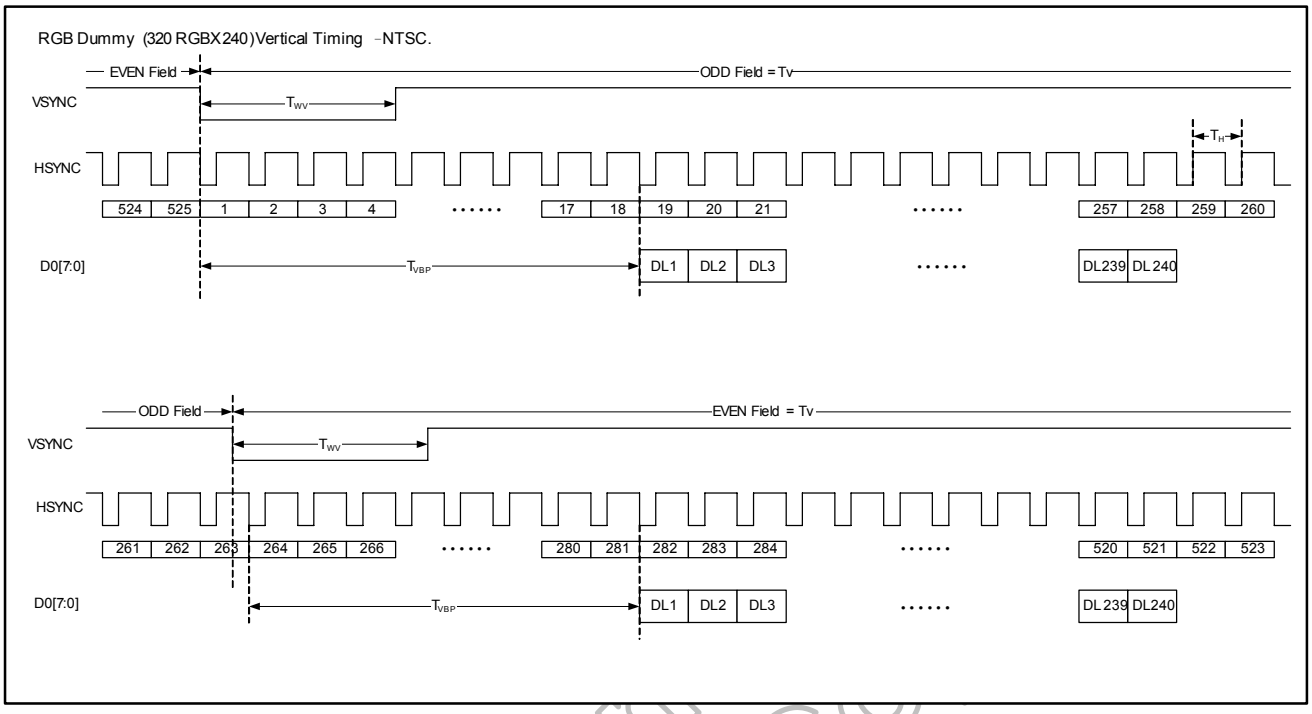


Figure 7. 10 RGBDummy NTSC mode Vertical Data Format for 262.5H

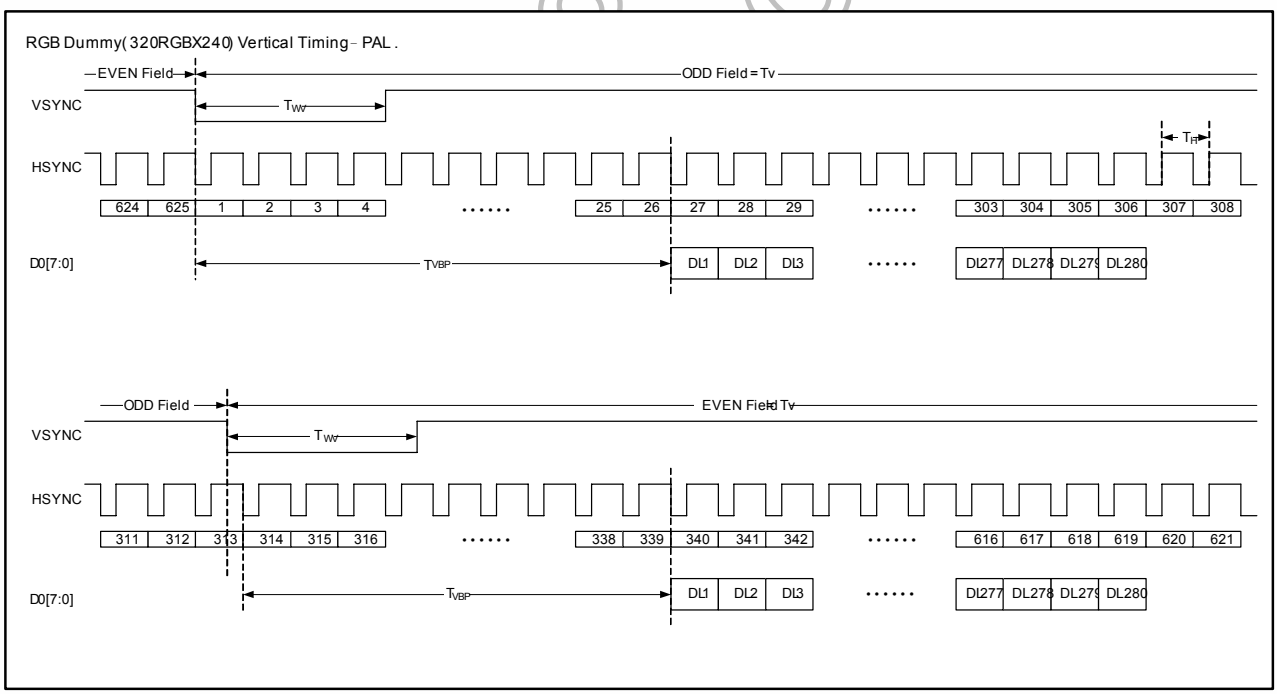


Figure 7. 11 RGBDummy PAL mode Vertical Data Format for 312.5H

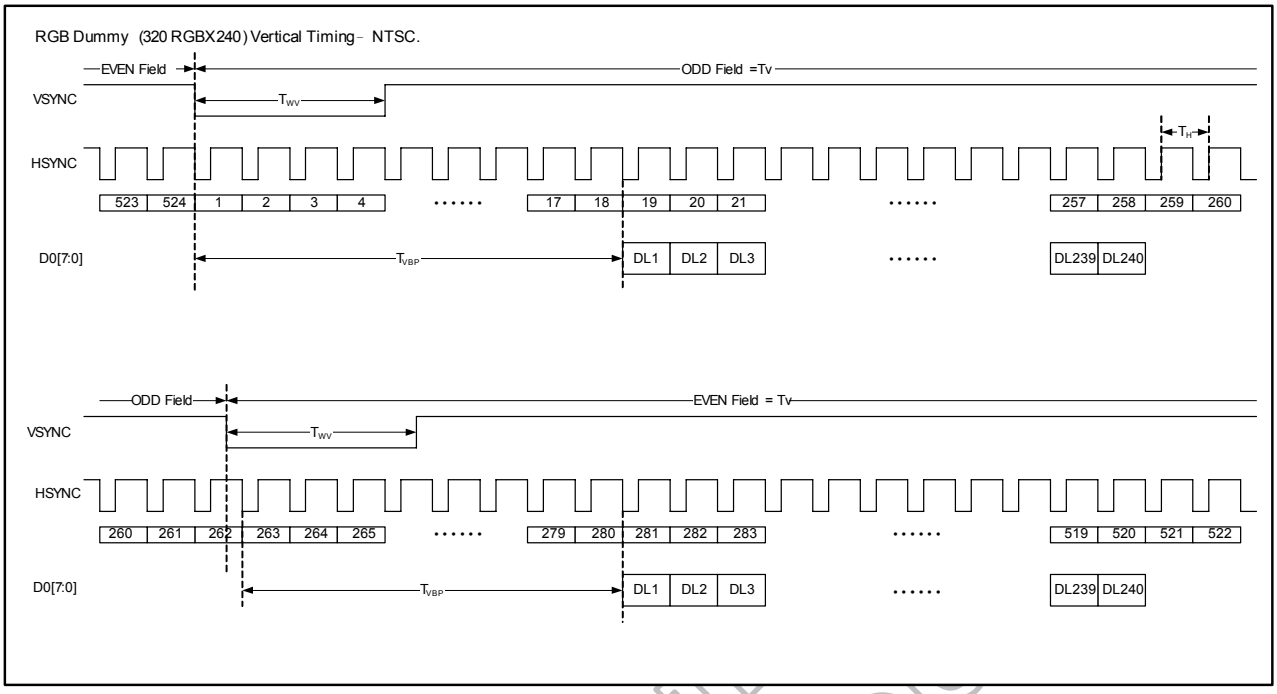


Figure 7. 12 RGBDummy NTSC mode Vertical Data Format for 262H

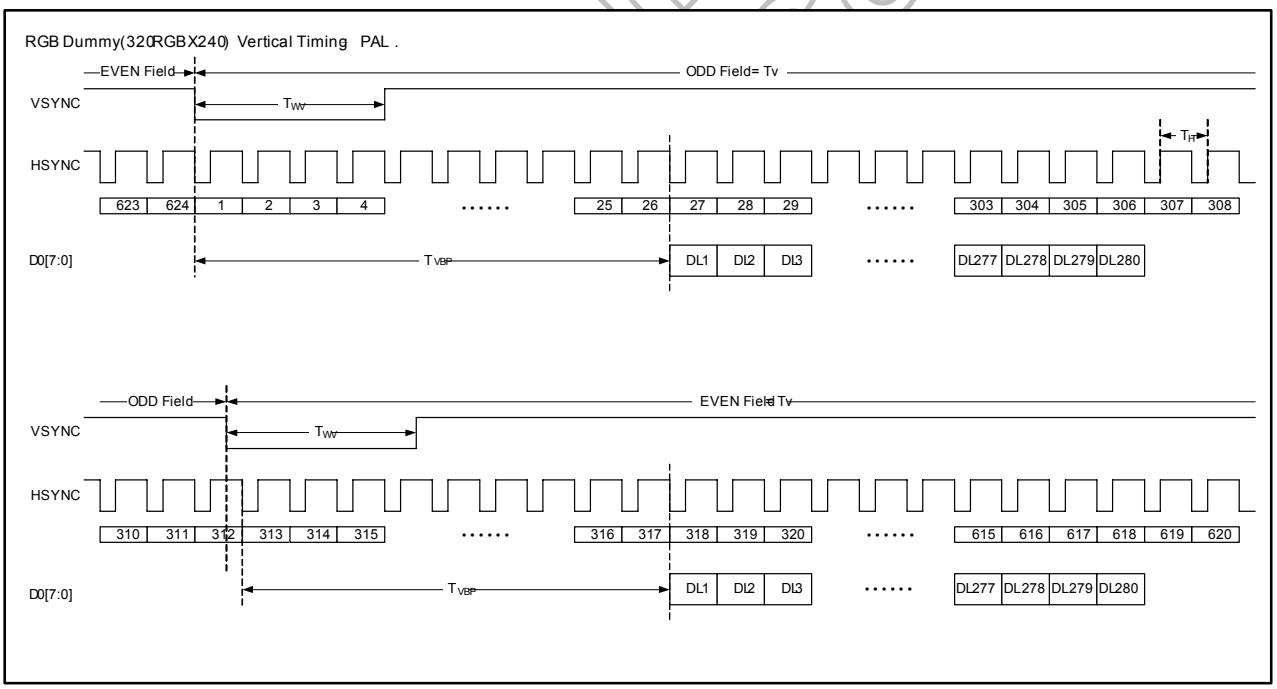


Figure 7. 13 RGBDummy PAL mode Vertical Data Format for 312H

7.3.13 CCIR601 interface (320RGBx240 and 480RGBx234 resolution)

(For 24.54MHz, NTSC mode)

PARAMETER	Symbol	Min.	Typ.	Max.	Unit
DCLK frequency	F_{CPH}	-	24.54	-	MHz
DCLK period	T_{CPH}	-	40.7	-	ns
DCLK pulse duty	T_{CWH}	40	50	60	%
HSYNC period	T_H	-	1560	-	T_{CPH}
Horizontal active data area	T_{HA}	-	1280	-	T_{CPH}
VSYNC pulse width	T_{WV}		1.5		T_H
VSYNC-1st Data input time	T_{VBP}	4	17	-	T_H
VSYNC period	T_V	-	262.5	-	T_H

PARAMETER	Symbol	Min.	Typ.	Max.	Unit
SW pulse width	T_4	-	123	-	T_{CPH}
SW-SW non-overlap time	T_3	-	37	-	T_{CPH}
SOUT-SW front time	T_F	-	6	-	T_{CPH}
SW-SOUT back time	T_B	-	18	-	T_{CPH}

(For 27MHz)

PARAMETER		Symbol	Min.	Typ.	Max.	Unit
DCLK frequency		F_{cph}	-	27	-	MHz
DCLK period		T_{cph}	-	37	-	ns
DCLK pulse duty		T_{CWH}	40	50	60	%
HSYNC period	NTSC	T_H	-	1716	-	T_{CPH}
	PAL	T_H	-	1728	-	T_{CPH}
Horizontal active data area		T_{HA}	-	1440	-	T_{CPH}
VSYNC pulse width		T_{WV}		1.5		T_H
VSYNC-1st Data input time		T_{VBP}	4	17	-	T_H
VSYNC period	NTSC	T_V	-	262.5	-	T_H
	PAL	T_V	-	312.5	-	T_H

PARAMETER	Symbol	Min.	Typ.	Max.	Unit
SW pulse width	T_4	-	135	-	T_{CPH}
SW-SW non-overlap time	T_3	-	40	-	T_{CPH}
SOUT-SW front time	T_F	-	6	-	T_{CPH}
SW-SOUT back time	T_B	-	20	-	T_{CPH}

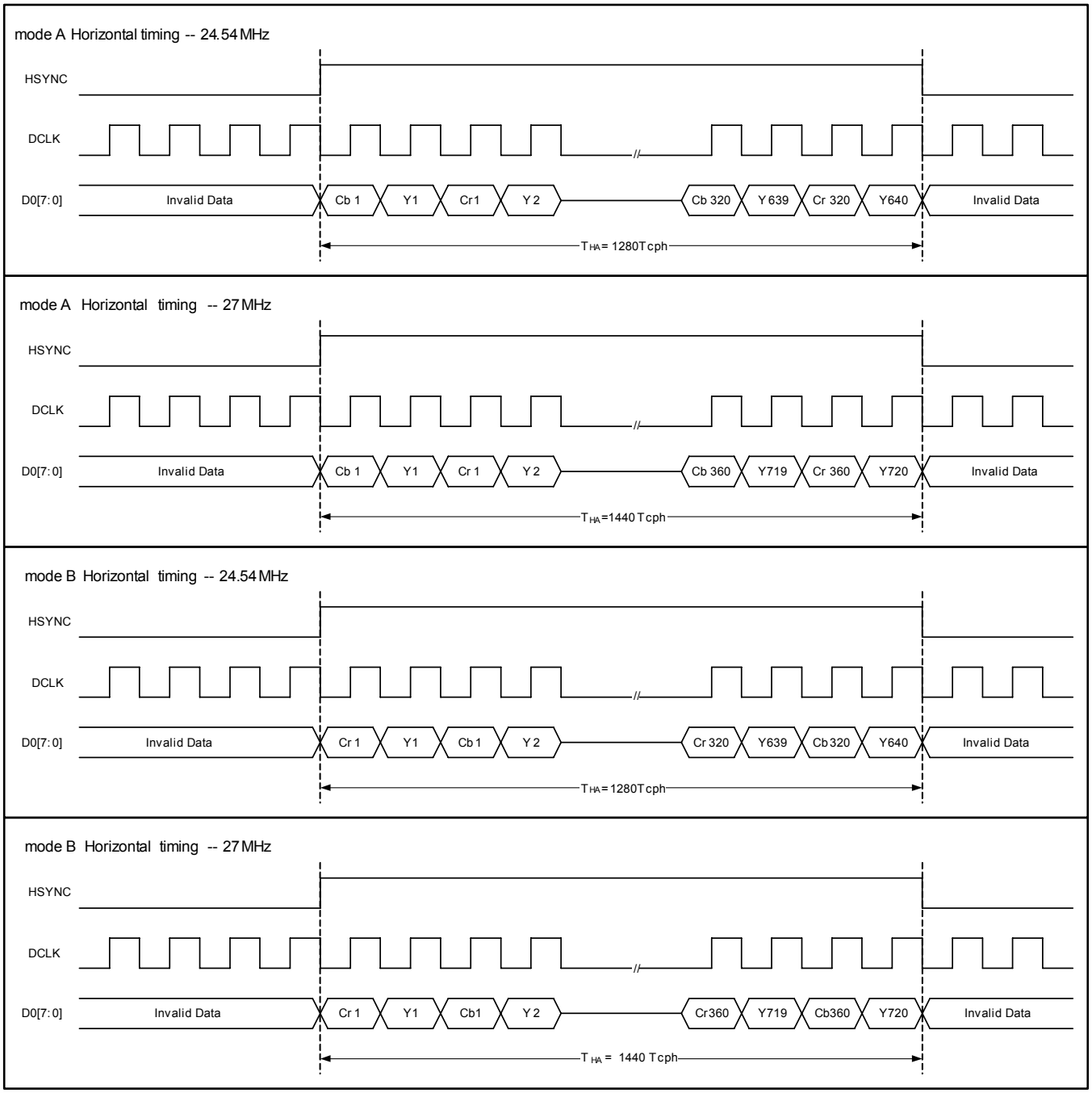


Figure 7. 14 CCIR601 Horizontal Data Format

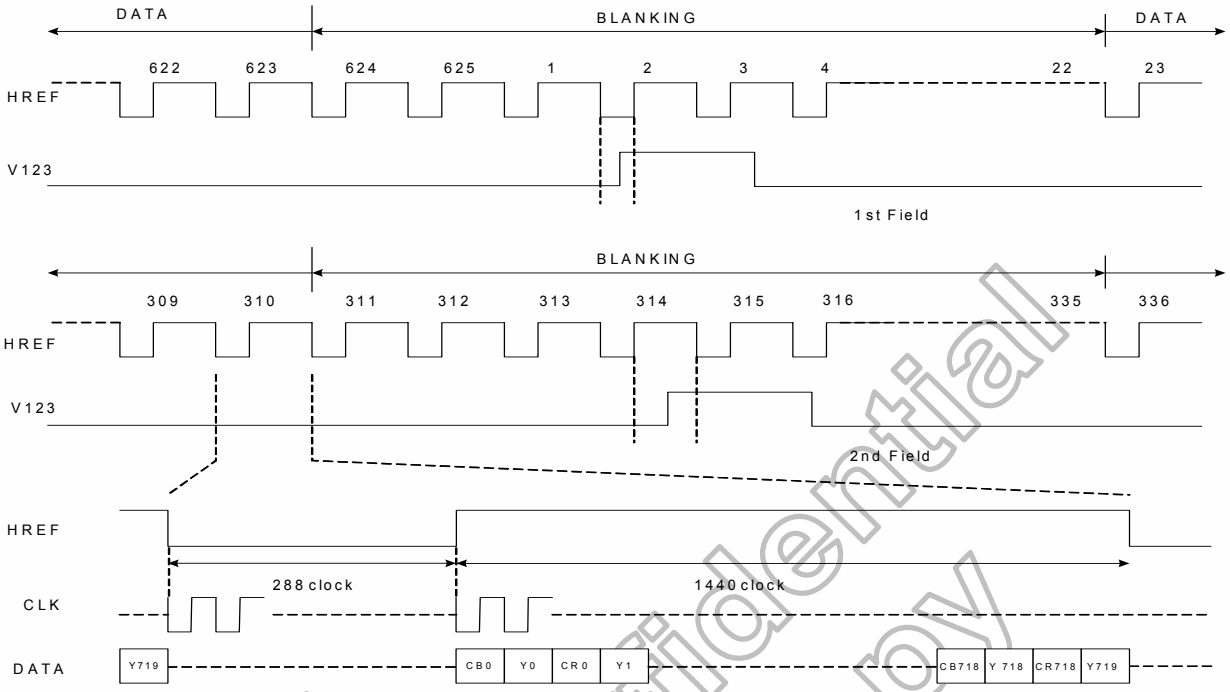


Figure 7. 15 CCIR601 Vertical Data Format -- NTSC

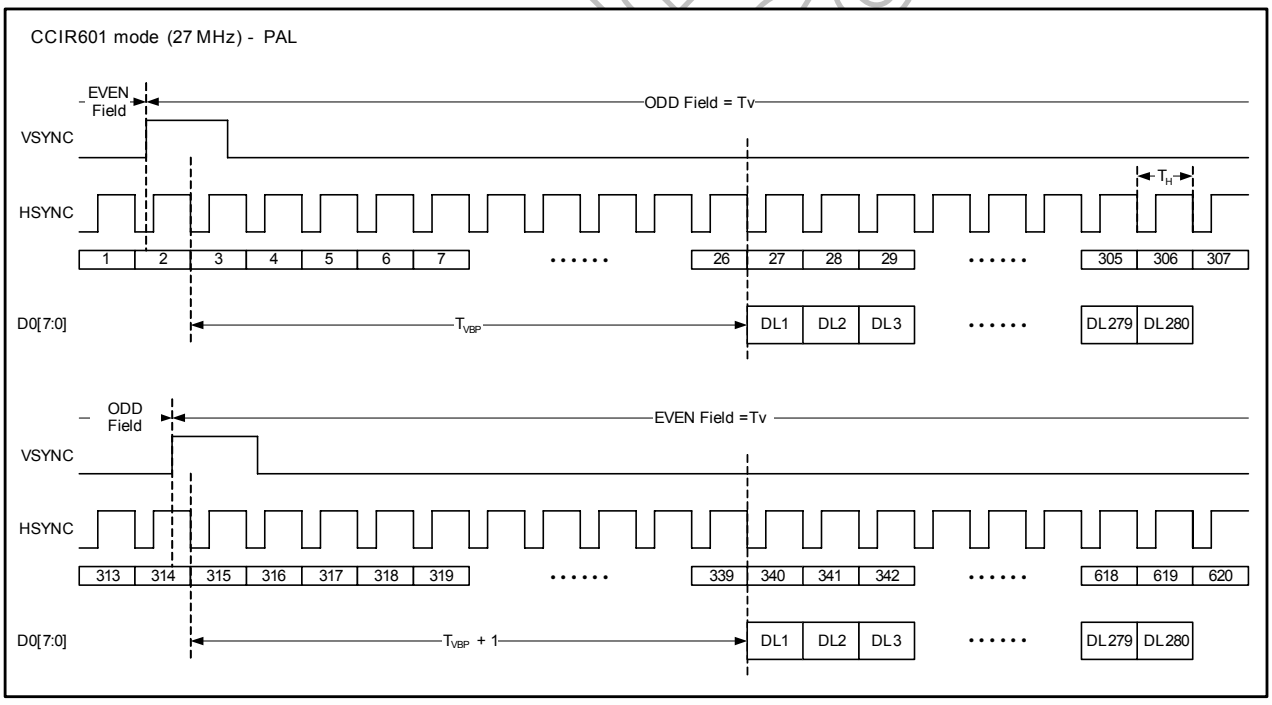


Figure 7. 16 CCIR601 Vertical Data Format -- PAL

7.3.14 CCIR656 interface (320RGBx240 and 480RGBx234 resolution)

PARAMETER		Symbol	Min.	Typ.	Max.	Unit
DCLK frequency		F_{CPH}	-	27	-	MHz
DCLK period		T_{CPH}	-	37	-	ns
DCLK pulse duty		T_{CWH}	40	50	60	%
HSYNC period	NTSC	T_H	-	1716	-	T_{CPH}
	PAL	T_H	-	1728	-	T_{CPH}
Horizontal active data area		T_{HA}	-	1440	-	T_{CPH}
VSYNC-1st Data input time	NTSC	T_{VBP}	-	20	-	T_H
	PAL	T_{VBP}	-	20	-	T_H
VSYNC period	NTSC	T_V	-	262.5	-	T_H
	PAL	T_V	-	312.5	-	T_H

PARAMETER	Symbol	Min.	Typ.	Max.	Unit
SW pulse width	T_4	-	135	-	T_{CPH}
SW-SW non-overlap time	T_3	-	40	-	T_{CPH}
SOUT-SW front time	T_F	-	6	-	T_{CPH}
SW-SOUT back time	T_B	-	20	-	T_{CPH}

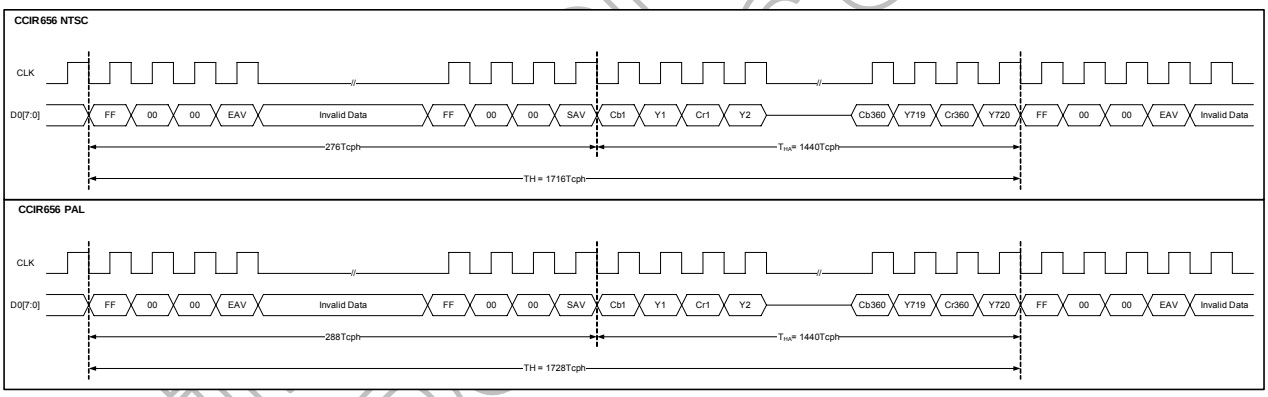


Figure 7. 17 CCIR656 Horizontal Data Format

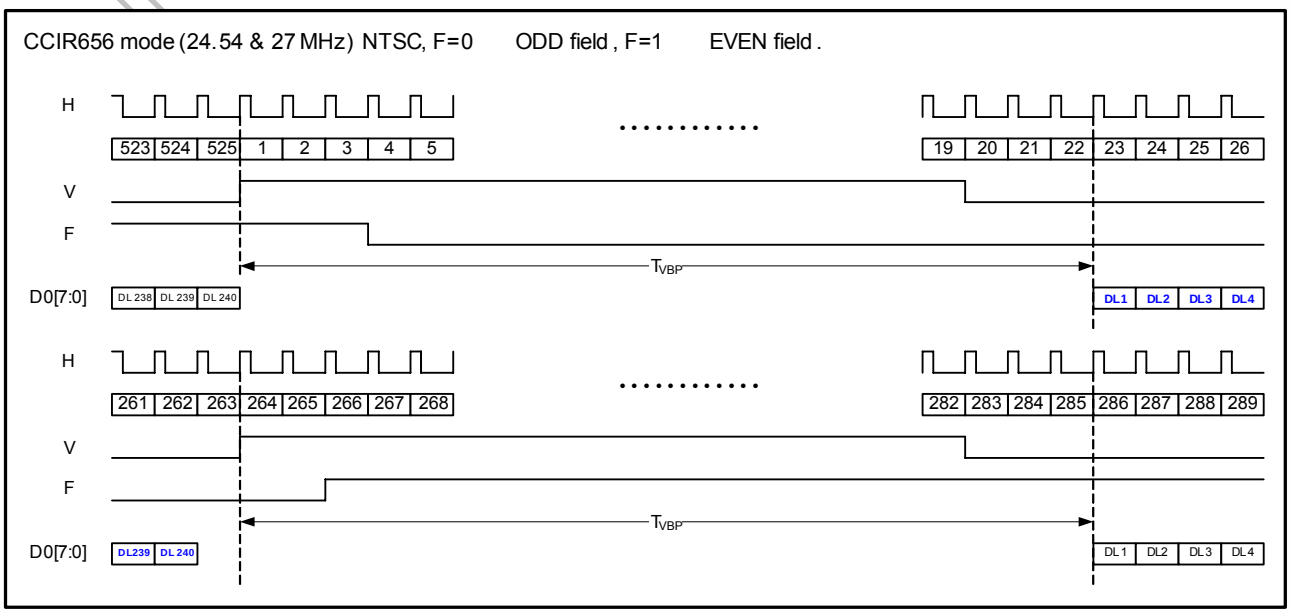


Figure 7. 18 CCIR656 NTSC Vertical Data Format -- NTSC

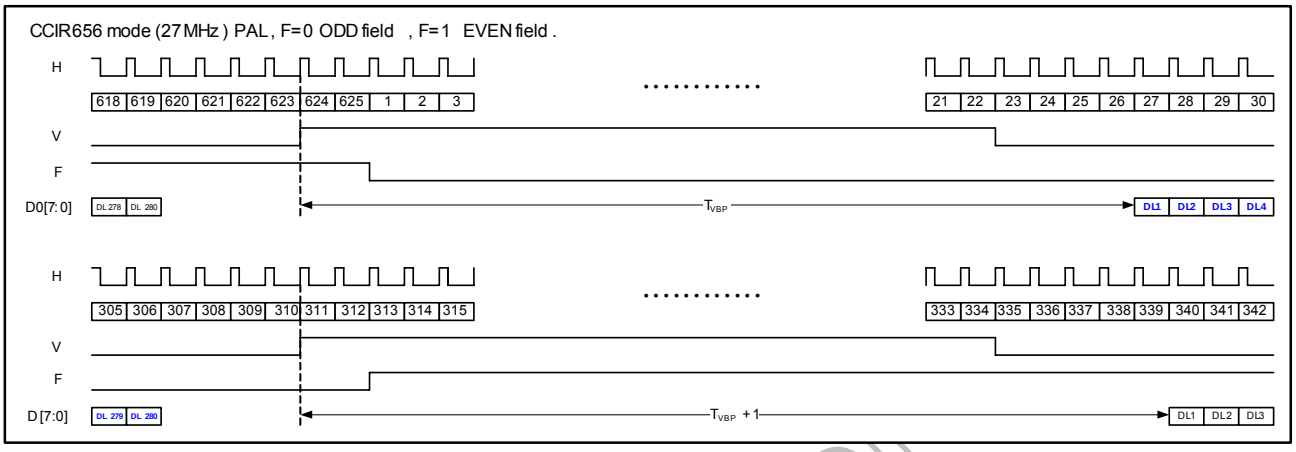


Figure 7. 19 CCIR656 NTSC Vertical Data Format -- PAL

7.3.15 Hardware reset timing

PARAMETER	Symbol	Min.	Typ.	Max.	Unit
RESETB low pulse width	T_{RSB}	10	-	-	µs
STB to Vsync Setup Time	T_{STB}	20	-	-	ns

7.4 Output waveform

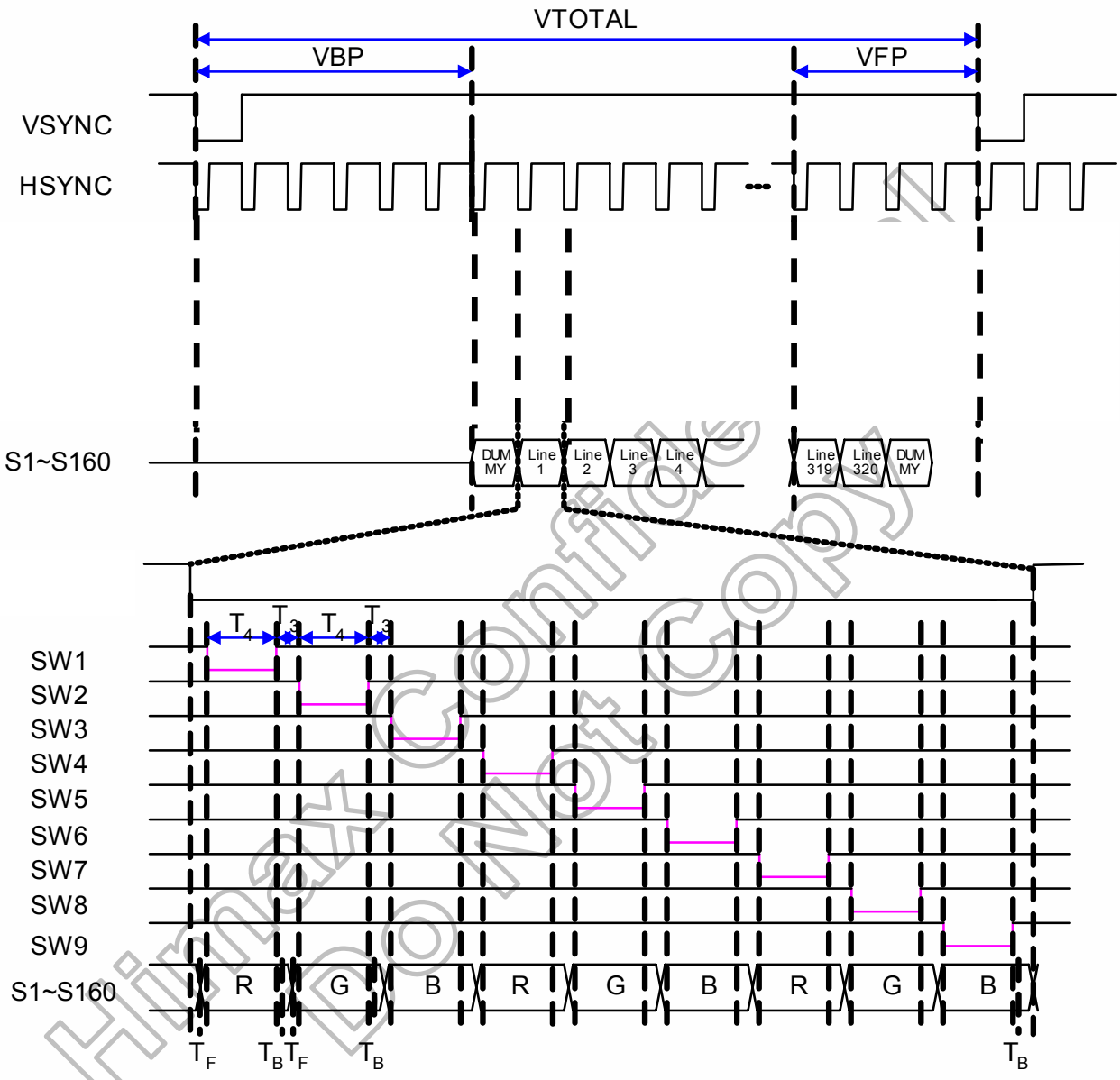


Figure 7. 20 SCAN output timing at odd line (SW=00, RL=1)

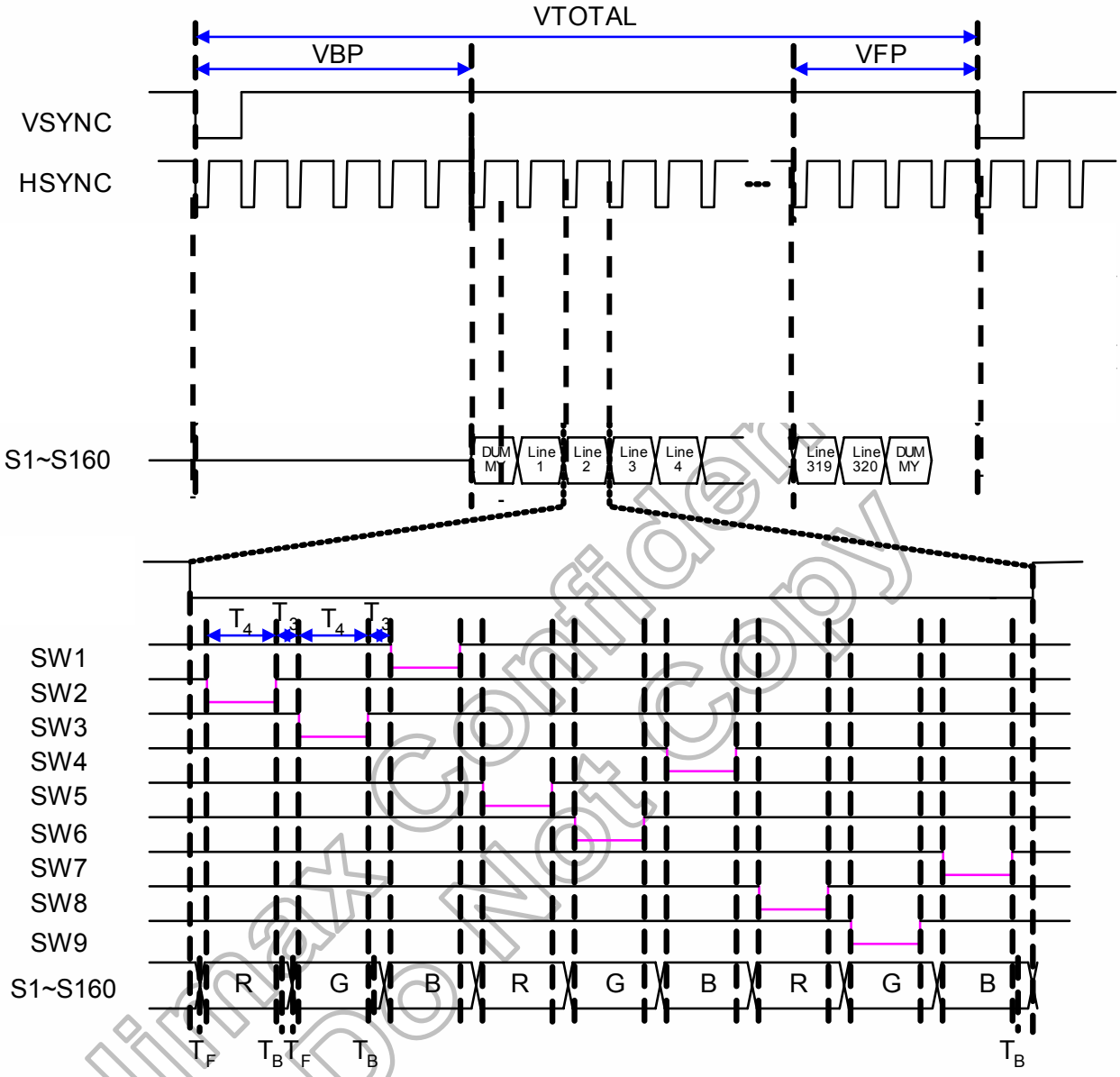


Figure 7. 21 SCAN output timing at even line (SW=00, RL=1)