PCB Libraries – Library Specification

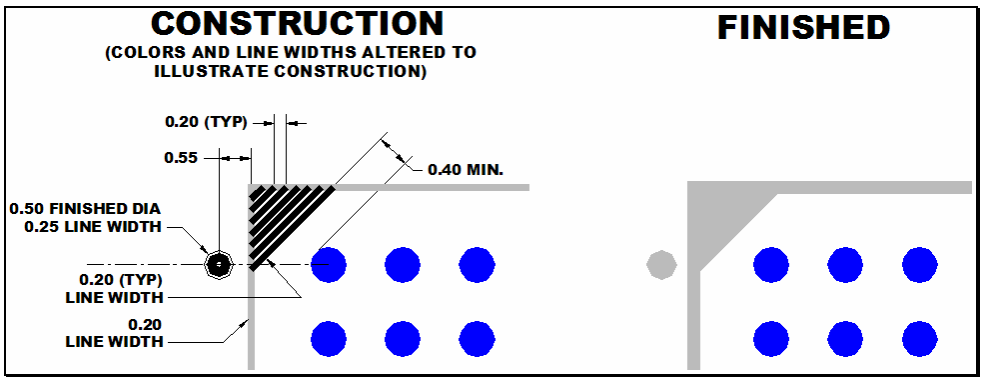
Assembly Outline

1. Layer_27 (Assembly Top)
2. Line Width: 0.2mm
3. Shape: Closed Polygon

Assembly Reference Designator

1. Size: 2mm Height X 0.2mm Width
2. Justification: Center / Center
3. Right Reading: Orthogonal
4. Location: 0.1mm X 0.1mm (except through hole connectors, then check for Ref Des on pad)
5. Layer_27

BGA Polarity Marking Detail



Geometry Height

1. PRO-E Height is defined in the Part-Type Attribute Geometry.Height
2. The Geometry.Height is defined in mm
3. A .001 closed polygon component outline is drawn on layer_25

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Land Pattern Origin

1. All SMT devices have centroid origins
2. Through Hole Connectors have Pin 1 origins
3. When the origin is not on a through hole pad, an origin crosshair should exist:
    a. 0.1mm Line Width
    b. Layer_20
    c. Overall height & Width 1mm x 1mm
    d. Shape: Path

Library Documentation

1. See **Library_Index.doc** for the master Table of Contents. Folder: Metric Environment\Library Documentation

Local Fiducials

1. Placed on QFPS landpatterns when the Pin Pitch is below 0.635mm as the last two pins in the part
2. Layer 1 Pad Size 1mm Round
3. Assembly Top Pad Size 1mm Round
4. Solder Mask Pad Size 2mm Round
5. Drill Size 0 (Zero)

Metric System

1. All parts are built in metric units
2. Check for any coordinates that go beyond more than three places past the decimal point
3. All numbers on any feature (except Post Assembly Dots) should be divisible by 0.05mm

Mounting Holes

1. Inch Sizes: #2, #4, #6 and #8
2. Metric Sizes: M2, M2.5, M3 and M3.5
3. Available with 8 via holes
4. Available Plated or Non-plated
5. See **Padstacks.pdf**

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Naming Convention

1. See **Landpattern Naming Convention.pdf**

Padstacks - Through Hole and Connector Libraries

1. See **Padstacks.pdf** Excel spreadsheet for Plated & Non-plated sizes
2. Padstack Features:
    a. Full padstacks include Solder Mask and Assembly data
    b. Hole size is 0.3mm larger than lead size
    c. All hole sizes are in increments of 0.05mm
    d. Pad sizes are gradually scaled up to establish correct current carrying capability
    e. Split/Mixed Anti-pad & Custom Thermals are defined on “Inner Layers”
3. Non-plated holes have a keepout on All Layers 0.6mm greater than hole size
4. Minimum of 0.30mm space between pads

Padstacks – Surface Mount SML, SMN & SMM and SMT Connector Libraries

1. See **IPC-SM-782** for Toe, Heel and side fillet data
2. Padstack Features:
    a. Full padstacks include Solder Mask, Paste Mask and Assembly data
    b. Solder Mask size is 1:1 scale of pad size
    c. Paste Mask size is 1:1 scale of pad size
    d. Inner and Bottom Layers are Zero Width and Round Shape
3. Non-plated holes have a keepout on All Layers 0.6mm greater than hole size
4. Hole Size 0 (Zero)

Pick and Place Rotation

1. The JEDEC JEP95 publication was used as a reference to decide all land pattern zero rotation
2. When adding parts to a particular family, use same rotation (Orientation)

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Placement Courtyard

(Used only on parts that have silkscreen outline inside the pins)

1. See IPC-SM-782_2002.doc for placement courtyard size and round-off data
2. Layer_20
3. Line Width 0.1mm
4. Shape: Closed Polygon
5. Use: To verify design rules for “Body to Body” clearance

Post Assembly Inspection Dots

(Used whenever a component can be assembled backwards)

1. Used whenever a component can be assembled backward (Inverted)
2. Size: 0.25mm Line Width X 0.125mm Radius = Overall Size: 0.5mm
3. Location 1: Placed by Pin 1, inside placement courtyard as much as possible
4. Location 2: Placed 0.25mm minimum away from exposed copper, 0.3mm preferred
5. Location 3: Placed 0.2mm away from silkscreen outline when the silkscreen is outside the pins
6. Layers 1 & 27

Silkscreen Outline

1. Layer_1
2. 0.2mm Width
3. Tolerance: 0.3mm away from exposed copper
4. See **Definitions_Index.Doc** for all Table of Contents to all the Library Definitions

Silkscreen “Free” Text (Not Ref Des)

1. Layer_26
2. Size: 1.5mm Height X 0.15mm Width
3. Justification: Left / Center

PCB Libraries – Library Specification

Silkscreen Polarity Marking

1. Layer_1
2. IC polarity markings: 2D-Line Circle 0.6mm Width X 0.3mm Diameter (Overall Finished Size: 1.2mm)
3. IC polarity marking location: Placed 1mm X 1mm from silkscreen outline corner closest to pin 1
4. Diode polarity markings: 2D-Line Paths spaced 0.15mm apart. Overall Finished Size: 1mm
5. Diode location: Placed on the Anode side of the diode
6. Through Hole Capacitor polarity markings: 0.2mm wide 2D-Line crosshair. Size: 1.5mm X 1.5mm
7. Capacitor location: Inside the silkscreen outline near the upper left corner

Silkscreen Reference Designator

1. Size: 1.5mm Text Height X 0.15mm Font Line Width
2. Justification: Left / Center
3. Right Reading: Orthogonal
4. Location: -1.3mm X 0.1mm
5. Layer_1

Three Complexity Levels for SMT Landpatterns

1. Least Environment Use
2. Nominal Environment Use
3. Maximum Environment Use

Tab: Part-Type “General”

1. If a part is in a connector library, the Connector Box should be checked
2. Check for any coordinates that go beyond more than three places past the decimal point
3. ECO Registered Part

Tab: Part-Type “PCB Decals”

1. Decal Name and Part-Type Name must match (except the MISC Library)

PCB Libraries – Library Specification

Tab: Part-Type “Attribute”

1. Checked By
2. Checked Date (YY-MM-DD)
3. Created By
4. Created Date (YY-MM-DD)
5. Description
6. Geometry.Height (the value is always followed by “mm”
7. Manufactured By #1
8. Manufactured By #2
9. Part Number

Tab: Part-Type “Alphanumeric Pins”

1. If one pin is assigned an Alphanumeric value that all pins are assigned an Alphanumeric value
2. Common Pin Names:

Diode:	Anode = A
	Cathode = C
Transistor:	Base = B
	Emitter = E
	Collector = C
Power Fet:	Source = S
	Gate = G
	Drain = D

Through Hole Diode Polarity Marking Detail