PCB Design Optimization Starts in the CAD Library

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PCB Libraries™

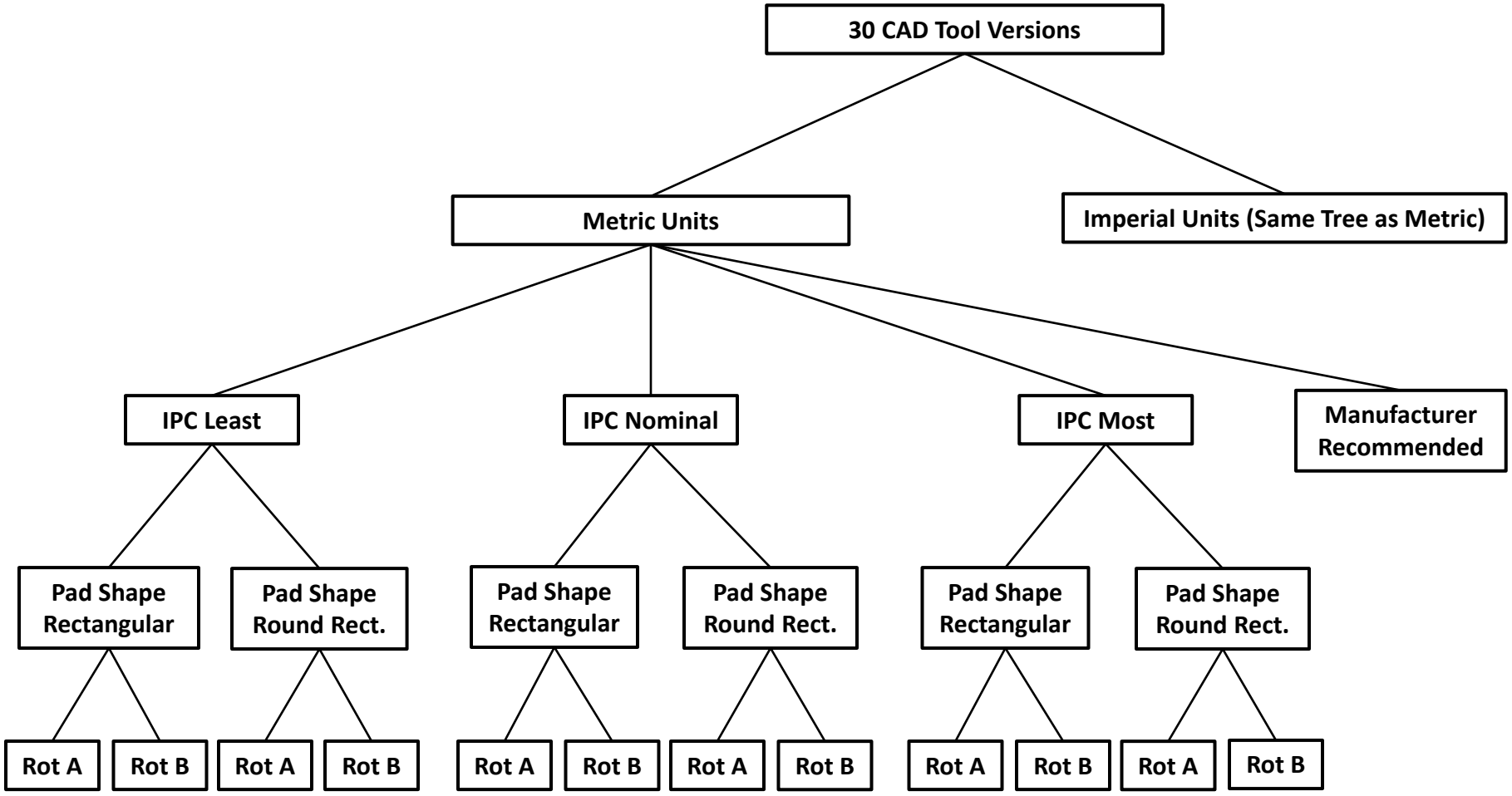
Market & Standards Confusion

- The electronics industry is split down the middle, Metric units Vs. Inch units. CAD vendors, PCB Fabrication and most American government contractors default to the Inch Unit System, while private enterprise companies use the Metric Unit system.
- Terms & Definitions – Footprint Vs. Land pattern
  - Footprint, mid 1980's OrCAD Capture for PCB library part
  - Land Pattern, March 1987 IPC-SM-782, however the IPC-T-50 definition of "Footprint" is "**See Land Pattern**". But some say a Footprint is really the component pattern
- Terms & Definitions – Pad Vs. Land (all CAD vendors use Pad)
- Terms & Definitions – Chip Component names, Metric units Vs. Inch units (1206 or 3216, 0805 or 2012, 0603 or 1608)
- IC Land (Pad) Shape – Rectangle, Oblong & Rounded Rectangle

Challenges For Library Automation

- Companies use various CAD tools and various versions of CAD tools and the PCB library is usually not backward compatible due to new features. Some companies even use obsolete CAD tools like P-CAD, OrCAD Layout and Protel.
- CAD vendors are consistently upgrading their tools and the format is consistently changing. Writing translators for each CAD tool version is challenging.
- CAD vendors do not support importing a neutral library format and they protect their data via Binary code or Encrypted data.
- Component manufacturer's cannot be responsible for creating PCB libraries that support over 30 different CAD tool versions.
- Component manufacturer's are creating unique component packages that require complex land patterns (footprints)
- There are too many land pattern (footprint) options.

Land Pattern (Footprint) Options



30 CAD tools X 2 (metric & mils) = 60 x 4 tiers = 240 X 3 pad shapes = 720 X 2 Rotations = 1,440

Land Pattern (Footprint) Preferences

Drafting Options

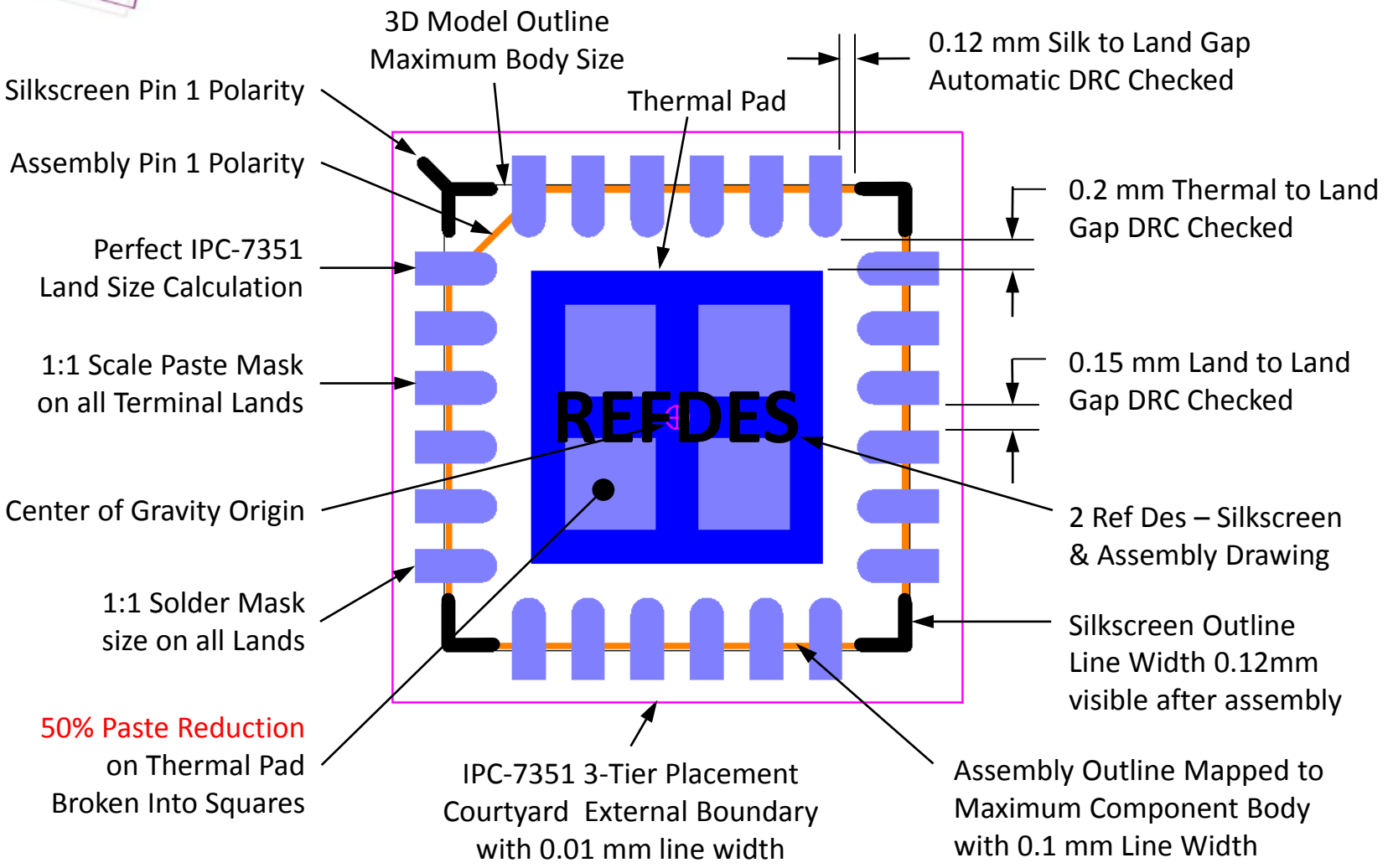
- Silkscreen Outline Line Width
- Silkscreen Outline Polarity Marker
- Map Silkscreen to Nom or Max Body
- Silkscreen to Land (Pad) Clearance
- Silkscreen Place Round-off
- Silkscreen Ref Des Height
- Assembly Outline Line Width
- Assembly Outline Polarity Marker
- Map Assembly to Nom or Max Body
- Assembly Outline Place Round-off
- Assembly Ref Des Min/Max Heights
- Courtyard Line Width
- 3D Model Line Width

Design Rule Options

- Metric or Mils
- 3-Tier Environment
- Land (Pad) Shape
- Land to Land Clearance
- Land to Thermal Pad Clearance
- Gang Mask Contour or Block
- Minimum Pad Trim Height
- Rounded Rectangle % of Width
- Rounded Rectangle Max Radius
- Rounded Rectangle Round-off
- Solder/Paste Mask Over/Under
- Thermal Paste Mask Reduction
- Local Fiducial Sizes & Min Pitch

Anatomy of a PCB Library

QFN Land Pattern Details



Anatomy of a PCB Library

- IPC-7351 3-Tier Library System for SMT
- Solder Joint Calculations & Manufacturing Tolerances
- Component Package Lead Styles
- Land Pattern Naming Convention
- Padstack Naming Convention
- Placement Courtyard
- Local Fiducials
- Zero Component Orientation
- Land Pattern Origins
- Silkscreen & Assembly Outlines and Polarity Marking
- Reference Designators
- 3D Modeling

Past & Future Innovation

Old Concepts	New Ideas
Universal Grid Round-off 0.05 (2 mils)	Universal Grid Round-off 0.01 (1 mil)
Silkscreen Outline Under Components	Functional Silkscreen Outline
1 Local Fiducial Size for 3-Tiers	3 Local Fiducial Sizes for 3-Tiers
1 Silkscreen Line Width for 3-Tiers	3 Silkscreen Line Widths for 3-Tiers
1 Silkscreen Ref Des Height for 3-Tiers	3 Silkscreen Ref Des Heights for 3-Tiers
1 Silkscreen to Land Clearance 0.25 (10)	3-Tier Silkscreen to Land Clearance
Multiple Shape Polarity Marking	Single Shape Polarity Marking
Multiple Assembly Polarity Markings	Single Assembly Polarity Marking
Lands on Assembly Drawing	On/Off Switch for Lands on Assembly
IPC/EIA Component Dimension Letters	JEDEC Component Dimension Letters
Predominant Metric Units	Acceptance of Imperial & Metric Units
Land Trim Component Stand-off 0.15 (6)	No Land Trimming Under Components
Thermal Pad Paste Mask Reduction 40%	Thermal Pad Paste Mask Reduction 50%
Minimum Land to Land Space 0.20 (8)	Minimum Land to Land Space 0.15 (6)

IPC-7351 3-Tier Library System

- Three land pattern geometry variations are supplied for each of the device families; Maximum Land Protrusion (Density Level A), Nominal Land Protrusion (Density Level B) and Least Land Protrusion (Density Level C).
- **Density Level A:** Maximum (Most) Land Protrusion – For low-density product applications, the 'maximum' land pattern condition has been developed to accommodate wave or flow solder of leadless chip devices and leaded gull wing devices. The geometry furnished for these devices, as well as inward and "J" - formed lead contact device families, may provide a wider process window for reflow solder processes as well.

Note: Some companies use Most Land Protrusion but Nominal Placement Courtyard & Silkscreen Marking

IPC-7351 3-Tier Library System

- **Density Level B**: Median (Nominal) Land Protrusion – Products with a moderate level of component density may consider adapting the 'median' land pattern geometry
- The median land patterns furnished for all device families will provide a robust solder attachment condition for reflow solder processes and should provide a condition suitable for wave or reflow soldering of leadless chip and leaded Gull Wing type devices

- **Note: there is no “special” land pattern requirement for Wave Solder**

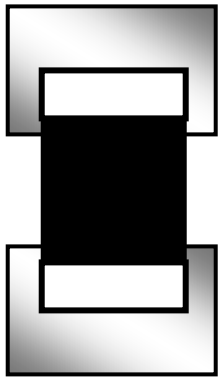
IPC-7351 3-Tier Library System

- **Density Level C**: Minimum (Least) Land Protrusion – High component density typical of portable and hand-held product applications may consider the 'minimum' land pattern geometry variation
- Selection of the minimum land pattern geometry may not be suitable for all product use categories. The use of classes of performance 1, 2, and 3 is combined with that of component density levels A, B, and C in explaining the condition of an electronic assembly
- As an example, combining the description as Levels 1A or 3B or 2C, would indicate the different combinations of performance and component density to aid in understanding the environment and the manufacturing requirements of a particular assembly.

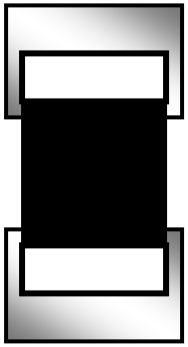
IPC Performance Classifications

- ***Class 1 General Electronic Products*** – Includes consumer products, some computer and computer peripherals, and hardware suitable for applications where the major requirement is function of the completed assembly.
- ***Class 2 Dedicated Service Electronic*** – Products Includes communications equipment, sophisticated business machines, and instruments where high performance and extended life is required, and for which uninterrupted service is desired but not mandatory. Typically the end-use environment would not cause failures.
- ***Class 3 High Reliability Electronic Products*** – Includes all equipment where continued performance or performance-on-demand is mandatory. Equipment downtime cannot be tolerated, end-use environment may be uncommonly harsh, and the equipment must function when required, such as life support systems and other critical systems.

3-Tier Land Pattern Variations



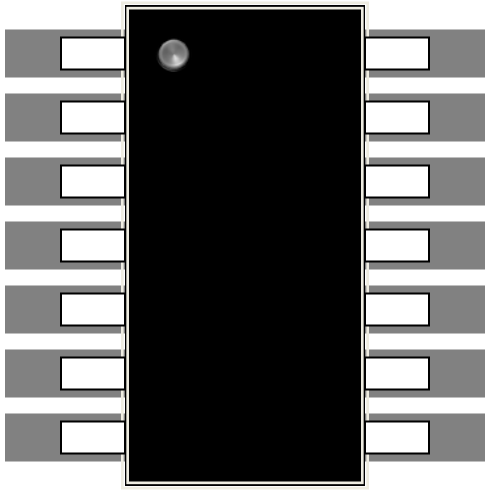
Density Level A
Very Robust
Solder Joint



Density Level B
General Purpose
Solder Joint

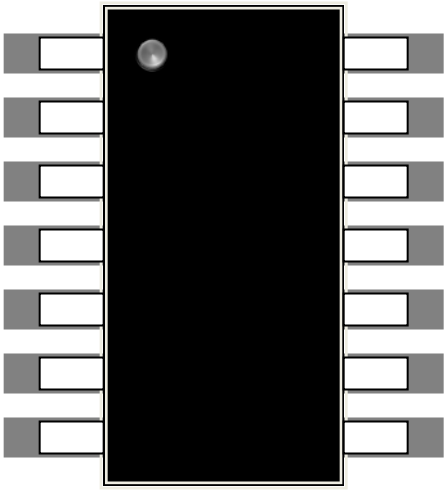
Density Level C
Minimal Solder
Joint
High Density
Applications

3-Tier Land Pattern Variations



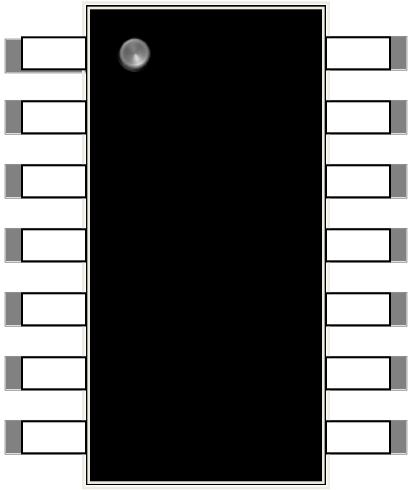
Density Level A

Very Robust
Solder Joint



Density Level B

General Purpose
Solder Joint



Density Level C

Minimal Solder
Joint
High Density
Applications

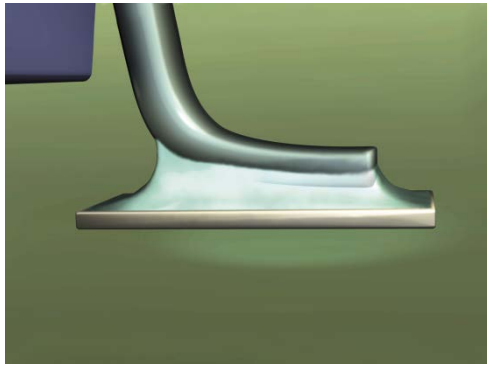
Solder Joint Calculations

- These 7 factors are used to calculate the optimum Land Size –

1. Component Body Tolerance – ± 0.1 (4) thru ± 0.3 (12)
2. Component Terminal Tolerance – ± 0.2 (8) thru ± 0.5 (20)
3. Fabrication Tolerance – ± 0.05 (2)
4. Placement Tolerance – ± 0.025 (1)
5. Land Size Round-off – ± 0.01 (1)
6. Land Spacing Round-off – ± 0.01 (1)
7. Solder Joint Goals for Toe, Heel and Side

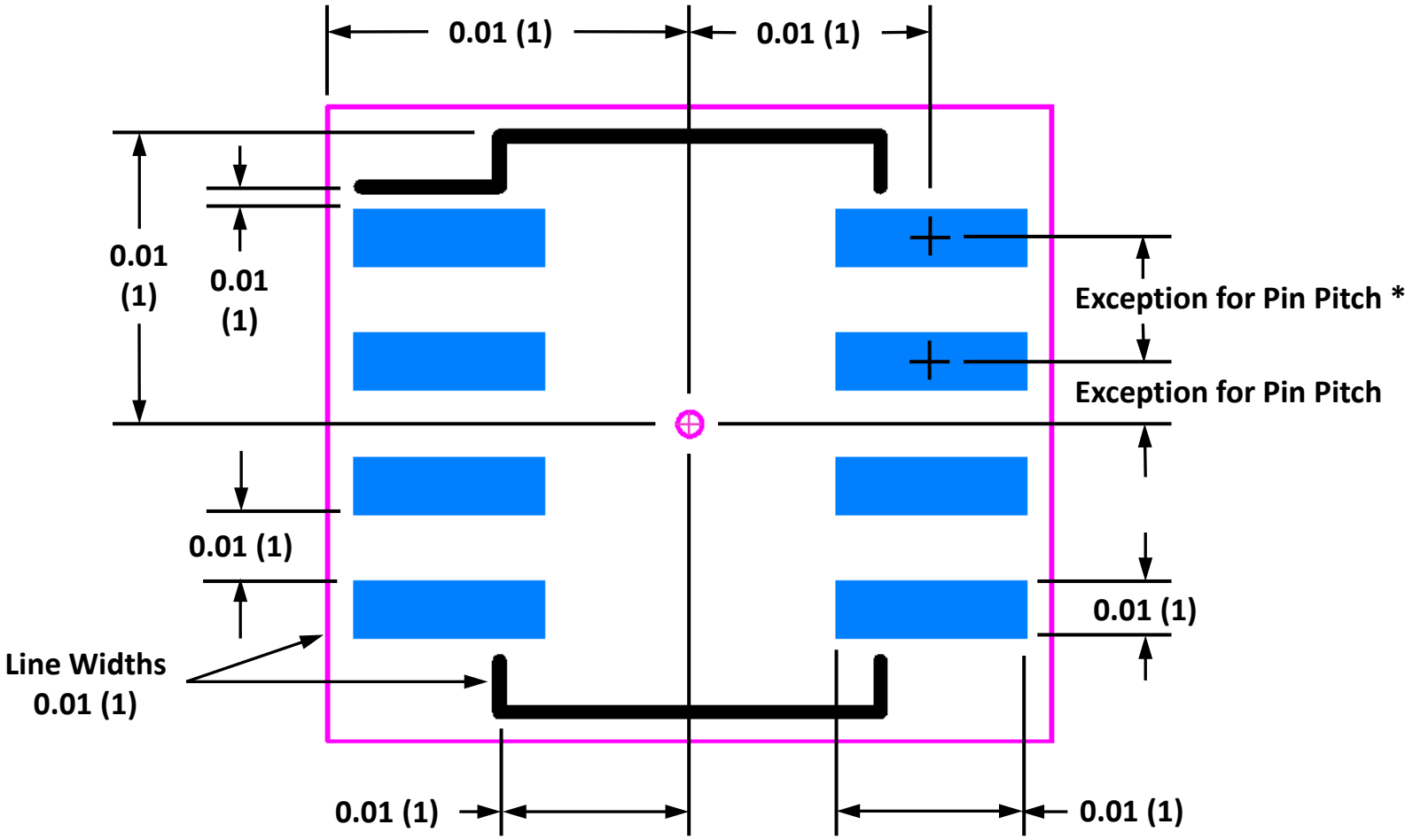
$$\sqrt{T^2 + F^2 + P^2}$$

Gull Wing Lead	Least Level C	Nominal Level B	Most Level A
Toe (J_T)	0.15	0.35	0.55
Heel (J_H)	0.25	0.35	0.45
Side (J_S)	0.01	0.03	0.05
Round-off factor	Round off to the nearest 0.05		
Courtyard excess	0.1	0.25	0.5



Land Pattern Feature Rounding

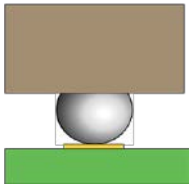
All Land Pattern Features are in 0.01 mm Increments for Metric and (1 mil) for Imperial units



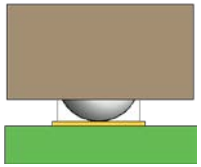
*Japanese 80% rule

Component Lead Styles

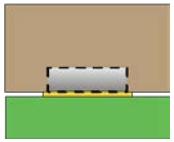
Ball Grid Array



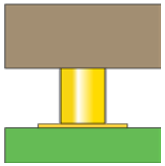
Bump Grid Array



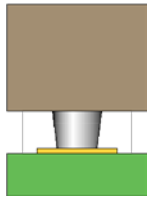
Bottom Grid Array



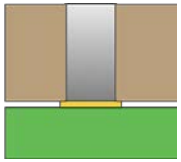
Column Grid Array



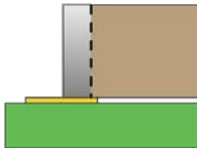
Pillar Grid Array



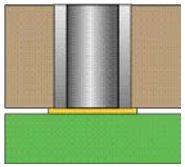
Flat Side



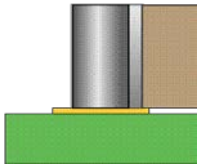
Convex Side



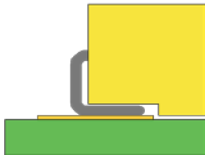
Concave Side



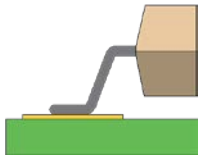
Corner Concave



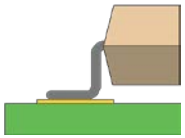
Inward L



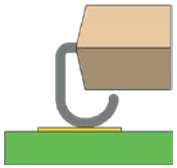
Gull Wing



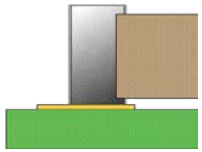
Outward L



J-Lead

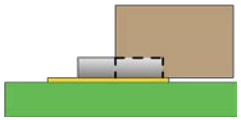


End Cap

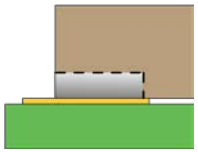


Under Body L

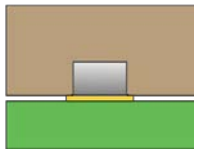
Flat



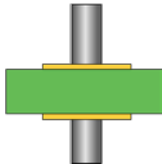
Flat Bottom



No-Lead



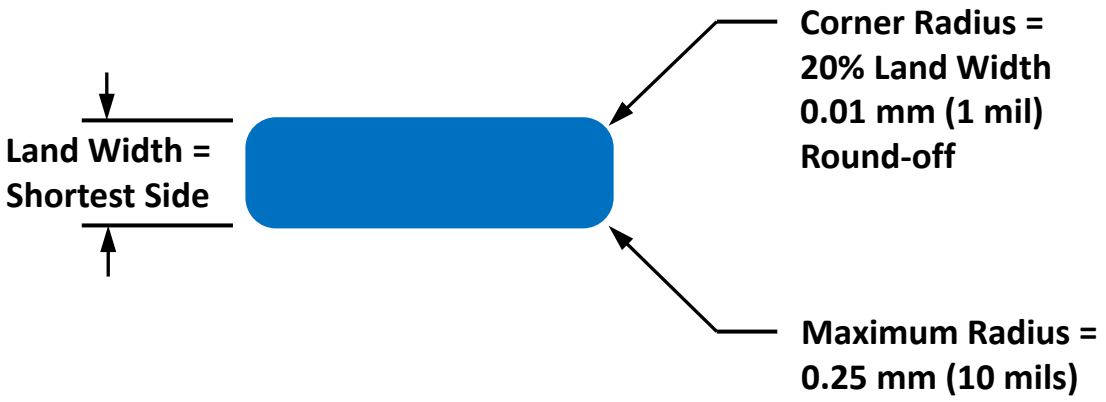
Through-hole



Rounded Rectangular Land Shape

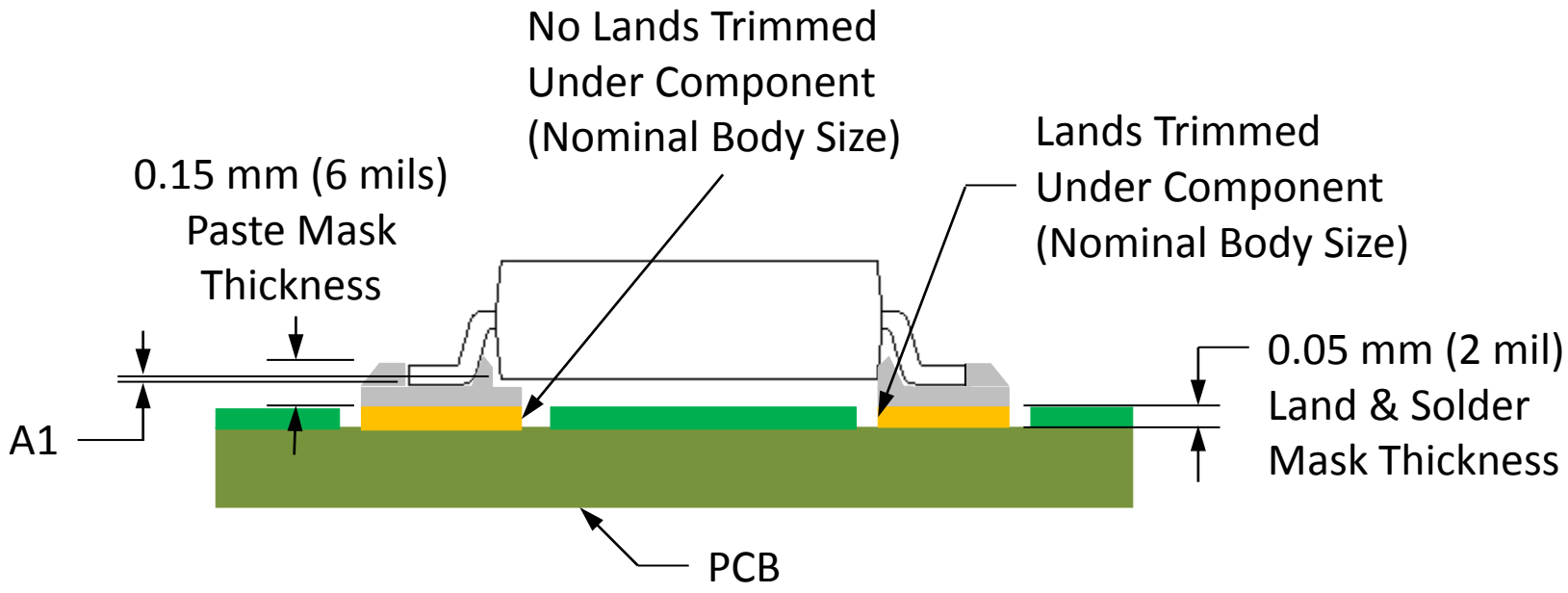
- Used For These Component Lead Styles –
  1. Gull Wing & J-Lead
  2. Inward, Outward & Under Body “L Bend”
  3. Side Flat, Convex & Concave and Corner Concave
  4. End Cap Termination

IPC LP Calculator Rounded Rectangular Corner Radius Default Calculation

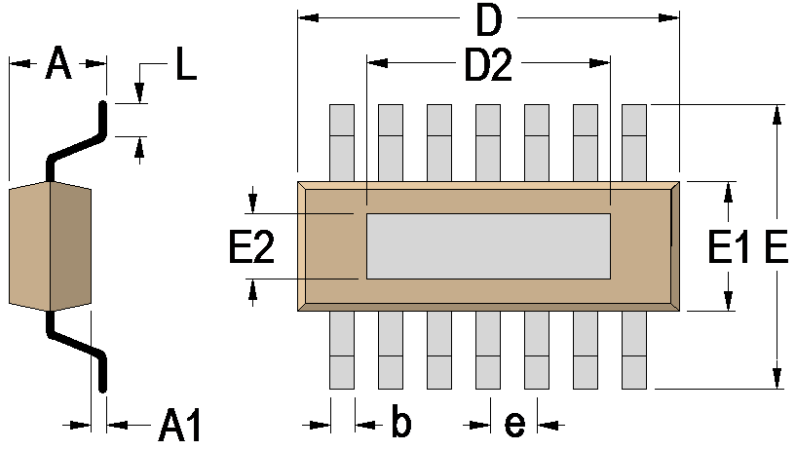


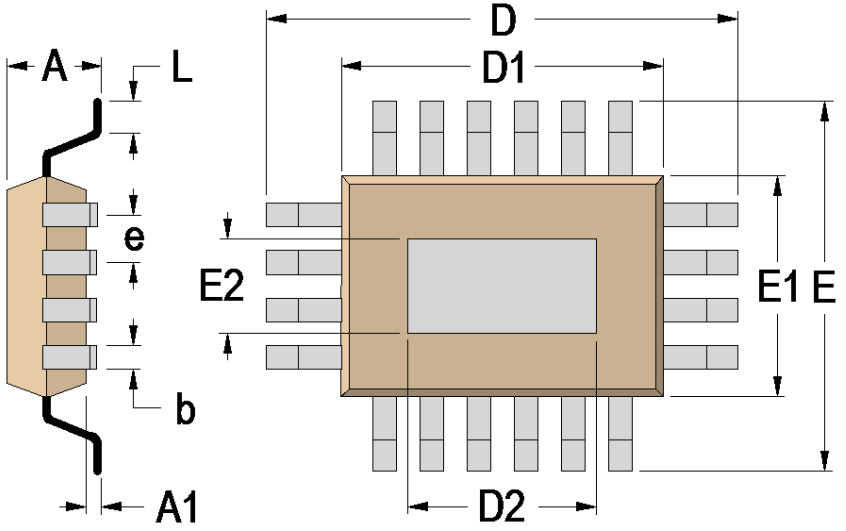
Land Trimming Under Components

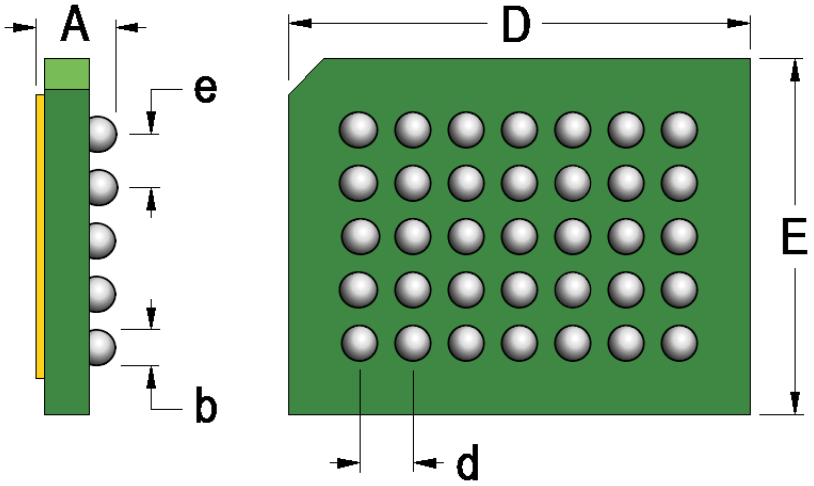
- For Gull Wing Component Lead Styles
  1. The original concept was to trim lands under the “Gull Wing” component body for low profile (A1) stand-off
  2. The new concept is No Land Trimming is necessary except to meet the minimum Land to Land and/or thermal pad to land clearance

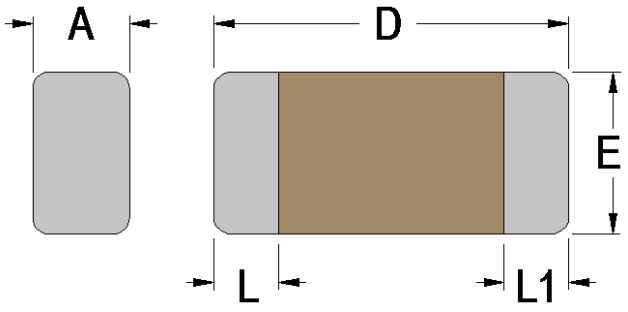


JEDEC Component Dimensioning









Land Pattern Naming Convention

- The original IPC-7351 land pattern naming convention does not include component tolerances, thermal pad sizes or various pin assignments into account. Therefore, the same component with different tolerances can produce a different land size and spacing with the same land pattern name.
- A land pattern name of **SOP50P710X120-14N** can have version A, B, C, D which do not indicate the variances.
- Define a list of 3 characters for each component manufacturer
  - Texas Instruments = **TI**
- Here is a sample Texas Instruments land pattern name – **SOP50P710X120-14N-TI**. This eliminates all confusion.
- For component manufacturer recommended land patterns drop the environment level character after the pin qty - **SOP50P710X120-14-TI**

Land Pattern Naming Convention

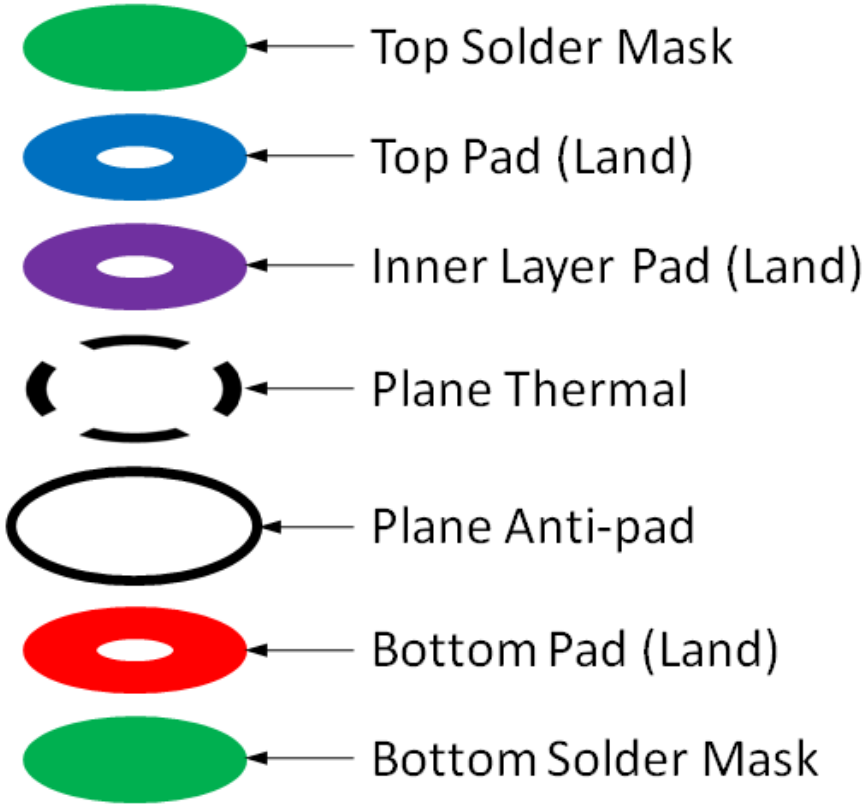
- The IPC-7351 land pattern and padstack naming convention strictly adheres to the metric unit system.
- However, not everyone in the electronics industry has adopted the metric unit system.
- Component manufacturer's name their Chip Components after the Inch Unit system. i.e.: 1206, 0805, 0603, 0402, etc.
- Under pressure from the electronics industry to not force companies and PCB designers into using metric units for PCB layout, everyone using the Inch unit system have requested Inch based land pattern and padstack names

Surface Mount Padstacks

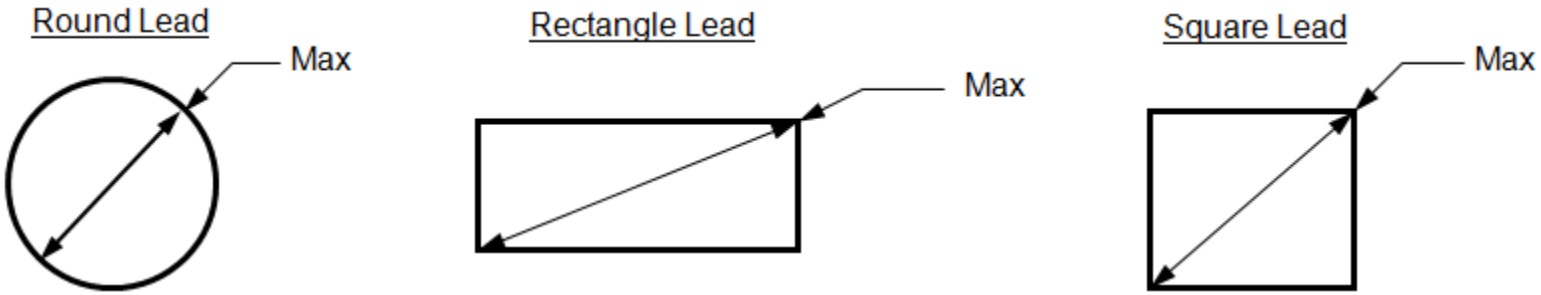
- The surface mount component padstack consists of a solder land (pad), solder mask and solder paste
- The solder mask and paste mask size are typically the same as the pad size
- **Solder Mask** – Allow the PC Board manufacturer to expand the solder mask size according to the trace/space DRC rule technology that the PCB designer used in the PCB design the layout
- **Solder Paste** – Allow the stencil manufacturer to over/under size the solder paste to match the specifications of the assembly shop that the paste mask stencil is being made for

Plated Through-hole Padstacks

- This is what a typical Through Hole Padstack is built like:
  - Top Solder Mask
  - Top Pad
  - Inner Layer Pad
  - Plane Thermal Relief
  - Plane Anti-pad
  - Bottom Pad
  - Bottom Solder Mask
  - Drilled Hole



Plated Hole Size Calculations



IPC-2222 Table 9-3		
Maximum Lead + Environment Level = Minimum Hole		
Level A	Level B	Level C
0.25 mm (10 mils)	0.20 mm (8 mils)	0.15 mm (6 mils)

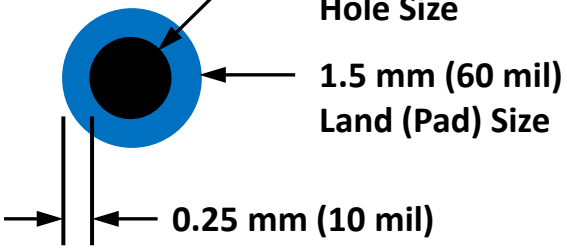
Proportional PTH Padstacks

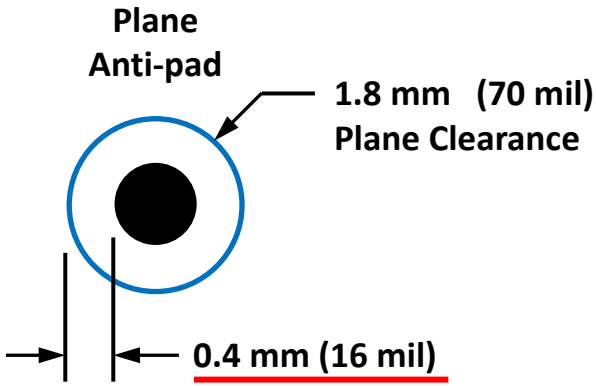
Max Lead Ø	Finished hole	Mounted Land	Inner Land	Opposite Land	Solder Mask Top & Bot	Plane Anti-pad	Thermal ID x OD	Thermal Spoke	Padstack Name Circular Land	Padstack Name Square Land
0.30	0.50	1.00	1.00	1.00	1.00	1.25	1x1.25	0.40	c100h50	s100h100
0.35	0.55	1.05	1.05	1.05	1.05	1.35	1.05x1.35	0.40	c105h55	s105h105
0.40	0.60	1.10	1.10	1.10	1.10	1.40	1.1x1.4	0.40	c110h60	s110h110
0.45	0.65	1.15	1.15	1.15	1.15	1.45	1.15x1.45	0.40	c115h65	s115h115
0.50	0.70	1.20	1.20	1.20	1.20	1.50	1.2x1.5	0.40	c120h70	s120h120
0.55	0.75	1.25	1.25	1.25	1.25	1.55	1.25x1.55	0.40	c125h75	s125h125
0.60	0.80	1.30	1.30	1.30	1.30	1.60	1.3x1.6	0.40	c130h80	s130h130
0.65	0.85	1.35	1.35	1.35	1.35	1.65	1.35x1.65	0.40	c135h85	s135h135
0.70	0.90	1.40	1.40	1.40	1.40	1.70	1.4x1.7	0.40	c140h90	s140h140
0.75	0.95	1.45	1.45	1.45	1.45	1.75	1.45x1.75	0.40	c145h95	s145h145
0.80	1.00	1.50	1.50	1.50	1.50	1.80	1.5x1.8	0.40	c150h100	s150h150
0.85	1.05	1.60	1.60	1.60	1.60	1.90	1.55x1.9	0.40	c160h105	s160h160
0.90	1.10	1.65	1.65	1.65	1.65	1.95	1.6x1.95	0.40	c165h110	s165h165
0.95	1.15	1.75	1.75	1.75	1.75	2.00	1.65x2	0.40	c175h115	s175h175
1.00	1.20	1.80	1.80	1.80	1.80	2.05	1.7x2.05	0.40	c180h120	s180h180
1.05	1.25	1.90	1.90	1.90	1.90	2.10	1.75x2.1	0.45	c190h125	s190h190
1.10	1.30	1.95	1.95	1.95	1.95	2.15	1.8x2.15	0.45	c195h130	s195h195
1.15	1.35	2.05	2.05	2.05	2.05	2.20	1.85x2.2	0.45	c205h135	s205h205
1.20	1.40	2.10	2.10	2.10	2.10	2.25	1.9x2.25	0.45	c210h140	s210h210
1.25	1.45	2.20	2.20	2.20	2.20	2.30	1.95x2.3	0.45	c220h145	s220h220
1.30	1.50	2.25	2.25	2.25	2.25	2.35	2x2.35	0.45	c225h150	s225h225
1.35	1.55	2.35	2.35	2.35	2.35	2.45	2.05x2.45	0.45	c235h155	s235h235
1.40	1.60	2.40	2.40	2.40	2.40	2.50	2.1x2.5	0.45	c240h160	s240h240
1.45	1.65	2.50	2.50	2.50	2.50	2.55	2.15x2.55	0.45	c250h165	s250h250
1.50	1.70	2.55	2.55	2.55	2.55	2.60	2.2x2.6	0.45	c255h170	s255h255

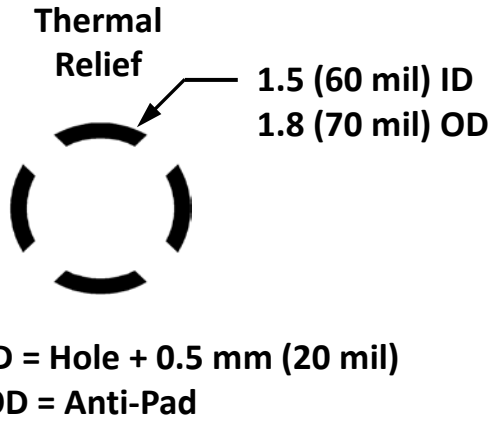
All Plated & Non-plated Through-hole Padstack Values are in 0.05 increments

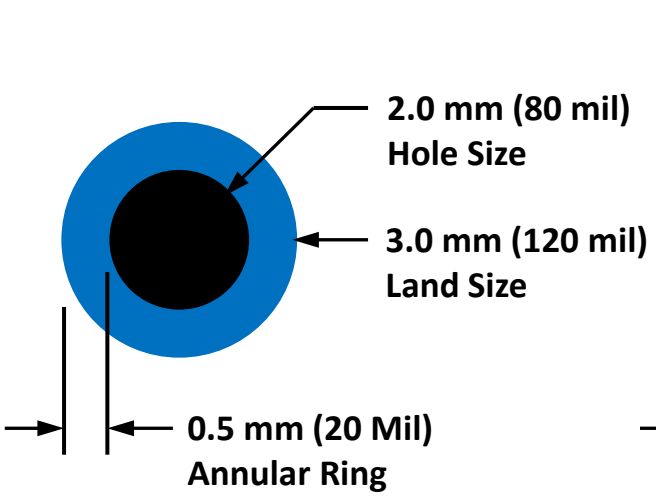
Proportional PTH Padstacks

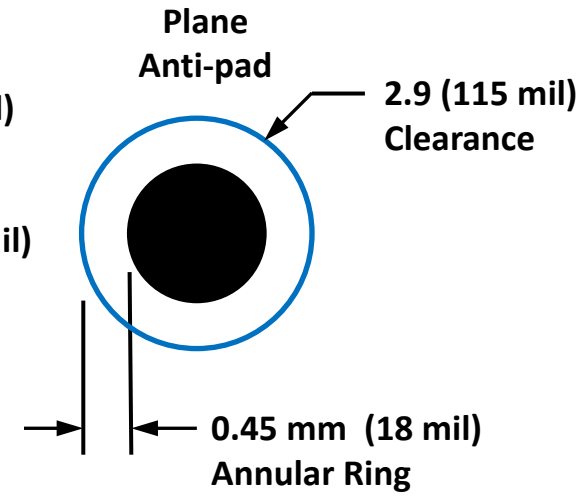
The larger the hole size the larger the annular ring on the land but the Plane Anti-pad and the Thermal Relief maintain strict fabrication DRC rules to minimize the clearance and maximize the plane copper. For large hole sizes, the land size is larger than the Plane Clearance.

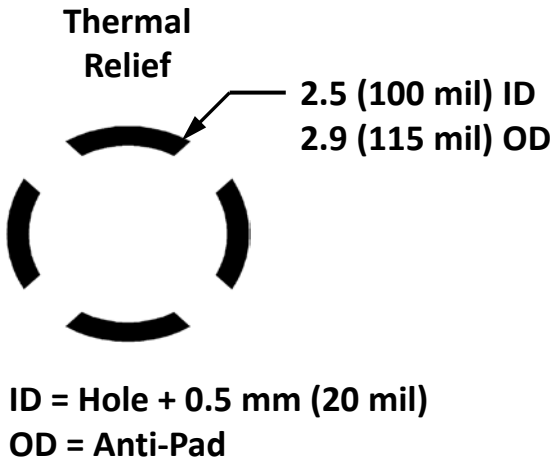




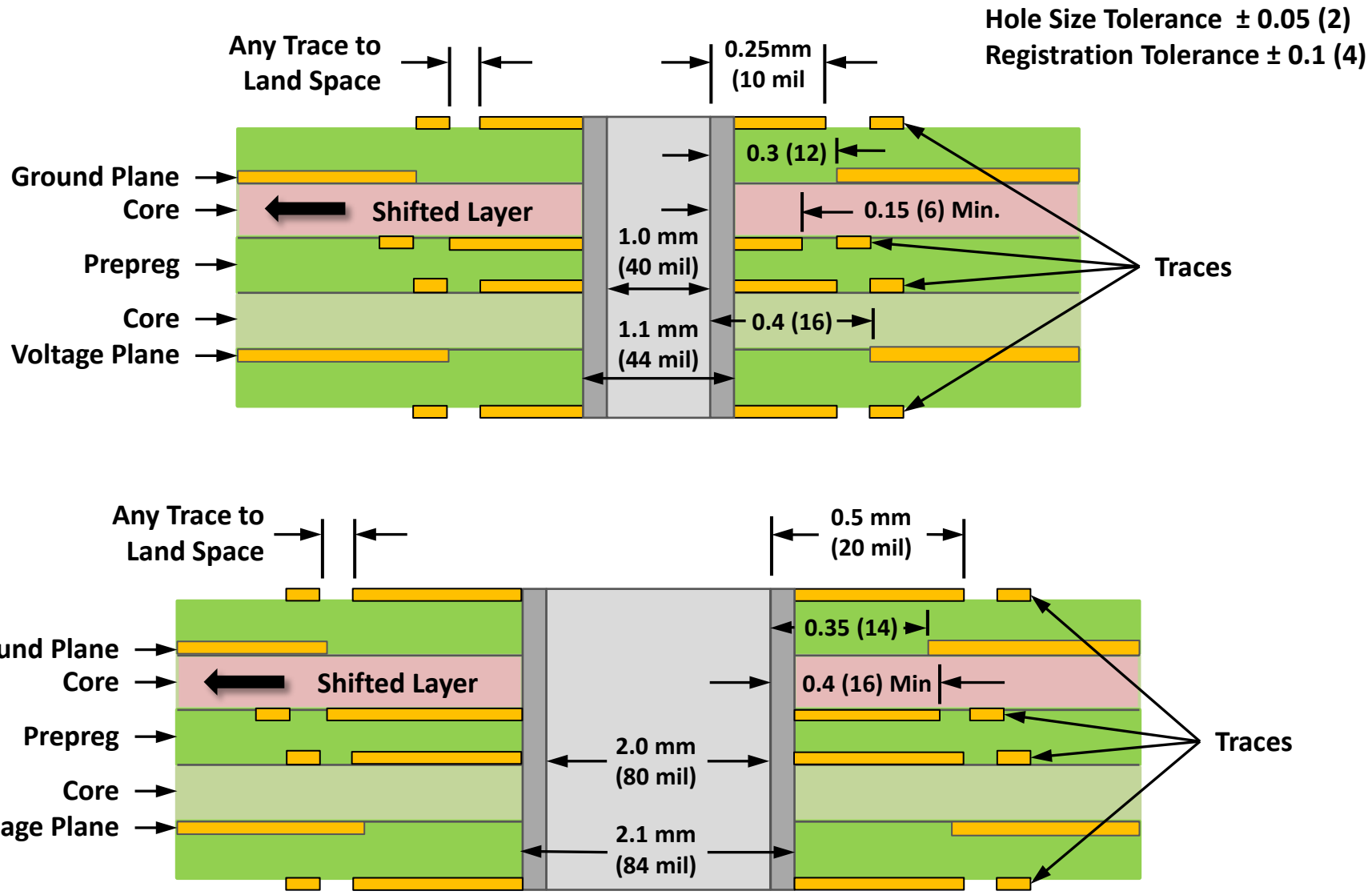








Plated Through Holes



Plated Through Holes

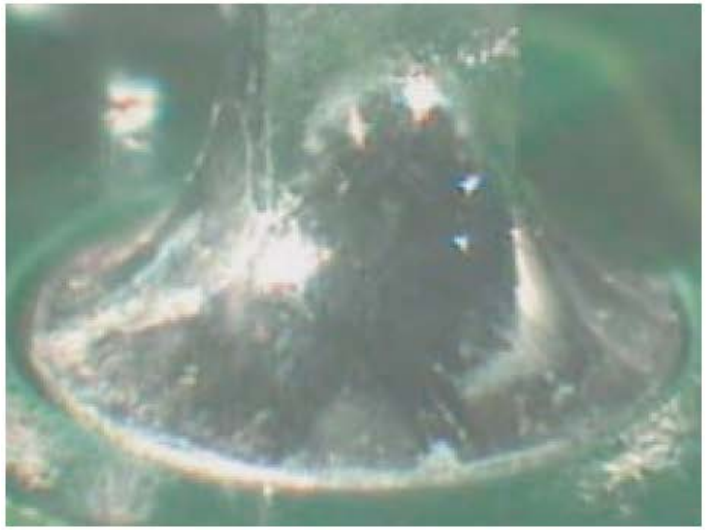


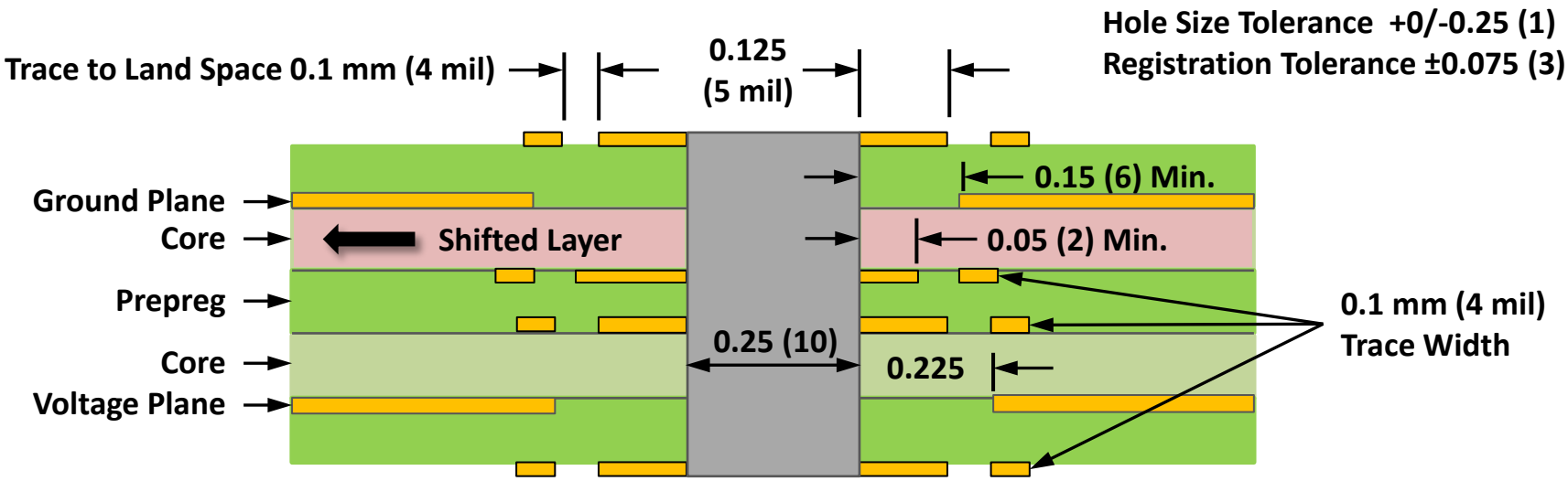
Figure E-13 SnPb Solder

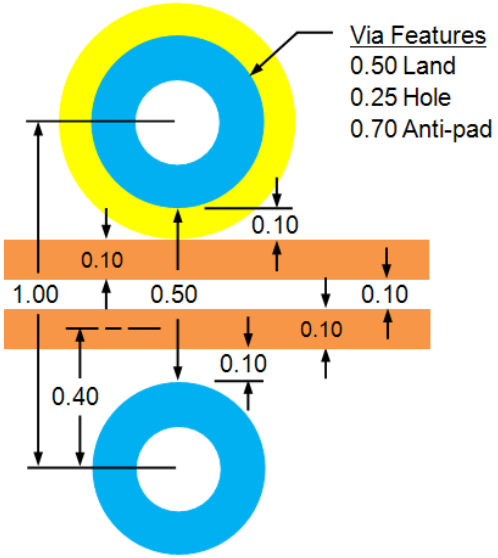
Figure E-14 SnAgCu Solder

Figure E-15 SnPb Solder

Figure E-16 SnAgCu Solder

Plated Through Vias

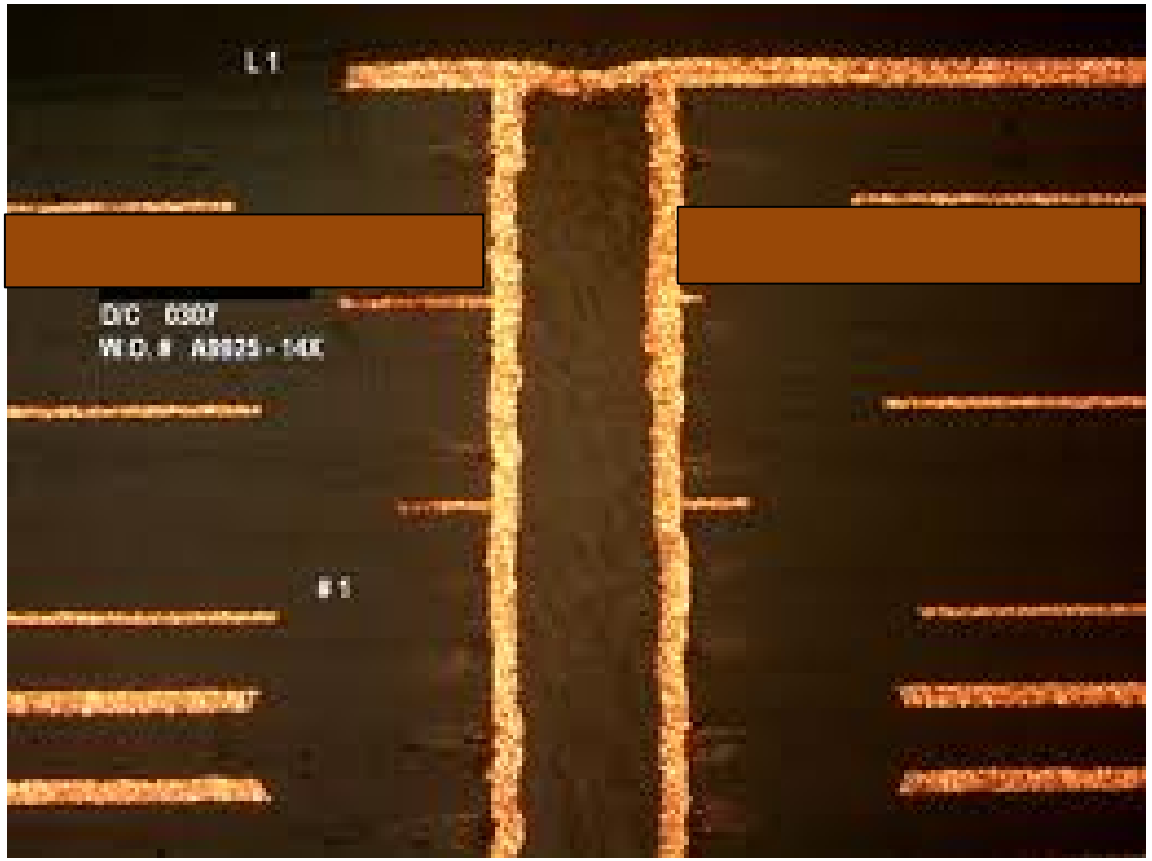




- The 0.5 via is widely used as the 1.0 pitch BGA dog-bone fanout to route two 0.1 (4 mil) width traces between
- The 0.5 via is also used for 0.8 pitch BGA dog-bone fanout to route one 0.1 mm (4 mil) width trace between

Plated Through Holes

PCB cross-section Illustration of registration tolerance



Proportional NPTH Padstacks

Finished Hole	Mounted Land	Inner Land	Opposite Land	Plane Clearance	Solder Mask Top & Bot	Assembly Top & Bot	Keep-out Diameter	Padstack Name
0.50	0.20	0.20	0.20	1.25	0.50	0.50	1.10	c20hn50
0.55	0.20	0.20	0.20	1.35	0.55	0.55	1.15	c20hn55
0.60	0.50	0.50	0.50	1.40	0.60	0.60	1.20	c50hn60
0.65	0.50	0.50	0.50	1.45	0.65	0.65	1.25	c50hn65
0.70	0.50	0.50	0.50	1.50	0.70	0.70	1.30	c50hn70
0.75	0.50	0.50	0.50	1.55	0.75	0.75	1.35	c50hn75
0.80	0.50	0.50	0.50	1.60	0.80	0.80	1.40	c50hn80
0.85	0.50	0.50	0.50	1.65	0.85	0.85	1.45	c50hn85
0.90	0.50	0.50	0.50	1.70	0.90	0.90	1.50	c50hn90
0.95	0.50	0.50	0.50	1.75	0.95	0.95	1.55	c50hn95
1.00	0.50	0.50	0.50	1.80	1.00	1.00	1.60	c50hn100
1.05	0.50	0.50	0.50	1.90	1.05	1.05	1.65	c50hn105
1.10	1.00	1.00	1.00	1.95	1.10	1.10	1.70	c100hn110
1.15	1.00	1.00	1.00	2.00	1.15	1.15	1.75	c100hn115
1.20	1.00	1.00	1.00	2.05	1.20	1.20	1.80	c100hn120
1.25	1.00	1.00	1.00	2.10	1.25	1.25	1.85	c100hn125
1.30	1.00	1.00	1.00	2.15	1.30	1.30	1.90	c100hn130
1.35	1.00	1.00	1.00	2.20	1.35	1.35	1.95	c100hn135
1.40	1.00	1.00	1.00	2.25	1.40	1.40	2.00	c100hn140
1.45	1.00	1.00	1.00	2.30	1.45	1.45	2.05	c100hn145
1.50	1.00	1.00	1.00	2.35	1.50	1.50	2.10	c100hn150
1.55	1.00	1.00	1.00	2.45	1.55	1.55	2.15	c100hn155
1.60	1.00	1.00	1.00	2.50	1.60	1.60	2.20	c100hn160
1.65	1.00	1.00	1.00	2.55	1.65	1.65	2.25	c100hn165
1.70	1.00	1.00	1.00	2.60	1.70	1.70	2.30	c100hn170

Non-plated holes with no annular ring are used for plastic alignment pegs
All Non-plated Through-hole Padstack Values are in 0.05 (2 mil) increments

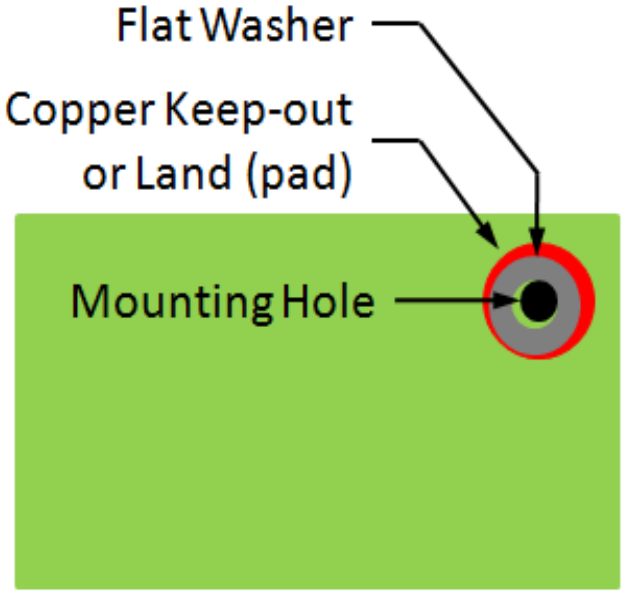
Mounting Holes

- Mounting holes are on every PCB design
- Mounting hardware normally consists of these 4 items:
  - Phillips Head Screw
  - Lock Washer
  - Flat Washer
  - Hex Nut

- There are 4 types of mounting holes:
  - Supported – Plated through with annular ring
  - Supported – Plated through with annular ring with vias
  - Unsupported – Non-plated and with copper pads
  - Tooling Holes and Plastic Peg Alignment – Non-plated and with no copper pads
- The supported mounting hole usually gets tied to the GND plane without a Thermal Relief

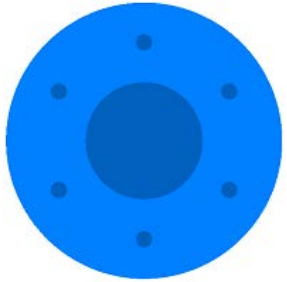
Mounting Holes

- The unsupported (non-plated) hole has no connection to a GND plane layer
- Unsupported (non-plated) hole require an outer layer keep-out defined that compensates for the hardware tolerances
- The Supported Land Size or Unsupported Hole have a slop tolerance for the flat washer and require a copper keep-out



Mounting Holes

- Vias are added to mounting holes to secure the GND connection and crush prevention during torque
- The average via size in a mounting hole is 0.5
- No need for Thermal Reliefs on MTG Holes
- Plane Clearance is 1 mm larger than hole size



- The “Loose Fit” mounting holes are normally used on large boards greater than 100 mm (4”) length or width
- “Tight Fit” mounting holes are used for smaller board sizes
- There are 3-Tiers for the Mounting Hole family, <u>but the only difference</u> is the “Placement Courtyard Excess”
  - Least – 0.1 mm (4 mils) annular
  - Nominal – 0.25 mm (10 mils) annular
  - Most – 0.5 mm (20 mils) annular

ISO Loose Fit Mounting Holes

ISO (metric) Nut, Screw and Washer Hardware Sizes					
Screw Size Dia x Thread	Pan Head	Hex Nut	Flat Washer	Washer ID	Lock Washer
M2 x 0.4	4.00	4.62	5.30	2.20	4.40
M2.5 x 0.45	5.00	5.77	6.80	2.70	5.10
M3 x 0.5	6.00	6.35	7.30	3.20	6.20
M3.5 x 0.6	7.00	6.93	8.40	3.80	6.90

ISO (metric) Hardware w/Plated & Non-plated Though Hole Padstack Data – Loose Fit									
Pan Head Screw Size	Hardware on PCB	Placement Courtyard	Hole Size	Top Pad	Inner Pad	Bottom Pad	Solder Mask	Plane Anti-Pad	Thermal Relief
M2 x 0.4	Pan Head	4.80	2.30	4.30	4.30	4.30	4.30	3.30	None
M2 x 0.4	Flat Washer	6.00	2.30	5.50	5.50	5.50	5.50	3.30	None
M2.5 x 0.45	Pan Head	5.90	2.85	5.40	5.40	5.40	5.40	3.85	None
M2.5 x 0.45	Flat Washer	7.60	2.85	7.10	7.10	7.10	7.10	3.85	None
M3 x 0.5	Pan Head	7.00	3.50	6.50	6.50	6.50	6.50	4.50	None
M3 x 0.5	Flat Washer	8.20	3.50	7.70	7.70	7.70	7.70	4.50	None
M3.5 x 0.6	Pan Head	7.90	3.90	7.40	7.40	7.40	7.40	4.90	None
M3.5 x 0.6	Flat Washer	9.20	3.90	8.70	8.70	8.70	8.70	4.90	None

ISO Tight Fit Mounting Holes

ISO (metric) Nut, Screw and Washer Hardware Sizes					
Screw Size Dia x Thread	Pan Head	Hex Nut	Flat Washer	Washer ID	Lock Washer
M2 x 0.4	4.00	4.62	5.30	2.20	4.40
M2.5 x 0.45	5.00	5.77	6.80	2.70	5.10
M3 x 0.5	6.00	6.35	7.30	3.20	6.20
M3.5 x 0.6	7.00	6.93	8.40	3.80	6.90

ISO (metric) Hardware w/Plated & Non-plated Though Hole Padstack Data – Tight Fit									
Pan Head Screw Size	Hardware on PCB	Placement Courtyard	Hole Size	Top Pad	Inner Pad	Bottom Pad	Solder Mask	Plane Anti-Pad	Thermal Relief
M2 x 0.4	Pan Head	4.60	2.10	4.10	4.10	4.10	4.10	3.10	None
M2 x 0.4	Flat Washer	5.80	2.10	5.30	5.30	5.30	5.30	3.10	None
M2.5 x 0.45	Pan Head	5.60	2.60	5.10	5.10	5.10	5.10	3.60	None
M2.5 x 0.45	Flat Washer	7.30	2.60	6.80	6.80	6.80	6.80	3.60	None
M3 x 0.5	Pan Head	6.60	3.10	6.10	6.10	6.10	6.10	4.10	None
M3 x 0.5	Flat Washer	7.80	3.10	7.30	7.30	7.30	7.30	4.10	None
M3.5 x 0.6	Pan Head	7.60	3.60	7.10	7.10	7.10	7.10	4.60	None
M3.5 x 0.6	Flat Washer	8.90	3.60	8.40	8.40	8.40	8.40	4.60	None

ANSI Loose Fit Mounting Holes

ANSI Nut, Screw and Washer Hardware Chart					
Screw Size	Pan Head	Hex Nut	Flat Washer	Washer ID	Lock Washer
#2-48	4.24	5.51	6.35	2.39	4.36
#4-40	5.56	7.34	9.52	3.18	5.31
#6-32	6.85	9.17	11.13	3.96	6.35
#8-32	8.18	10.08	12.70	4.78	7.44

ANSI Hardware w/Plated & Non-plated Though Hole Padstack Data – Loose Fit									
Pan Head Screw Size	Hardware on PCB	Placement Courtyard	Hole Size	Top Pad	Inner Pad	Bottom Pad	Solder Mask	Plane Anti-Pad	Thermal Relief
#2 - 48	Pan Head	5.00	2.45	4.50	4.50	4.50	4.50	3.45	None
#2 - 48	Flat Washer	7.40	2.45	6.90	6.90	6.90	6.90	3.45	None
#4 - 40	Pan Head	6.60	3.70	6.10	6.10	6.10	6.10	4.70	None
#4 - 40	Flat Washer	10.60	3.70	10.10	10.10	10.10	10.10	4.70	None
#6 - 32	Pan Head	7.80	3.90	7.30	7.30	7.30	7.30	4.90	None
#6 - 32	Flat Washer	12.50	3.90	12.00	12.00	12.00	12.00	4.90	None
#8 - 32	Pan Head	9.10	4.60	8.60	8.60	8.60	8.60	5.60	None
#8 - 32	Flat Washer	14.30	4.60	13.80	13.80	13.80	13.80	5.60	None

ANSI Tight Fit Mounting Holes

ANSI Nut, Screw and Washer Hardware Chart					
Screw Size	Pan Head	Hex Nut	Flat Washer	Washer ID	Lock Washer
#2-48	4.24	5.51	6.35	2.39	4.36
#4-40	5.56	7.34	9.52	3.18	5.31
#6-32	6.85	9.17	11.13	3.96	6.35
#8-32	8.18	10.08	12.70	4.78	7.44

ANSI Hardware w/Plated & Non-plated Though Hole Padstack Data – Tight Fit									
Pan Head Screw Size	Hardware on PCB	Placement Courtyard	Hole Size	Top Pad	Inner Pad	Bottom Pad	Solder Mask	Plane Anti-Pad	Thermal Relief
#2 - 48	Pan Head	4.80	2.25	4.30	4.30	4.30	4.30	3.25	None
#2 - 48	Flat Washer	7.20	2.25	6.70	6.70	6.70	6.70	3.25	None
#4 - 40	Pan Head	6.20	3.30	5.70	5.70	5.70	5.70	4.30	None
#4 - 40	Flat Washer	10.20	3.30	9.70	9.70	9.70	9.70	4.30	None
#6 - 32	Pan Head	7.50	3.60	7.00	7.00	7.00	7.00	4.60	None
#6 - 32	Flat Washer	12.20	3.60	11.7	11.70	11.70	11.70	4.60	None
#8 - 32	Pan Head	8.90	4.30	8.40	8.40	8.40	8.40	5.30	None
#8 - 32	Flat Washer	14.00	4.30	13.5	13.50	13.50	13.50	5.30	None

Padstack Naming Convention

- The first character in the padstack naming convention defines the outer layer land (pad) shape
- The characters are “lower case” as the default
- There are six basic land shape identifiers
  - **c** = Circular
  - **s** = Square
  - **r** = Rectangle
  - **b** = Oblong
  - **d** = D-shape (Square one end & Circular on other end)
  - **u** = User defined contour (Irregular shape)
- Note: The “**b**” was used for Oblong because the letter “**o**” can easily be confused with the character zero “**0**”

Padstack Name Assumptions

- Solder Mask is 1:1 scale of the land size
- Paste Mask is 1:1 scale of the land size
- Inner Layer Land is the same shape as the outer layer land
- The Primary and Secondary lands are the same size
- The inner layer land shapes are Circular
- Vias are Circular
- Mounting Holes are Circular
- Thermal relief OD is the same size as Plane Clearance
- Thermal ID, OD and Spoke sizes use “Proportional Chart”
- Plane Clearance Anti-pad size use “Proportional Chart”
- Thermals have 4 spokes
- Illegal characters: “ ” , ; : / \ [ ] ( ) . { } * & % # $! @ ^ =

Padstack Name Single Modifiers

- **n** = Non-plated Hole
- **z** = Inner Layer land dimension if different than primary layer
- **x** = Special modifier used alone or following other modifiers for lands on opposite side to primary layer land dimension
- **t** = Thermal Relief; if different than standard padstack
- **m** = Solder Mask if different than default 1:1 scale of land
- **p** = Solder Paste if different than default 1:1 scale of land
- **y** = Plane Clearance if the value is different than Thermal OD
- **o** = Offset Land Origin
- **k** = Keep-out
- **r** = Radius for Rounded Rectangular Land Shape
- **c** = Chamfer for Chamfered Rectangular Land Shape

Padstack Name Double Modifiers

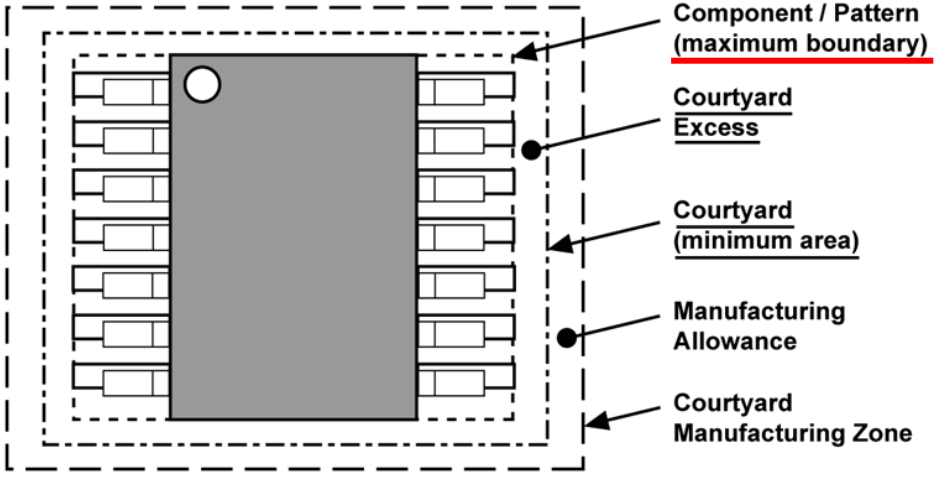
- **ts** = Thermal Square; if different than the top side land shape and dimensions
- **sw** = Thermal spoke width
- **zs** = Inner Layer Land Shape is Square (Note: The default is circular)
- **m0** = No Solder Mask
- **mxc** = Solder Mask Opposite Side Circular
- **mx0** = Solder Mask Opposite Side No Solder Mask
- **xc** = Opposite Side Circular
- **vs** = Via with Square land
- **hn** = Hole Non-plated

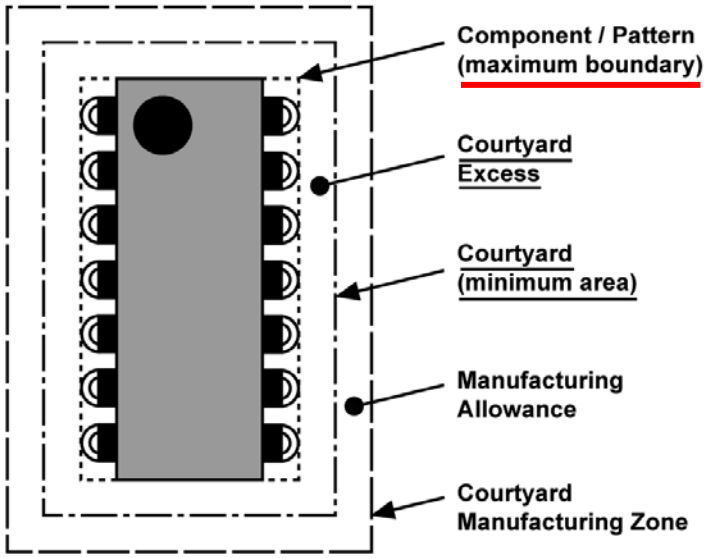
Padstack Name Examples

- **c150h90** = Default padstack with a 1.50 circular land with a 0.90 hole (no modifiers used)
- **c150h90z140** = Inner layer land is smaller than external lands 1.40 or 0.10 smaller
- **c150h90z140x170** = Opposite side land is larger than top side land 1.70 or 0.20 larger
- **c150h90z140x170m165mx185** = Solder mask opening for top and bottom lands 0.15 larger for each
- **c150h90z140x170m165mx185y300** = Plane clearance anti-pad diameter is 3.00
- **c150h90z140x170m165mx185y300t150_180_40** = Thermal ID 1.50, OD 1.80, Spoke Width 0.40, Anti-pad 1.80

Placement Courtyard

- IPC-7351 Placement Courtyard Oversize **Maximum** tolerance
  - Least – 0.12 mm (5 mils) Note: Current IPC-7351B Standard – 0.1 mm (4 mil)
  - Nominal – 0.25mm (10 mils) 0.1 mm (4 mil) component length < 2.0mm (8 mil)
  - Most – 0.5mm (20 mil) *No Most Environment for component length < 1.6mm*
- Placement Courtyard for most Connectors is 0.5 mm (20 mils)
- All Silkscreen Outlines must be located inside Courtyard so that they never intrude on another land pattern (footprint)



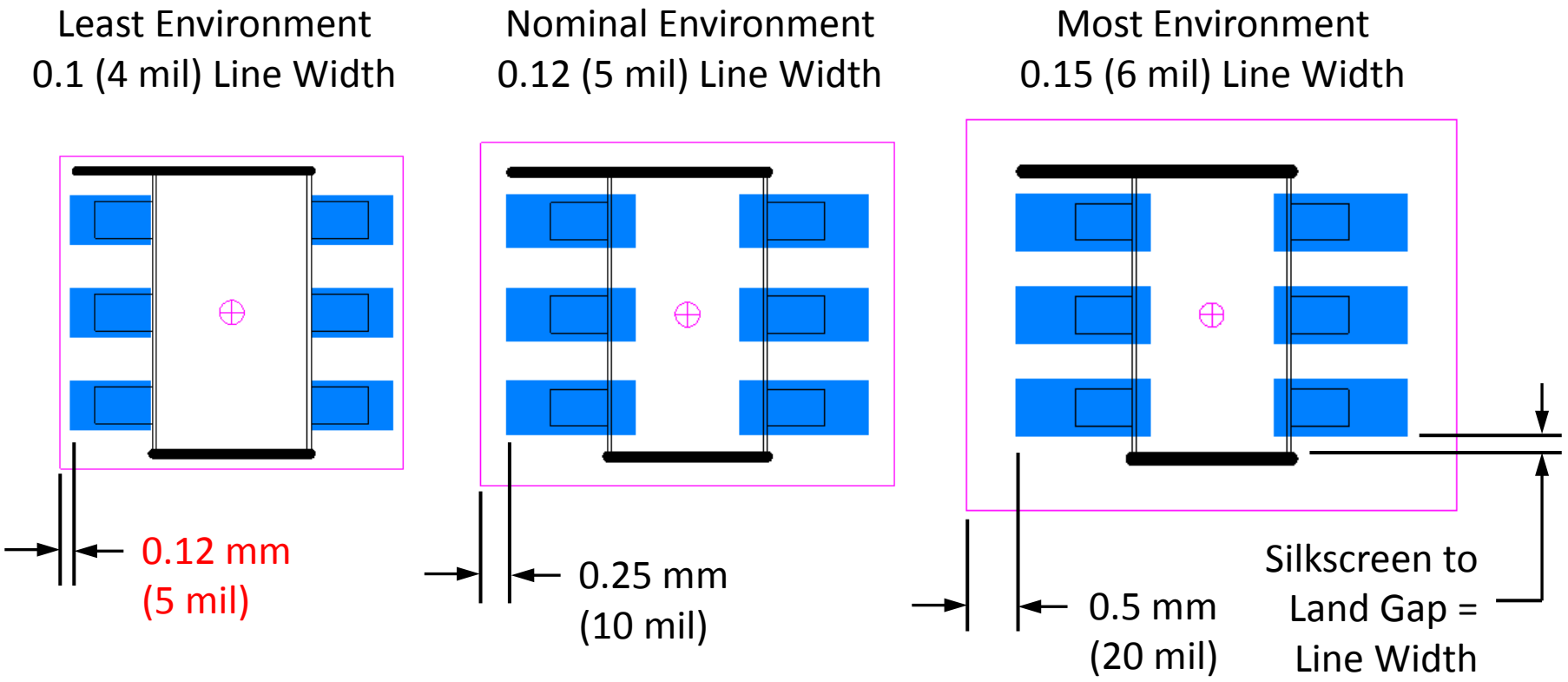


Silkscreen & Assembly Outlines

- Silkscreen outlines should never be located under the component because they are covered up during assembly
- Silkscreen Outlines should be located on the component edge or outside the component edge and used as crop marking for assembly placement registration accuracy
- Silkscreen Polarity Marking should indicate Pin 1 location and should be visible after assembly attachment
- Silkscreen line widths should be different sizes for 3-Tier
- All Silkscreen Outlines should be located inside Courtyard
- Assembly Outlines are the same size as the component
- Assembly Polarity Marking should be a consistent 1.0 mm (40 mils) 45° chamfer to indicate the location of Pin 1
- Assembly line widths should be one size for all 3-Tiers

3-Tier Silkscreen Outlines

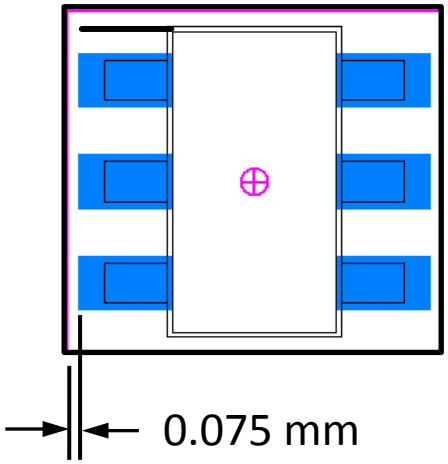
- The preliminary recommendation for 3-Tier line widths and Silkscreen to Land Gap are illustrated in the pictures below



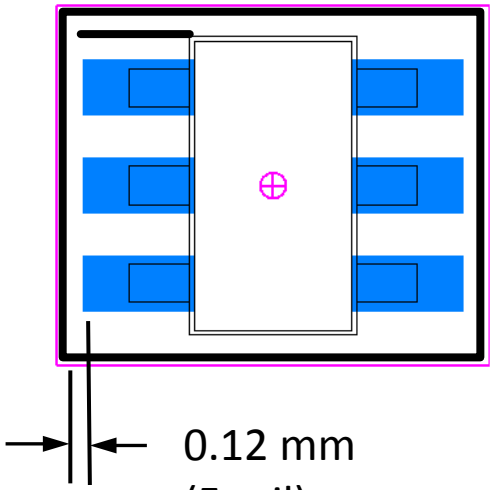
3-Tier Silkscreen Outlines

- The preliminary recommendation for 3-Tier line widths and Silkscreen to Land Gap are illustrated in the pictures below
- The full silkscreen radius potential blocks Ref Des locations

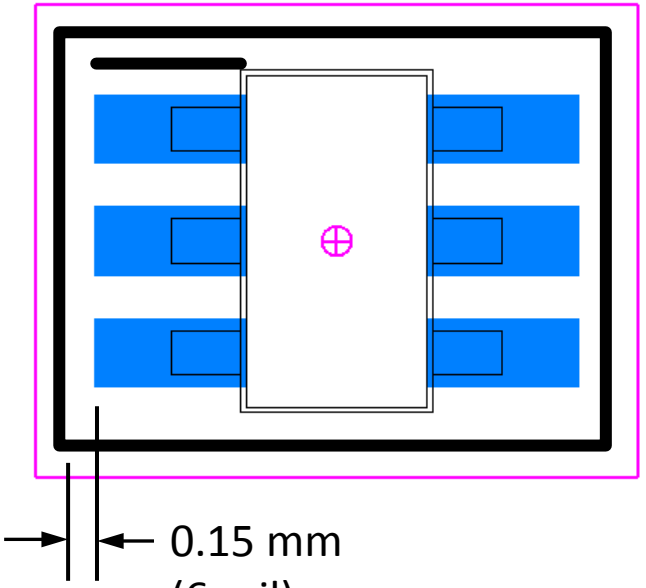
Least Environment
0.1 (4 mil) Line Width



Nominal Environment
0.12 (5 mil) Line Width

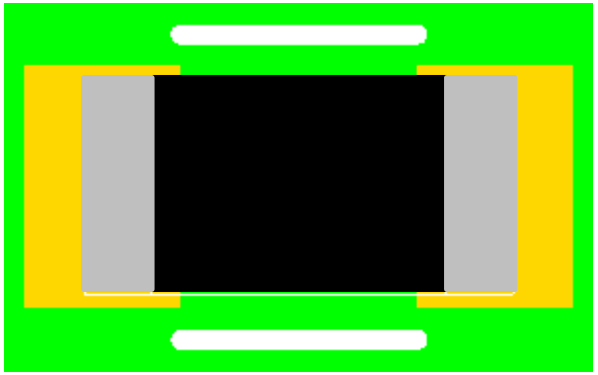


Most Environment
0.15 (6 mil) Line Width

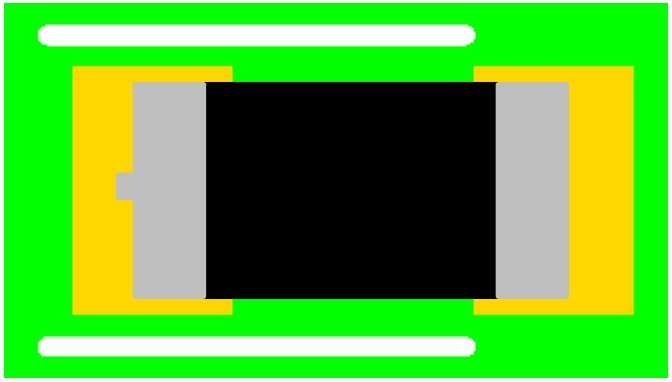


2-Pin (Chip, MELF, SOD) Outlines

Non-polarized Silkscreen



Polarized Silkscreen

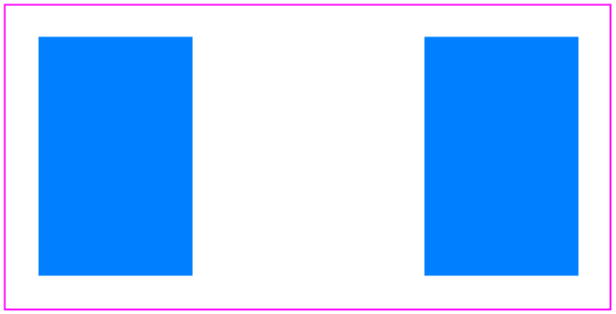


Assembly

Polarized Assembly

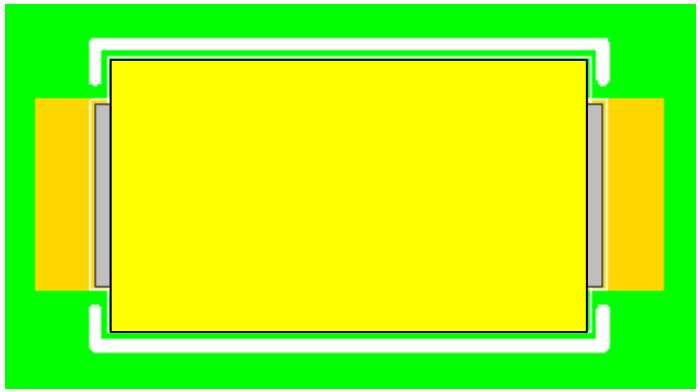
3D Model

Courtyard

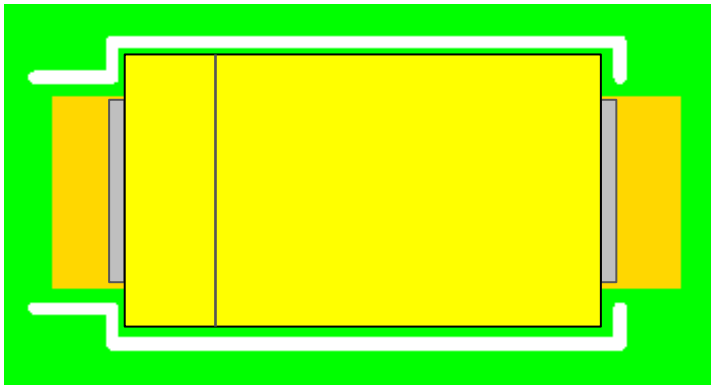


Molded Body Outlines

Non-polarized Silkscreen



Polarized Silkscreen

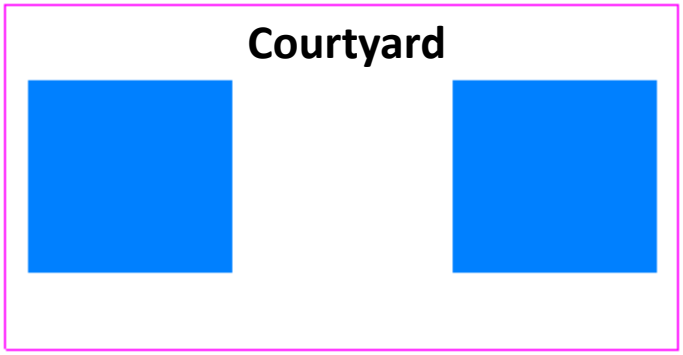


Assembly

Polarized Assembly

3D Model

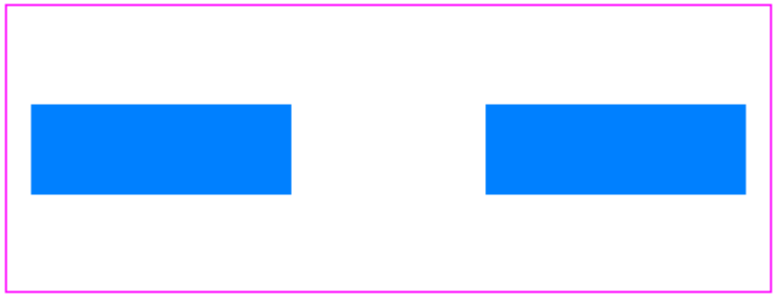
Courtyard



Crystal Outlines

Silkscreen

Courtyard



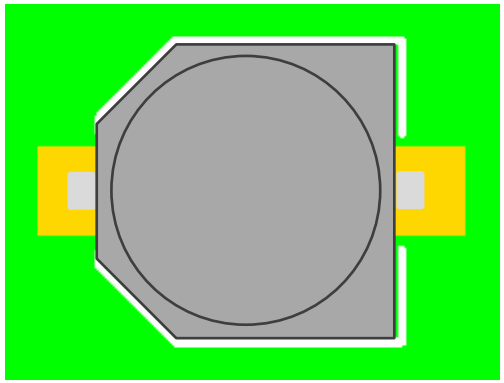
3D Model

IDF Model

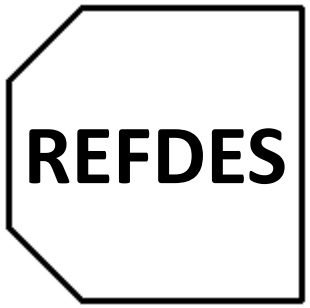
Assembly

Aluminum Electrolytic Capacitor Outlines

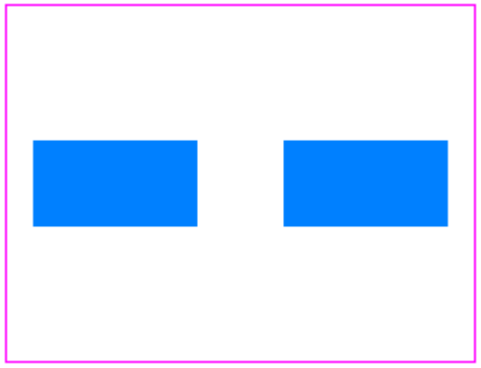
Silkscreen



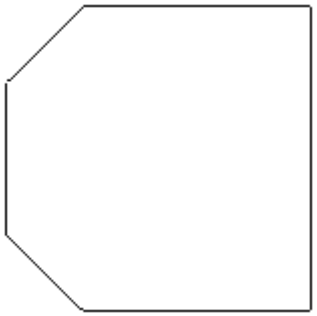
Assembly



Courtyard

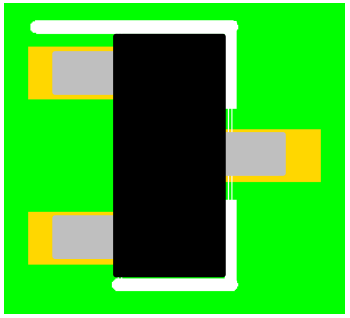


3D IDF Model

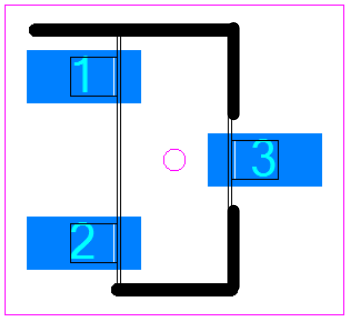


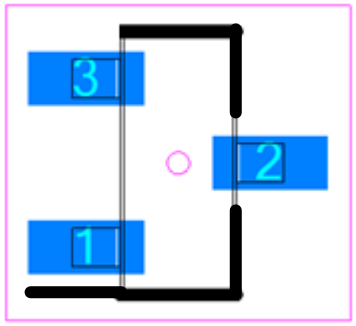
SOT23-3 Outlines

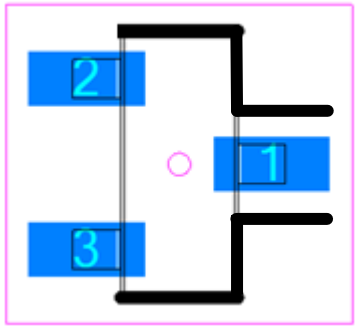
Component



Various Silkscreen Outlines with Polarity on Pin 1

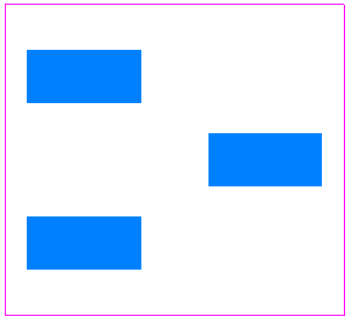




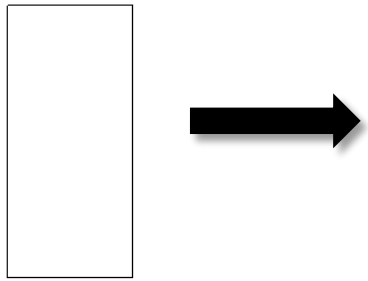


Assembly

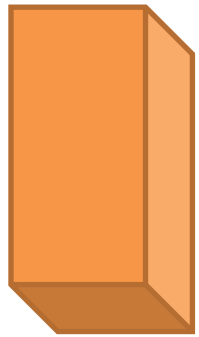
Courtyard



3D Model

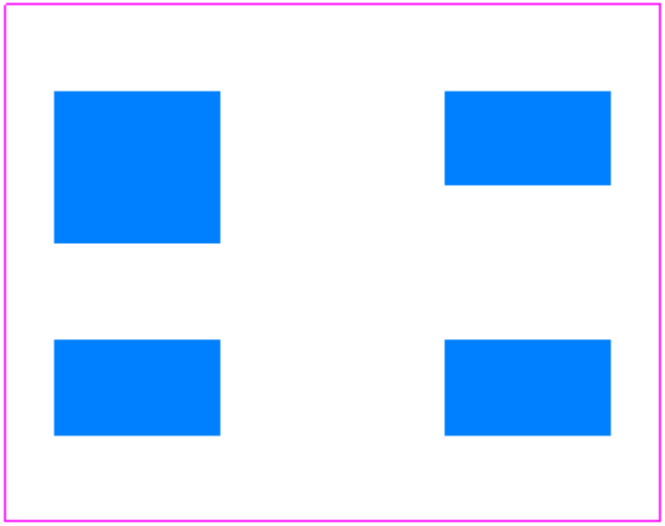


IDF Model

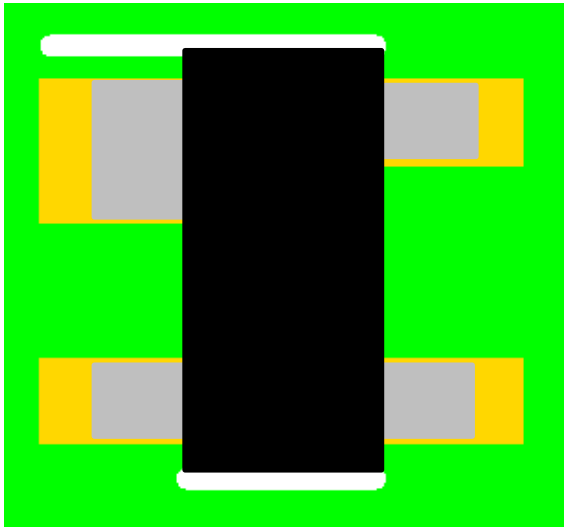


SOT143 & SOT343 Outlines

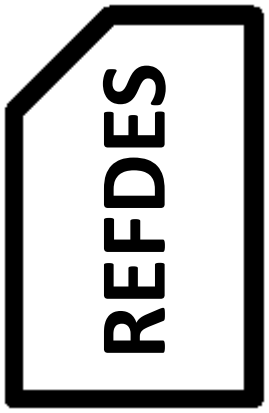
Courtyard



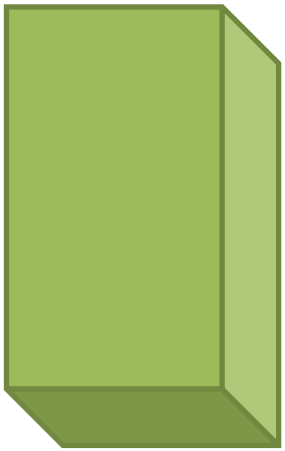
Silkscreen w/Polarity



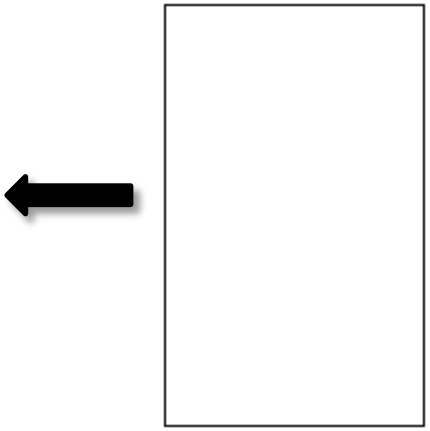
Assembly



IDF Model

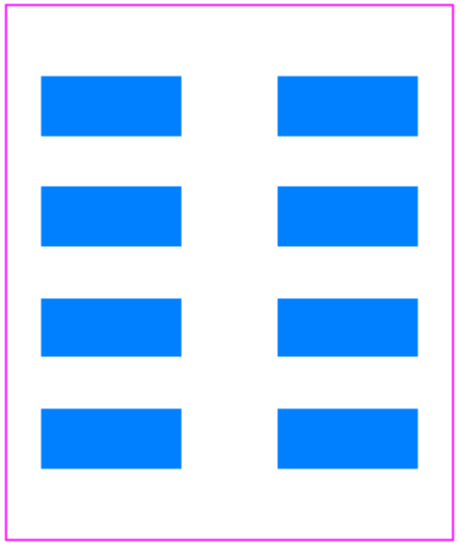


3D Model

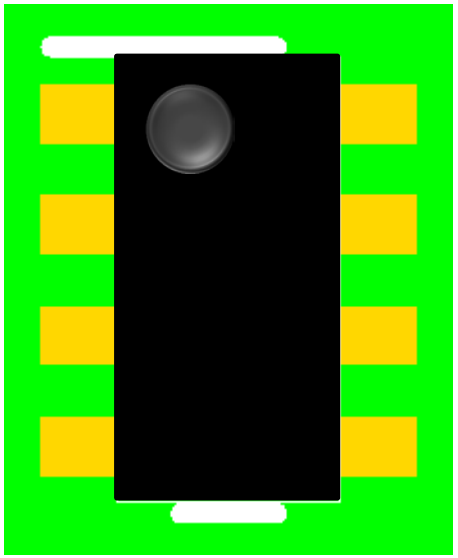


2-Sided Chip Array Outlines

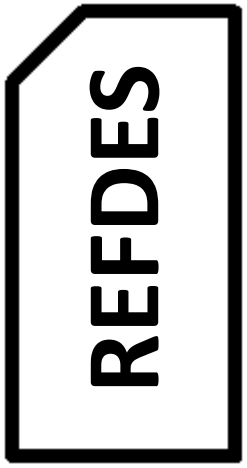
Courtyard



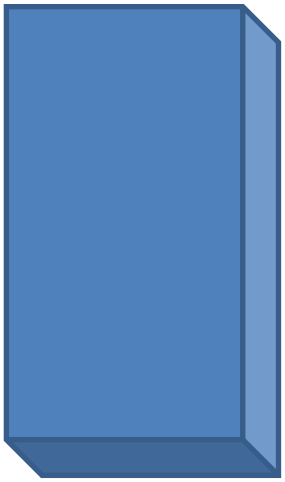
Silkscreen w/Polarity



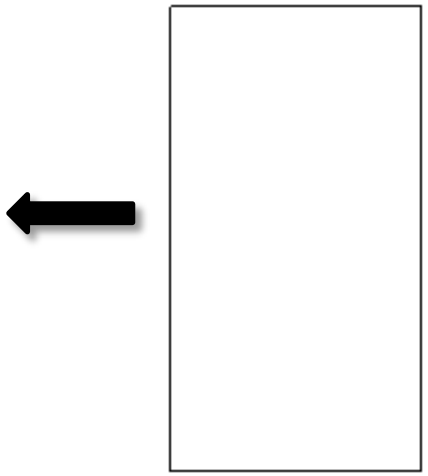
Assembly



IDF Model

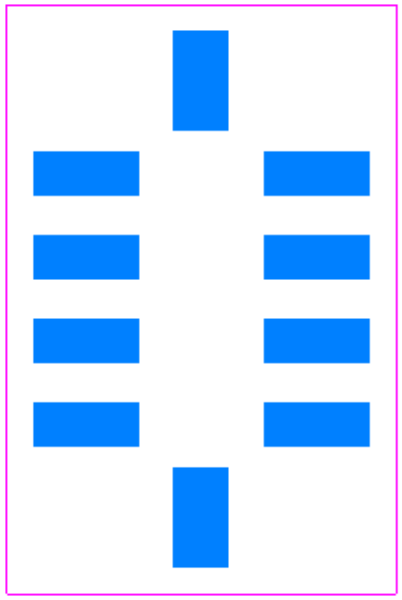


3D Model

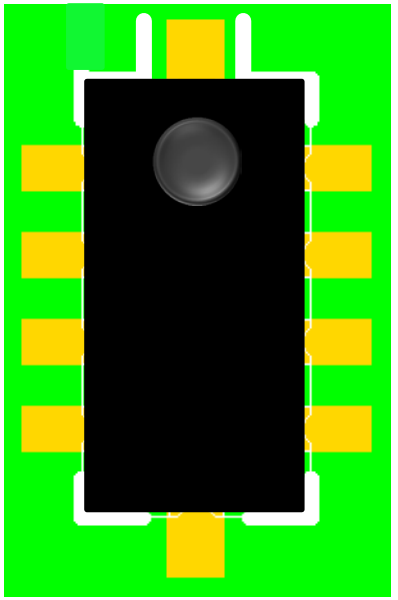


4-Sided Chip Array Outlines

Courtyard

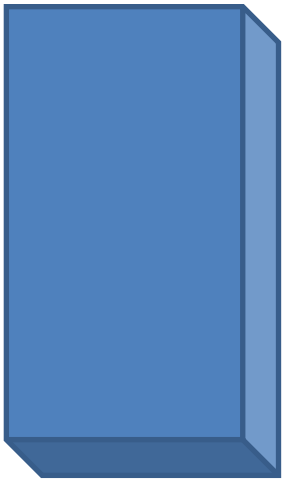


Silkscreen w/Polarity

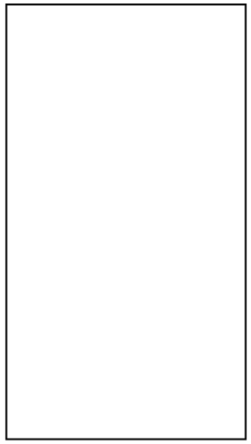


Assembly

IDF Model

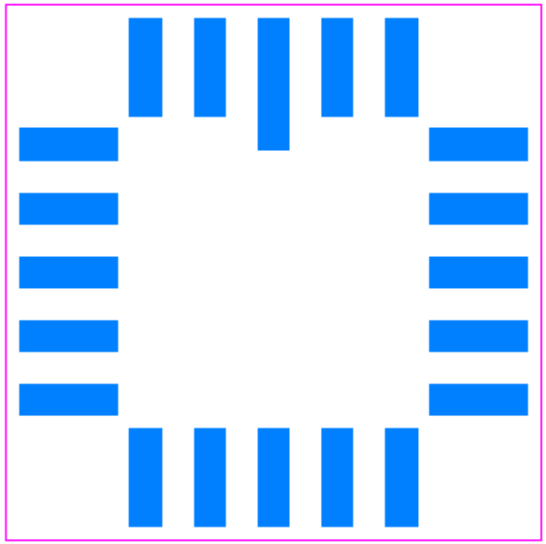


3D Model

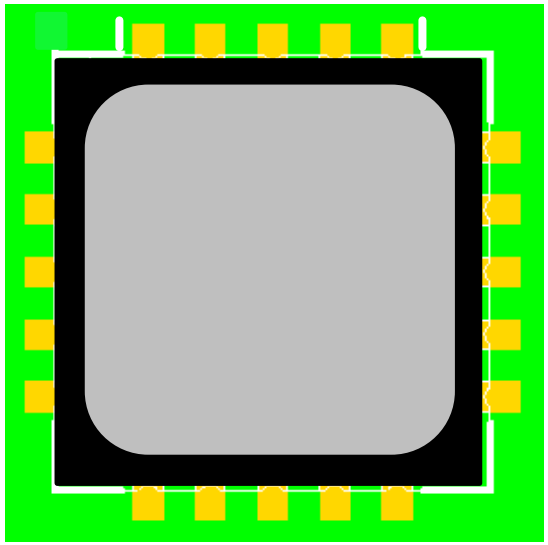


Chip Carrier (LCC & PLCC) Outlines

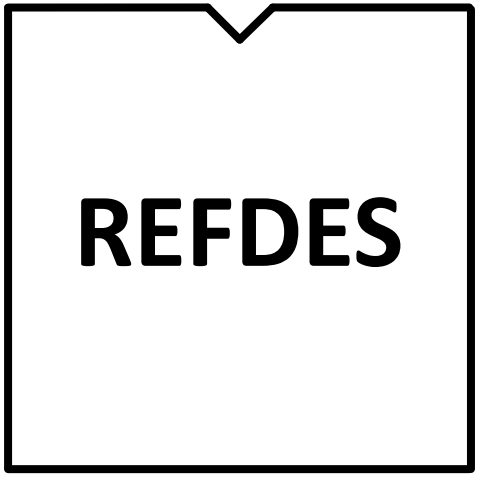
Courtyard



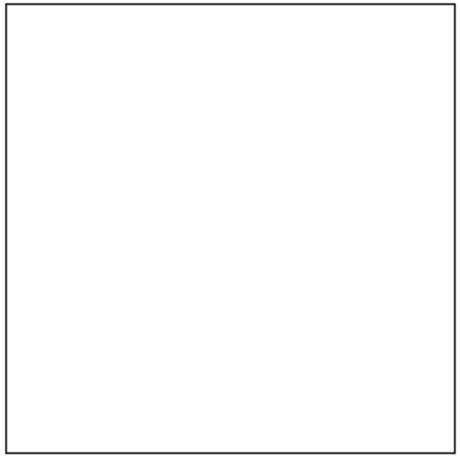
Silkscreen w/Polarity



Assembly

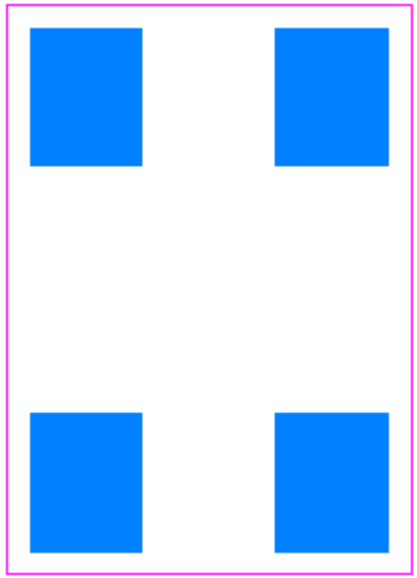


3D Model

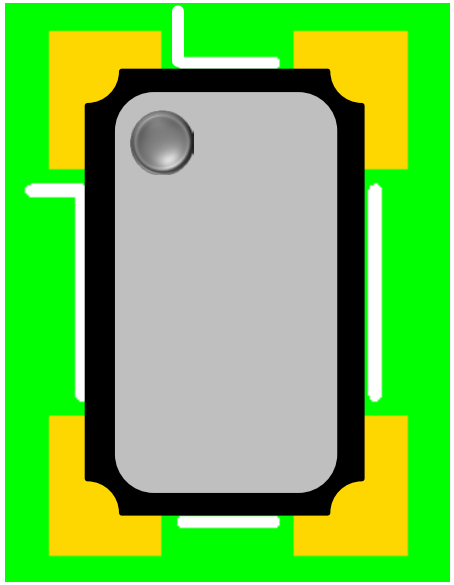


Corner Concave Oscillator Outlines

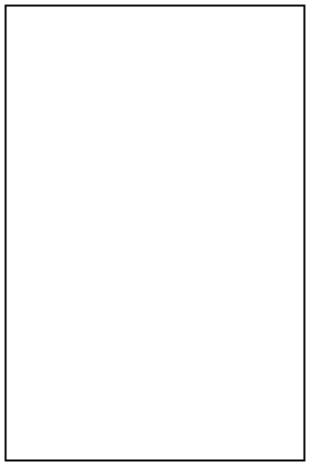
Courtyard



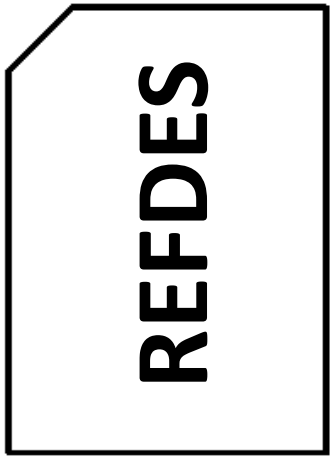
Silkscreen w/Polarity



3D Model



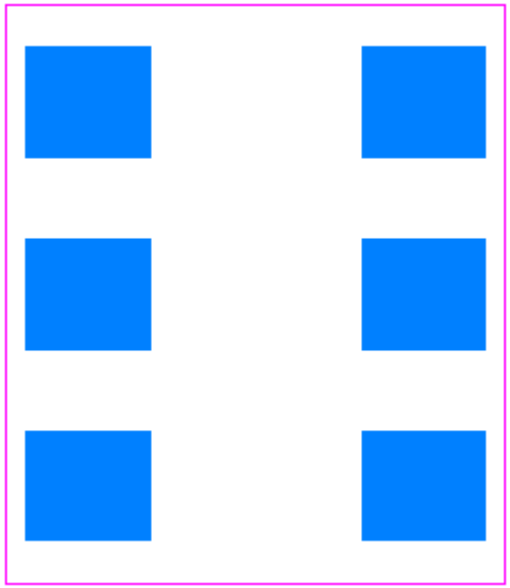
Assembly



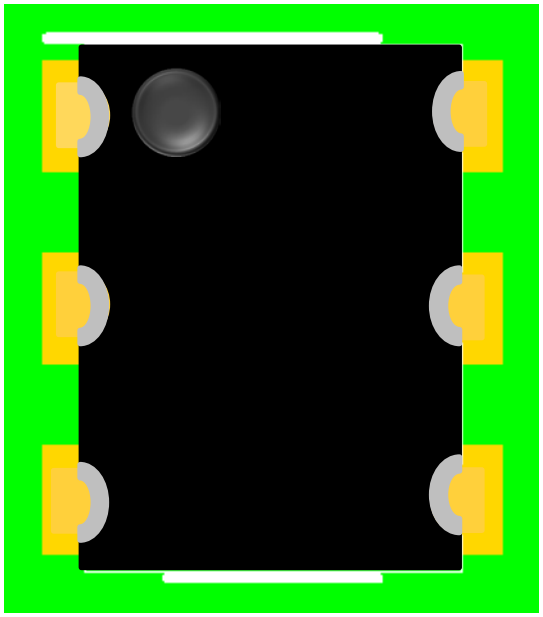
IDF Model

Side Concave Oscillator Outlines

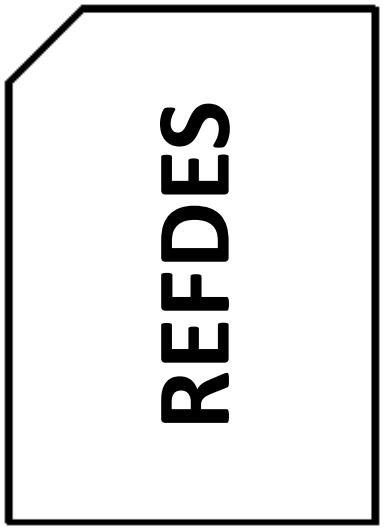
Courtyard



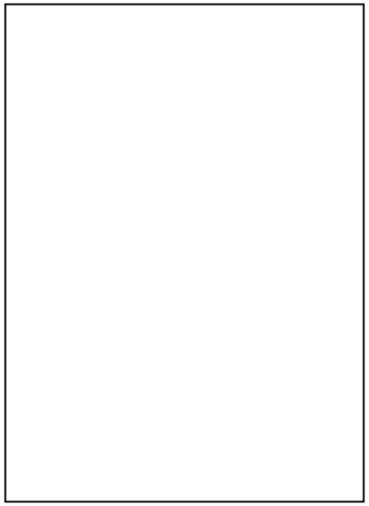
Silkscreen w/Polarity



Assembly



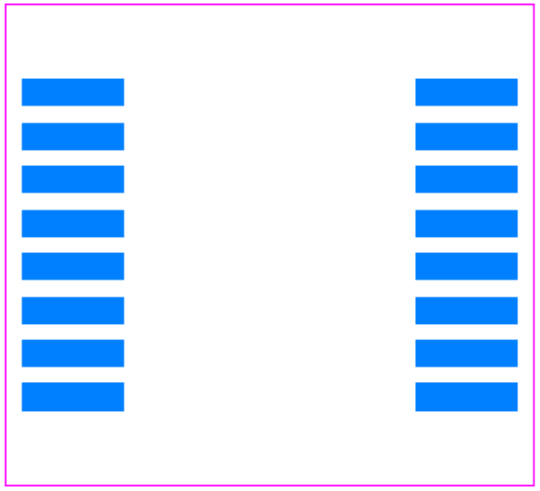
3D Model



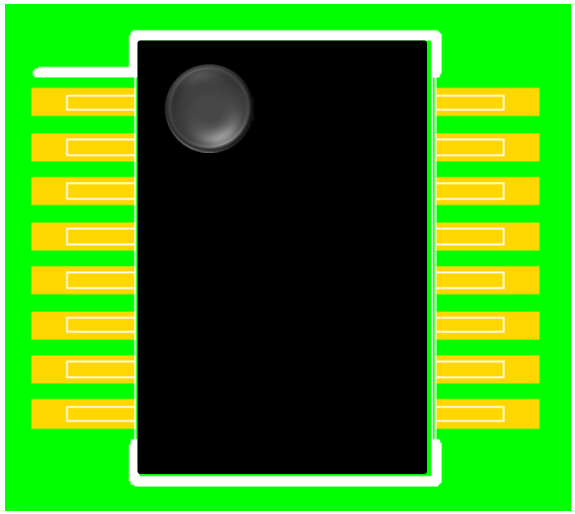
IDF Model

Small Outline (SOP, SON, SOT) Outlines

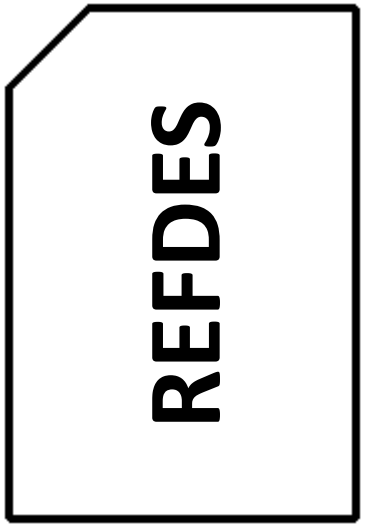
Courtyard



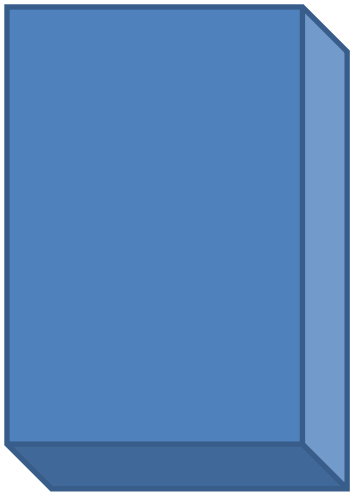
Silkscreen w/Polarity



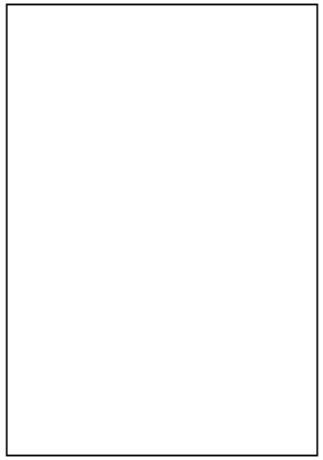
Assembly



IDF Model

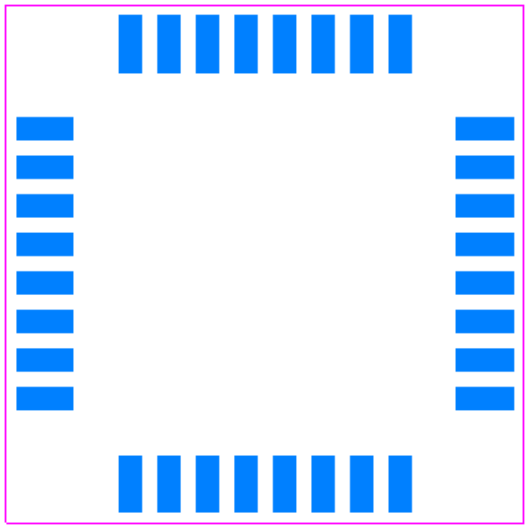


3D Model

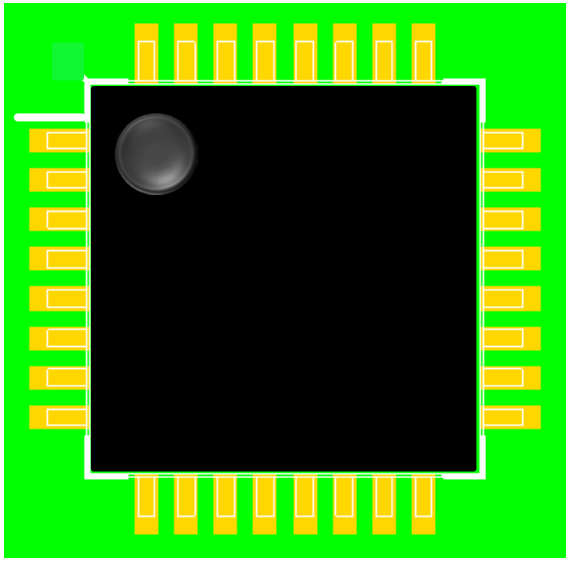


Quad Pack (QFP & QFN) Outlines

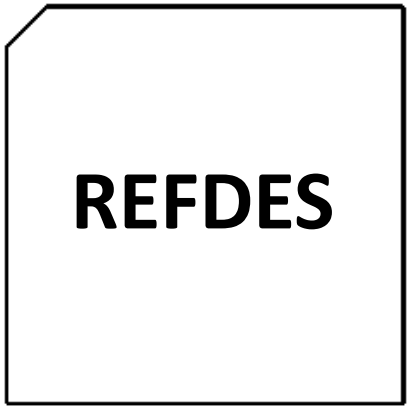
Courtyard



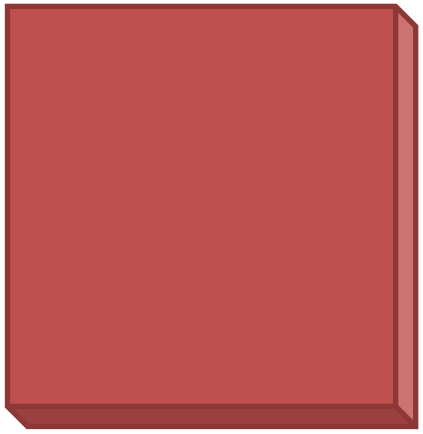
Silkscreen w/Polarity



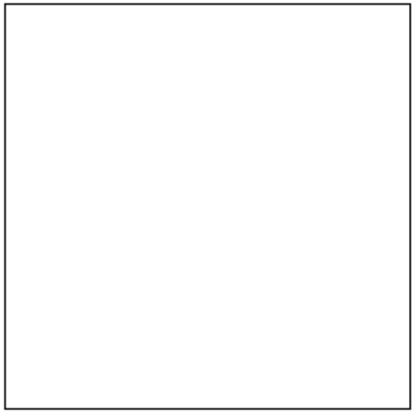
Assembly



IDF Model

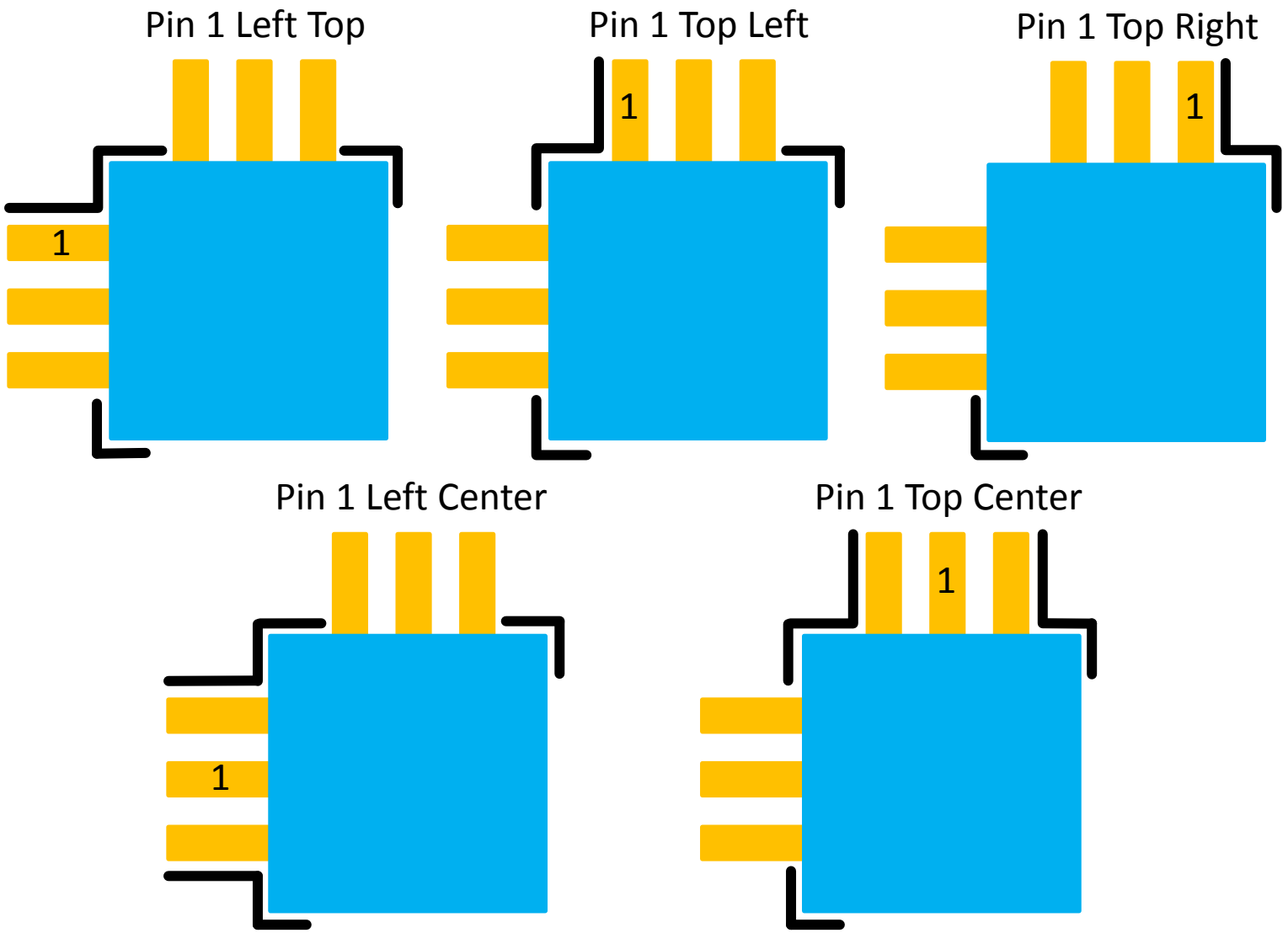


3D Model



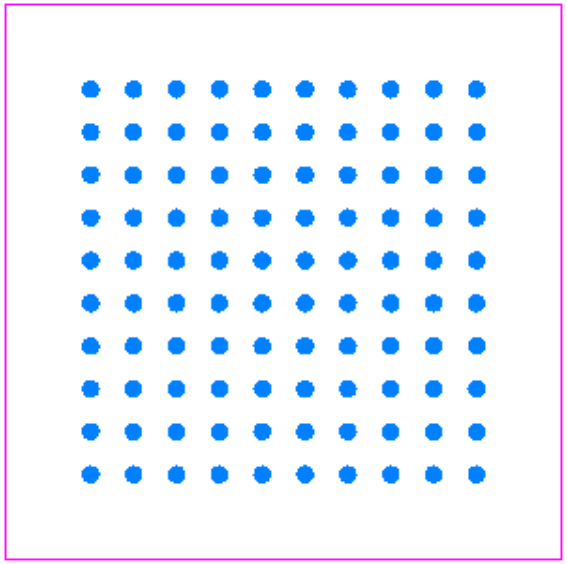
Quad Pack (QFP & QFN) Outlines

New recommendations for quad flat pack outlines & polarity

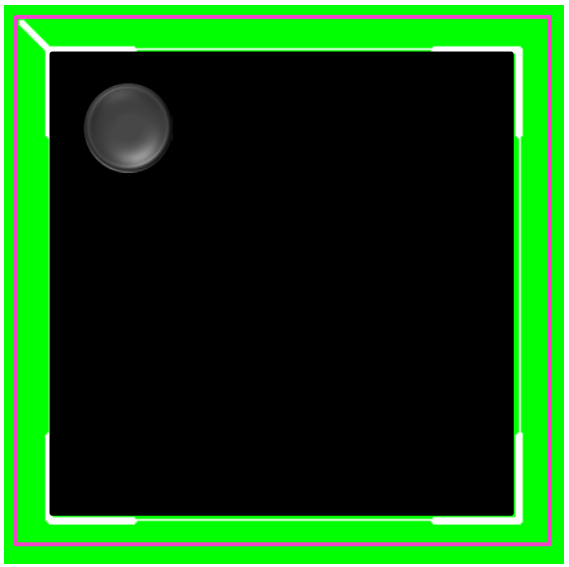


Grid Array (BGA, LGA, CGA) Outlines

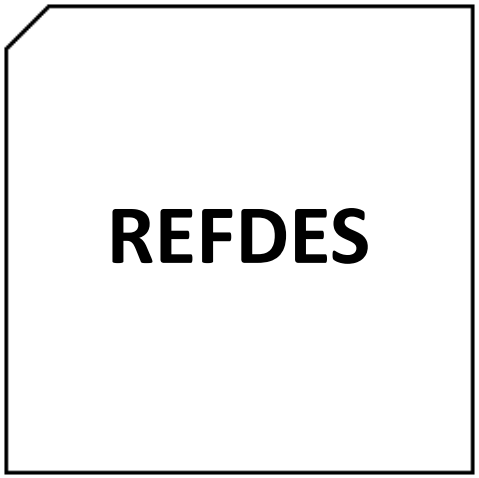
Courtyard



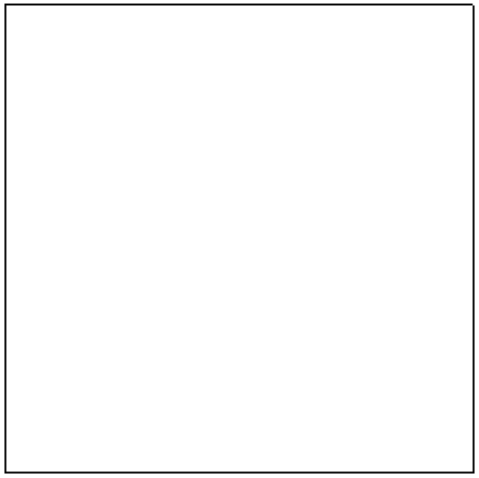
Silkscreen w/Polarity



Assembly



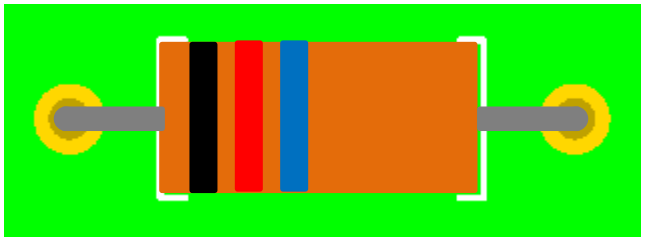
3D Model



Axial Lead Non-polarized Outlines

Silkscreen – Capacitor

Silkscreen - Resistor



Courtyard

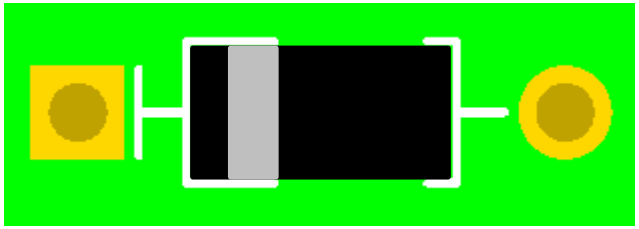
Assembly

IDF Model

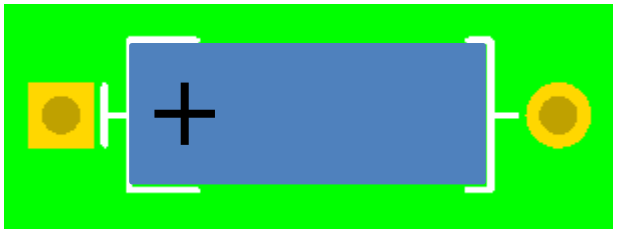
3D Model

Axial Lead Polarized Outlines

Silkscreen - Diode



Silkscreen – Polarized Capacitor



Assembly

Assembly

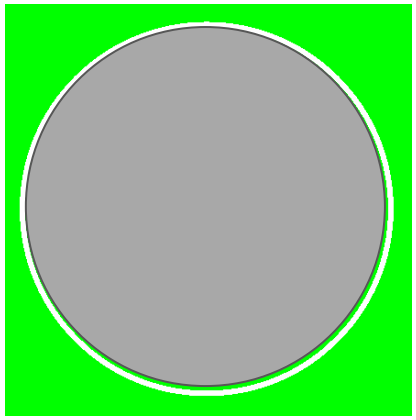
Courtyard

IDF Model

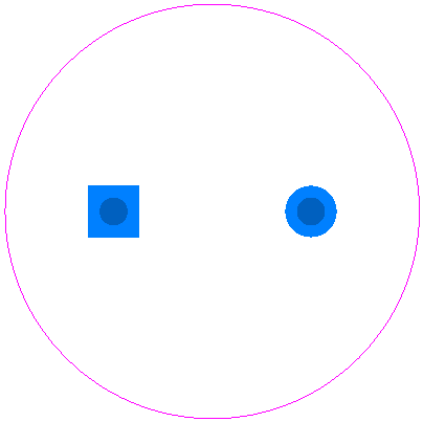
3D Model

Radial Lead Polarized Outlines

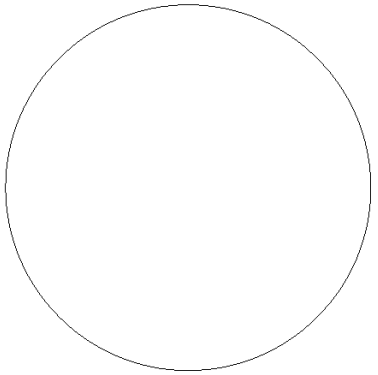
Silkscreen



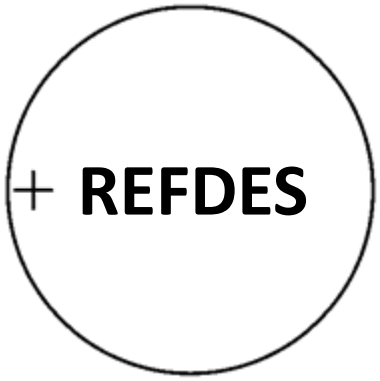
Courtyard



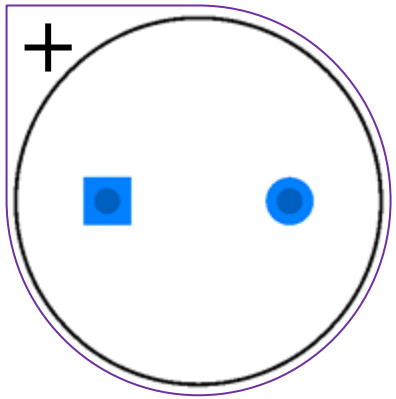
3D Model



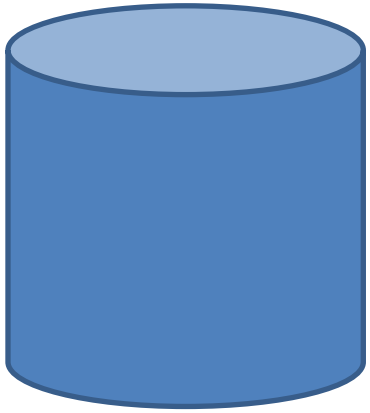
Assembly



Optional Courtyard & Polarity Marking



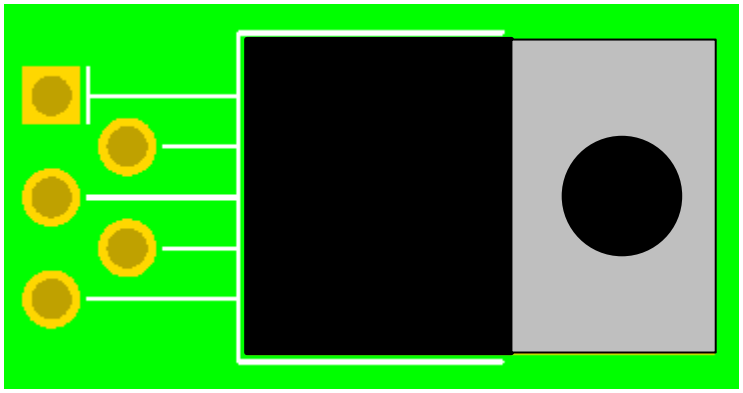
IDF Model



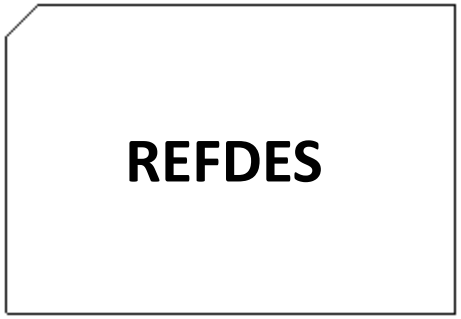
Flange Mount Outlines

Courtyard

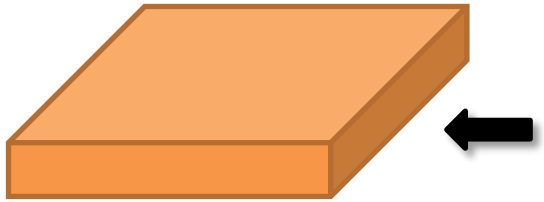
Silkscreen



Assembly



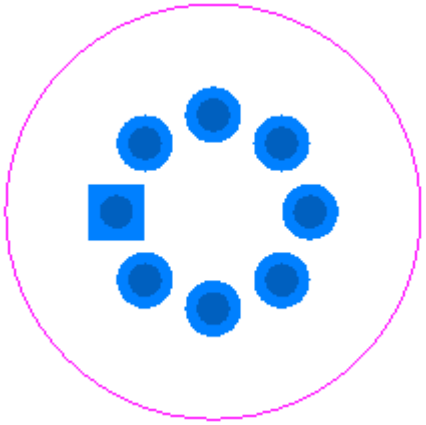
IDF Model



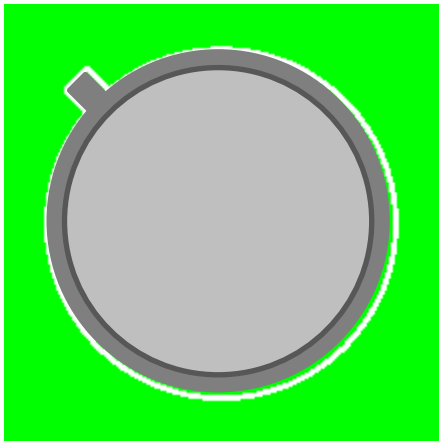
3D Model

Cylindrical Mount Outlines

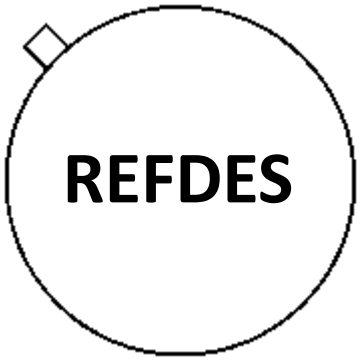
Courtyard



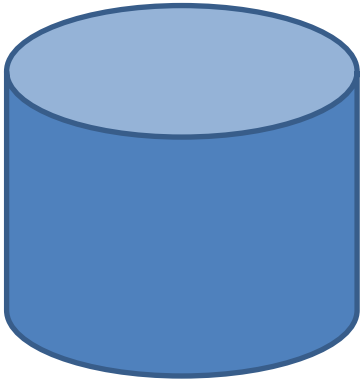
Silkscreen



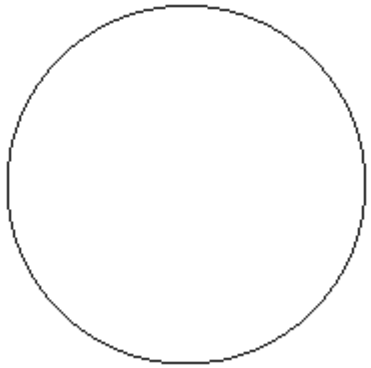
Assembly



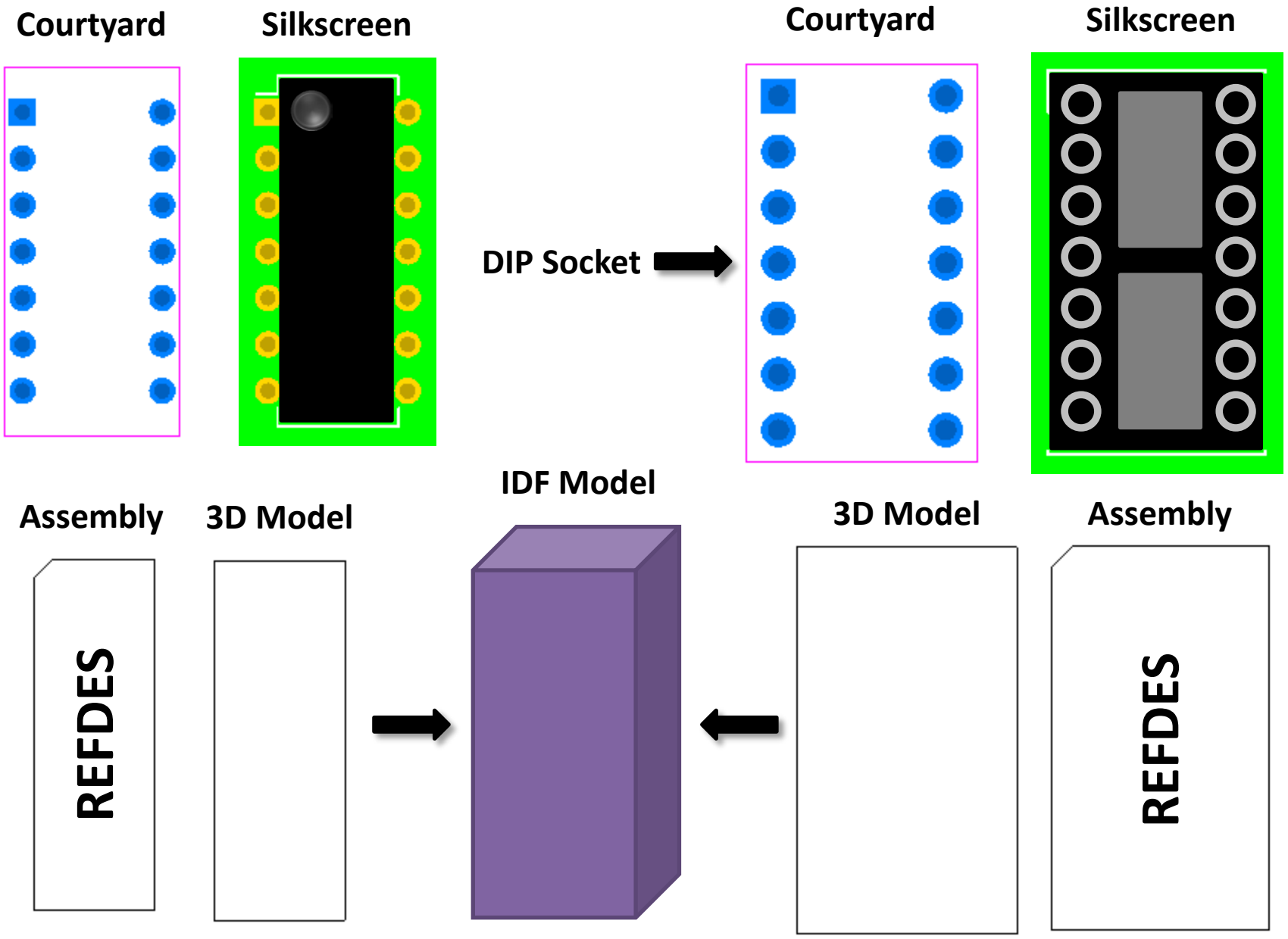
IDF Model



3D Model

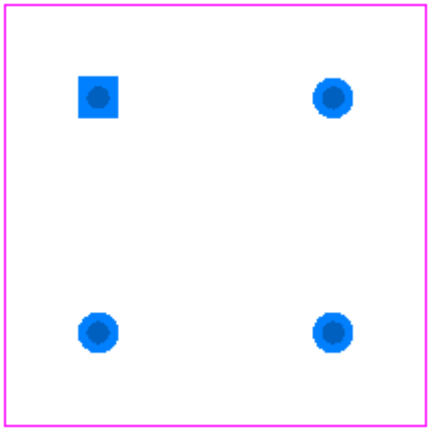


Dual-In-Line Package (DIP) Outlines

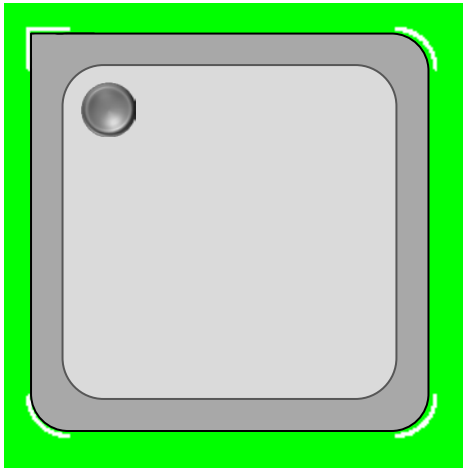


Through-hole Oscillator Outlines

Courtyard

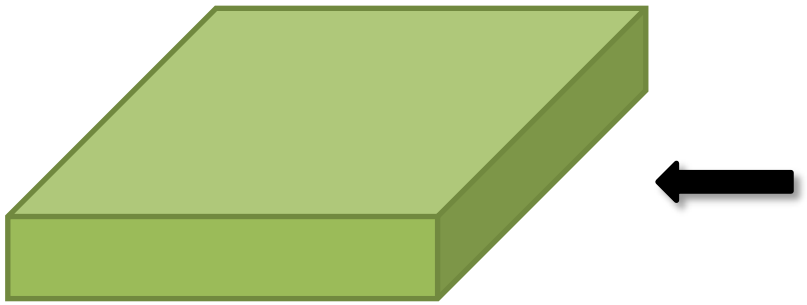


Silkscreen

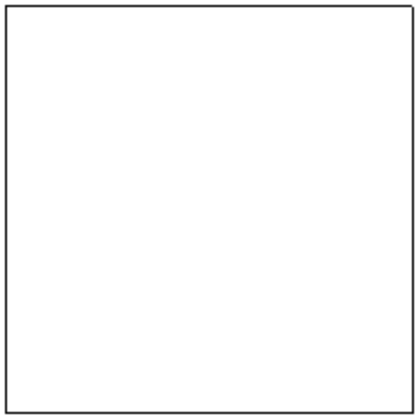


Assembly

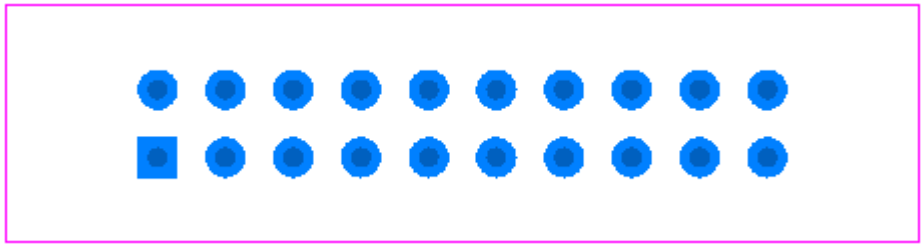
IDF Model



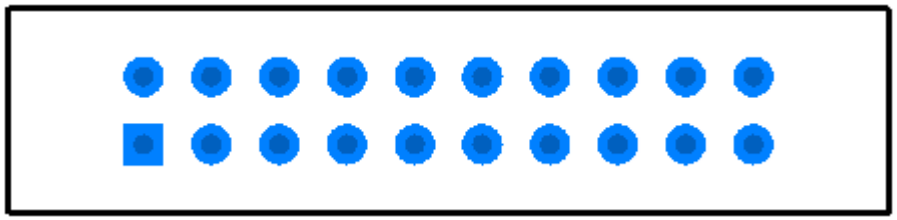
3D Model



Through-hole Connector Outlines

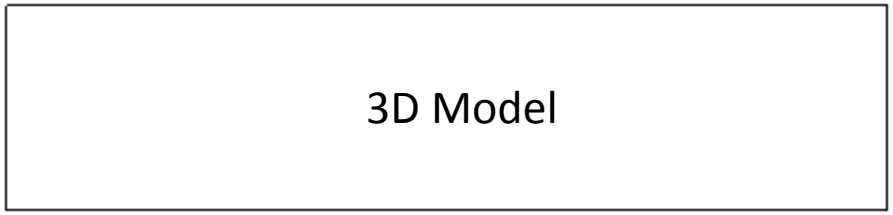


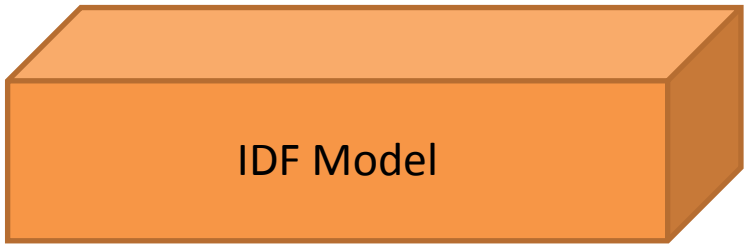
Courtyard



Silkscreen

Assembly





Assembly Reference Designators

0.6 x 0.3

Height 0.5

1.0 x 0.5

Height 0.7

1.6 x 0.8

Height 1.2

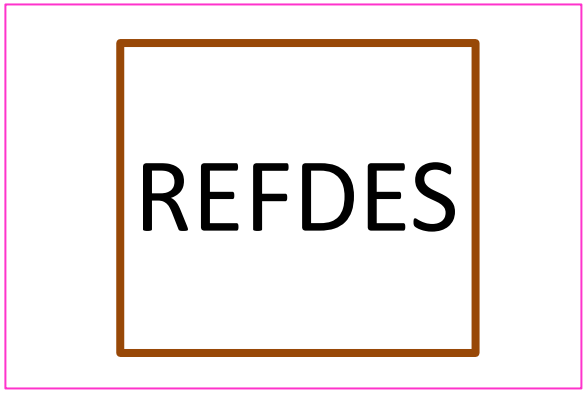
2.0 x 1.25

Height 0.9

3.2 x 1.6

Height 1.2

4.5 x 3.2

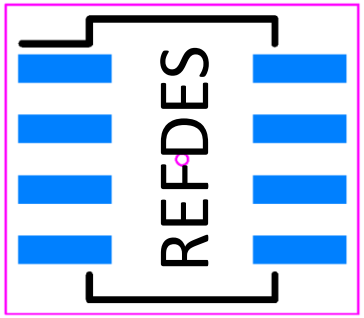


Height 1.5

- The default assembly Ref Des height is 1.5, but for miniature components the text height must be scalable to fit
- For all parts smaller than 2.0 the assembly outline is enlarged to fit Ref Des, but 0.5 is the smallest text height
- The default rotation of the assembly reference designator is associated with the component body length

Silkscreen Reference Designators

- Silkscreen reference designators are normally placed inside the courtyard during library construction and typically located on the land pattern origin. After part placement has been approved, the silkscreen ref des are relocated outside the component body so they are visible after assembly.
- In the past, we always made silkscreen reference designators 1.5 height but now that fabrication technology has improved it's time to support a 3-Tier reference designator option
- The ref des line width is normally 10% of the text height
- Here are the new recommendations for the 3-Tier ref des
  - Least – 1.0 (40 mils) Height
  - Nominal – 1.2 (50 mils) Height
  - Most – 1.5 (60 mils) Height

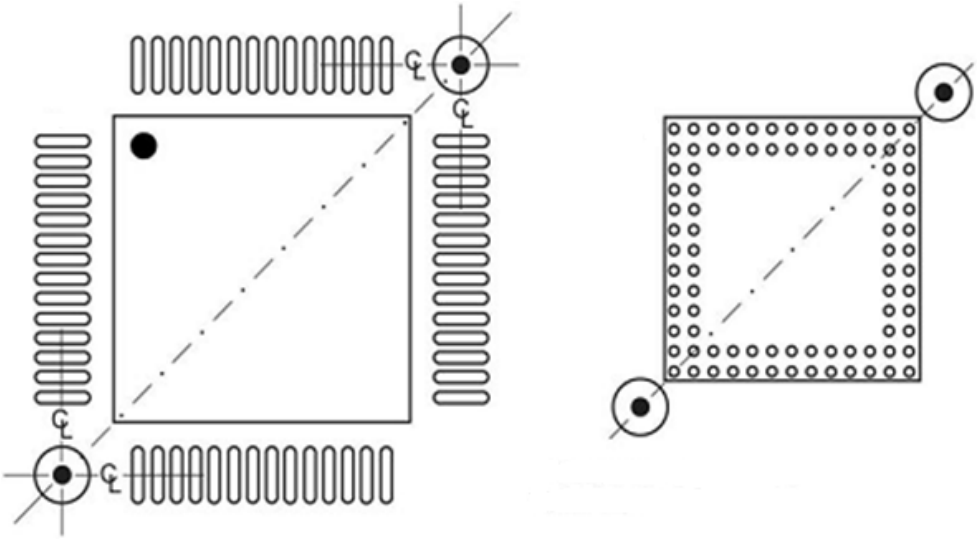


Common Reference Designations

A	separable assembly
AR	amplifier
AT	attenuator; isolator
B	blower, motor
BT	battery
C	capacitor
CB	circuit breaker
CP	connector adapter, coupling
CN	capacitor network
D or **CR**	diode
D or **VR**	breakdown diode
DC	directional coupler
DL	delay line
DS	display, lamp
E	terminal
F	fuse
FD	fiducial
FL	filter
G	generator, oscillator
GN	general network
H	hardware
HY	circulator, directional coupler
J	connector, jack, female
K	contactor, relay
L	coil, inductor, bead, ferrite bead
LS	loudspeaker, buzzer
M	meter
MG	motor-generator
MH	mounting hole
MK	microphone
MP	mechanical part
P	connector, plug, male
PS	power supply
Q	transistor
R	resistor
RN	resistor network
RT	thermistor
S	switch
T	transformer
TB	terminal board, terminal strip
TC	thermocouple
TP	test point, In-circuit test points
TZ	transzorb
U	inseparable assembly, IC pkg
V	electron tube
VR	voltage regulator
W	wire, cable, cable assembly
X	fuseholder, lampholder, socket
Y	crystal, magnetostriction oscillator
Z	miscellaneous

Local Fiducials

- Local Fiducials have been used only on fine pitch QFP and BGA land patterns
  - Fine pitch QFP = Less than 0.635 mm (25 mil) pitch
  - Fine pitch BGA = Less than 0.8 mm (32 mil) pitch
- Future Local Fiducial sizes will be:
  - Level A (Most) = 1.0 mm (40 mil) with 2.0 (80 mil) solder mask & keep-out
  - Level B (Nominal) = 0.75 mm (30 mil) with 1.5 (60) solder mask & keep-out
  - Level C (Least) = 0.5 mm (20 mil) with 1.0 (40 mil) solder mask & keep-out

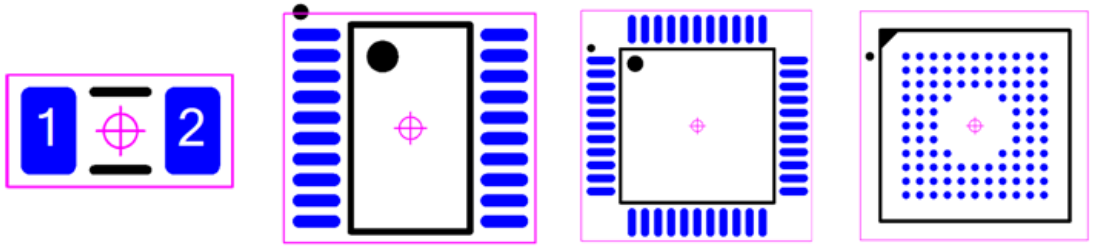


Zero Component Orientation

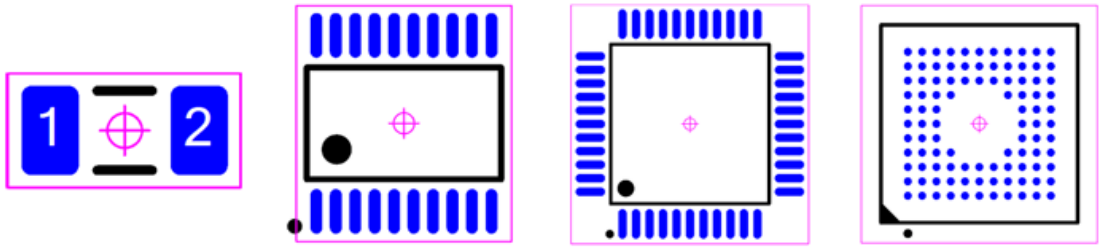
- In 2005 IPC-7351 released the first zero component orientation standard regarding the location of “Pin 1”
- The goal was to define a consistent method for land pattern creation with the main objective to define a “One World CAD Library” to achieve the highest level of electronic product development automation
- In May 2009 IEC land pattern committee voted and approved a new zero component orientation and referred to IPC-7351 as “Level A” and the new standard “Level B”
- The EIA-481-D publishes documentation for component packaging standards for tape & reel, tubes and trays and the component orientation in the packaging should match the orientation of land pattern creation, but component manufacturer’s don’t always adhere to the EIA-481-D

Zero Component Orientation

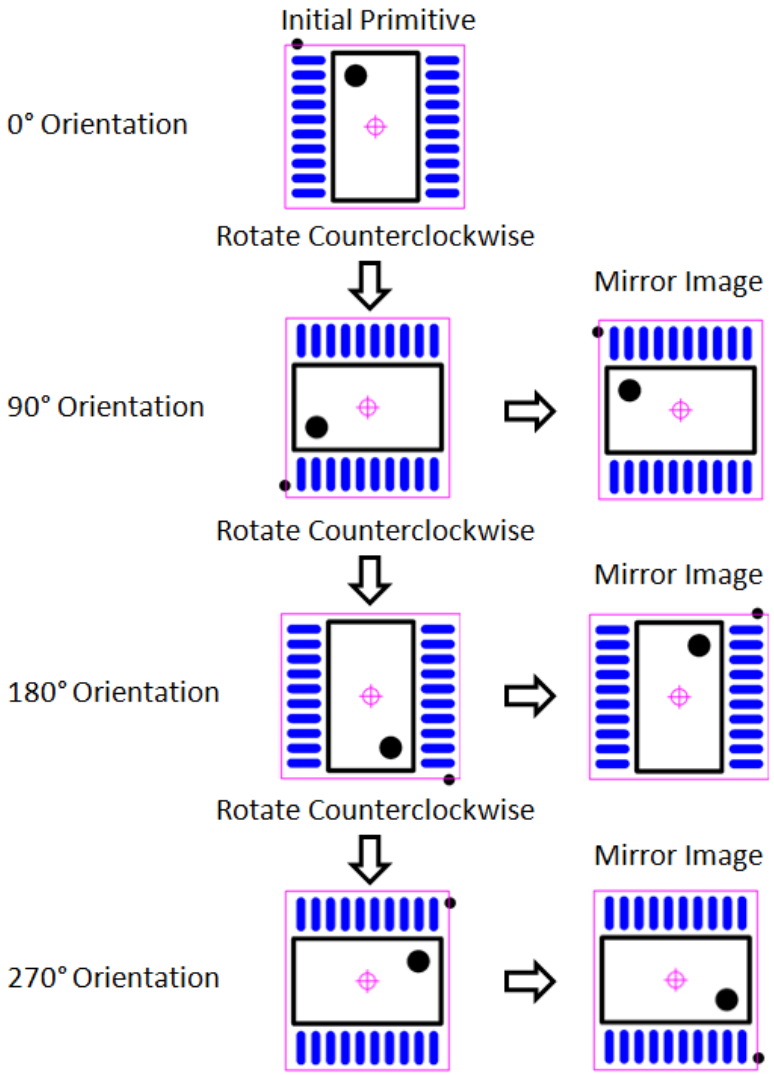
Zero Orientation with Pin 1 in Upper Left Corner
Introduced in 2007 in the IPC-7351A Publication



Zero Orientation with Pin 1 in Lower Left Corner
Introduced in 2009 in the IEC 61188-7 publication



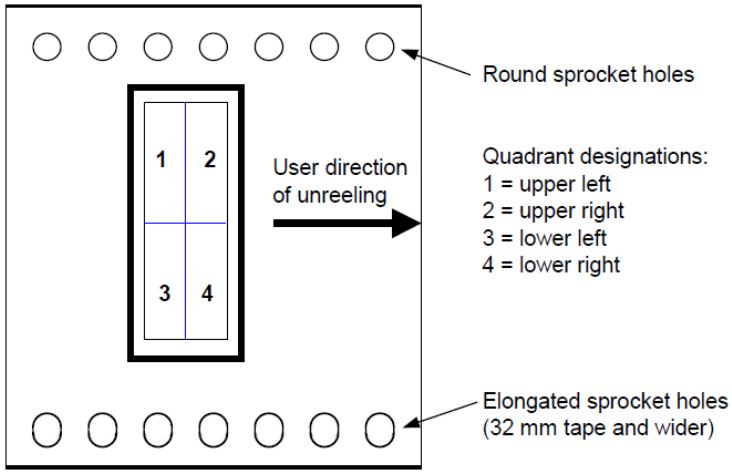
Zero Component Orientation



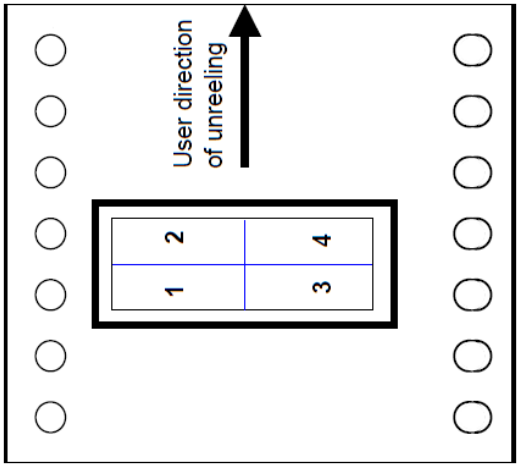
With two variations of “zero component orientation” levels in the description of the CAD system library, it is a mandatory requirement to define which level was used (level A or Level B) for the component descriptions in the data file.

This information is a mandatory requirement in the Header of any file that incorporates land patterns using these principles of zero-based orientation.

EIA-481-D Component Orientation



EIA-481-D standard tape and reel pictures quadrant designations



This picture represents zero component orientation for PCB CAD tool libraries.

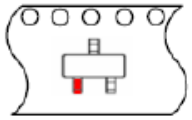
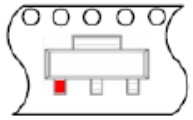
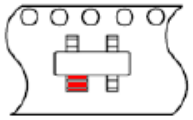
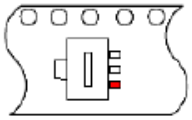
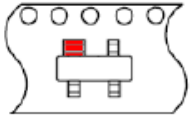
IPC-7351 uses quadrant 2 for zero component orientation and IEC uses quadrant 1 for zero component orientation

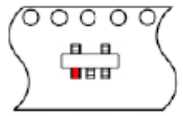
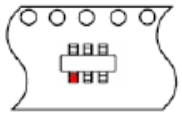
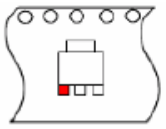
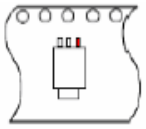
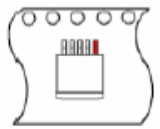
EIA-481-D Component Orientation

Note: IPC-7351 uses quadrant 2 and IEC uses quadrant 1

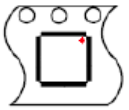
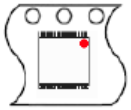
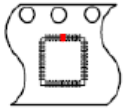
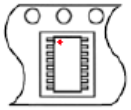
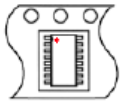
Orientation Guide for Commonly Used Devices

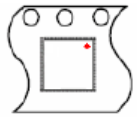
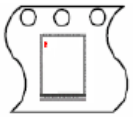
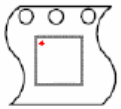
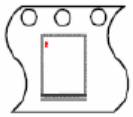
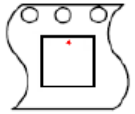
DIRECTION OF UNREELING

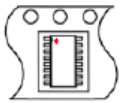
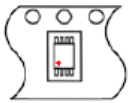
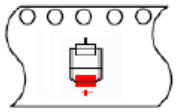
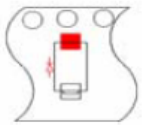
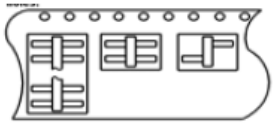
Component Package	SOT23	SOT223	SOT143	SOT89	SOT343
Orientation in carrier					
Termination 1 Orientation by Quadrant	1 2 / **3** 4	1 2 / **3** 4	1 2 / **3** 4	1 2 / 3 **4**	**1** 2 / 3 4

Component Package	SOT23-5 / SC70-5 / SSOP-5	SOT23-6 / SC70-6 / SSOT-6	TO-89	DPAK / D2PAK / TO-252 / TO-220	D2PAK-5P / TO-263-5
Orientation in carrier					
Termination 1 Orientation by Quadrant	1 2 / **3** 4	1 2 / **3** 4	1 2 / **3** 4	1 **2** / 3 4	1 **2** / 3 4

EIA-481-D Component Orientation

Component Package	QFP	TSOP	PLCC	SOIC	DIP
Orientation in carrier					
Termination 1 Orientation by Quadrant	1 **2** 3 4	1 **2** 3 4	**1** **2** 3 4	**1** 2 3 4	1 **2** 3 4

Component Package	QFN (Square geometry)	QFN (Rectangular geometry)	BGA (Square geometry)	BGA (Rectangular geometry)	LCC
Orientation in carrier					
Termination 1 Orientation by Quadrant	1 **2** 3 4	**1** 2 3 4	**1** 2 3 4	**1** 2 3 4	**1** **2** 3 4

Component Package	SSOP / TSSOP / MSOP	Ultra Thin SO8 (US8)	Tantalum Capacitor	DIODE / LED	Connectors (square or rectangular)
Orientation in carrier					
Termination 1 Orientation by Quadrant	**1** 2 3 4	1 2 **3** 4	1 2 **3** **4**	**1** **2** 3 4	**1** **2** 3 4

Zero Component Orientation

Component Family	IPC-7x51 (Level A)	IEC 61188-7 (Level B)	EIA-481-D
Chip (All Families)	Polarization On Left	Polarization On Left	Polarization On Left
Tantalum Capacitor	Polarization On Left	Polarization On Left	Polarization On Right
Molded Body Diode	Polarization On Left	Polarization On Left	Polarization On Left
SODFL	Polarization On Left	Polarization On Left	Polarization On Left
MELF	Polarization On Left	Polarization On Left	Polarization On Left
Aluminum Capacitor	Polarization On Left	Polarization On Left	Polarization On Left
Precision Inductors	Left	Left	Left
PLCC, LCC	Upper Center	Left Center	Left Center
QFP & CQFP	Upper Left	Lower Left	Upper Left
Bump QFP Side	Upper Left	Lower Left	Upper Left
Bump QFP Center	Upper Center	Left Center	Left Center
SOIC, SOP, CFP, SOJ	Upper Left	Lower Left	Lower Left
BGA, LGA, CGA, PGA	Upper Left	Lower Left	Lower Left
QFN Square	Upper Left	Lower Left	Upper Left
QFN Rectangle	Upper Left	Lower Left	Lower Left
Chip Array	Upper Left	Lower Left	Lower Left
DFN	Upper Left	Lower Left	Lower Right
SON	Upper Left	Lower Left	Lower Right
SOT23, SOT223	Upper Left	Lower Left	Lower Right
SOT143	Upper Left	Lower Left	Lower Right
SOT343	Upper Left	Lower Left	Upper left
SOT89	Upper Left	Lower Left	Upper Right
SOTFL	Upper Left	Lower Left	Lower Right
TO-252	Upper Left	Lower Left	Upper Left
TO-263	Upper Left	Lower Left	Upper Left
Oscillator (Multi-pin)	Upper Left	Lower Left	Lower Left
Crystal (2-pin)	Left	Left	Left
SMT Connectors	Left	Left	Left
PTH Connectors	Left	Left	Left
DIP	Upper Left	Lower Left	Lower Left
SIP	Upper	Left	Left
Axial Lead	Polarization On Left	Polarization On Left	Polarization On Left
Radial Lead	Polarization On Left	Polarization On Left	Polarization On Left

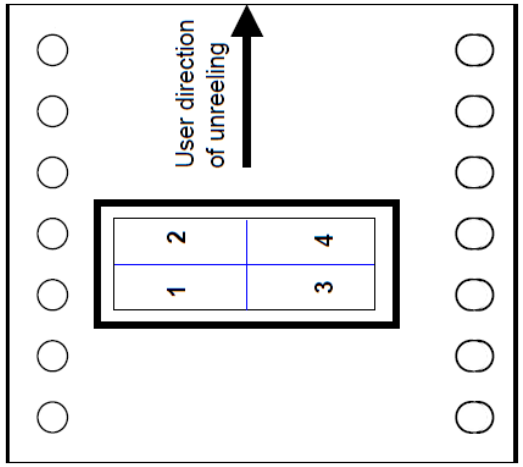
EIA Color Code:

Green = Match

Red = No Match

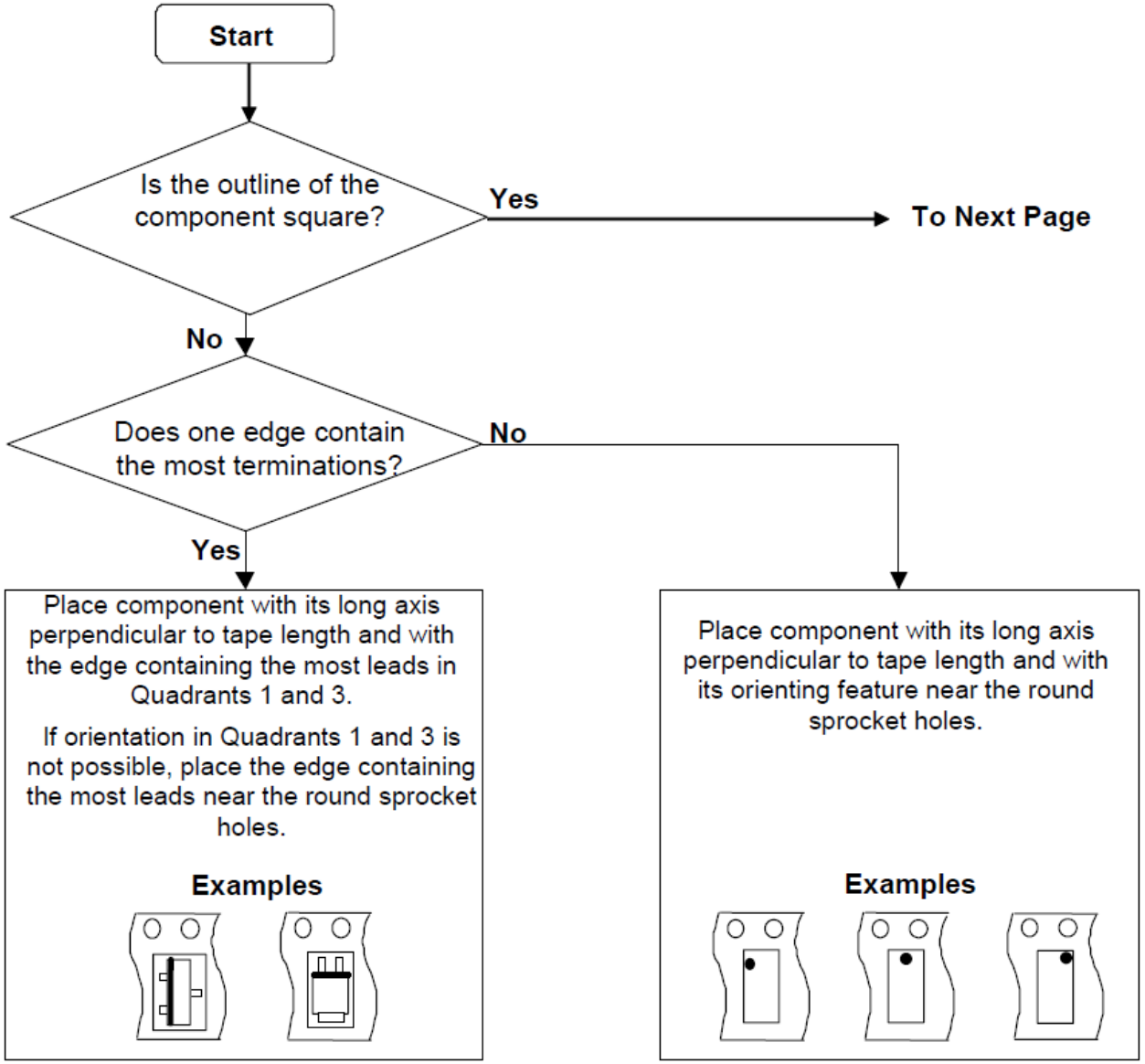
Purple = IPC

Blue = IEC



EIA-481-D Component Orientation

Rules for determining orientation of component in tape pocket (1 of 2)



EIA-481-D Component Orientation

Rules for determining orientation of component in tape pocket (2 of 2)

From Previous Page

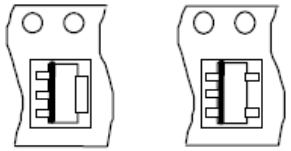
Does one edge contain the most terminations?

No

Yes

Place component with the edge containing most terminations in Quadrants 1 and 3.

Examples



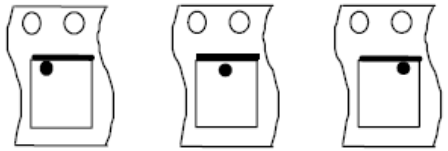
Is the orienting feature close to or associated with only one edge?

No

Yes

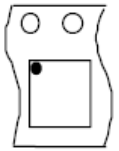
Place component with the edge associated with the orienting feature near the round sprocket holes.

Examples



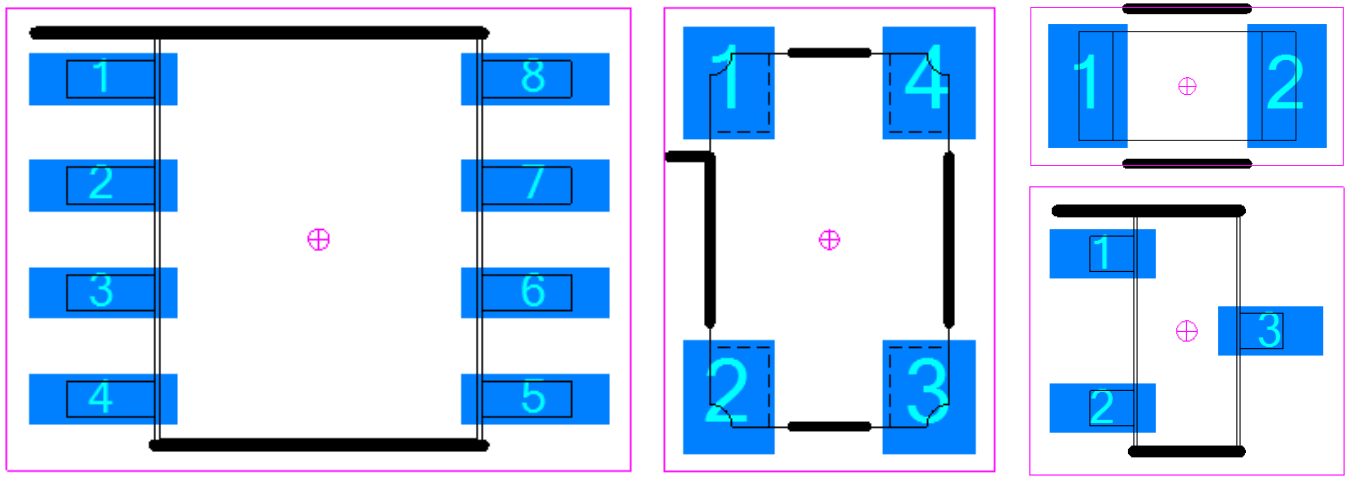
Place component with its orienting feature in Quadrant 1.

Example



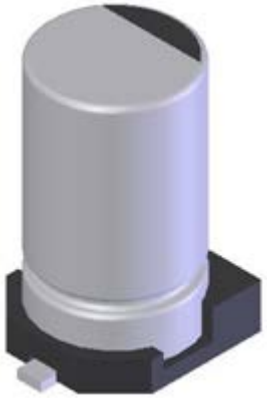
Land Pattern Origins

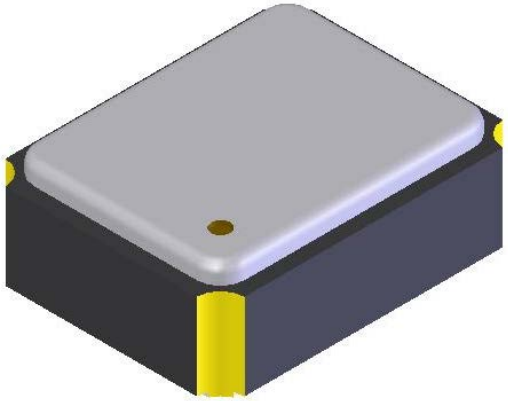
- The land pattern origin is typically located at the center of gravity of the component, but sometimes this is difficult to calculate with irregular shaped components, so Pin 1 is used in these cases. Also Pin 1 in most through-hole connectors.
- The centroid origin marking in the picture below is an unfilled 0.5 (20 mil) diameter circle with a 0.01 (1 mil) line width with a 0.8 (32 mil) crosshair for cursor alignment.

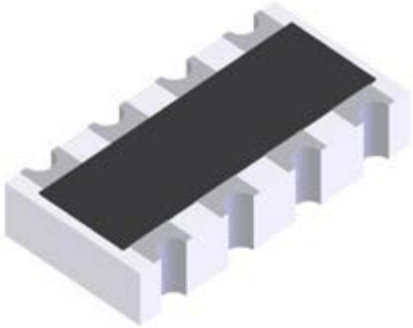


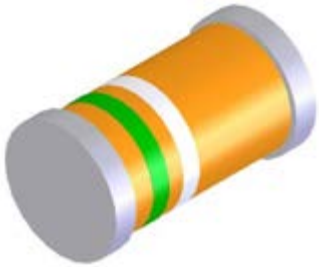
3D Modeling

- Every CAD tool has a different approach to handling 3D Models of component data. Some are much more elaborate than others.
- The CAD Library of the Future will have 3D IDF Model attributes built into every land pattern to use as a mechanical drafting aid for the reduction of errors in product packaging
- Best 3D “Solid” Model format today is “STEP”









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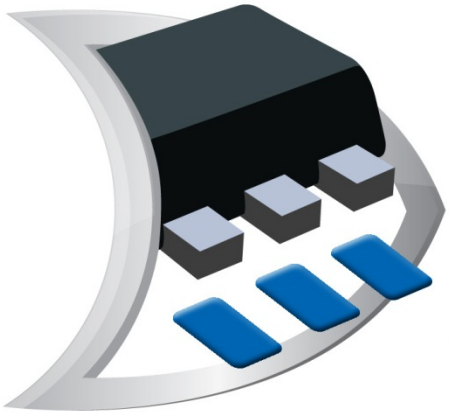
- PCB Libraries, Inc. is interested in selling the library parts that you create using the new PCBL Calculator for a 25% lifetime royalty via Pay Pal. This is the **POD** (Parts On Demand) project.
- PCB Libraries, Inc. is also interested in selling your schematic symbols, 3D models and non-standard PCB library parts on our website and pay you a 25% lifetime royalty via Pay Pal.
- The new web-based Vending Machine will open in Summer 2012 and all library uploads are a first come first serve basis. If you upload a library part first, you lock into the sales of that part.



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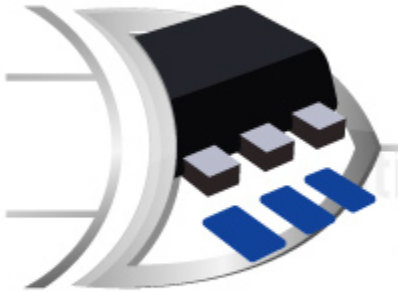

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