



## UNIVERSAL ACTIVE FILTER

Check for Samples: [UAF42](#)

### FEATURES

- **VERSATILE:**
  - Low-Pass, High-Pass
  - Band-Pass, Band-Reject
- **SIMPLE DESIGN PROCEDURE**
- **ACCURATE FREQUENCY AND Q:**
  - Includes On-Chip 1000pF  $\pm 0.5\%$  Capacitors

### APPLICATIONS

- **TEST EQUIPMENT**
- **COMMUNICATIONS EQUIPMENT**
- **MEDICAL INSTRUMENTATION**
- **DATA ACQUISITION SYSTEMS**
- **MONOLITHIC REPLACEMENT FOR UAF41**

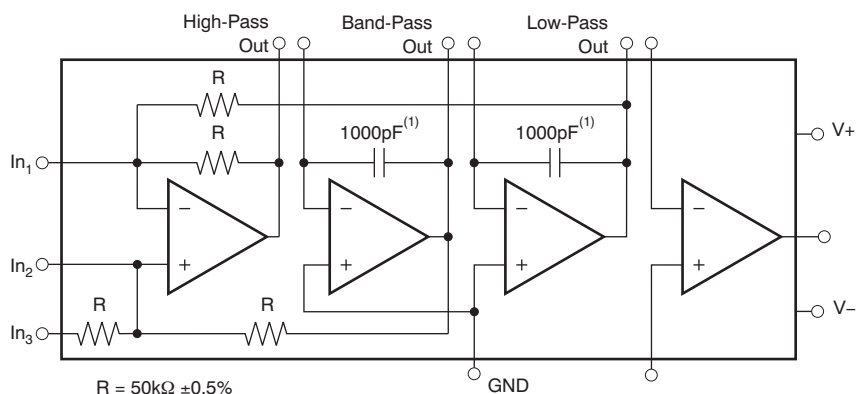
### DESCRIPTION

The UAF42 is a universal active filter that can be configured for a wide range of low-pass, high-pass, and band-pass filters. It uses a classic state-variable analog architecture with an inverting amplifier and two integrators. The integrators include on-chip 1000pF capacitors trimmed to 0.5%. This architecture solves one of the most difficult problems of active filter design—obtaining tight tolerance, low-loss capacitors.

A DOS-compatible filter design program allows easy implementation of many filter types, such as Butterworth, Bessel, and Chebyshev. A fourth, uncommitted FET-input op amp (identical to the other three) can be used to form additional stages, or for special filters such as band-reject and Inverse Chebyshev.

The classical topology of the UAF42 forms a time-continuous filter, free from the anomalies and switching noise associated with switched-capacitor filter types.

The UAF42 is available in 14-pin plastic DIP and SOIC-16 surface-mount packages, specified for the  $-25^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  temperature range.



NOTE: (1)  $\pm 0.5\%$ .



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Over operating free-air temperature range unless otherwise noted.

	UAF42	UNIT
Power Supply Voltage	$\pm 18$	V
Input Voltage	$\pm V_S \pm 0.7$	V
Output Short-Circuit	Continuous	
Operating Temperature	$-40$ to $+85$	$^{\circ}\text{C}$
Storage Temperature	$-40$ to $+125$	$^{\circ}\text{C}$
Junction Temperature	$+125$	$^{\circ}\text{C}$

- (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended period may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.

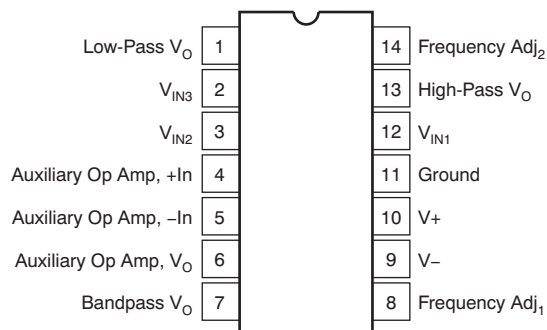
## ORDERING INFORMATION<sup>(1)</sup>

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING
UAF42AP	PDIP-14	N	UAF42AP
UAF42APG4			
UAF42AU	SOIC-16	DW	UAF42AU
UAF42AUE4			

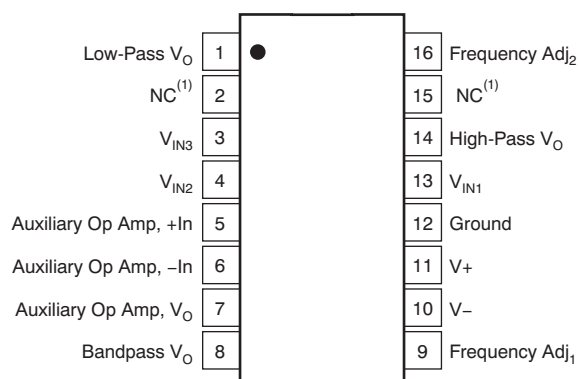
- (1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).

## PIN CONFIGURATIONS

**P PACKAGE  
PDIP-14  
(TOP VIEW)**



**U PACKAGE  
SOIC-16  
(TOP VIEW)**



NOTE: (1) NC = no connection. For best performance connect all NC pins to ground to minimize inter-lead capacitance.

## ELECTRICAL CHARACTERISTICS

At  $T_A = +25^\circ\text{C}$ , and  $V_S = \pm 15\text{V}$ , unless otherwise noted.

PARAMETER	CONDITIONS	UAF42AP, AU			UNIT
		MIN	TYP	MAX	
<b>FILTER PERFORMANCE</b>					
Frequency Range, $f_n$	$f = 1\text{kHz}$		0 to 100		kHz
Frequency Accuracy vs Temperature			0.01	1	%
Maximum Q			400		—
Maximum (Q • Frequency) Product			500		kHz
Q vs Temperature	$(f_O \cdot Q) < 10^4$		0.01		%/°C
	$(f_O \cdot Q) < 10^5$		0.025		%/°C
Q Repeatability	$(f_O \cdot Q) < 10^5$		2		%
Offset Voltage, Low-Pass Output				±5	mV
Resistor Accuracy			0.5	1	%
<b>OFFSET VOLTAGE<sup>(1)</sup></b>					
Input Offset Voltage	$V_S = \pm 6\text{V to } \pm 18\text{V}$		±0.5	±5	mV
vs Temperature			±3		μV/°C
vs Power Supply		80	96		dB
<b>INPUT BIAS CURRENT<sup>(1)</sup></b>					
Input Bias Current	$V_{CM} = 0\text{V}$		10	50	pA
Input Offset Current	$V_{CM} = 0\text{V}$		5		pA
<b>NOISE</b>					
Input Voltage Noise					
Noise Density: $f = 10\text{Hz}$					
Noise Density: $f = 10\text{kHz}$					
Voltage Noise: BW = 0.1Hz to 10Hz					
Input Bias Current Noise					
Noise Density: $f = 10\text{kHz}$					
<b>INPUT VOLTAGE RANGE<sup>(1)</sup></b>					
Common-Mode Input Range	$V_{CM} = \pm 10\text{V}$		±11.5		V
Common-Mode Rejection		80	96		dB
<b>INPUT IMPEDANCE<sup>(1)</sup></b>					
Differential			$10^{13} \parallel 2$		Ω    pF
Common-Mode			$10^{13} \parallel 6$		Ω    pF
<b>OPEN-LOOP GAIN<sup>(1)</sup></b>					
Open-Loop Voltage Gain	$V_O = \pm 10\text{V}, R_L = 2\text{k}\Omega$	90	126		dB
<b>FREQUENCY RESPONSE</b>					
Slew Rate	$G = +1$		10		V/μs
Gain-Bandwidth Product			4		MHz
Total Harmonic Distortion			0.1		%
<b>OUTPUT<sup>(1)</sup></b>					
Voltage Output	$R_L = 2\text{k}\Omega$	±11	±11.5		V
Short Circuit Current			±25		mA

(1) Specifications apply to uncommitted op amp,  $A_4$ . The three op amps forming the filter are identical to  $A_4$  but are tested as a complete filter.

**ELECTRICAL CHARACTERISTICS (continued)**At  $T_A = +25^{\circ}\text{C}$ , and  $V_S = \pm 15\text{V}$ , unless otherwise noted.

PARAMETER	CONDITIONS	UAF42AP, AU			UNIT
		MIN	TYP	MAX	
POWER SUPPLY					
Specified Operating Voltage			±15		V
Operating Voltage Range		±6		±18	V
Current			±6	±7	mA
TEMPERATURE RANGE					
Specified		−25		+85	°C
Operating		−25		+85	°C
Storage		−40		+125	°C
Thermal Resistance, θJA			100		°C/W

## APPLICATION INFORMATION

The UAF42 is a monolithic implementation of the proven state-variable analog filter topology. This device is pin-compatible with the popular UAF41 analog filter, and it provides several improvements.

The slew rate of the UAF42 has been increased to 10V/μs, versus 1.6V/μs for the UAF41. Frequency • Q product of the UAF42 has been improved, and the useful natural frequency extended by a factor of four to 100kHz. FET input op amps on the UAF42 provide very low input bias current. The monolithic construction of the UAF42 provides lower cost and improved reliability.

### DESIGN PROGRAM

Application report [SBFA002](#) (available for download at [www.ti.com](http://www.ti.com)) and a computer-aided design program also available from Texas Instruments, make it easy to design and implement many kinds of active filters. The DOS-compatible program guides you through the design process and automatically calculates component values.

Low-pass, high-pass, band-pass and band-reject (notch) filters can be designed. The program supports the three most commonly-used all-pole filter types: Butterworth, Chebyshev and Bessel. The less-familiar inverse Chebyshev is also supported, providing a smooth passband response with ripple in the stop band.

With each data entry, the program automatically calculates and displays filter performance. This feature allows a spreadsheet-like *what-if* design approach. For example, a user can quickly determine, by trial and error, how many poles are required for a desired attenuation in the stopband. Gain/phase plots may be viewed for any response type.

The basic building element of the most commonly-used filter types is the second-order section. This section provides a complex-conjugate pair of poles. The natural frequency,  $\omega_n$ , and Q of the pole pair determine the characteristic response of the section. The low-pass transfer function is shown in [Equation 1](#):

$$\frac{V_O(s)}{V_I(s)} = \frac{A_{LP}\omega_n^2}{s^2 + s\omega_n/Q + \omega_n^2} \quad (1)$$

The high-pass transfer function is given by [Equation 2](#):

$$\frac{V_{HP}(s)}{V_I(s)} = \frac{A_{HP}s^2}{s^2 + s\omega_n/Q + \omega_n^2} \quad (2)$$

The band-pass transfer function is calculated using [Equation 3](#):

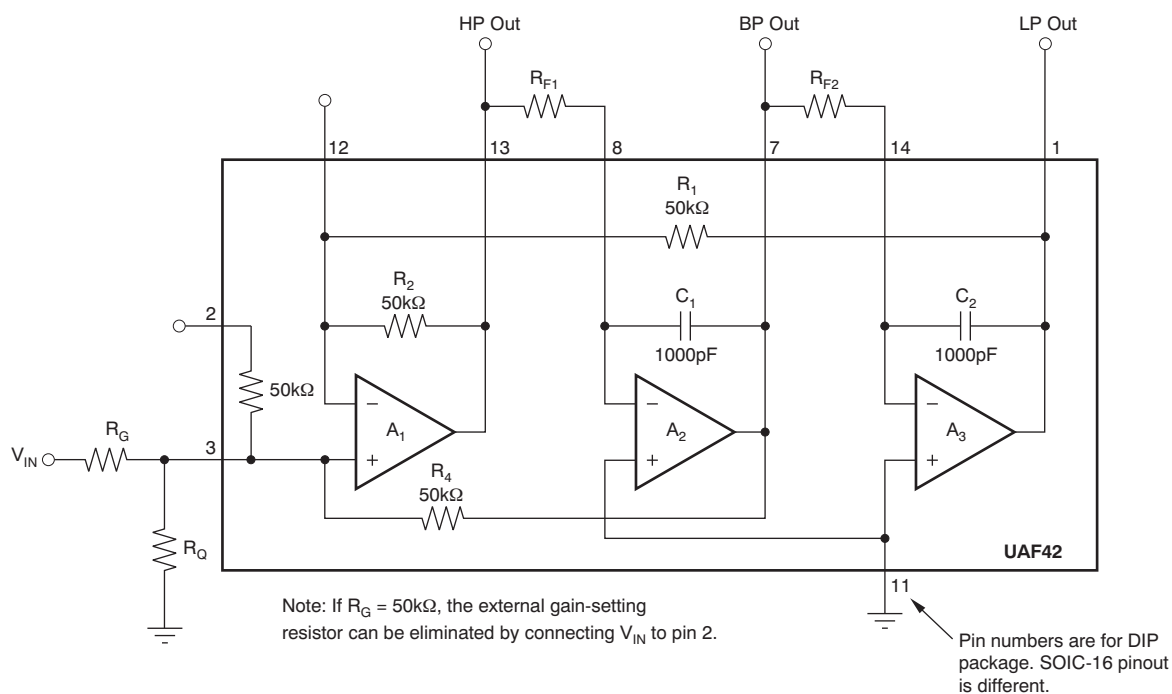
$$\frac{V_{BP}(s)}{V_I(s)} = \frac{A_{BP}(\omega_n/Q)s}{s^2 + s\omega_n/Q + \omega_n^2} \quad (3)$$

A band-reject response is obtained by summing the low-pass and high-pass outputs, yielding the transfer function shown in [Equation 4](#):

$$\frac{V_{BR}(s)}{V_I(s)} = \frac{A_{BR}(s^2 + \omega_n^2)}{s^2 + s\omega_n/Q + \omega_n^2} \quad (4)$$

The most common filter types are formed with one or more cascaded second-order sections. Each section is designed for  $\omega_n$  and Q according to the filter type (Butterworth, Bessel, Chebyshev, etc.) and cutoff frequency. While tabulated data can be found in virtually any filter design text, the design program eliminates this tedious procedure.

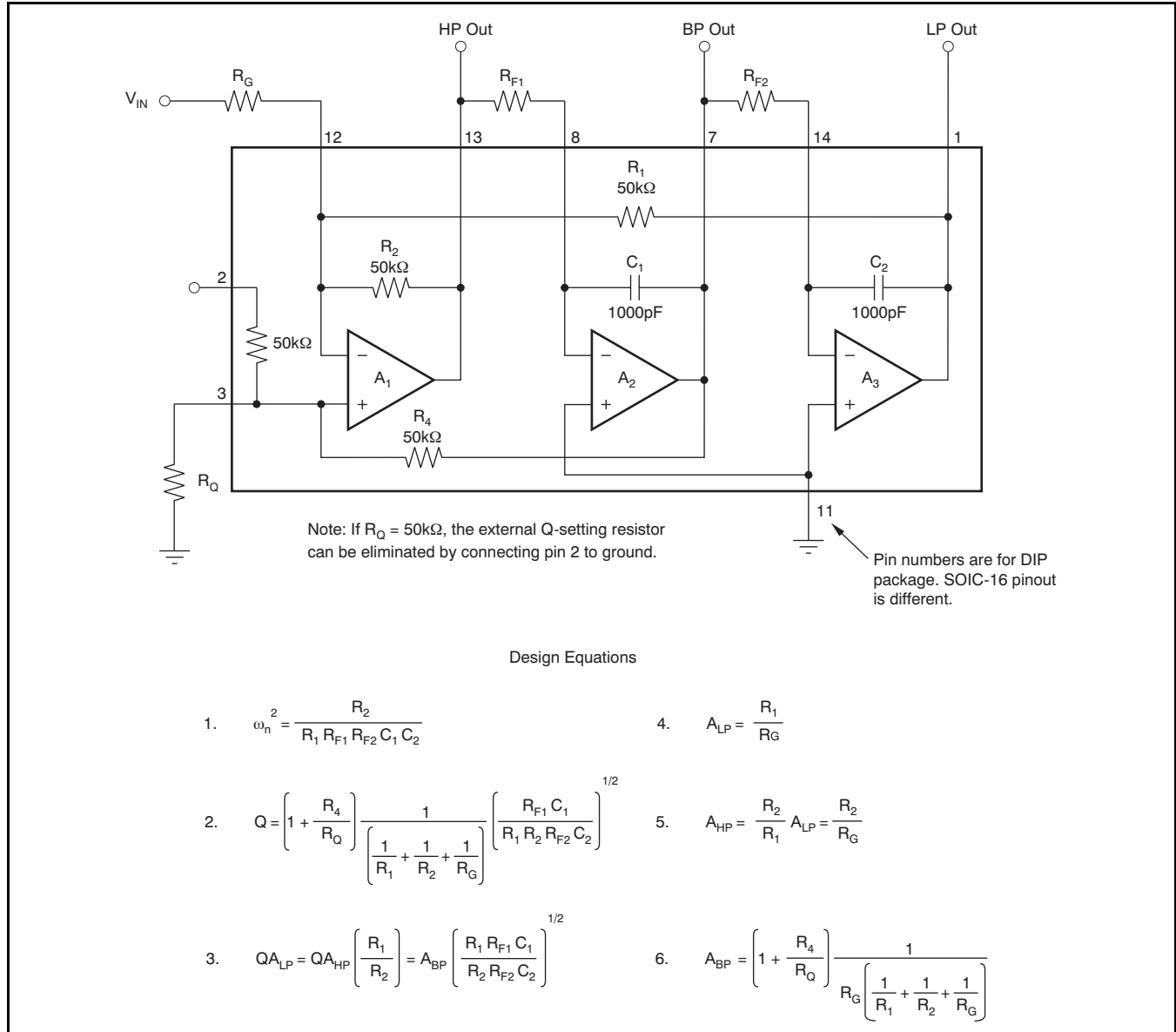
Second-order sections may be noninverting ([Figure 1](#)) or inverting ([Figure 2](#)). Design equations for these two basic configurations are shown for reference. The design program solves these equations, providing complete results, including component values.



## Design Equations

$$\begin{aligned}
 1. \quad \omega_n^2 &= \frac{R_2}{R_1 R_{F1} R_{F2} C_1 C_2} \\
 2. \quad Q &= \frac{1 + \frac{R_4 (R_G + R_Q)}{R_G R_Q}}{1 + \frac{R_2}{R_1}} \left( \frac{R_2 R_{F1} C_1}{R_1 R_{F2} C_2} \right)^{1/2} \\
 3. \quad QA_{LP} &= QA_{HP} \left( \frac{R_1}{R_2} \right) = A_{BP} \left( \frac{R_1 R_{F1} C_1}{R_2 R_{F2} C_2} \right)^{1/2} \\
 4. \quad A_{LP} &= \frac{1 + \frac{R_1}{R_2}}{R_G \left( \frac{1}{R_G} + \frac{1}{R_Q} + \frac{1}{R_4} \right)} \\
 5. \quad A_{HP} &= \frac{R_2}{R_1} A_{LP} = \frac{1 + \frac{R_2}{R_1}}{R_G \left( \frac{1}{R_G} + \frac{1}{R_Q} + \frac{1}{R_4} \right)} \\
 6. \quad A_{BP} &= \frac{R_4}{R_G}
 \end{aligned}$$

**Figure 1. Noninverting Pole-Pair**



**Figure 2. Inverting Pole-Pair**

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (November, 2007) to Revision B	Page
• Corrected package marking information shown in <i>Ordering Information</i> table .....	<a href="#">2</a>



## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UAF42AP	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		UAF42AP	<a href="#">Samples</a>
UAF42APG4	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		UAF42AP	<a href="#">Samples</a>
UAF42AU	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-25 to 85	UAF42AU	<a href="#">Samples</a>
UAF42AUE4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-25 to 85	UAF42AU	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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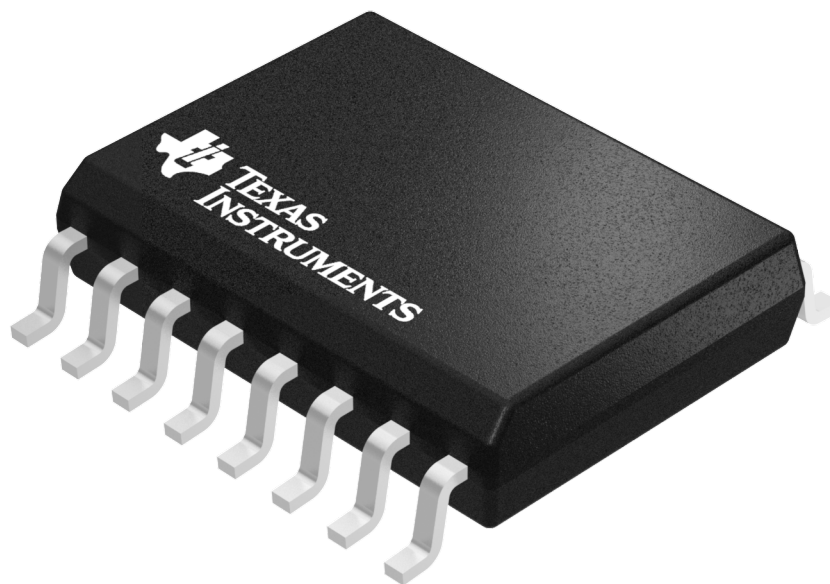
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**DW 16**

## GENERIC PACKAGE VIEW

**SOIC - 2.65 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4040000-2/H



DW0016A

# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



4220721/A 07/2016

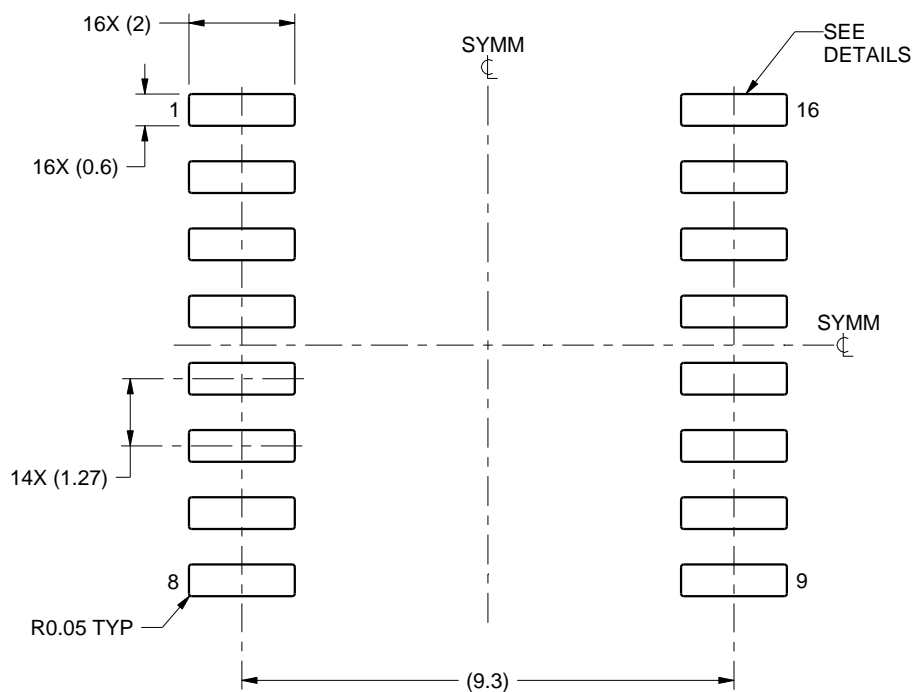
### NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

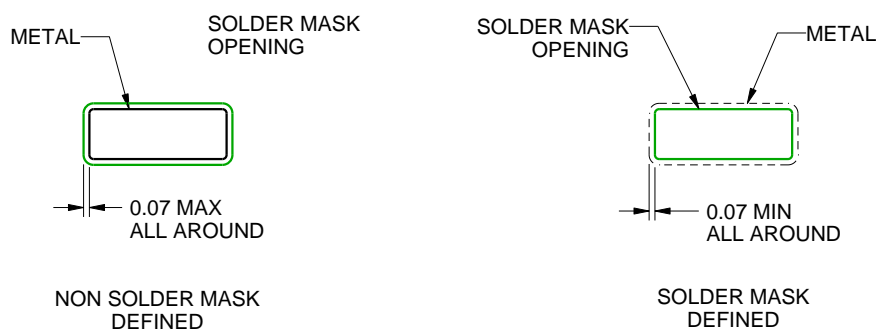
**DW0016A**

## SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:7X



## SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

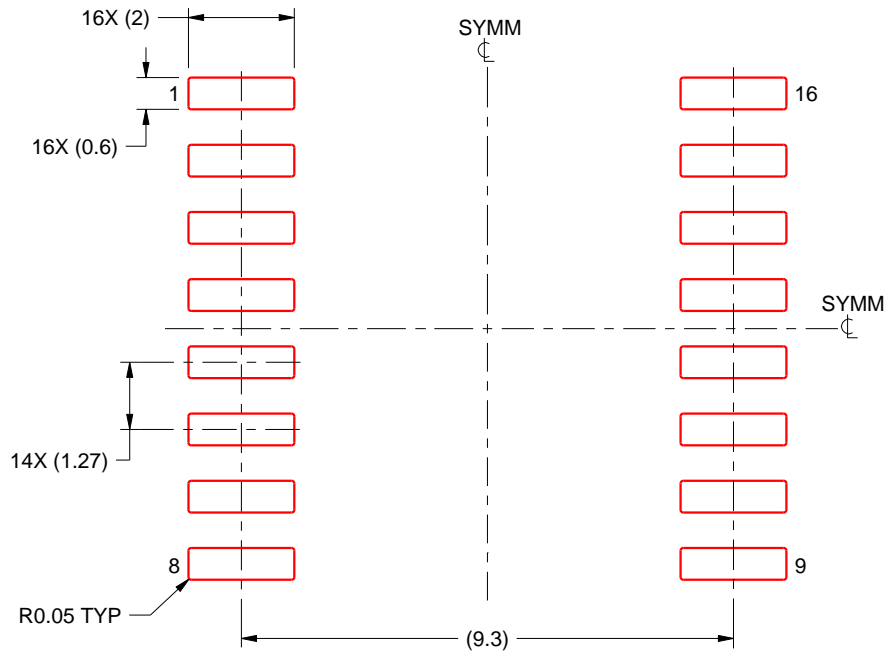
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0016A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  -  The 20 pin end lead shoulder width is a vendor option, either half or full width.

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