HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HA-4920/4925

High Speed Quad Comparator

2

FEATURES

- FAST RESPONSE TIME
- LOW OFFSET VOLTAGE
- STANDARD POWER SUPPLIES
- ACTIVE PULL-UP/PULL-DOWN OUTPUT CIRCUIT – NO EXTERNAL RESISTORS REQUIRED
- TTL AND ECL COMPATIBLE

APPLICATIONS

- A/D CONVERTERS
- THRESHOLD DETECTOR
- ZERO-CROSSING DETECTOR
- LOGIC SYSTEM INTERFACES
- HIGH FREQUENCY OSCILLATORS

DESCRIPTION

HA-4920/4925 are monolithic, quad, high speed comparators offering a combination of speed, precision, and flexibility never before available in a quad comparator. 40ns response time and 2.0mV offset voltage makes these comparators ideally suited for precise signal level detection and fast response times to large and small input signal levels. These dielectrically isolated devices employ unique input/output stages which prevent troublesome ground coupling inherent in combined analog/digital systems.

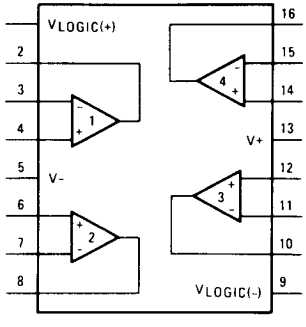
The flexibility/speed of HA-4920/4925 assures easy application in fast data acquisition systems, analog to logic interface networks, and test equipment.

Both devices are available in 16 pin dual-in-line ceramic packages. The HA-4920 operates from -55°C to +125°C and the HA-4925 operates over a 0°C to +75°C temperature range.

PINOUT

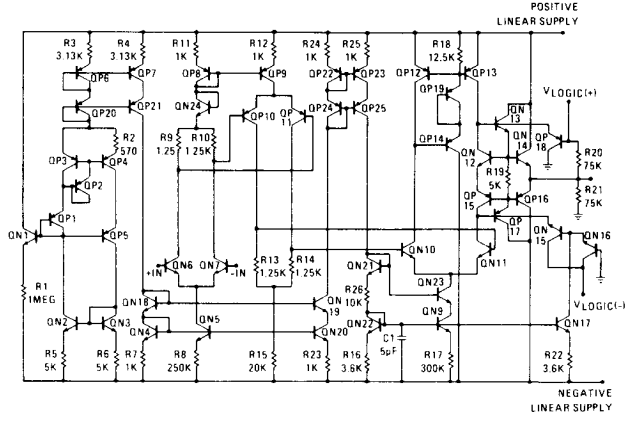
Package Code 4Z

QUAD COMPARATOR



TOP VIEW

SCHEMATIC



ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage between V+ and V-	40V
Voltage between $V_{Logic}(+)$ and $V_{Logic}(-)$	7V
Differential Input Voltage	±6V
Peak Ouput Current	50mA
Internal Power Dissipation (Note 2)	850mW
Storage Temperature Range	$-65^oC \leq T_A \leq 150^oC$
Positive and Negative Voltage Clamp	5V below Supply Voltage

ELECTRICAL CHARACTERISTICS

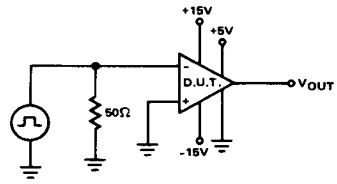
V+ = +15.0V $V_{Logic}(+)$ = 5.0V
V- = -15.0V $V_{Logic}(-)$ = GND

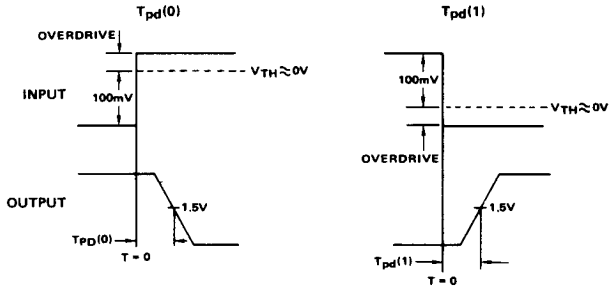
		HA-4920: -55°C/+125°C			HA-4925: 0°C/+75°C			
PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage (Note 3)	+25°C		2.0	3.0		4.0	6.0	mV
	Full			4.0			8.0	mV
Input Offset Current	+25°C		.5	1.5		1.5	2.0	µa
	Full			2.0			3.0	
Input Bias Current	+25°C		.8	6.0		2.0	8.0	µa
	Full			8.0			10.0	µa
Input Sensitivity (Note 4)	Full		.4	.6		.7	.8	mV
Common Mode Range (CMR)	Full	±10			±10			V
Large Signal Voltage Gain	+25°C		25K			25K		V/V
Response Time Tpd0 (Note 5)	+25°C		35	50		35	50	ns
Response Time Tpd1 (Note 5)	+25°C		30	50		30	50	ns
Output Voltage Level (Note 6) V_{OL}	Full		.15	.4		.15	.4	V
Output Voltage Level (Note 6) V_{OH}	Full	3.5	4.2		3.5	4.2		V
Output Current I_{Sink} (Note 7)	Full	3.2			3.2			mA
Output Current I_{Source} (Note 7)	Full	3.2			3.2			mA
Power Supply Current I_{CC+}	+25°C		14	20		14	20	mA
Power Supply Current I_{CC-}	+25°C		10	20		10	20	mA
Power Supply Current I_{Logic+}	+25°C		4.8	8.0		4.8	8.0	mA

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. Derate by 5.8 mW/°C above +75°C.
3. Minimum differential input voltage required to ensure a defined output state.
4. $R_S \leq 200$ ohms; $V_{in} \leq$ Common Mode Range. Input sensitivity is the worst case minimum differential input voltage required to guarantee a given output logic state, after offset voltage is nulled. This parameter includes the effects of offset current, common mode rejection, and voltage gain.
5. For $T_{pd}(1)$; 100mV input step, -5mV overdrive. For $T_{pd}(0)$; -100mV input step, +5mV overdrive. Frequency ≈ 100Hz; Duty Cycle ≈ 50%; Inverting input driven. See Test Circuit below.
6. For V_{OH} and V_{OL}: I_{Sink} = 3.5mA, I_{Source} = 3.0mA. For other values of V_{Logic}; V_{OH} (min.) = V_{Logic} + -1.5V.
7. Per Comparator.

RESPONSE TIME TEST CIRCUITS



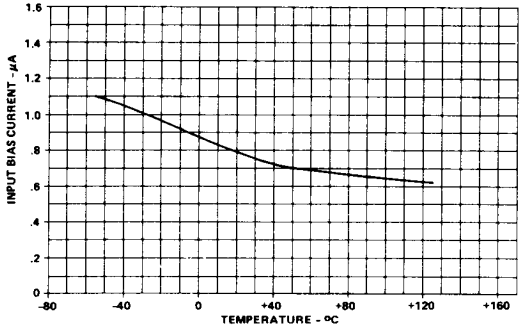


Input and output voltage waveforms for various input overdrives are shown on the following page.

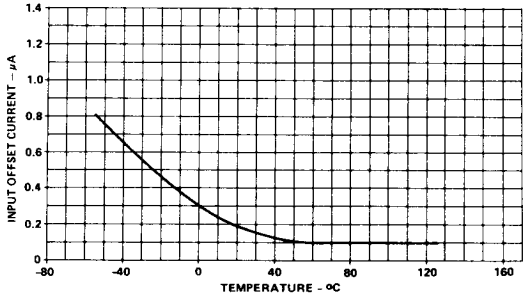
PERFORMANCE CURVES

V+ = 15V, V- = -15V, $V_{Logic}(+)$ = 5.0V, $V_{Logic}(-)$ = 0V, T_A = +25°C, Unless Otherwise Stated.

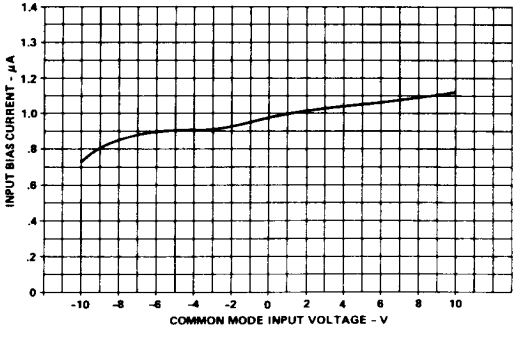
INPUT BIAS CURRENT VS. TEMPERATURE



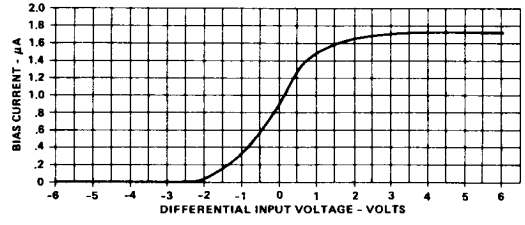
INPUT OFFSET CURRENT VS. TEMPERATURE



INPUT BIAS CURRENT VS. COMMON MODE VOLTAGE

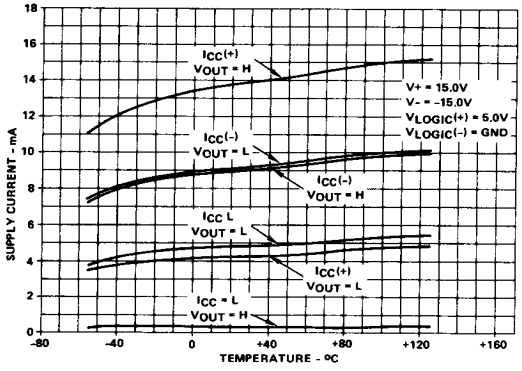


INPUT BIAS CURRENT VS. DIFFERENTIAL INPUT VOLTAGE

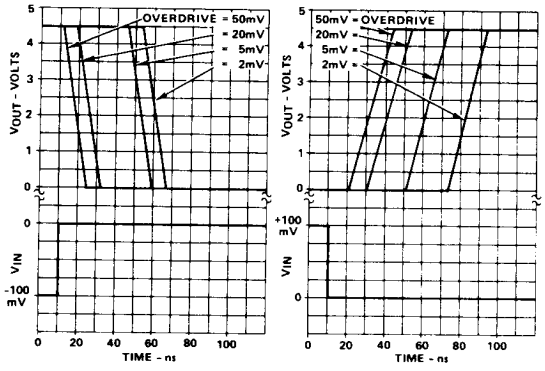


PERFORMANCE CURVES (cont'd)

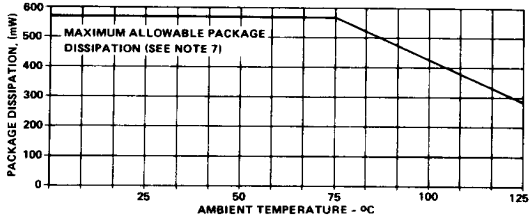
SUPPLY CURRENT VS. TEMPERATURE FOR ±15V SUPPLIES AND +5V LOGIC SUPPLY



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



MAXIMUM PACKAGE DISSIPATION VS. $T_{AMBIENT}$



APPLYING THE HA-4920/25

1. SUPPLY CONNECTIONS: This device is exceptionally versatile in working with most available power supplies. The voltage applied to the V+ and V- terminals determines the allowable input signal range; while the voltage applied to the V_L+ and V_L- determines the output swing. In systems where dual analog supplies are available, these would be connected to V+ and V-, while the logic supply and return would be connected to V_{Logic}+ and V_{Logic}-. The analog and logic supply commons can be connected together at one point in the system, since the comparator is immune to noise on the logic supply ground. A negative output swing may be obtained by connecting V_L+ to ground and V_L- to a negative supply. Bipolar output swings (5V P-P, max.) may be obtained using dual supplies. Applied input signals should not exceed V_{Supply} and the maximum differential input voltage values.

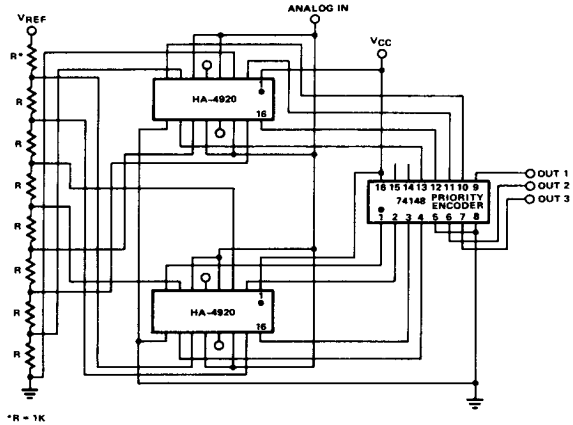
2. UNUSED INPUTS: Inputs of unused comparator sections should be tied to a differential voltage source to prevent output "chatter". Differential voltage values should exceed the offset voltage plus input sensitivity voltage values for a particular device.

3. CROSSTALK: Simultaneous high frequency operation of all other channels in the package will not affect the output logic state of a given channel, provided that its differential input voltage is sufficient to define a given logic state ($\Delta V_{IN} \geq \pm V_{OS}$). Low level or high impedance input lines should be shielded from other signal sources to reduce crosstalk and interference.

4. POWER SUPPLY DECOUPLING: Decouple all power supply lines with .01 μF ceramic capacitors to a ground line located near the package to reduce coupling between channels or from external sources.

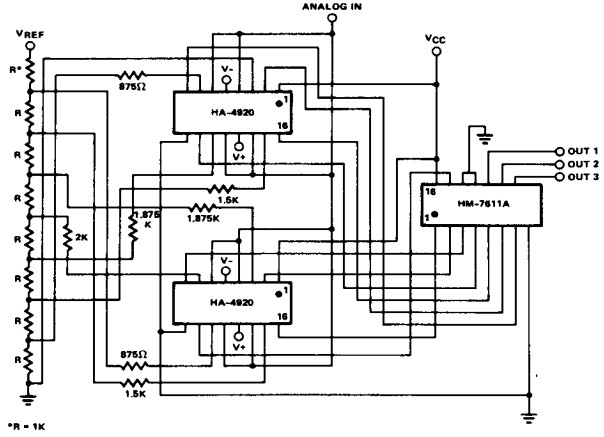
5. R.F.I.: High speed comparators may generate high frequency oscillations when the applied differential input voltage is less that the offset voltage plus input sensitivity value. This can be minimized by adding positive feedback hysteresis networks (see Harris App. Note 505). Alternately, ferrite beads surrounding the input and output lines will help reduce RF interference to other circuitry.

3 BIT PARALLEL COMPARATOR A/D CONVERTER USING TTL LOGIC

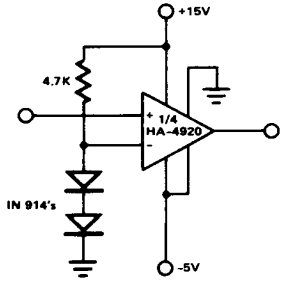


*R = 1K
Input Balancing Resistors Optional
(See Next Figure)
Experimental Results ≈ 50ns

3 BIT PARALLEL COMPARATOR A/D CONVERTER USING 256 x 4 PROM



LOGIC LEVEL TRANSLATOR TTL TO ECL



TRUTH TABLE FOR 3 BIT PARALLEL COMPARATOR A/D CONVERTER

ENCODER/PROM INPUTS							OUTPUTS		
1	2	3	4	5	6	7	0	1	2
0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	1	1	0
1	1	1	1	0	0	0	0	0	1
1	1	1	1	1	0	0	1	0	1
1	1	1	1	1	1	0	0	1	1
1	1	1	1	1	1	1	1	1	1