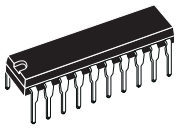
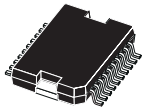
L6205

DMOS DUAL FULL BRIDGE DRIVER

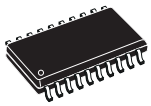
- OPERATING SUPPLY VOLTAGE FROM 8 TO 52V
- 5.6A OUTPUT PEAK CURRENT (2.8A DC)
- $R_{DS(ON)}$ 0.3Ω TYP. VALUE @ T_j = 25 °C
- OPERATING FREQUENCY UP TO 100KHz
- NON DISSIPATIVE OVERCURRENT PROTECTION
- PARALLELED OPERATION
- CROSS CONDUCTION PROTECTION
- THERMAL SHUTDOWN
- UNDER VOLTAGE LOCKOUT
- INTEGRATED FAST FREE WHEELING DIODES



PowerDIP20 (16+2+2)



PowerSO20



SO20 (16+2+2)

ORDERING NUMBERS:
L6205N (PowerDIP20)
L6205PD (PowerSO20)
L6205D (SO20)

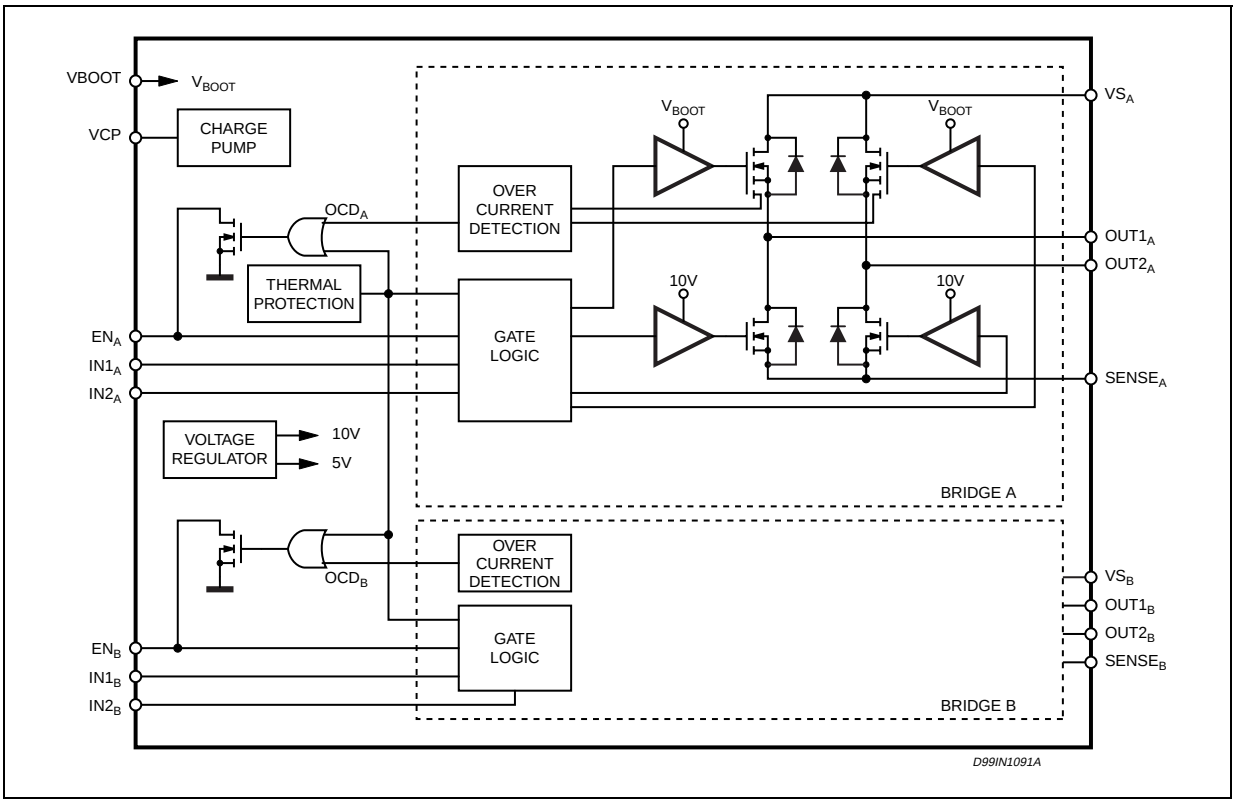
TYPICAL APPLICATIONS

- BIPOLAR STEPPER MOTOR
- DUAL OR QUAD DC MOTOR

DESCRIPTION

The L6205 is a DMOS Dual Full Bridge designed for motor control applications, realized in MultiPower-BCD technology, which combines isolated DMOS Power Transistors with CMOS and bipolar circuits on the same chip. Available in PowerDIP20 (16+2+2), PowerSO20 and SO20(16+2+2) packages, the L6205 features a non-dissipative protection of the high side PowerMOSFETs and thermal shutdown.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Test conditions	Value	Unit
V_S	Supply Voltage		60	V
V_{IN},V_{EN}	Input and Enable Voltage Range		-0.3 to +7	V
V_{SENSE}	DC Sensing Voltage Range		-1 to +4	V
V_{BOOT}	Bootstrap Peak Voltage		V_S + 10	V
$I_{S(peak)}$	Pulsed Supply Current (for each VS pin), internally limited by the overcurrent protection	t_{PULSE} < 1ms	7.1	A
I_S	DC Supply Current (for each VS pin)		2.8	A
V_{OD}	Differential Voltage Between VS_A, $OUT1_A$, $OUT2_A$, $SENSE_A$ and VS_B, $OUT1_B$, $OUT2_B$, $SENSE_B$	$VS_A = VS_B$ = 60V $SENSE_A = SENSE_B$ = GND	60	V
T_{stg}, T_{OP}	Storage and Operating Temperature Range		-40 to 150	°C

RECOMMENDED OPERATING CONDITIONS

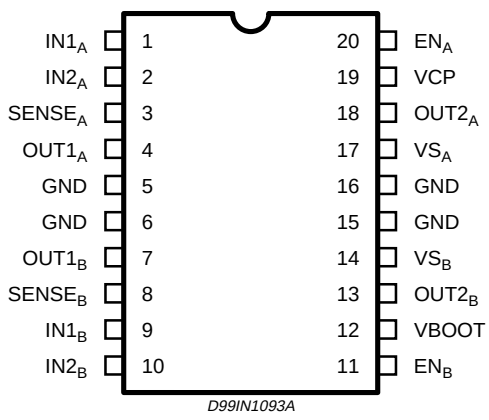
Symbol	Parameter	MIN	MAX	Unit
V_S	Supply Voltage	12	52	V
V_{OD}	Differential Voltage Between VS_A, $OUT1_A$, $OUT2_A$, $SENSE_A$ and VS_B, $OUT1_B$, $OUT2_B$, $SENSE_B$		52	V
V_{SENSE}	Sensing voltage (pulsed tw<t_{rr}) (DC)	 -6 -1	 6 1	 V V
I_{OUT}	DC Output Current		2.8	A
T_j	Operating Junction Temperature	-25	+125	°C
F_{sw}	Commutation Frequency		100	kHz

THERMAL DATA

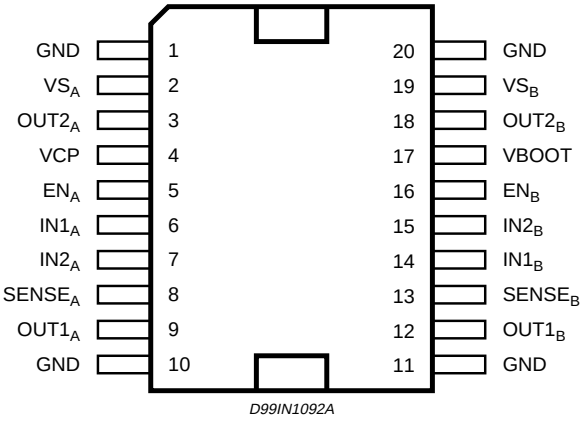
Symbol	Description	PowerDIP20	SO20	PowerSO20	Unit
$R_{th\text{-}j\text{-}pins}$	MaximumThermal Resistance Junction-Pins	12	14	-	°C/W
$R_{th\text{-}j\text{-}case}$	Maximum Thermal Resistance Junction-Case	-	-	1	°C/W
$R_{th\text{-}j\text{-}amb1}$	MaximumThermal Resistance Junction-Ambient [1]	40	51	-	°C/W
$R_{th\text{-}j\text{-}amb1}$	Maximum Thermal Resistance Junction-Ambient [2]	-	-	35	°C/W
$R_{th\text{-}j\text{-}amb1}$	MaximumThermal Resistance Junction-Ambient [3]	-	-	15	°C/W
$R_{th\text{-}j\text{-}amb2}$	Maximum Thermal Resistance Junction-Ambient [4]	56	77	62	°C/W

<1> Mounted on a multilayer FR4 PCB with a dissipating copper surface on the bottom side of 6 cm^2 (with a thickness of 35 µm).
<2> Mounted on a multilayer FR4 PCB with a dissipating copper surface on the top side of 6 cm^2 (with a thickness of 35 µm).
<3> Mounted on a multilayer FR4 PCB with a dissipating copper surface on the top side of 6 cm^2 (with a thickness of 35 µm), 16 via holes and a ground layer.
<4> Mounted on a multilayer FR4 PCB without any heat sinking surface on the board.

PIN CONNECTIONS (Top View)



PowerDIP20/SO20



PowerSO20

PIN DESCRIPTION

PACKAGE		Name	Type	Function
SO20/ PowerDIP20	PowerSO20			
PIN #	PIN #			
1	6	$IN1_A$	Logic Input	Bridge A Logic Input 1.
2	7	$IN2_A$	Logic Input	Bridge A Logic Input 2.
3	8	$SENSE_A$	Power Supply	Bridge A Source Pin. This pin must be connected to Power Ground directly or through a sensing power resistor.
4	9	$OUT1_A$	Power Output	Bridge A Output 1.
5, 6, 15, 16	1, 10, 11, 20	GND	GND	Signal Ground terminals. In PowerDIP and SO packages, these pins are also used for heat dissipation toward the PCB.
7	12	$OUT1_B$	Power Output	Bridge B Output 1.
8	13	$SENSE_B$	Power Supply	Bridge B Source Pin. This pin must be connected to Power Ground directly or through a sensing power resistor.
9	14	$IN1_B$	Logic Input	Bridge B Logic Input 1.
10	15	$IN2_B$	Logic Input	Bridge B Logic Input 2.
11	16	EN_B	Logic Input (*)	Bridge B Enable. LOW logic level switches OFF all Power MOSFETs of Bridge B. This pin is also connected to the collector of the Overcurrent and Thermal Protection transistor to implement over current protection. If not used, it has to be connected to +5V through a resistor.
12	17	VBOOT	Supply Voltage	Bootstrap Voltage needed for driving the upper PowerMOSFETs of both Bridge A and Bridge B.
13	18	$OUT2_B$	Power Output	Bridge B Output 2.
14	19	VS_B	Power Supply	Bridge B Power Supply Voltage. It must be connected to the supply voltage together with pin VS_A.
17	2	VS_A	Power Supply	Bridge A Power Supply Voltage. It must be connected to the supply voltage together with pin VS_B.
18	3	$OUT2_A$	Power Output	Bridge A Output 2.
19	4	VCP	Output	Charge Pump Oscillator Output.
20	5	EN_A	Logic Input (*)	Bridge A Enable. LOW logic level switches OFF all Power MOSFETs of Bridge A. This pin is also connected to the collector of the Overcurrent and Thermal Protection transistor to implement over current protection. If not used, it has to be connected to +5V through a resistor.

(*) Also connected at the output drain of the Overcurrent and Thermal protection MOSFET. Therefore, it has to be driven putting in series a resistor with a value in the range of 500Ω - 22KΩ, recommended 10kΩ

ELECTRICAL CHARACTERISTICS

(T_{amb} = 25 °C, V_S = 48V, unless otherwise specified)

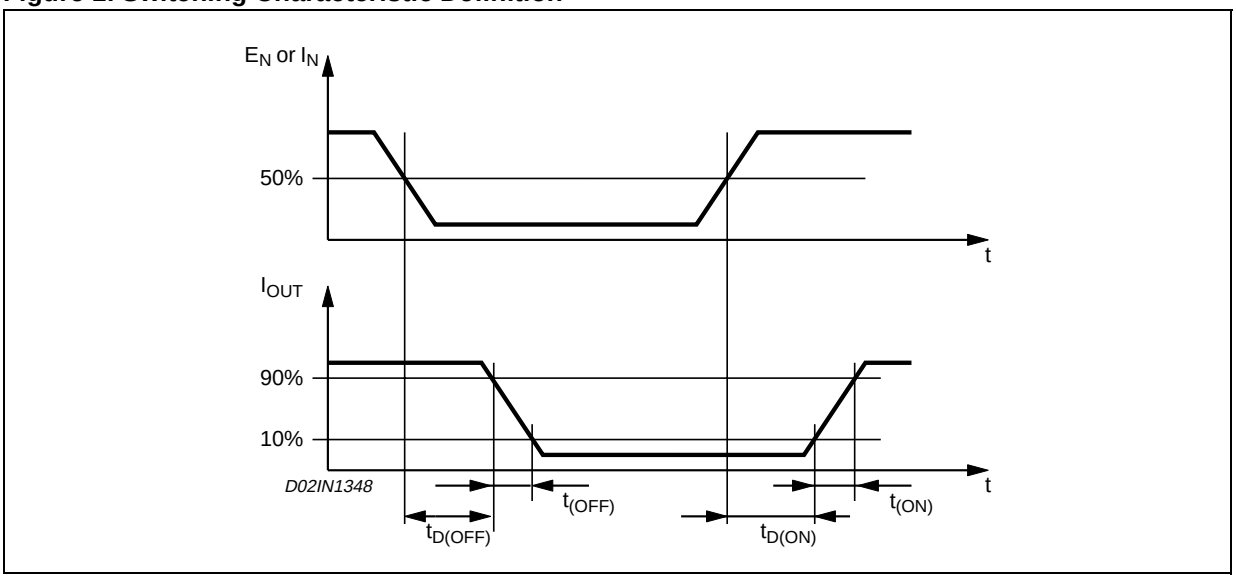
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_S	Supply Voltage		8		52	V
I_S	Quiescent Supply Current	All Bridges OFF; -25°C<T_j <125°C		5.5	10	mA
T_j	Thermal Shutdown Temperature		150			°C
Output DMOS Transistors						
I_{DSS}	Leakage Current	V_S = 52V		10		µA
$R_{DS(ON)}$	High-side Switch ON Resistance	T_j = 25 °C		0.34	0.4	Ω
		T_j =125 °C		0.53	0.59	Ω
	Low-side Switch ON Resistance	T_j = 25 °C		0.28	0.34	Ω
		T_j =125 °C		0.47	0.53	Ω
Source Drain Diodes						
V_{SD}	Forward ON Voltage	I_{SD} = 2.8A, EN = LOW		1.2	1.4	V
t_{rr}	Reverse Recovery Time	I_f = 2.8A		300		ns
t_{fr}	Forward Recovery Time			200		ns
Switching Characteristics						
$t_{D(on)EN}$	Enable to out turn ON delay time (5)	I_{LOAD} =2.8A, Resistive Load		250		ns
$t_{D(on)IN}$	Input to out turn ON delay time (5)	I_{LOAD} =2.8A, Resistive Load		600		ns
t_{ON}	Output rise time(5)	I_{LOAD} =2.8A, Resistive Load	20	105	300	ns
$t_{D(off)EN}$	Enable to out turn OFF delay time (5)	I_{LOAD} =2.8A, Resistive Load		450		ns
$t_{D(off)IN}$	Input to out turn OFF delay time (5)	I_{LOAD} =2.8A, Resistive Load		500		ns
t_{OFF}	Output Fall Time (5)	I_{LOAD} =2.8A, Resistive Load	20	78	300	ns
t_{dt}	Dead Time Protection			1		µs
f_{CP}	Charge pump frequency	-25°C<T_j <125°C		0.75	1	MHz
UVLO comp						
$V_{th(ON)}$	Turn ON threshold		6.6	7	7.4	V
$V_{th(OFF)}$	Turn OFF threshold		5.6	6	6.4	V
Logic Input						
V_{INL}	Low level logic input voltage		-0.3		0.8	V
V_{INH}	High level logic input voltage		2		7	V
I_{INH}	High level logic input current	5 V Logic Input Voltage			70	µA

ELECTRICAL CHARACTERISTICS (continued)
(T_{amb} = 25 °C, V_S = 48V, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{INL}	Low level logic input current	GND Logic Input Voltage			-10	µA
Over Current Protection						
$I_{S\ OVER}$	Input Supply Over Current Protection Threshold	-25°C<T_j <125°C	4	5.6	7.1	A
R_{OPDR}	Open Drain ON Resistance	I = 4mA		60		Ω

<(5)> See Fig. 1.

Figure 1. Switching Characteristic Definition



CIRCUIT DESCRIPTION

POWER STAGES and CHARGE PUMP

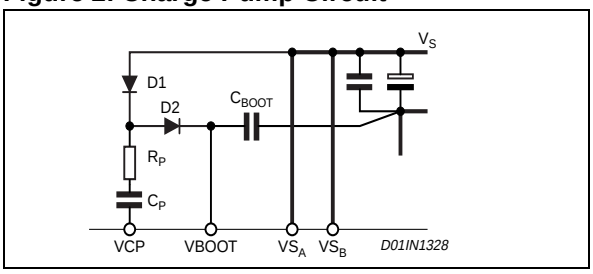
The L6205 integrates two independent Power MOS Full Bridges. Each Power MOS has an Rdson=0.3ohm (typical value @25°C), with intrinsic fast freewheeling diode. Cross conduction protection is achieved using a dead time (td = 1µs typical) between the switch off and switch on of two Power MOS in one leg of a bridge.

Using N Channel Power MOS for the upper transistors in the bridge requires a gate drive voltage above the power supply voltage. The Bootstrapped (Vboot) supply is obtained through an internal Oscillator and few external components to realize a charge pump circuit as shown in Figure 2. The oscillator output (VCP) is a square wave at 750kHz (typical) with 10V amplitude. Recommended values/part numbers for the charge pump circuit are shown in Table1.

Table 1. Charge Pump External Components Values

C_{BOOT}	220nF
C_P	10nF
R_P	100Ω
D1	1N4148
D2	1N4148

Figure 2. Charge Pump Circuit



LOGIC INPUTS

Pins $IN1_A$, $IN2_A$, $IN1_B$ and $IN2_B$ are TTL/CMOS and µC compatible logic inputs. The internal structure is shown in Fig. 3. Typical value for turn-on and turn-off thresholds are respectively Vthon=1.8V and Vthoff=1.3V.

Pins EN_A and EN_B have identical input structure with the exception that the drains of the Overcurrent and thermal protection MOSFETs (one for the Bridge A and one for the Bridge B) are also connected to these pins. Due to these connections some care needs to be taken in driving these pins. The EN_A and EN_B inputs may be driven in one of two configurations as shown in figures 4 or 5. If driven by an open drain (collector) structure, a pull-up resistor R_{EN} and a capacitor C_{EN} are connected as shown in Fig. 4. If the driver is a standard Push-Pull structure the resistor R_{EN} and the capacitor C_{EN} are connected as shown in Fig. 5. The resistor R_{EN} should be chosen in the range from 500Ω to 22KΩ. Recommended values for R_{EN} and C_{EN} are respectively 10KΩ and 100nF. More information on selecting the values is found in the Overcurrent Protection section.

Figure 3. Logic Inputs Internal Structure

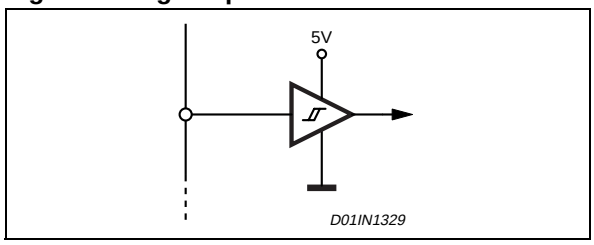


Figure 4. EN_A and EN_B Pins Open Collector Driving

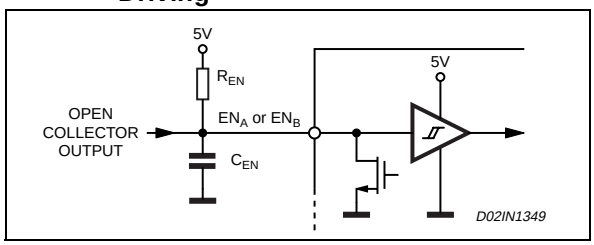
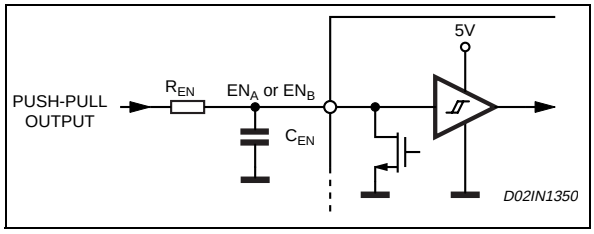


Figure 5. EN_A and EN_B Pins Push-Pull Driving



TRUTH TABLE

INPUTS			OUTPUTS	
EN	**IN1**	**IN2**	**OUT1**	**OUT2**
L	X	X	High Z	High Z
H	L	L	GND	GND
H	H	L	Vs	GND
H	L	H	GND	Vs
H	H	H	Vs	Vs

X = Don't care

High Z = High Impedance Output

NON-DISSIPATIVE OVERCURRENT PROTECTION

In addition to the PWM current control, an overcurrent detection circuit (OCD) is integrated for full protection. This circuit provides protection against a short circuit to ground or between two phases of the bridge. With this internal over current detection, the external current sense resistor normally used and its associated power dissipation are eliminated. Figure 6 shows a simplified schematic of the overcurrent detection circuit for the Bridge A. Bridge B is provided of an analogous circuit.

To implement the over current detection, a sensing element that delivers a small but precise fraction of the output current is implemented with each high side power MOS. Since this current is a small fraction of the output current there is very little additional power dissipation. This current is compared with an internal reference current I_{REF}. When the output current reaches the detection threshold (typically 5.6A) the OCD comparator signals a fault condition. When a fault condition is detected, the EN pin is pulled below the turn off threshold (1.3V typical) by an internal open drain MOS with a pull down capability of 4mA. By using an external R-C on the EN pin, the off time before recovering normal operation can be easily programmed by means of the accurate thresholds of the logic inputs. Figure 7 shows the OCD operation.

Figure 6. Overcurrent Protection Simplified Schematic

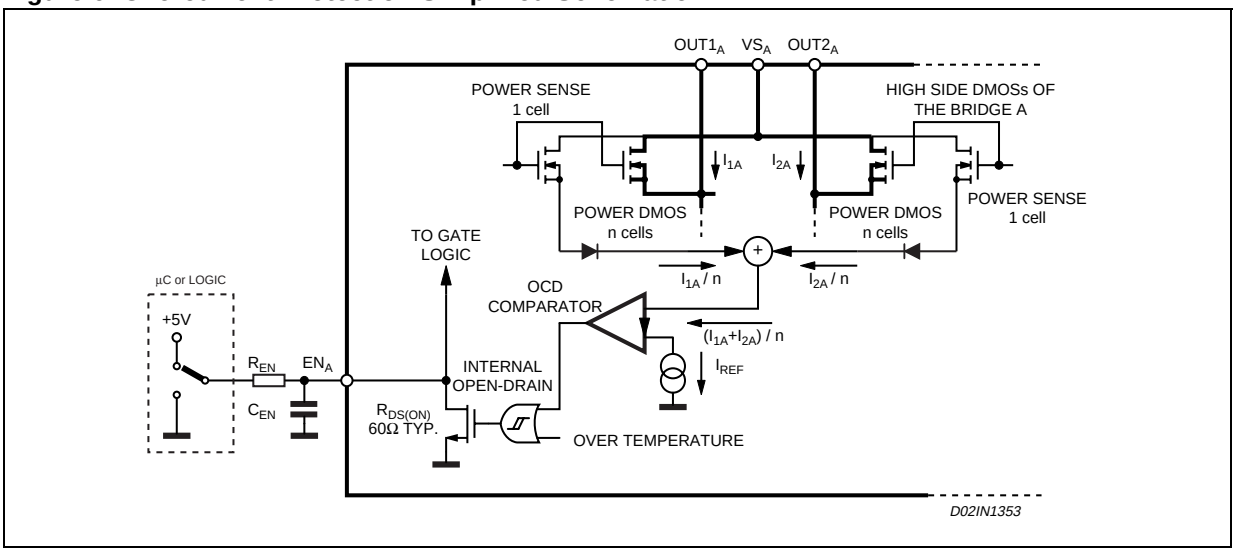
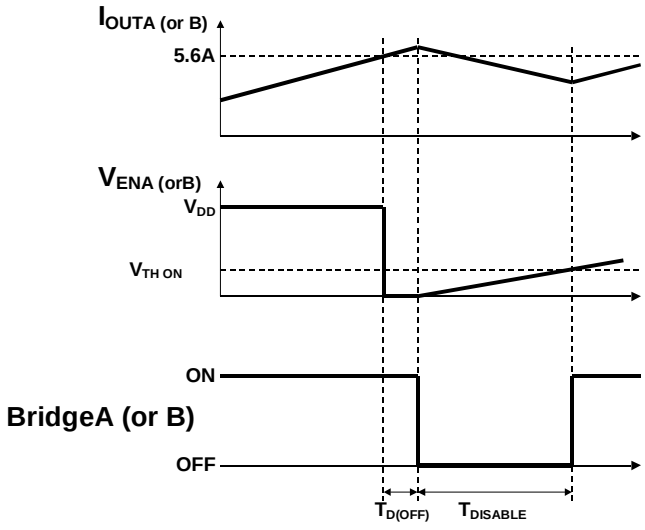


Figure 7. Overcurrent Protection Waveforms



APPLICATION INFORMATION

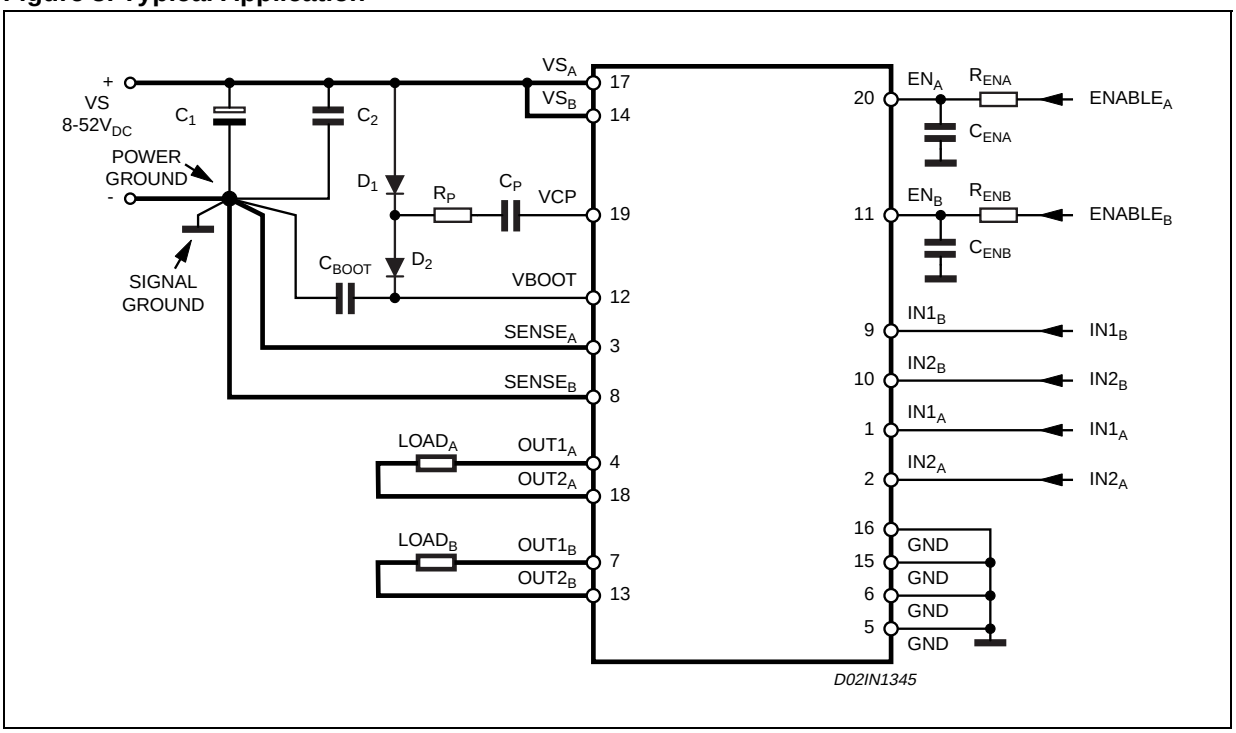
A typical application using L6205 is shown in Fig. 8. Typical component values for the application are shown in Table 2. A high quality ceramic capacitor in the range of 100 to 200 nF should be placed between the power pins (VS_A and VS_B) and ground near the L6205 to improve the high frequency filtering on the power supply and reduce high frequency transients generated by the switching. The capacitors connected from the EN_A and EN_B inputs to ground set the shut down time for the Brgidge A and Bridge B respectively when an over current is detected (see Overcurrent Protection). The two current sources ($SENSE_A$ and $SENSE_B$) should be connected to Power Ground with a trace length as short as possible in the layout. To increase noise immunity, unused logic pins (except EN_A and EN_B) are best connected to 5V (High Logic Level) or GND (Low Logic Level) (see pin description). It is recommended to keep Power Ground, Signal Ground and Charge Pump Ground (low side of C_{BOOT} capacitor) separated on PCB.

Table 2. Component Values for Typical Application

C_1	100uF
C_2	100nF
C_{BOOT}	220nF
C_P	10nF
C_{ENA}	100nF
C_{ENB}	100nF

D_1	1N4148
D_2	1N4148
R_{ENA}	2K2Ω
R_{ENB}	2K2Ω
R_P	100Ω

Figure 8. Typical Application



PARALLELED OPERATION

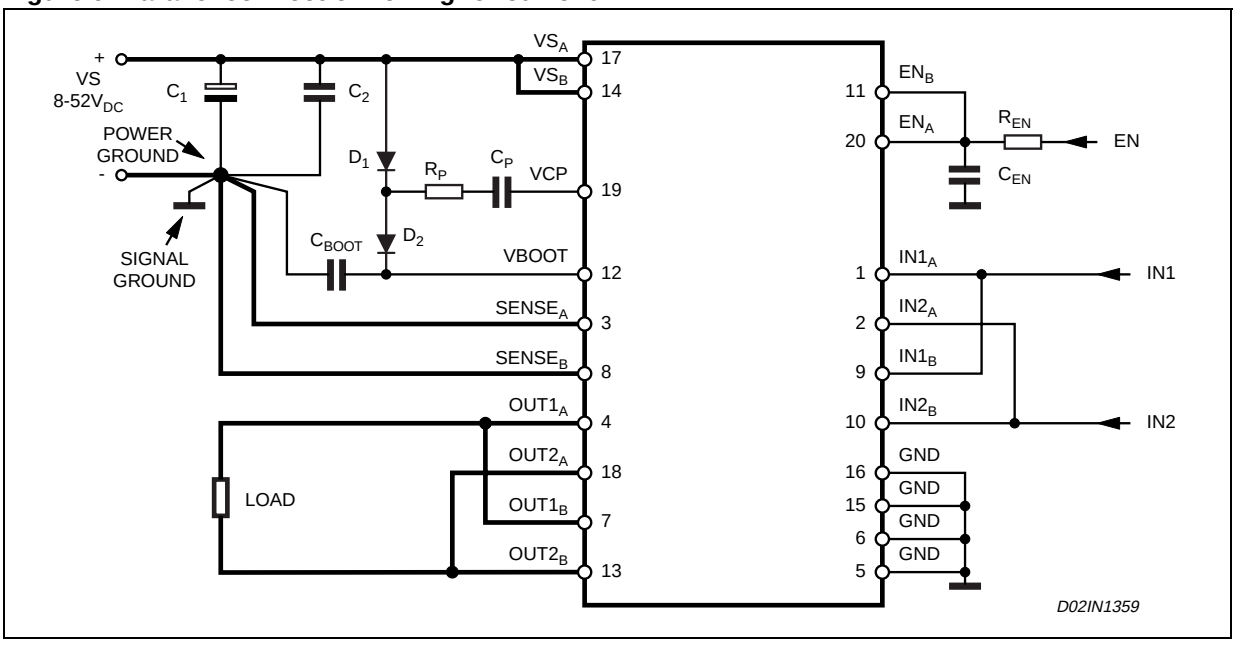
The outputs of the L6205 can be paralleled to increase the output current capability or reduce the power dissipation in the device at a given current level. It must be noted, however, that the internal wire bond connections from the die to the power or sense pins of the package must carry current in both of the associated half bridges. When the two halves of one full bridge (for example $OUT1_A$ and $OUT2_A$) are connected in parallel, the peak current rating is not increased since the total current must still flow through one bond wire on the power supply or sense pin. In addition, the over current detection senses the sum of the current in the upper devices of each bridge (A or B) so connecting the two halves of one bridge in parallel does not increase the over current detection threshold.

For most applications the recommended configuration is Half Bridge 1 of Bridge A paralleled with the Half Bridge 1 of the Bridge B, and the same for the Half Bridges 2 as shown in Figure 9. The current in the two devices connected in parallel will share very well since the $R_{DS(ON)}$ of the devices on the same die is well matched.

In this configuration the resulting Bridge has the following characteristics.

- Equivalent Device: FULL BRIDGE
- $R_{DS(ON)}$ 0.15Ω Typ. Value @ T_J = 25°C
- 5.6A max RMS Load Current
- 11.2A OCD Threshold

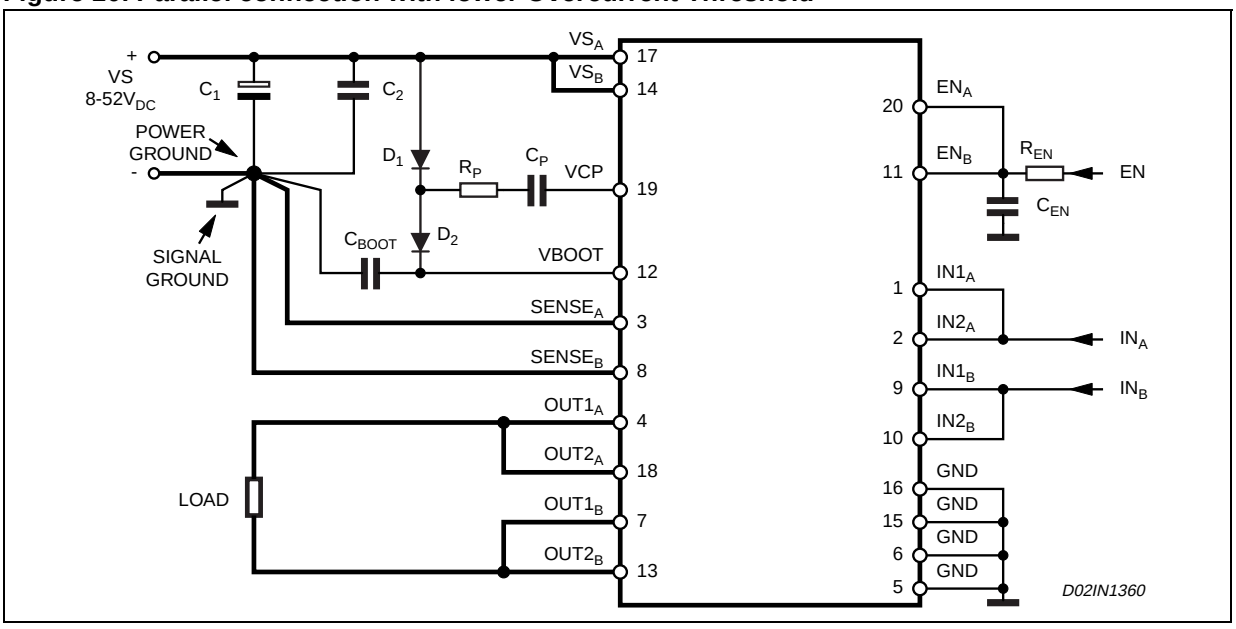
Figure 9. Parallel connection for higher current



To operate the device in parallel and maintain a lower over current threshold, Half Bridge 1 and the Half Bridge 2 of the Bridge A can be connected in parallel and the same done for the Bridge B as shown in Figure 10. In this configuration, the peak current for each half bridge is still limited by the bond wires for the supply and sense pins so the dissipation in the device will be reduced, but the peak current rating is not increased. This configuration, the resulting bridge has the following characteristics.

- Equivalent Device: FULL BRIDGE
- $R_{DS(ON)}$ 0.15Ω Typ. Value @ T_J = 25°C
- 2.8A max RMS Load Current
- 5.6A OCD Threshold

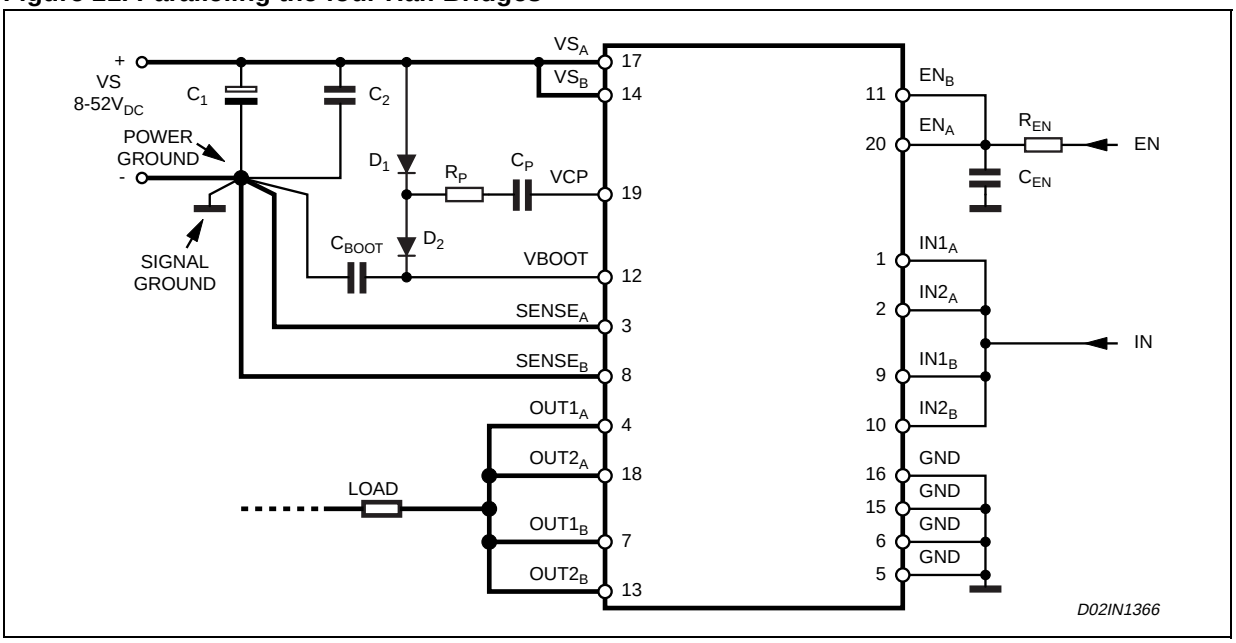
Figure 10. Parallel connection with lower Overcurrent Threshold



It is also possible to parallel the four Half Bridges to obtain a simple Half Bridge as shown in Fig. 11 The resulting half bridge has the following characteristics.

- Equivalent Device: HALF BRIDGE
- $R_{DS(ON)}$ 0.075Ω Typ. Value @ T_J = 25°C
- 5.6A max RMS Load Current
- 11.2A OCD Threshold

Figure 11. Paralleling the four Half Bridges



OUTPUT CURRENT CAPABILITY AND IC POWER DISSIPATION

In Fig. 12 and Fig. 13 are shown the approximate relation between the output current and the IC power dissipation using PWM current control driving two loads, for two different driving types:

– One Full Bridge ON at a time (Fig. 12) in which only one load at a time is energized.

– Two Full Bridges ON at the same time (Fig. 13) in which two loads at the same time are energized.

For a given output current and driving type the power dissipated by the IC can be easily evaluated, in order to establish which package should be used and how large must be the on-board copper dissipating area to guarantee a safe operating junction temperature (125°C maximum).

Figure 12. IC Power Dissipation versus Output Current with One Full Bridge ON at a time.

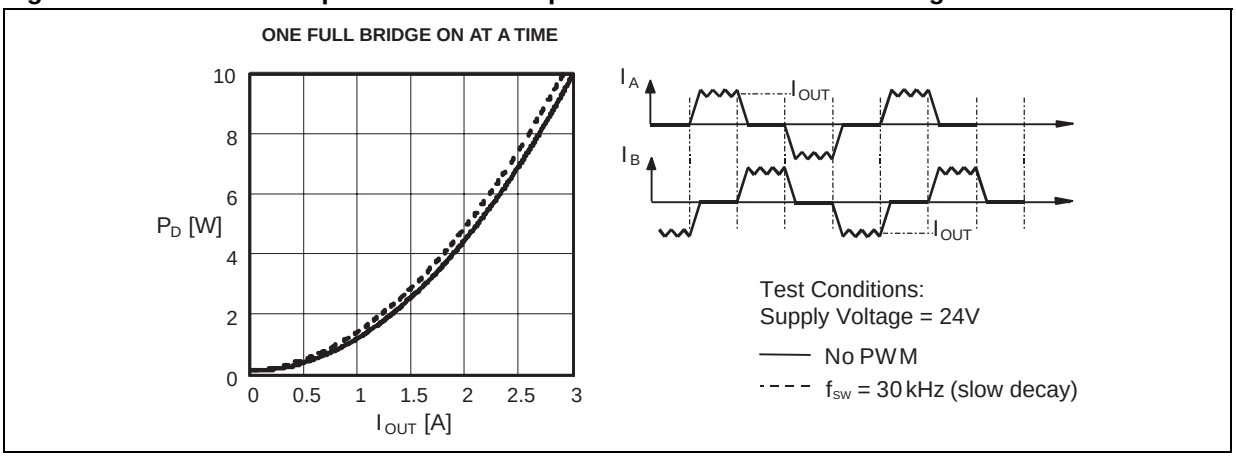
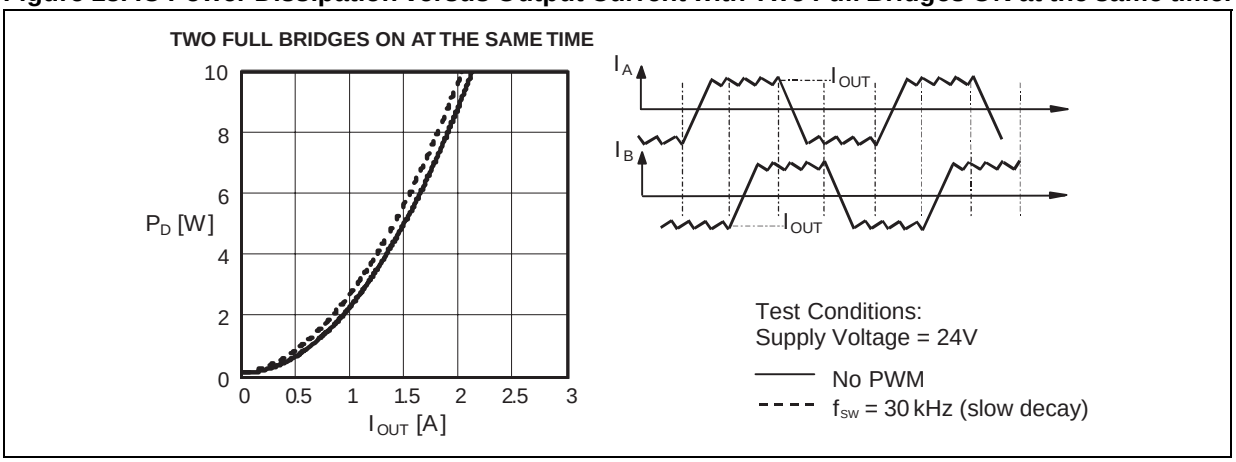


Figure 13. IC Power Dissipation versus Output Current with Two Full Bridges ON at the same time.



THERMAL MANAGEMENT

In most applications the power dissipation in the IC is the main factor that sets the maximum current that can be deliver by the device in a safe operating condition. Therefore, it has to be taken into account very carefully. Besides the available space on the PCB, the right package should be chosen considering the power dissipation. Heat sinking can be achieved using copper on the PCB with proper area and thickness. Figures 15, 16 and 17 show the Junction-to-Ambient Thermal Resistance values for the PowerSO20, PowerDIP20 and SO20 packages.

For instance, using a PowerSO package with copper slug soldered on a 1.5 mm copper thickness FR4 board with 6cm^2 dissipating footprint (copper thickness of 35µm), the $R_{th\ j\text{-}amb}$ is about 35°C/W. Fig. 14 shows mounting methods for this package. Using a multi-layer board with vias to a ground plane, thermal impedance can be reduced down to 15°C/W.

Figure 14. Mounting the PowerSO package.

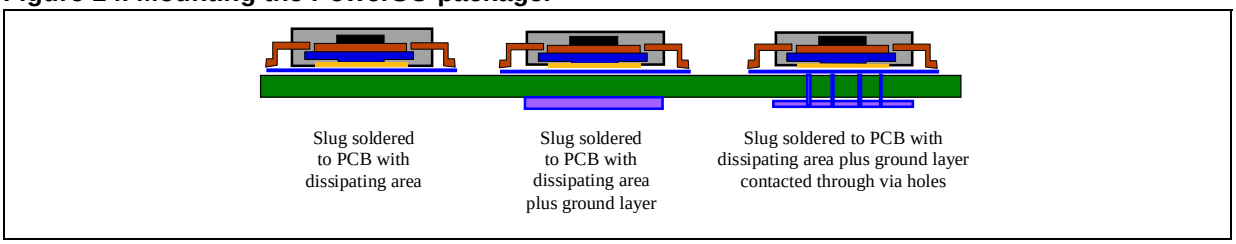


Figure 15. PowerSO20 Junction-Ambient thermal resistance versus on-board copper area.

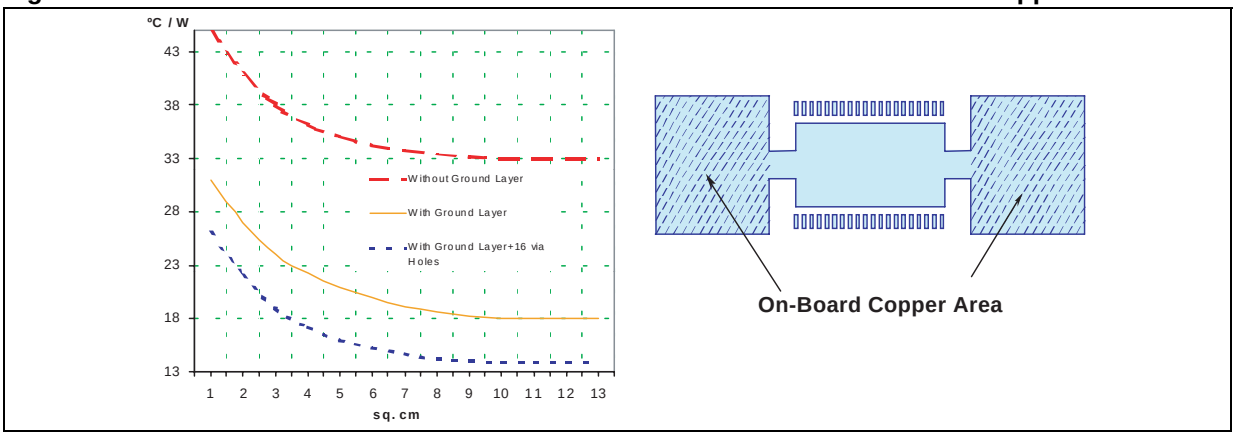


Figure 16. PowerDIP20 Junction-Ambient thermal resistance versus on-board copper area.

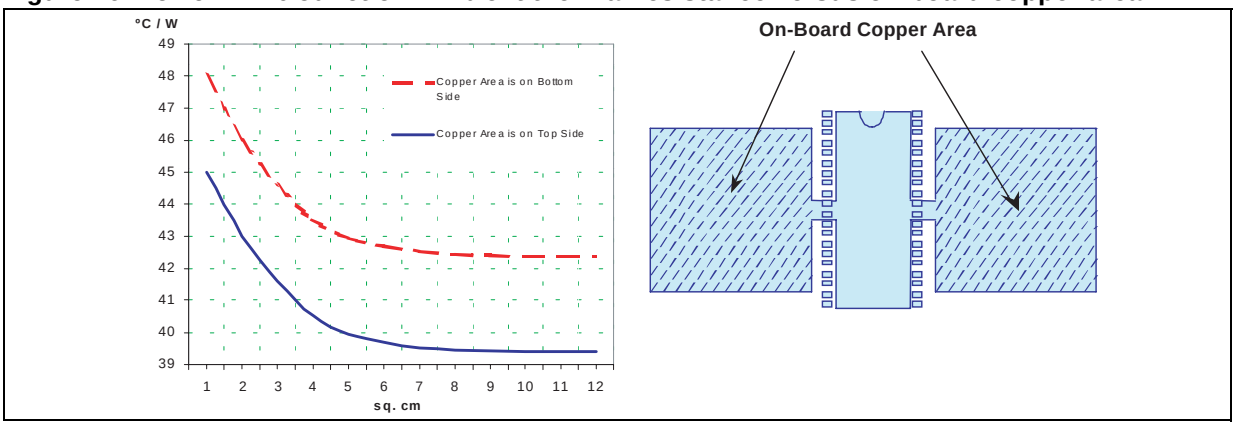


Figure 17. SO20 Junction-Ambient thermal resistance versus on-board copper area.

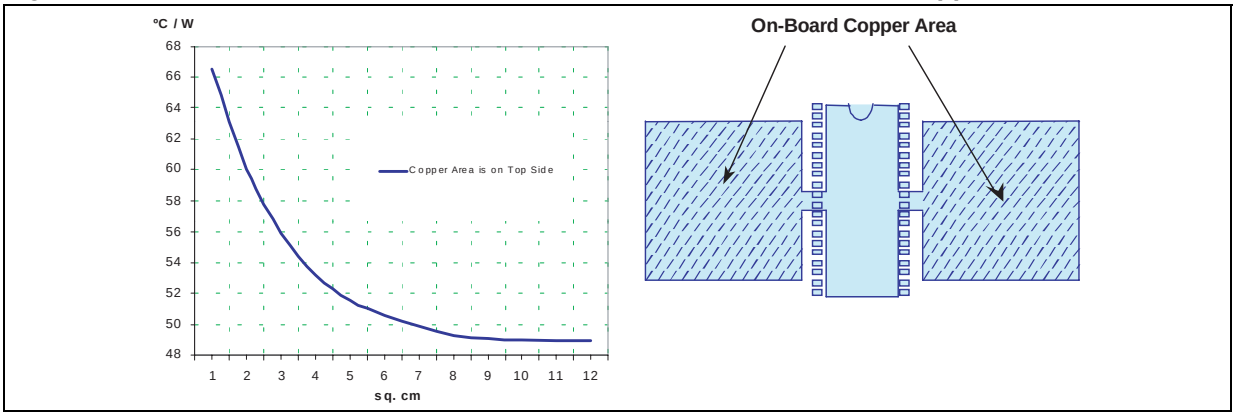


Figure 18. Typical Quiescent Current vs. Supply Voltage

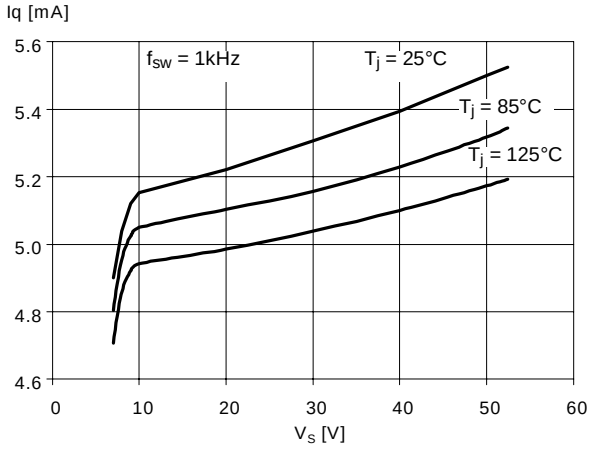


Figure 19. Normalized Typical Quiescent Current vs. Switching Frequency

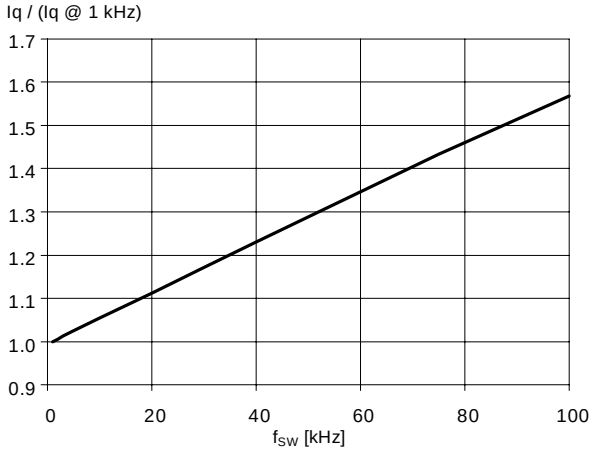


Figure 20. Typical Low-Side $R_{DS(ON)}$ vs. Supply Voltage

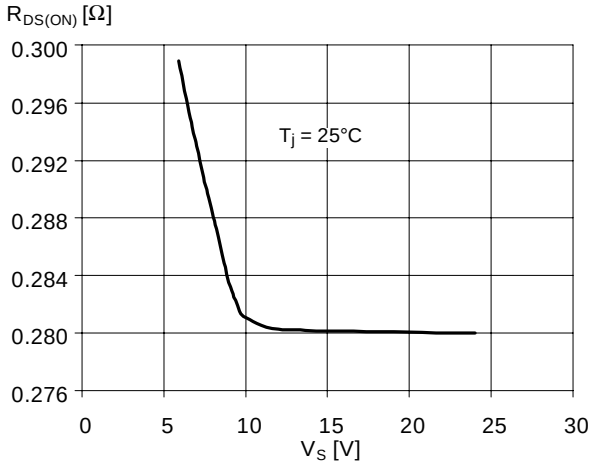


Figure 21. Typical High-Side RDS(ON) vs. Supply Voltage

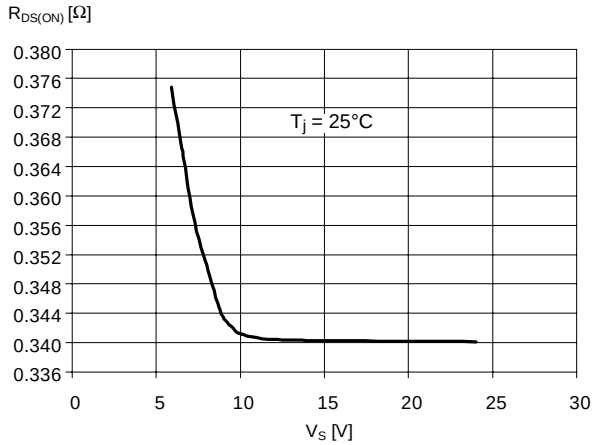


Figure 22. Normalized $R_{DS(ON)}$ vs.Junction Temperature (typical value)

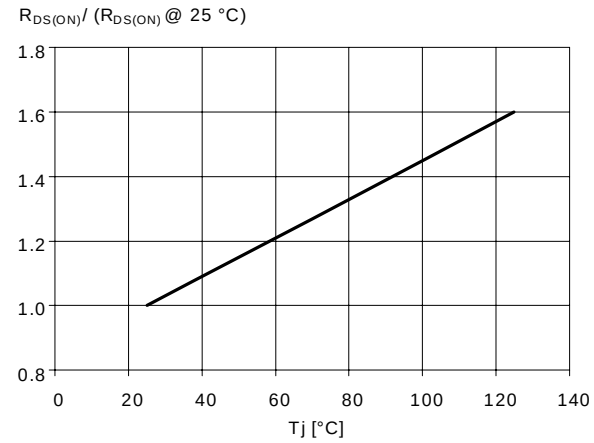
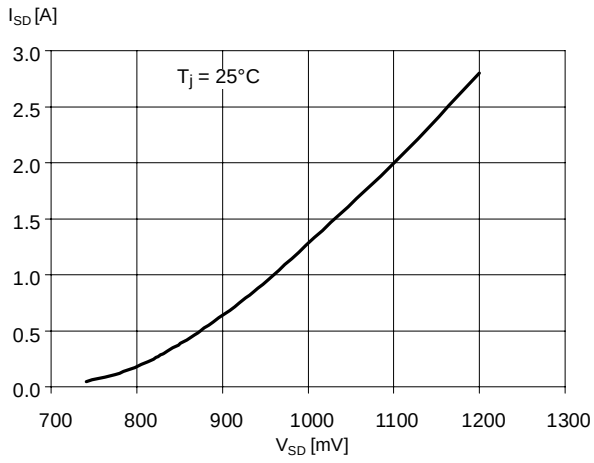


Figure 23. Typical Drain-Source Diode Forward ON Characteristic

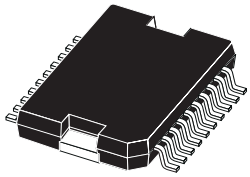


DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			3.6			0.142
a1	0.1		0.3	0.004		0.012
a2			3.3			0.130
a3	0		0.1	0.000		0.004
b	0.4		0.53	0.016		0.021
c	0.23		0.32	0.009		0.013
D (1)	15.8		16	0.622		0.630
D1	9.4		9.8	0.370		0.386
E	13.9		14.5	0.547		0.570
e		1.27			0.050	
e3		11.43			0.450	
E1 (1)	10.9		11.1	0.429		0.437
E2			2.9			0.114
E3	5.8		6.2	0.228		0.244
G	0		0.1	0.000		0.004
H	15.5		15.9	0.610		0.626
h			1.1			0.043
L	0.8		1.1	0.031		0.043
N	8° (typ.)					
S	8° (max.)					
T		10			0.394	

(1) “D and E1” do not include mold flash or protusions.
- Mold flash or protusions shall not exceed 0.15mm (0.006”)
- Critical dimensions: “E”, “G” and “a3”.

OUTLINE AND MECHANICAL DATA

Weight: 1.9gr



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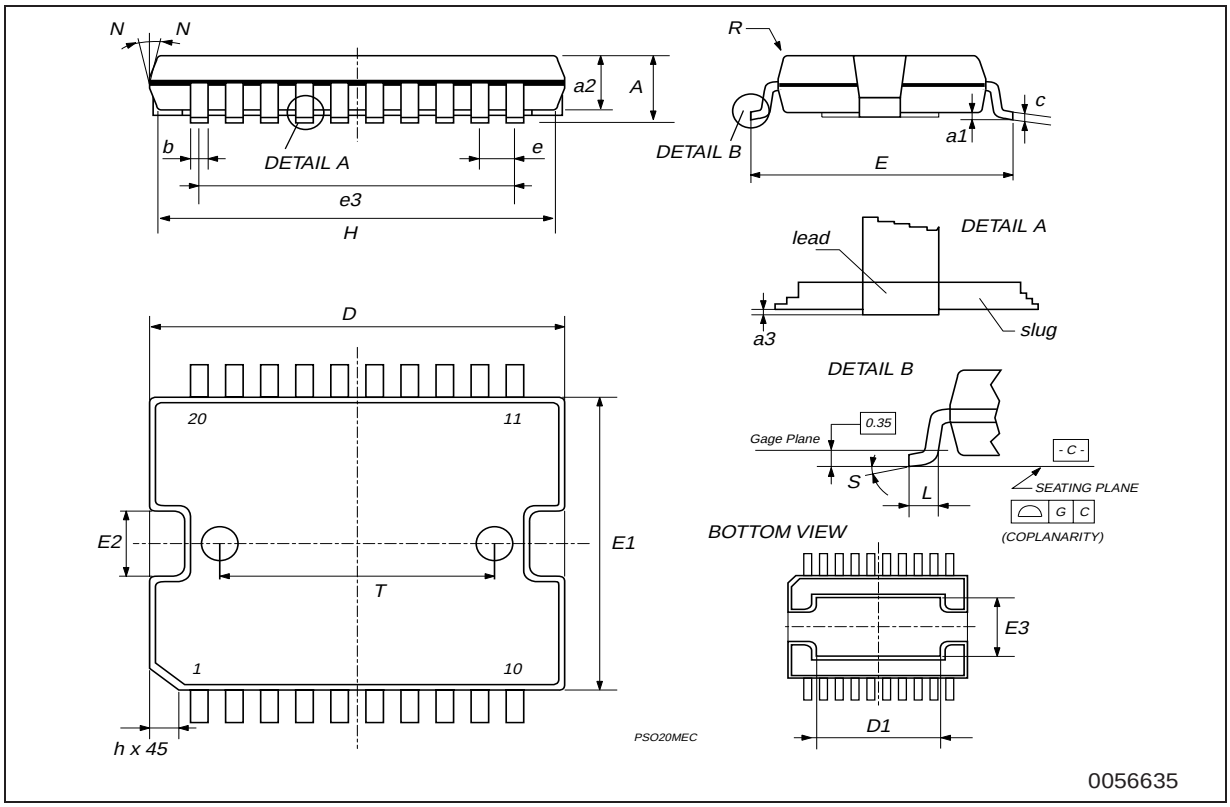
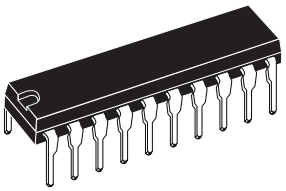
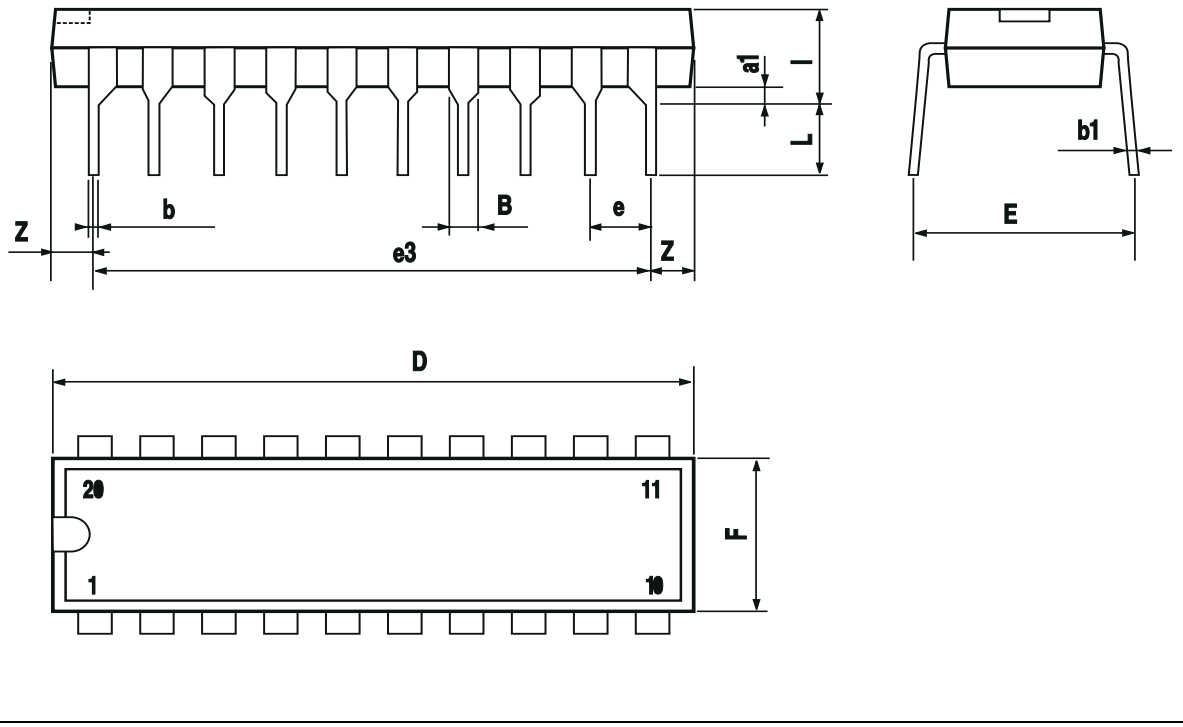


DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.85		1.40	0.033		0.055
b		0.50			0.020	
b1	0.38		0.50	0.015		0.020
D			24.80			0.976
E		8.80			0.346	
e		2.54			0.100	
e3		22.86			0.900	
F			7.10			0.280
I			5.10			0.201
L		3.30			0.130	
Z			1.27			0.050

OUTLINE AND MECHANICAL DATA

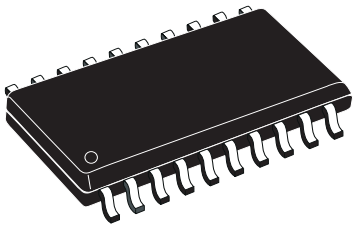


Powerdip 20



DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.35		2.65	0.093		0.104
A1	0.1		0.3	0.004		0.012
B	0.33		0.51	0.013		0.020
C	0.23		0.32	0.009		0.013
D	12.6		13	0.496		0.512
E	7.4		7.6	0.291		0.299
e		1.27			0.050	
H	10		10.65	0.394		0.419
h	0.25		0.75	0.010		0.030
L	0.4		1.27	0.016		0.050
K	0˚ (min.)8˚ (max.)					

OUTLINE AND MECHANICAL DATA



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