Optocoupler SFH6156, Phototransistor Output, DC Input

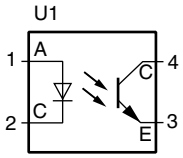
DESCRIPTION

This device consists of a phototransistor optically coupled to a gallium arsenide infrared-emitting diode in 4 pin plastic package. The base terminal of the phototransistor is not connected, resulting in substantially improved common-mode interference immunity.

The PSpice models have been written from device characterization data and were tested with simulation program OrCAD16.6.

The symbol and model files as well as the netlist are in the symbol library file SFH6156.olb, model library file SFH6156.lib and netlist file SFH6156.txt respectively for this model.

This document is intended as a guideline of simulating with provided model and does not constitute as commercial product, neither a substitute to datasheet.

PART	MODEL DESCRIPTION	SYMBOL FILE	MODEL FILE
SFH6156	DC input, phototransistor output	 SFH6156 SFH6156.olb	SFH6156.lib

RECOMMENDED USE OF THE MODEL

- This model is designed only for use at 25 °C and should be used as is.
- This model has been created and tested with OrCAD version 16.6.
- The olb file (symbol) is not down-compatible. Users of the earlier versions need to create the symbols on their platform and associate with relative PSpice model data.
- The CTR simulated data is simulation result with default value of model parameter REL_CTR = 1. To obtain different CTR values, it can be modified with Property Editor of OrCAD Capture CIS and used with different REL_CTR values as shown in the table below.

CTR BIN	CTR (typ.)	REL_CTR
1	60	0.36
2	90	0.55
3	150	1.0 (default)
4	240	1.67

NETLIST OF MODEL

Following list shows the netlist of the model:

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* Library of DC Input Phototransistor Output Optocoupler SFH6156
* Copyright VISHAY, Inc. 2016 All Rights Reserved.
*
* ==== SFH6156-3 ====
* A = diode anode
* K = diode cathode
* C = BJT collector
* E = BJT emitter
*$
.SUBCKT SFH6156 A K C E PARAMS: REL_CTR=1
D1 A D D9508   ;IRED
Vsense D K 0 ;IF Current sense
Hd R 0 Vsense 1           ;I-V
Rd R T 10K
Cd T 0 0.2n
Rdummy B 0 4G
Q1 C B E E QT1090 ;phototransistor
* V-I
Gpcg C B TABLE  ;Photodetector {(IC vs IF) / Q1 BF}
+ {0.8*(V(T)^1.658*exp(limit(4.36-60*V(T),-50,50))*REL_CTR/100)}
+ (0,0) (10,10)
.model D9508 D IS=1P N=1.948621 RS=1.560495 BV=6 IBV=10U
+ CJO=18.8P VJ=0.532794 M=0.27985 EG=1.424 TT=500N
.model QT1090 NPN IS=3.64P BF=100 NF=1.193293 BR=10 TF=30N TR=350n
+ CJE=5.16P VJE=0.99 MJE=0.2411274 CJC=18P VJC=0.597478 MJC=0.431978
+ ISC=0.207N VAF=65 IKF=0.09 ISS=0 CJS=7.74p VJS=0.61 MJS=0.31
.ends
*$
**=====================================================================*
* Note:                                                               *
* Although models can be a useful tool in evaluating device           *
* performance, they cannot model exact device performance             *
* under all conditions, nor are they intended to replace              *
* breadboarding for final verification!                               *
*                                                                     *
* Models provided by VISHAY Semiconductors GmbH are not               *
* as fully representing all of the specifications and operating       *
* characteristics of the semiconductor product to which the           *
* model relates.                                                      *
* The models describe the characteristics of typical devices.         *
* In all cases, the current data sheet information for a given        *
* device is the final design guideline and the only actual            *
* performance specification.                                          *
* VISHAY Semiconductors does not assume any liability arising         *
* from the model use. VISHAY Semiconductors reserves the right to     *
* change models without prior notice.                                 *
**=====================================================================*
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SIMULATED PARAMETERS (T_{amb} = 25 °C, unless otherwise specified)				
PARAMETER	**TEST CONDITION**	**SYMBOL**	**SIMULATION DATA**	**UNIT**
INPUT				
Forward voltage	I_F = 10 mA	V_F	1.18	V
COUPLER				
Current transfer ratio = (I_C/I_F)	V_{CE} = 5 V, I_F = 10 mA	CTR	154	%
SWITCHING (1)				
Turn-on time	V_S = 5 V, I_F = 10 mA, R_L= 1 kΩ (saturated operation)	t_{on}	3	µs
Turn-off time		t_{off}	17	

Note

(1) See Switching Time and Timing Simulation Setup for switching parameters.

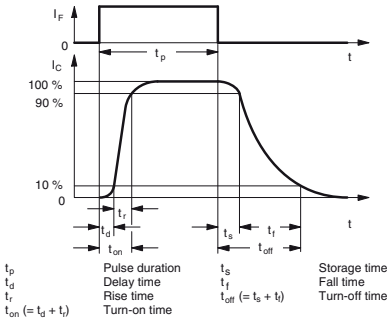

Fig. 1 - Switching Times

EXAMPLE SIMULATION PLOTS USING OrCAD

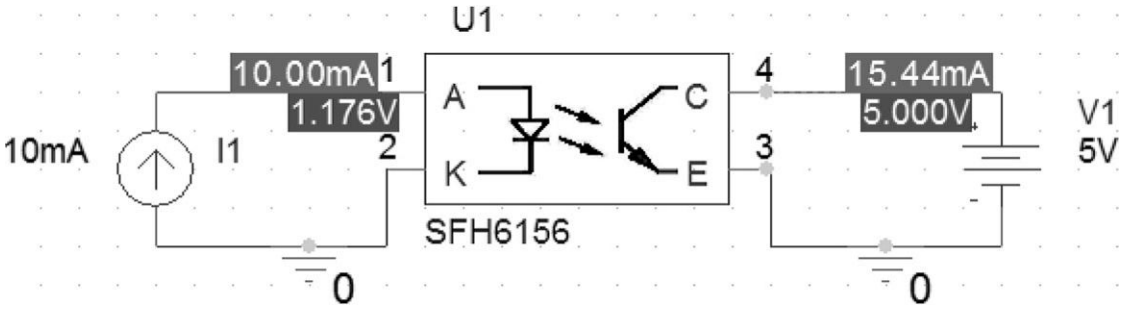

Fig. 2 - Simulation Setup for the Following DC Curves

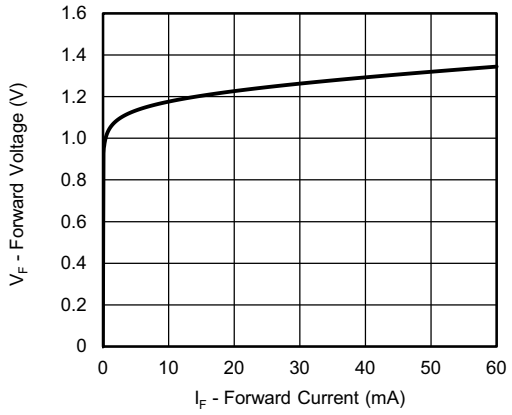

Fig. 3 - Forward Current vs. Forward Voltage

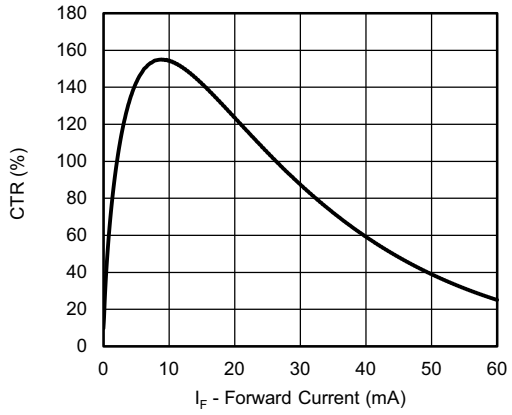

Fig. 4 - CTR vs. Forward Current
(non-saturated)

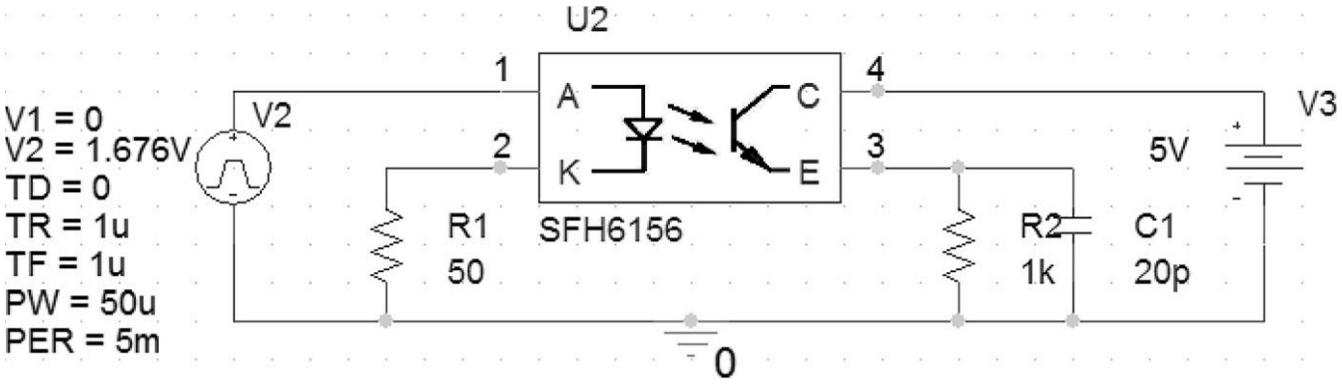

Fig. 5 - Timing Simulation Setup (V_{CC} = 5 V, I_F = 10 mA, R_L = 1.0 kΩ) Saturated Operation

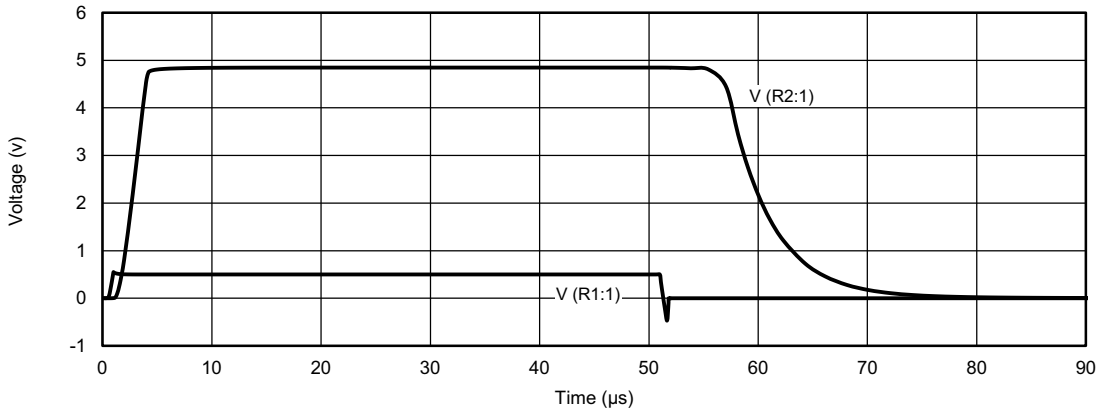

Fig. 6 - Timing Simulation Output Data
(saturated)