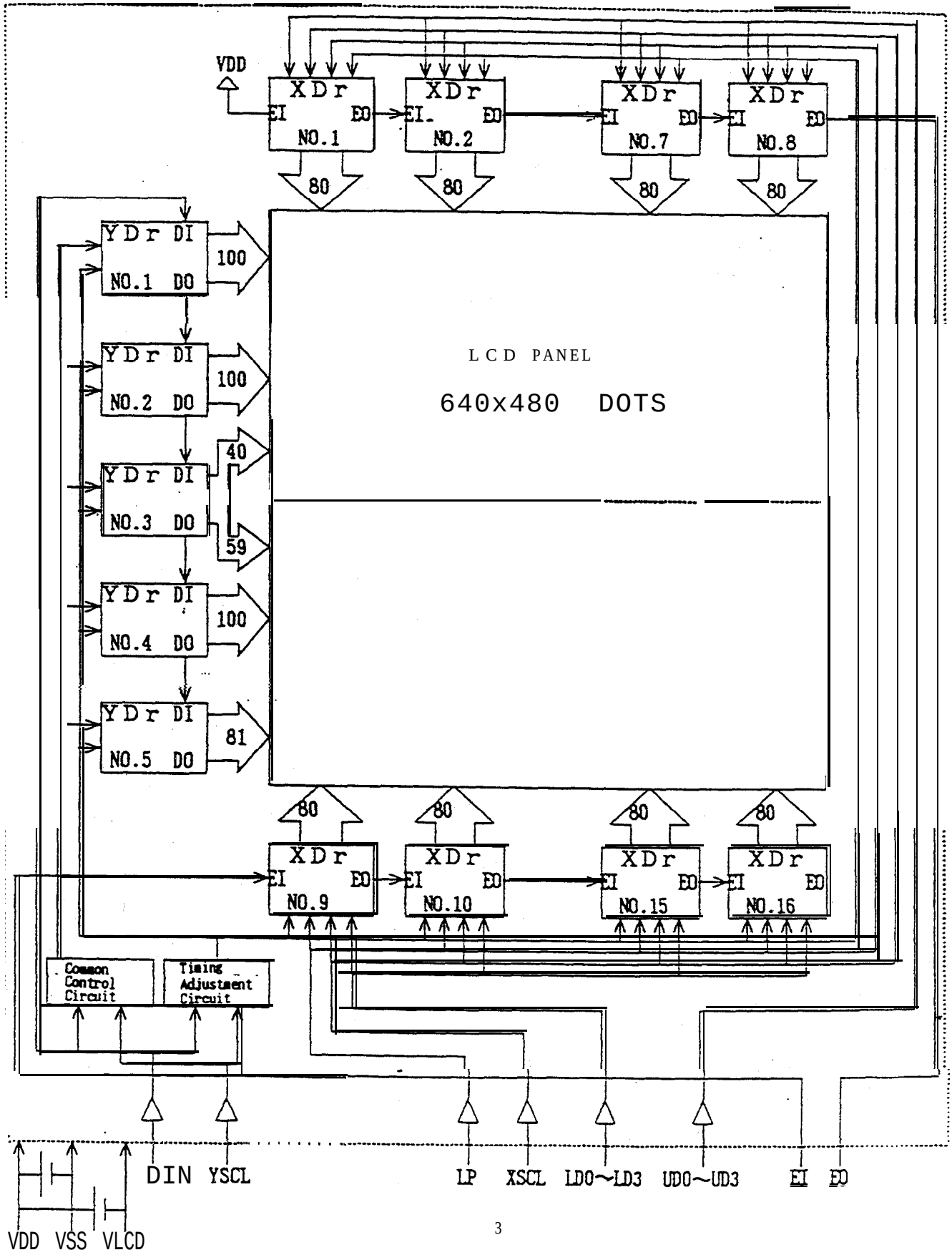
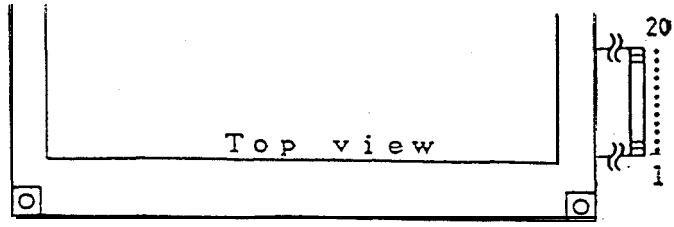
3. Block diagram



4. I/O Terminals

4.1 Terminal Configuration



4.2 Terminal Functions

Pin No.	Signal	Name	Function
1	VDD	Power Supply Voltage	+5.0V±5%
2	vss	GND	0V
3	VLCD	Power Supply (LCD)	Contrast Variable Power
4	LP	Latch Pulse	Data Latch
5	NC	NC	
6	NC	NC	
7	YSCL	Y Shift Clock	Data Shift Clock
8	DIN	Synchronous Pulse	Scan Start Pulse
9	XSCL	X Shift Clock	Data Shift Clock
10	NC	NC	
11	UD0	Data	Display Data Input for Upper Half Screen
12	UD1		
13	UD2		
14	UD3		
15	LD0	Data	Display Data Input for Lower Half Screen
16	LD1		
17	LD2		
18	LD3		
19	EI	Enable IN	Enable Signal Input for XDr(5) *
20	EO	Enable OUT	Connecting with VSS Internally

*4 bit input : Connect EI EI to EO
8 bit input : EI - VDD, ED - NC

5. DATA INPUT FORMAT (640 x 480 dots)

5.1 Display Dot Map

Column→ / Row ↓	1 D	2 D	3 D	4 D	5 D	6 D	...	635 D	636 D	637 D	638 D	639 D	640 D
1 D	1 . 1	1 . 2	1 . 3	1 . 4	1 . 5	1 . 6		1 .635	1 .636	1 .637	1 .638	1 .639	1 .640
2 D	2 . 1	2 . 2	2 . 3	2 . 4	2 . 5	2 . 6		2 .635	2 .636	2 .637	2 .638	2 .639	2 .640
⋮	⋮	⋮	⋮	⋮	⋮	⋮	...	⋮	⋮	⋮	⋮	⋮	⋮
239 D	239.1	239.2	239.3	239.4	239.5	239.6		239.635	1239.636	239.637	239.638	239.639	239.640
240 D	240.1	240.2	240.3	240.4	240.5	240.6	t	240.635	1240.636	240.637	240.638	240,639	240.640
241 D	1 . 1	1 . 2	1 . 3	1 . 4	1 . 5	1 . 6		1 .635	1 .636	1 .637	1 .638	1 .639	1 .640
242 D	2 . 1	2 . 2	2 . 3	2 . 4	2 . 5	2 . 6		2 .635	2 .636	2 .637	2 .638	2 .639	2 .640
⋮	⋮	⋮	⋮	⋮	⋮	⋮	...	⋮	⋮	⋮	⋮	⋮	⋮
479 D	239.1	239.2	239.3	239.4	239.5	239.6		239.635	239.636	239.637	239.638	239.639	239.640
480 D	240.1	240.2	240.3	240.4	240.5	240.6		240.635	240.63;	240.637	240.638	240.639	240.640

The previous display dot map shows the entry order of data in terms of dots on the LCD.
Display data is sequentially entered in each UD0~UD3, LD0-LD3 on a 4 bits basis, from left to right, beginning with location "1.1".
This display from 1.1 ~ 1.4, 1.5 ~ 1.8, . . . to 1.640 on a 4 dots (bits) basis.

5.2 Correspndence of Data Input Terminals to Dot Numbers in a Row

Data Input Terminal	Dots (Row) on Display
UD0 / LD0	dot 4, dot 8 . . . . . dot 636, dot 640
UD1 / LD1	dot 3, dot 7 . . . . . dot 635, dot 639
UD2 / LD2	dot 2, dot 6 . . . . . dot 634, dot 638
UD3 / LD3	dot 1, dot 5 . . . . . dot 633, dot 637

Input data UD0~UD3, LD0~LD3 correspond. to display dots as shown above. The first input data corresponds to dot 4~1, and the last input data to dot 640,637.

5.3 Data Input Method

This module uses "Chip Enable Transmission System" to reduce its power consumption. Data is inputted directly into LCD drivers (chips) on a chip basis.' If the n-th chip in enable state becomes full of data, the Enable is transmitted by automaticaly to (n+1)th chip.

There are two methods to input signal into display as described below.

(1) To input the signal on 4 bit-bus with one line.(UD0~UD3)
In case of using the controller which outputs the signal on 4 bit-bus with one line, at first to short circuit the No.19 and 20th pin on I/O terminals and to connect UDO and LDO, UD1 and LD1, UD2 and LD2, UD3 and LD3. Next, to input the signal from UDO to UD3.
In this case signal shall be input from 1.1 ~ 1.640 {XDr(1) to XDr(8)} with each 4 bit into Upper screen, after that signal shall be input Lower screen by same system as Upper screen{XDr(9) to XDr(16)}

(2) To input the signal on 4 bit-bus with two line (UD0~UD3,LD0~LD3)
In case of using the controller which outputs the signal on 4 bit-bus with two line, to connect No.19 pin with VDD level and to open No.20 pin on I/O terminals. Next, to input the signal from UDO,LDO to UD3,LD3 in parallel.
In this case, signal shall be input from 1.1 ~ 1.640 with each 4 bit into Upper and Lower screen at the same time.