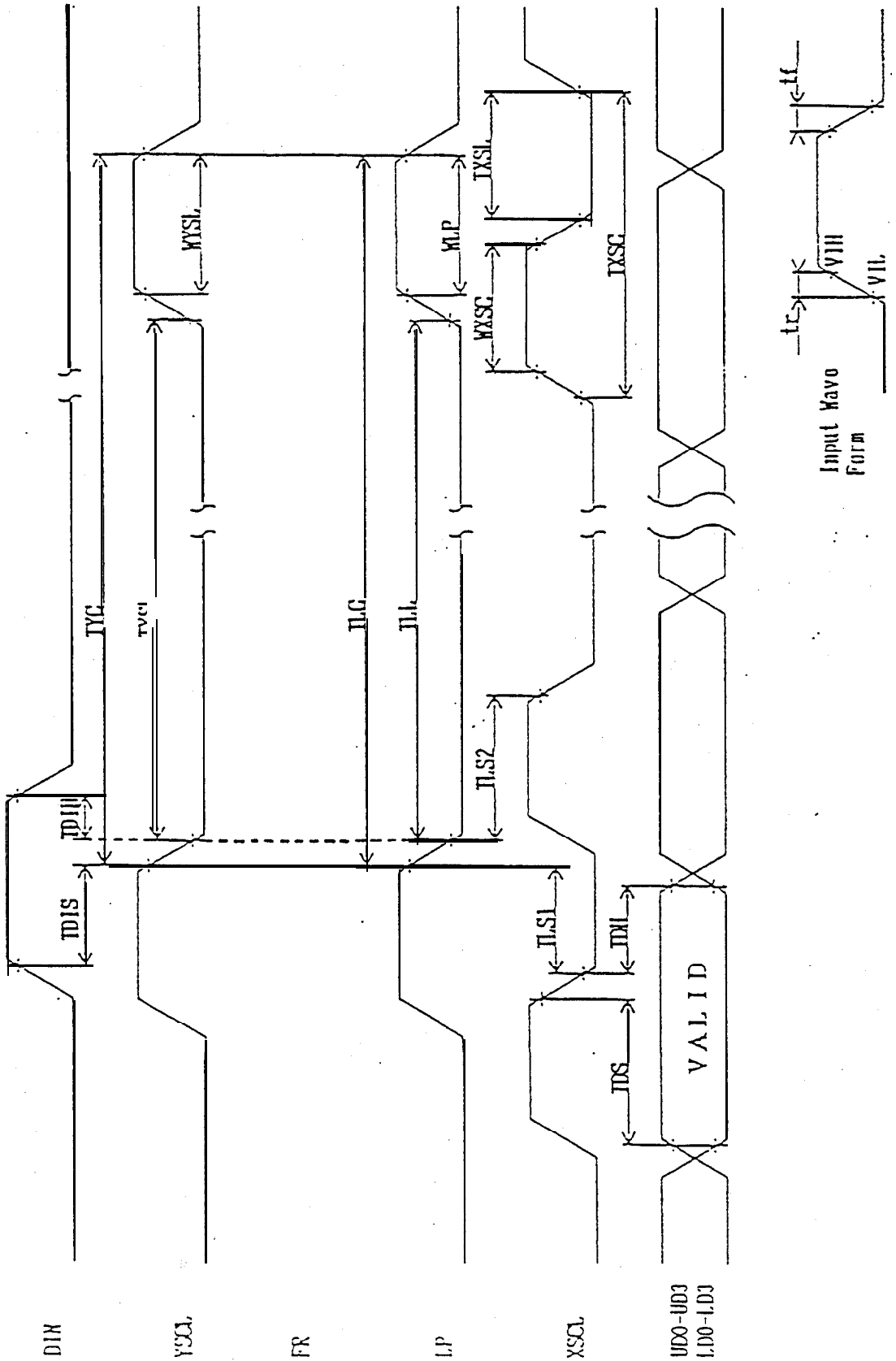
## 7.2 AC Characteristics

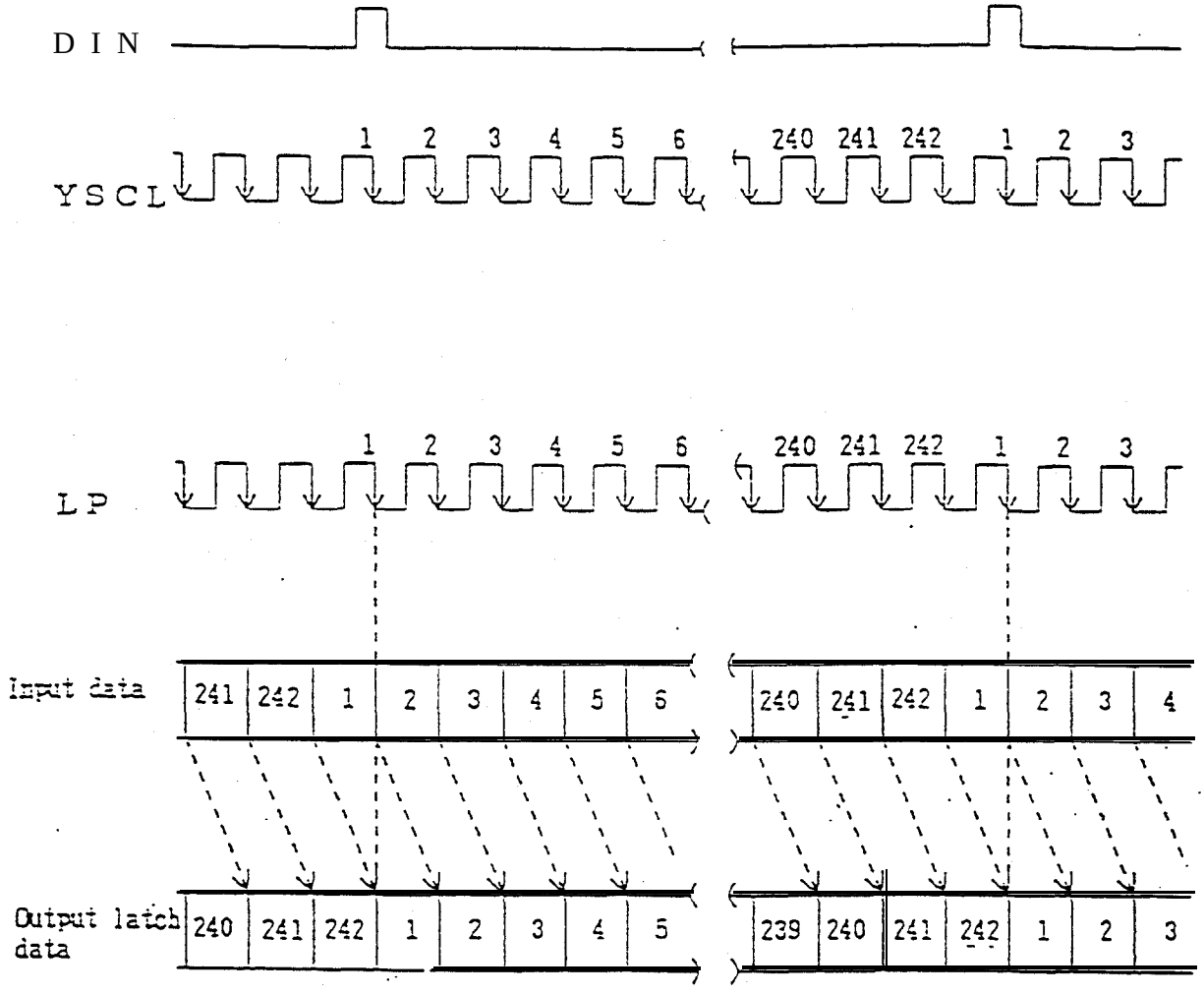
| Parameter | Symbol | Standard value Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| LP period | TLC | - | 55 | - | us | |
| XSCL period | TXSC | 166 | - | - | ns | |
| LP/YSCL"L"time | TLL | 330 | - | - | ns | |
| LP pulse width | WLP | 70 | - | - | ns | |
| XSCL "L" time | TXSL | 70 | - | - | ns | |
| XSCL pulse width | WXSC | 70 | - | - | ns | VDD=5V±5% |
| Latch timing | TLS1 | 70 | | - | - | ns |
| | TLS2 | 70 | - | - | | |
| | TLS3 | 70 | | - | - | |
| | TLD | 0 | - | - | | |
| Data setup time | TDS | 60 | - | - | ns | |
| Data hold time | TDH | 40 | - | - | ns | |
| DIN setup time | TDIS | 100 | - | - | ns | |
| DIN hold time | TDIH | 60 | - | - | ns | |
| Rise & Fall time | tr,tf | - | - | * | ns | |

* (TXSC-TXSL-WXSC)/2 with 50 ns Max.

## 7.2.1 Timing Chart of X(Column) Driver and Y(Row) Driver

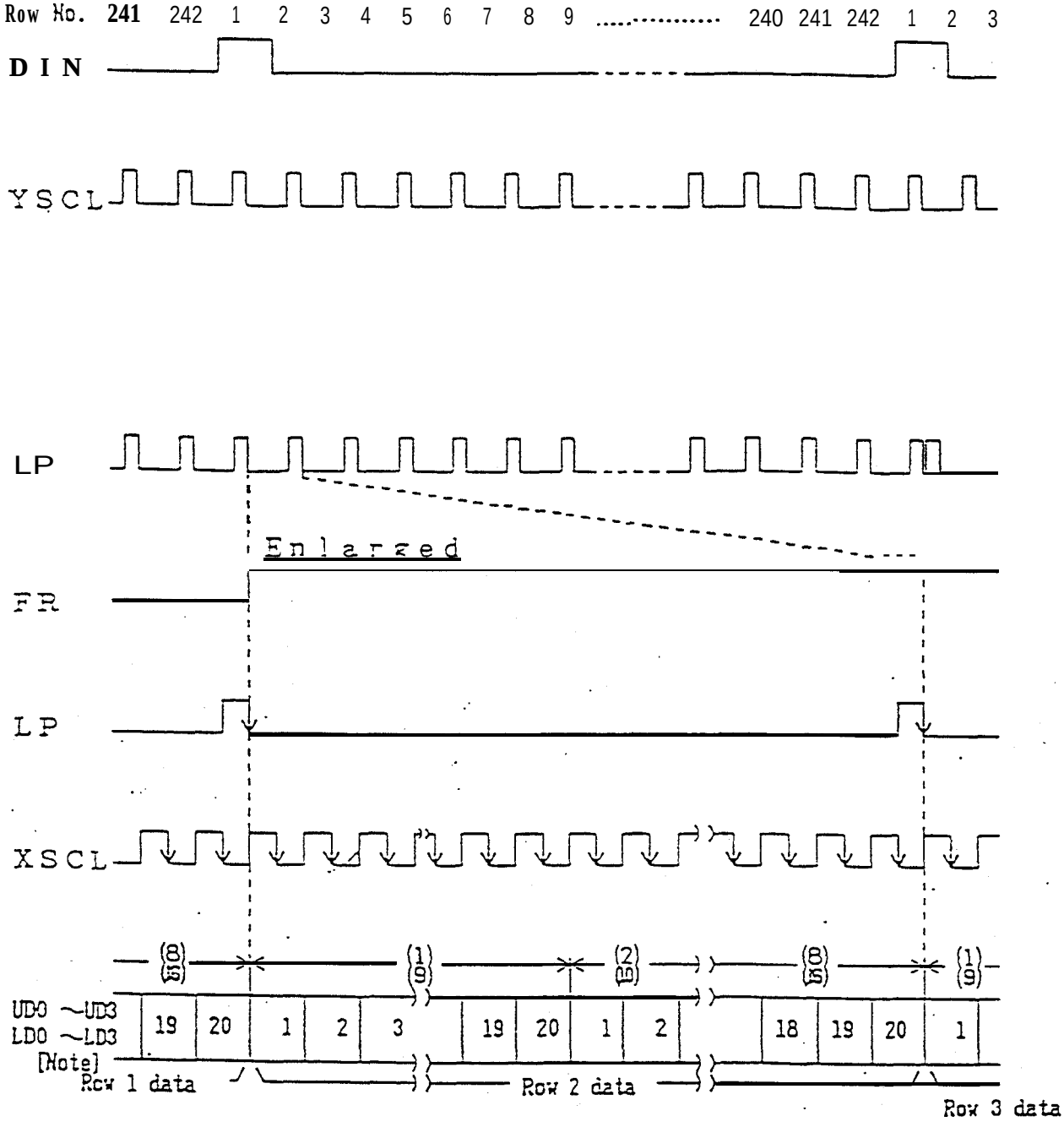


## 7.2.2 Relation of Input data/Output latch data




[Note]"1,2,—,239,240"Indicate row numbers.

## 7.2.3 Timing Chart of input Signals

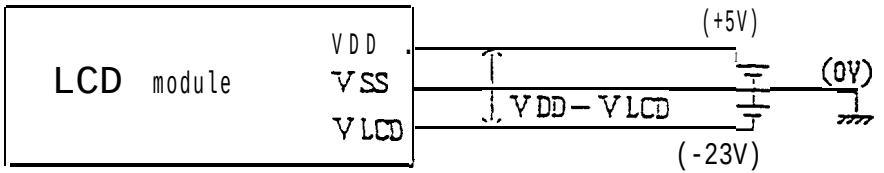



[Note 1] '(1) to (16)' of UD0-UD3 and LD0~LD3 indicate driver chip numbers.

[Note 21 In the display, UD0, LD0 to UD3, LD3 are located from right to left.

[Note 3During the time of row No.241 and 242, the same signal up to row No.240 shall be input to LP and YSCL.

## 8. POWER SUPPLY AND CONTRAST ADJUSTMENT




VDD - VLCD = LCD driving voltage

Display contrast of an LCD module depends on the voltage applied between the YDD and VLCD. Optimum display contrast can be obtained by adjusting **the slide bar of internal potentiomater** to set **a proper** LCD **driving voltage.**

The LCD driving voltage must be adjusted to accommodate for changes in viewing angle, ambient temperature and/or supply voltage which *affect* display contrast: