

EPSON

EG 9006F-NS

LCD Module for
640 x 480 dots

Preliminary

MAY 15, 1990

SEIKO EPSON CORPORATION

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** DRAWING **	

PRELIMINARY

1 Features

- (1) FTN - FEM Technology
- (2) Negative display
- (3) Transmissive type
- (4) 1/242 duty multiplexing drive V - 13.1 V
(Do not use this module by 1/240 and/or 1/241 duty)

(5) Colors

Display dots	----	White
Background	----	Black

(6) Viewing angle

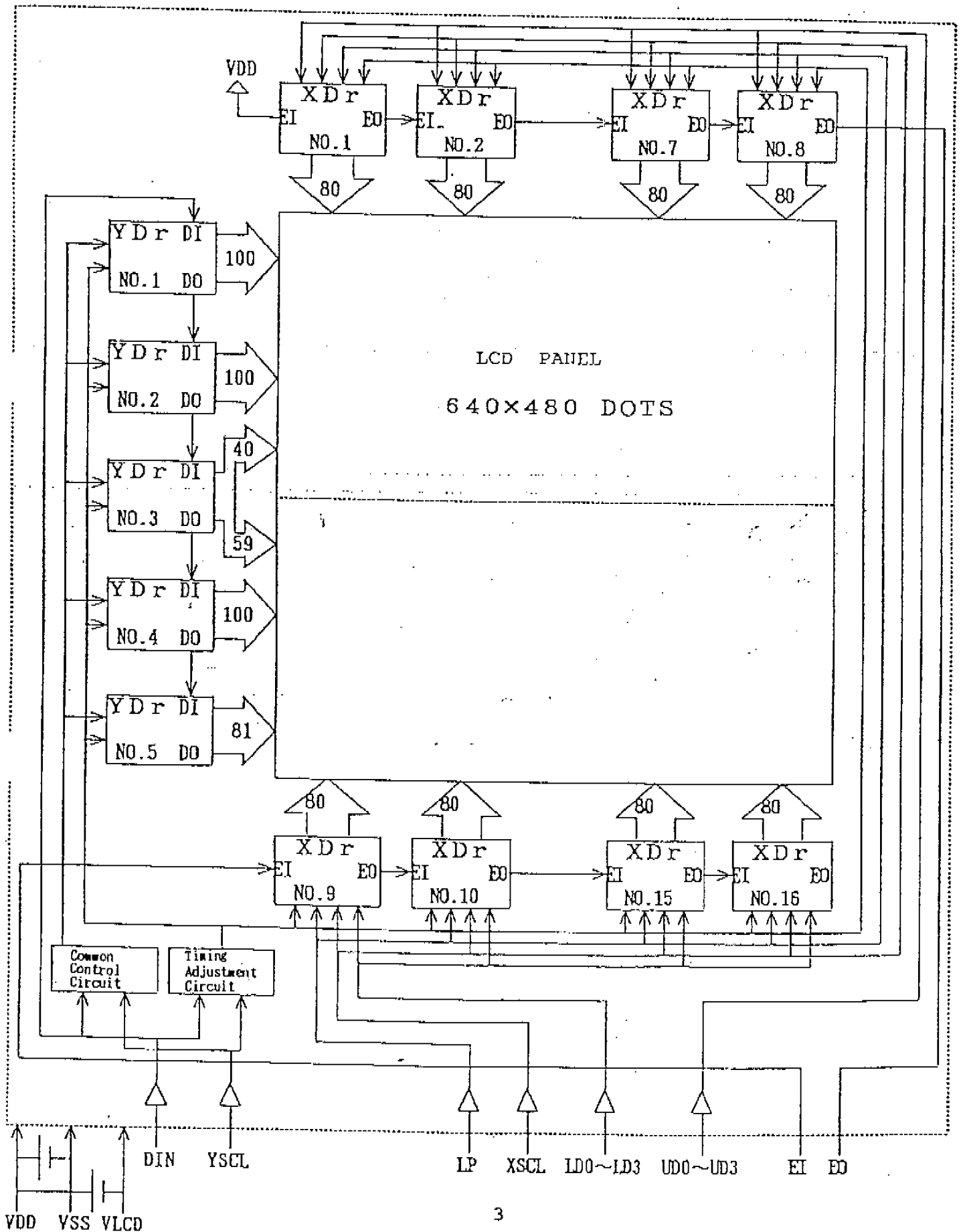
12 o'clock

2. Mechanical Specifications

Item	Specifications
Dot matrix	640×480(dots)
Overall dimensions (W x H x D)	253.5 x 164.0 x 15.0(MAX) *Excluding Mounting Tab
Viewing area (W x H)	180.0 x 134.6
Active area (L x W)	172.765 x 129.565
Dot pitch (L x W)	0.27 x 0.27
Dot size (L x W)	0.235 x 0.235
Weight	700 g

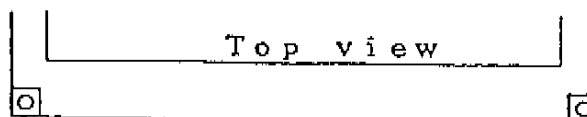
Unit : mm

3. Block diagram



4. I/O Terminals

4.1 Terminal Configuration



4.2 Terminal Functions

Pin No.	Signal	Name	Function
1	VDD	Power Supply Voltage	+5.0V±5%
2	VSS	GND	0V
3	VLCD	Power Supply (LCD)	Contrast Variable Power
4	LP	Latch Pulse	Data Latch
5	NC	NC	---
6	NC	NC	---
7	YSCL	Y Shift Clock	Data Shift Clock
8	DIN	Synchronous Pulse	Scan Start Pulse
9	XSCL	X Shift Clock	Data Shift Clock
10	NC	NC	---
11	UD0	Data	Display Data Input for Upper Half Screen
12	UD1		
13	UD2		
14	UD3		
15	LD0	Data	Display Data Input for Lower Half Screen
16	LD1		
17	LD2		
18	LD3		
19	EI	Enable IN	Enable Signal Input for XDr(5) *
20	EO	Enable OUT	Connecting with VSS Internally

* 4 bit input : Connect EI EI to EO

8 bit input : EI - VDD, EO - NC

5. DATA INPUT FORMAT (640 x 480 dots)

5.1 Display Dot Map

Column →	1°	2°	3°	4°	5°	6°	635°	636°	637°	638°	639°	640°
Row ↓												
1°	1.1	1.2	1.3	1.4	1.5	1.6	1.635	1.636	1.637	1.638	1.639	1.640
2°	2.1	2.2	2.3	2.4	2.5	2.6	2.635	2.636	2.637	2.638	2.639	2.640
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
239°	239.1	239.2	239.3	239.4	239.5	239.6	239.635	239.636	239.637	239.638	239.639	239.640
240°	240.1	240.2	240.3	240.4	240.5	240.6	240.635	240.636	240.637	240.638	240.639	240.640
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
241°	1.1	1.2	1.3	1.4	1.5	1.6	1.635	1.636	1.637	1.638	1.639	1.640
242°	2.1	2.2	2.3	2.4	2.5	2.6	2.635	2.636	2.637	2.638	2.639	2.640
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
479°	239.1	239.2	239.3	239.4	239.5	239.6	239.635	239.636	239.637	239.638	239.639	239.640
480°	240.1	240.2	240.3	240.4	240.5	240.6	240.635	240.636	240.637	240.638	240.639	240.640

The previous display dot map shows the entry order of data in terms of dots on the LCD. Display data is sequentially entered in each UD0~UD3, LD0~LD3 on a 4 bits basis, from left to right, beginning with location "1.1". This display from 1.1 ~ 1.4, 1.5 ~ 1.8, ... to 1.640 on a 4 dots (bits) basis.

5.2 Correspondence of Data Input Terminals to Dot Numbers in a Row

Data Input Terminal	Dots (Row) on Display
UD0 / LD0	dot 4, dot 8 dot 636, dot 640
UD1 / LD1	dot 3, dot 7 dot 635, dot 639
UD2 / LD2	dot 2, dot 6 dot 634, dot 638
UD3 / LD3	dot 1, dot 5 dot 633, dot 637

Input data UD0~UD3, LD0~LD3 correspond to display dots as shown above. The first input data corresponds to dot 4~1, and the last input data to dot 640~637.

5.3 Data Input Method

This module uses "Chip Enable Transmission System" to reduce its power consumption. Data is inputted directly into LCD drivers (chips) on a chip basis. If the n-th chip in enable state becomes full of data, the Enable is transmitted by automatically to (n+1)th chip.

There are two methods to input signal into display as described below.

- (1) To input the signal on 4 bit-bus with one line.(UD0~UD3)
 In case of using the controller which outputs the signal on 4 bit-bus with one line, at first to short circuit the No.19 and 20th pin on I/O terminals and to connect UD0 and LD0, UD1 and LD1, UD2 and LD2, UD3 and LD3. Next, to input the signal from UD0 to UD3.
 In this case signal shall be input from 1.1 ~ 1.640 {XDr(1) to XDr(8)} with each 4 bit into Upper screen, after that signal shall be input Lower screen by same system as Upper screen{XDr(9) to XDr(16)}.
- (2) To input the signal on 4 bit-bus with two line (UD0~UD3,LD0~LD3)
 In case of using the controller which outputs the signal on 4 bit-bus with two line, to connect No.19 pin with VDD level and to open No.20 pin on I/O terminals. Next, to input the signal from UD0,LD0 to UD3,LD3 in parallel.
 In this case, signal shall be input from 1.1 ~ 1.640 with each 4 bit into Upper and Lower screen at the same time.

6. Absolute Maximum Ratings

Parameter	Symbol	Standard Value	Unit
Supply voltage	VDD-VSS	0 ~ +7	V
	VDD-VLCD	0 ~ +28.0	
Input voltage	VIN	$VSS \leq VIN \leq VDD$	V
Operating temperature	Top	+5 ~ +40	°C
Storage temperature	Tst	-20 ~ +60	

7. Electrical Characteristics

7.1 DC Characteristics

$T_a = 25\text{ }^\circ\text{C}$
 $V_{DD} = 5\text{ V} \pm 5\%$

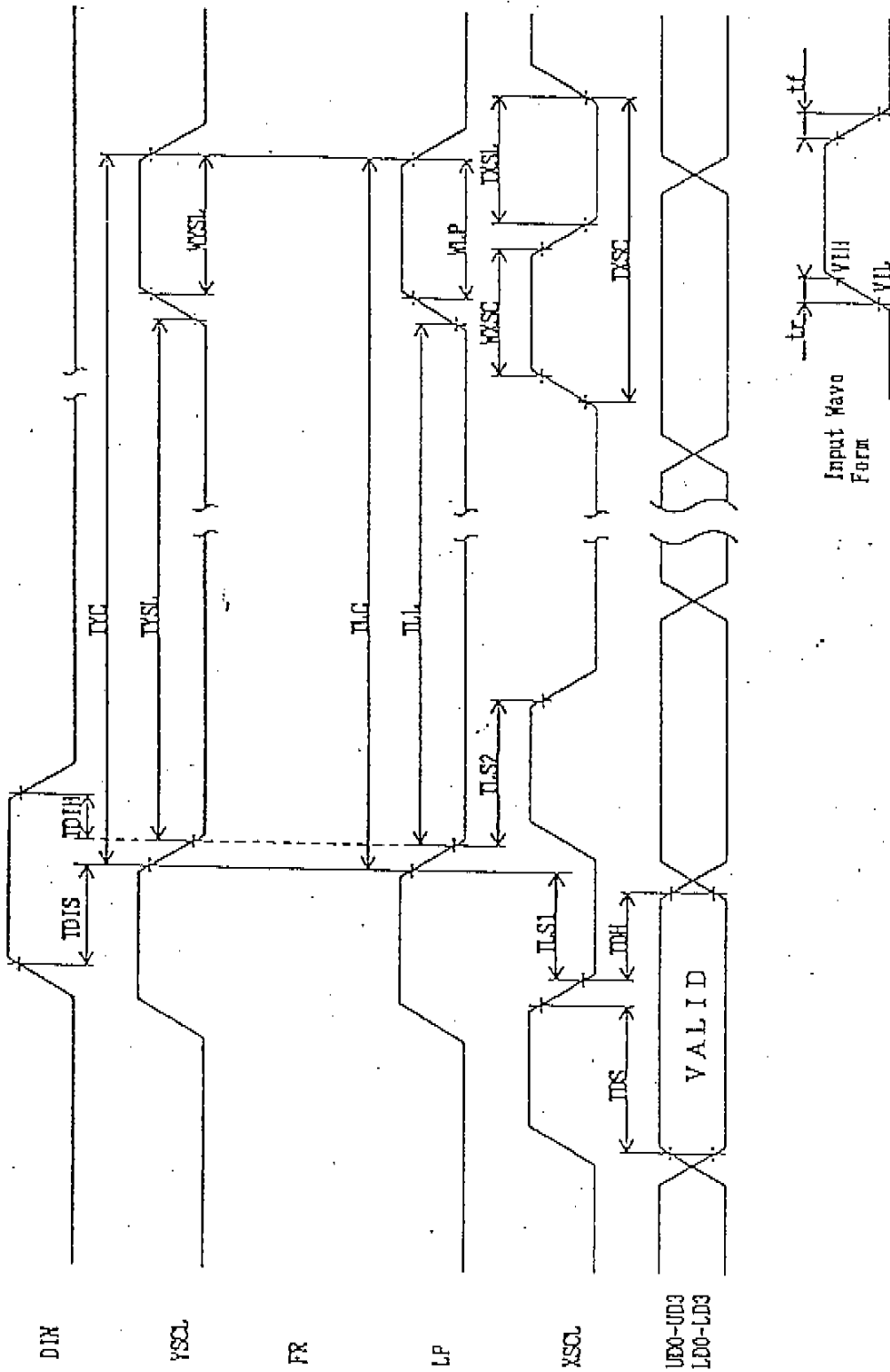
Parameter	Symbol	Standard value			Unit	Condition	Applicable Terminal	
		Min	Typ	Max				
Supply Voltage	VDD	4.75	5	5.25	V		VDD	
	VLCD	VDD - 15	--	--			VLCD	
"0" Input Voltage	VIL	--	--	0.2VDD	V		UD0 ~ UD3 LD0 ~ LD3 XSCL, LP YSCL, BIN	
"1" Input Voltage	VIH	0.8VDD	--	--				
"0" Input Current	IIL	- 0.1	--	--	μA			
"1" Input Current	IIH	--	--	0.1				
Supply Current	IDD	-	17.9	22.6	mA	VDD = 5.0 V		VDD
Supply Current (LCD)	ILCD	-	6.4	13.0	mA	VLCD = 16.0 V fFR = 70 Hz		VLCD

7.2 AC Characteristics

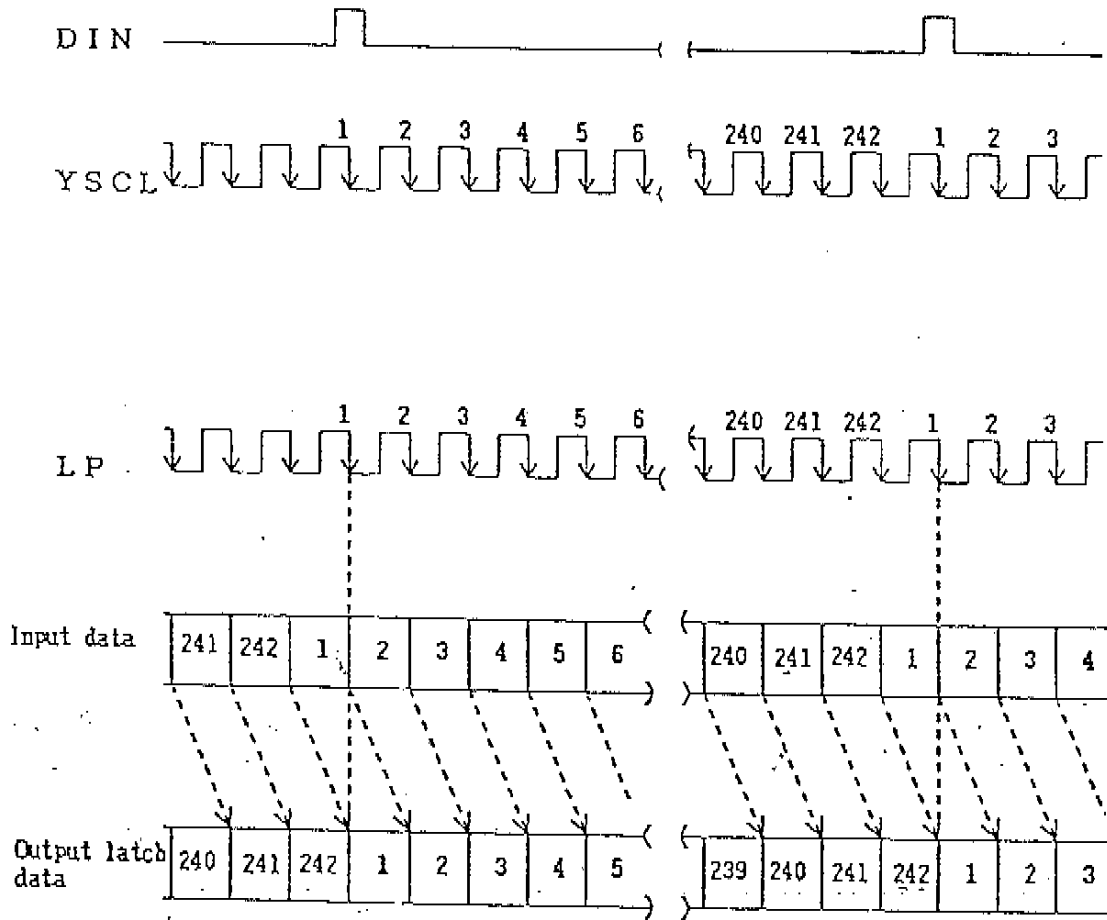
Parameter	Symbol	Standard value			Unit	Condition
		Min	Typ	Max		
LP period	TLC	-	55	-	us	
XSCL period	TXSC	166	-	-	ns	
LP/YSCL"L" time	TLL	330	-	-	ns	
LP pulse width	WLP	70	-	-	ns	
XSCL "L" time	TXSL	70	-	-	ns	
XSCL pulse width	WXSC	70	-	-	ns	VDD=5V±5%
Latch timing	TLS1	70	-	-	ns	
	TLS2	70	-	-		
	TLS3	70	-	-		
	TLD	0	-	-		
Data setup time	TDS	60	-	-	ns	
Data hold time	TDH	40	-	-	ns	
DIN setup time	TDIS	100	-	-	ns	
DIN hold time	TDIH	60	-	-	ns	
Rise & Fall time	tr,tf	-	-	*	ns	

* $(TXSC - TXSL - WXSC) / 2$ with 50 ns Max.

7.2.1 Timing Chart of X(Column) Driver and Y(Row) Driver

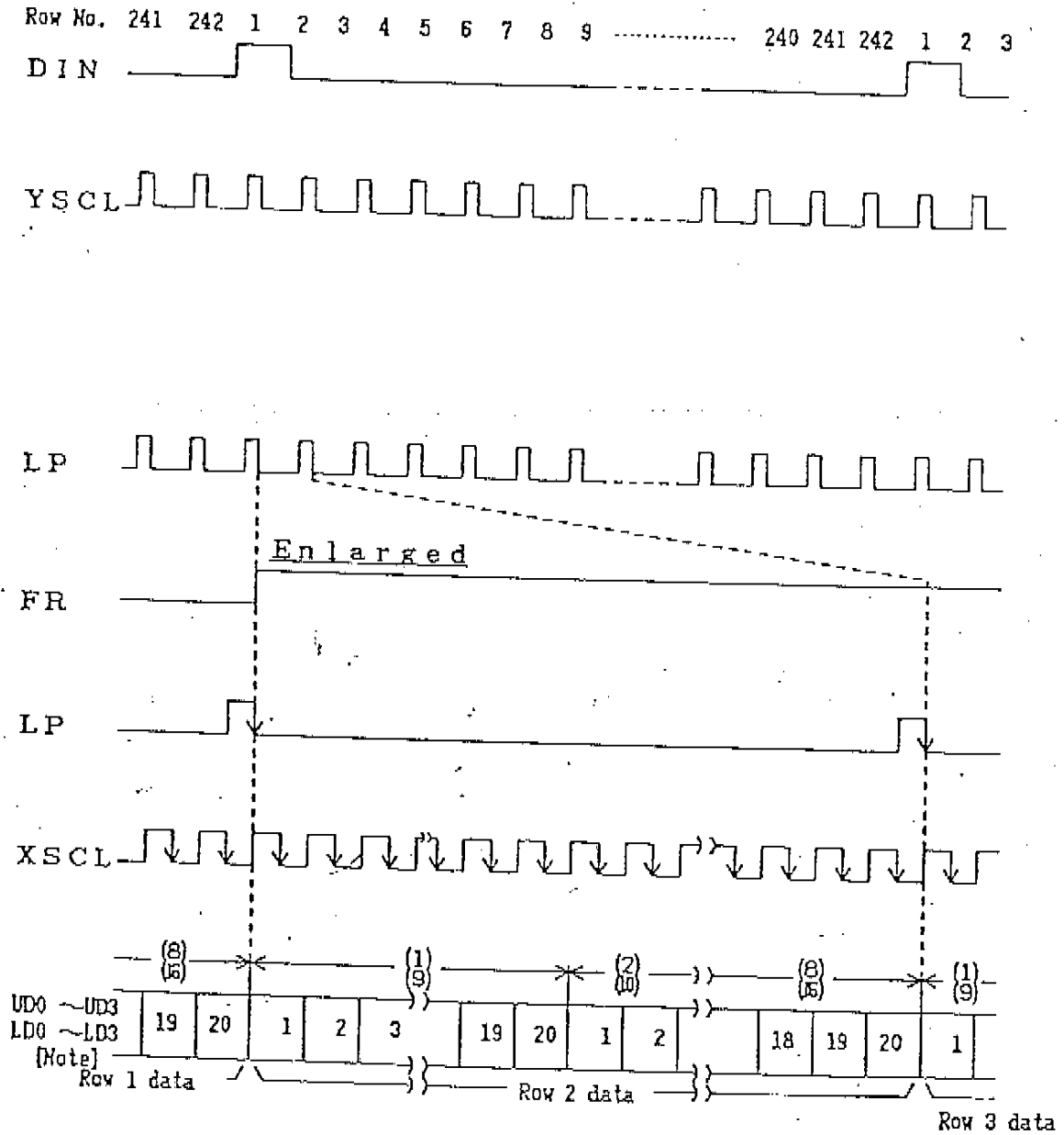


7.2.2 Relation of Input data/Output latch data



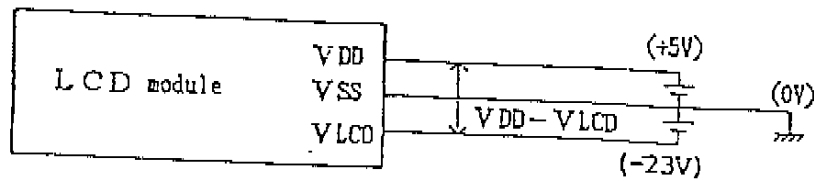
[Note] "1,2,...,239,240" indicate row numbers.

7.2.3 Timing Chart of Input Signals



- [Note 1] '(1) to (16)' of UD0~UD3 and LD0~LD3 indicate driver chip numbers.
- [Note 2] In the display, UD0, LD0 to UD3, LD3 are located from right to left.
- [Note 3] During the time of row No.241 and 242, the same signal up to row No.240 shall be input to LP and YSCL.

8. POWER SUPPLY AND CONTRAST ADJUSTMENT



$VDD - VLCD = \text{LCD driving voltage}$

Display contrast of an LCD module depends on the voltage applied between the VDD and VLCD. Optimum display contrast can be obtained by adjusting the slide bar of internal potentiometer to set a proper LCD driving voltage. The LCD driving voltage must be adjusted to accommodate for changes in viewing angle, ambient temperature and/or supply voltage which affect display contrast.

9. Optical Characteristics

9.1 LCD Driving Conditions

(Ta=25°C)

Item	Voltage	Duty	Bias
Standard	22.5 V	1/242	1/14

9.2 Electro-optical Characteristics

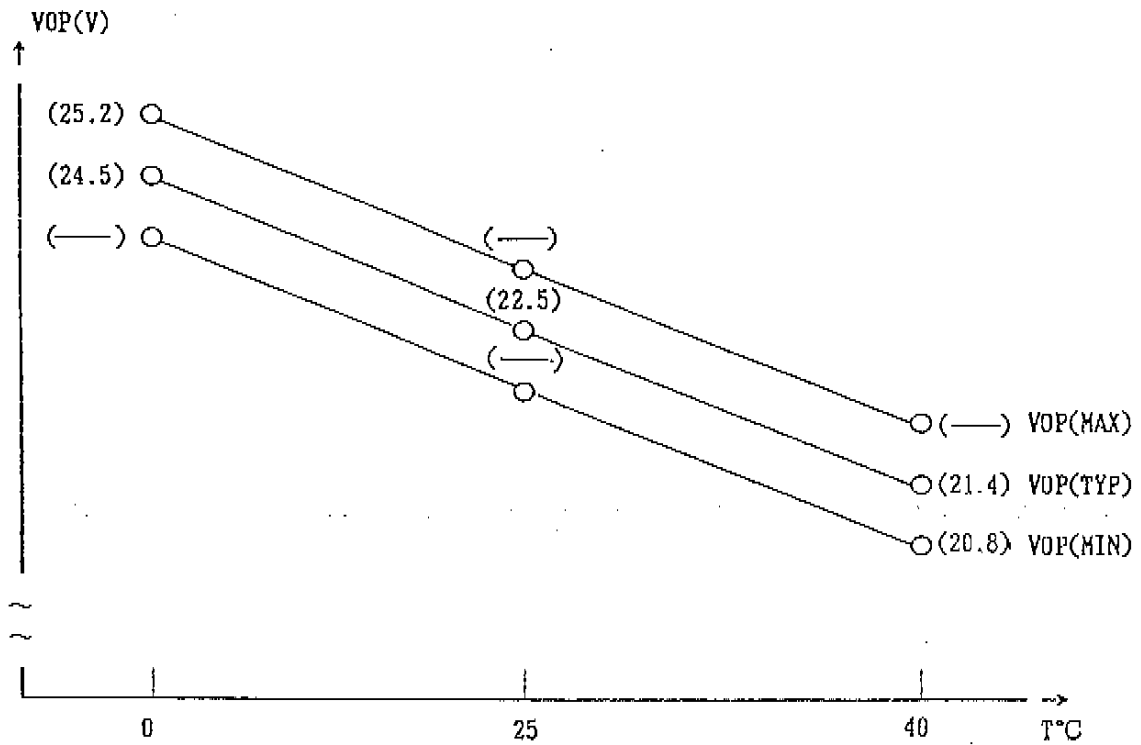
No.	Parameter	Symbol	Temperature (°C)	Standard			Unit	Remarks
				Min	Typ	Max		
1	Driving voltage (VDD-VLCD)	Vop	0	--	24.5	25.2	V	Note 1
			25	--	22.5	--		
			40	20.8	21.4	--		
2	Response time	Tr	0	--	720	1080	ms	Note 2
			25	--	260	390		
		Tf	0	--	500	750		
			25	--	120	180		
5	Recommended Viewing angle	$\theta Y1$	25	20	--	--	Degree	Note 3
		$\theta Y2$		30	--	--		
		$\theta X1$		20	--	--		
		$\theta X2$		20	--	--		
6	Contrast	K	25	--	5	--		Note 4

Note : Frame frequency is defined as follows:

Common side supply voltage

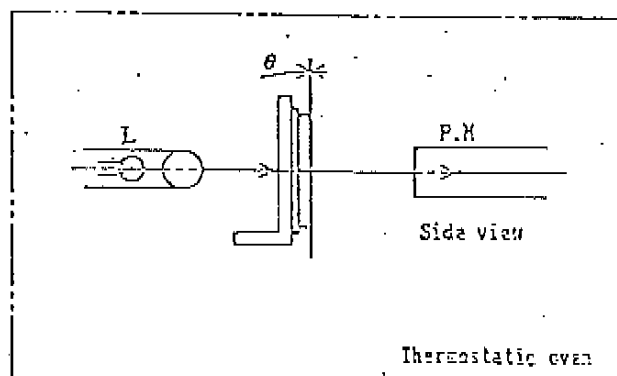
peak-to-peak/2 = 1 period

** < Vop vs. Temperature Curves >



[Note 1] Optical equipment for measurement

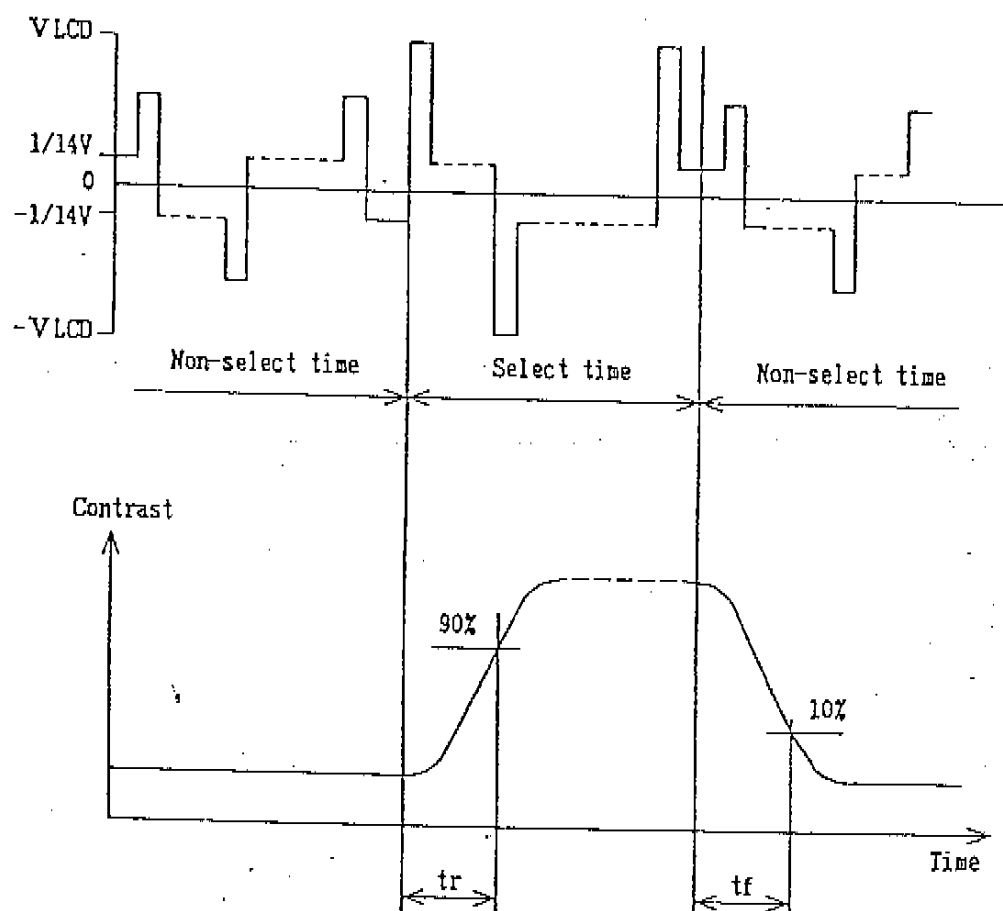
- Equipment : Canon LC-3SS brightness meter
Halogen lamp used for light source
- Conditions : Spot for brightness measurement - 0.3 mm
Spot from light source - 10 mm



- L : Light source
- P.M. : Light receiver of brightness meter

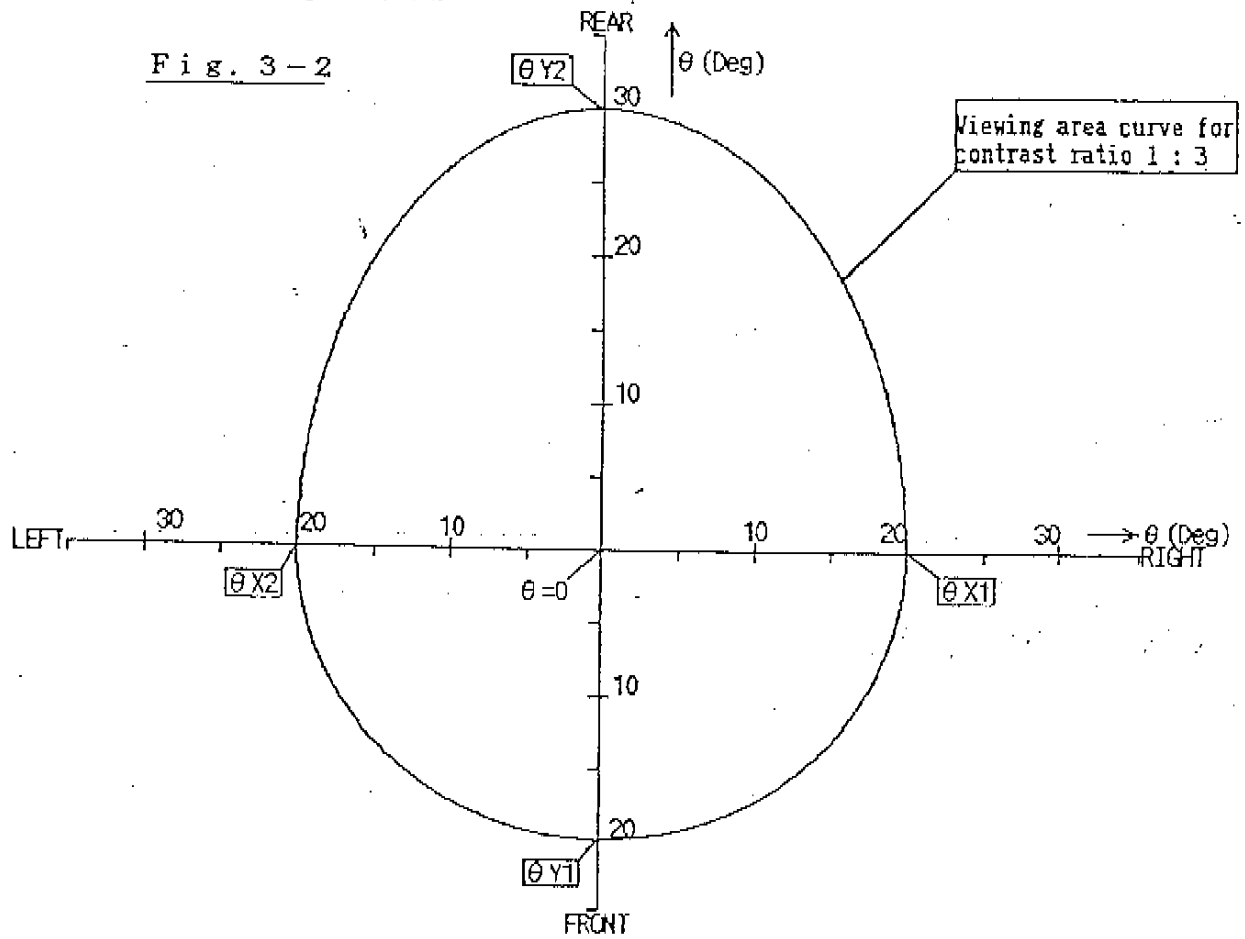
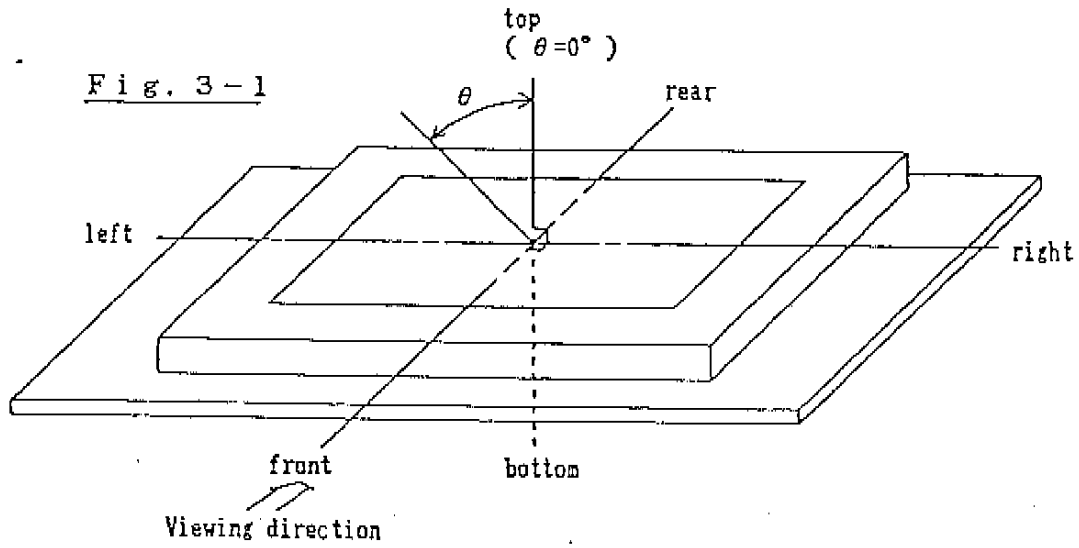
[Note 2] Definition of response time and measuring conditions

Fig. 2



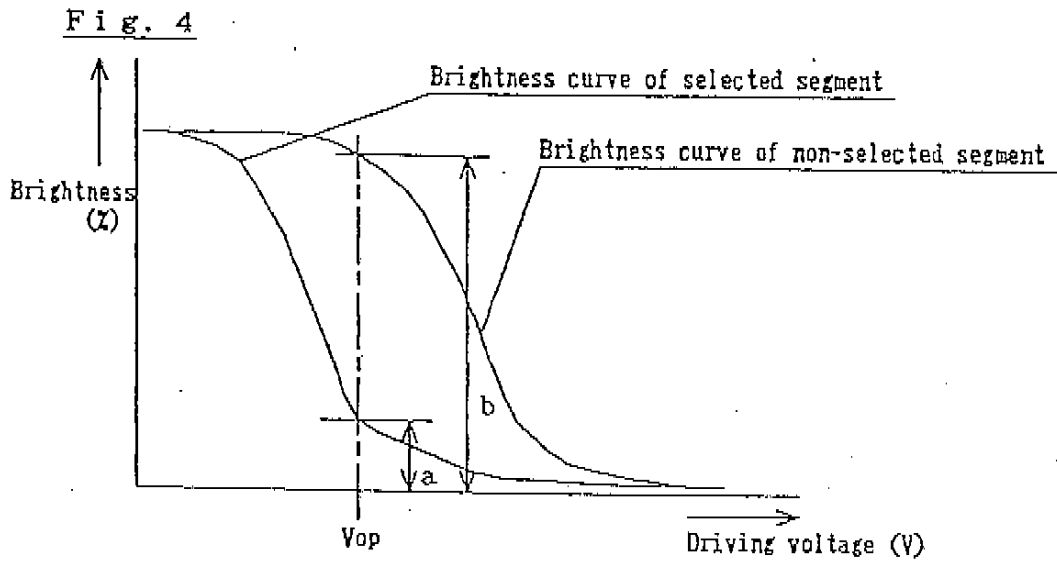
Parameter	Conditions
a) Ambient temperature	0°C , 25°C
b) Driving voltage	24.5 V, 22.5V
c) Viewing angle	0°
d) Frame frequency	70 Hz

[Note 3] Definition of viewing angle



Definition : Viewing area which gets contrast ratio 1 : 3, when operated by Vop (Typical) at 25°C .

[Note 4] Definition of contrast ratio



Definition :

$$\text{Contrast ratio} = \frac{\text{(Brightness in OFF state)}}{\text{(Brightness in ON state)}} = b/a$$

Parameter	Conditions
a) Ambient temperature	25 °C
b) Driving voltage	22.5 V
c) Viewing angle	0°

10. HANDLING PRECAUTIONS

- (1) The LCD panel of EPSON LCD modules consists of two thin glass pltets with polarizers (with UV cut filters) which easily get damaged. Extreme care should be used when handling the display panel.
- (2) When cleaning the display surface, use soft cloth (e.g., gauze) with a solvent (recommended below) and wipe lightly.

- isopropyl alcohol
- ethyl alcohol
- trichlorotrifloroethane

Do not wipe the display surface with dry or hard materials that will damage the polarizer surface.

Do not use the following solvents:

- water
- ketone
- aromatics

- (3) The LCD modules use CMOS LSI drivers, so we recommend that you:
 - a) connect any unused input terminal to VDD or VSS;
 - b) do not input any signals before power is turned on; and
 - c) ground your body, work/assembly areas, and assembly equipment to protect against static electricity.
- (4) Modules employ LCD elements, and must be treated as such. Avoid intense shock and falls from a height.
- (5) To prevent modules from degradation, do not operate or store them exposed direct to sunshine or high temperature/humidity.

11. OPERATIONAL PRECAUTIONS

- (1) If the LCD panel is driven on DC, the electrochemical reaction within it causes a rapid reduction in display performance. The duty 50%±1% of the FR signal must always be observed.
- (2) Follow the power on/off sequence shown in Fig. 1 to prevent a latch-up or DC operation of the LCD module.
- (3) No LCD module must exceed the absolute maximum ratings. If a module is operated with any value exceeding absolute maximum ratings, its performance will deteriorate and may no longer restore to normal. In designing a system using LCD modules, utmost care should be taken of ambient temperature, input voltage signal fluctuations, supply voltage fluctuations, etc.

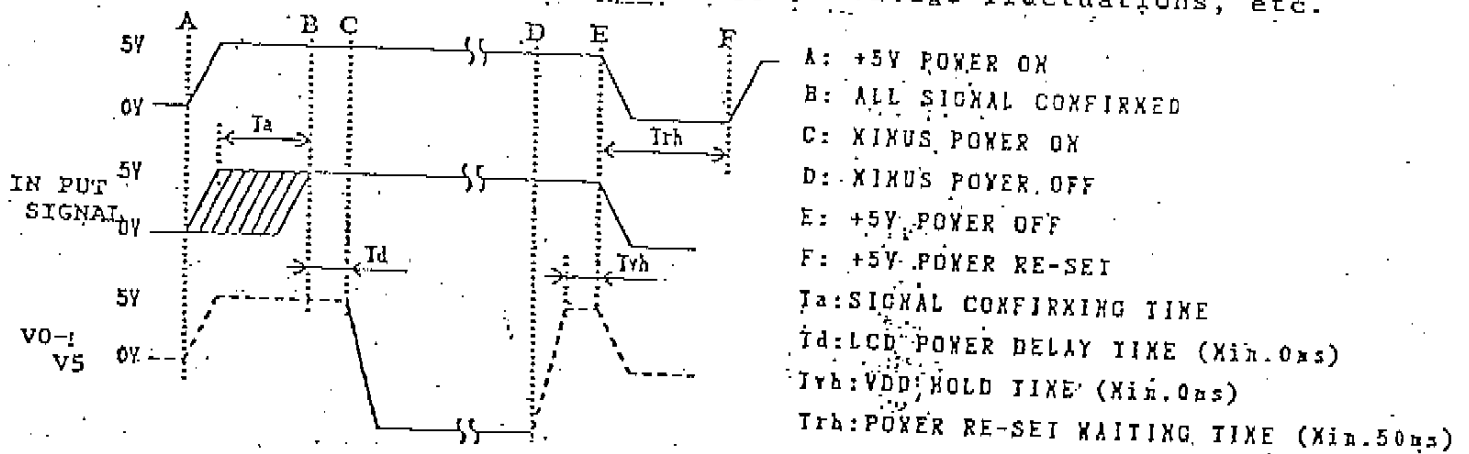


Fig. 1 Power On/Off Sequence

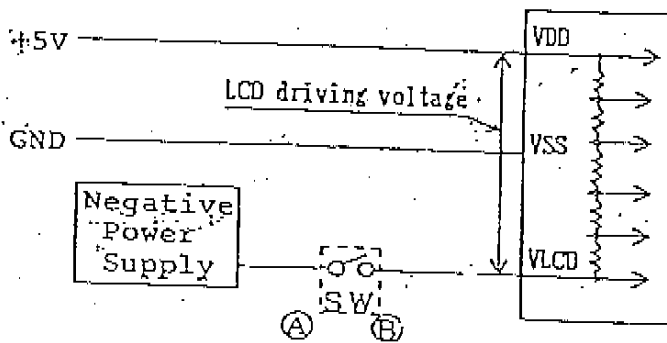


Fig. 2 Typical Power Supply Connection

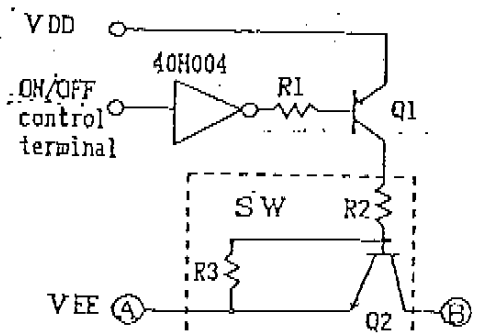


Fig. 3 Typical SW Circuit

- [Note 1] The VLCD on/off operation shown in Fig. 1 indicates the switching operation of Fig. 2.
- [Note 2] Turning off the SW (Fig. 2) will open the VLCD terminal. Therefore, the LCD driving voltage (VDD-VLCD) will become zero 100ms(Max.) later.
- [Note 3] A typical circuit for the SW portion of Fig. 2 is given in Fig. 3 for reference.

12. Backlight Specifications

12.1 Electrical Characteristics

Parameter	MIN	TYP	MAX	Unit	Condition
Tube Current	(5.0)	(6.0)	(7.0)	mA	---
Discharge Start(V)	---	---	TBD	V _{rms}	---
Tube Voltage	---	TBD	---	V _{o-p}	---
Frequency	(20)	(25)	(35)	KHz	---

Note : () shows temporary value.

* Above each value is for one tube

* This LCD Module has two tubes

12.2 Electric Optical Characteristics

Parameter	MIN	TYP	MAX	Unit	Condition
Brightness	400	---	---	cd/m ²	Tube Current(6.0 mA)
Brightness Uniformity	80	---	---	%	---

Note : - Above characteristics show the standard value on the lighting plate.

- The definition of brightness uniformity is $(MIN \div MAX) \times 100$.

12.3 Life Cycle

Parameter	MIN	TYP	MAX	Unit	Condition
Life Time	10,000	---	---	H	Tube Current(6.0 mA)

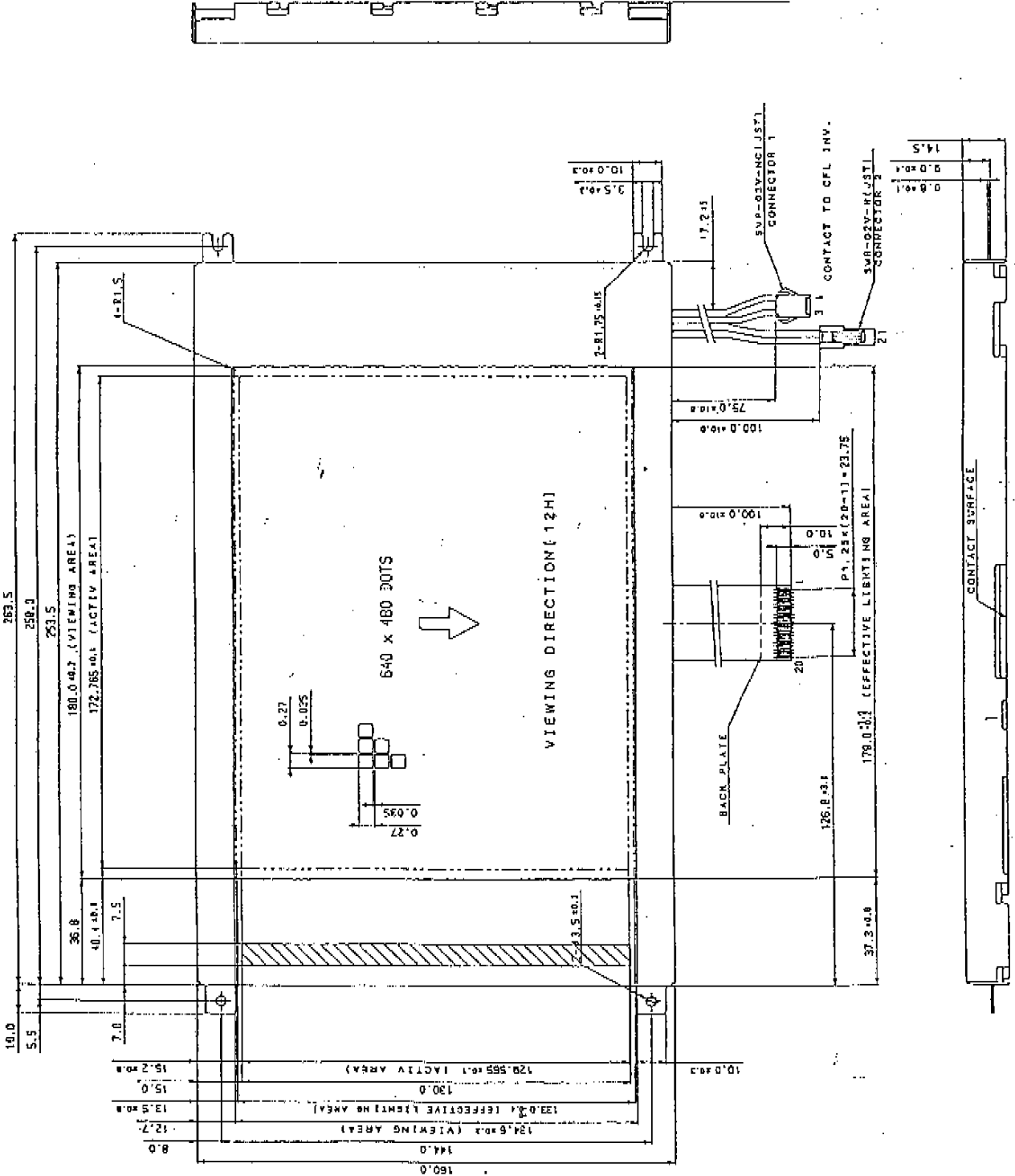
Note : Life is up to when brightness becomes 50% less than initial value

1	VDD
2	VSS
3	VCCD
4	LP
5	NC
6	NC
7	VSEL
8	EN
9	XSEL
10	NC
11	VDD0
12	VDD1
13	VDD2
14	VDD3
15	VDD
16	VDD
17	VDD
18	VDD3
19	NC
20	EO

CFL CONNECTOR 1	
1	VCL12
2	NC
3	VCL13

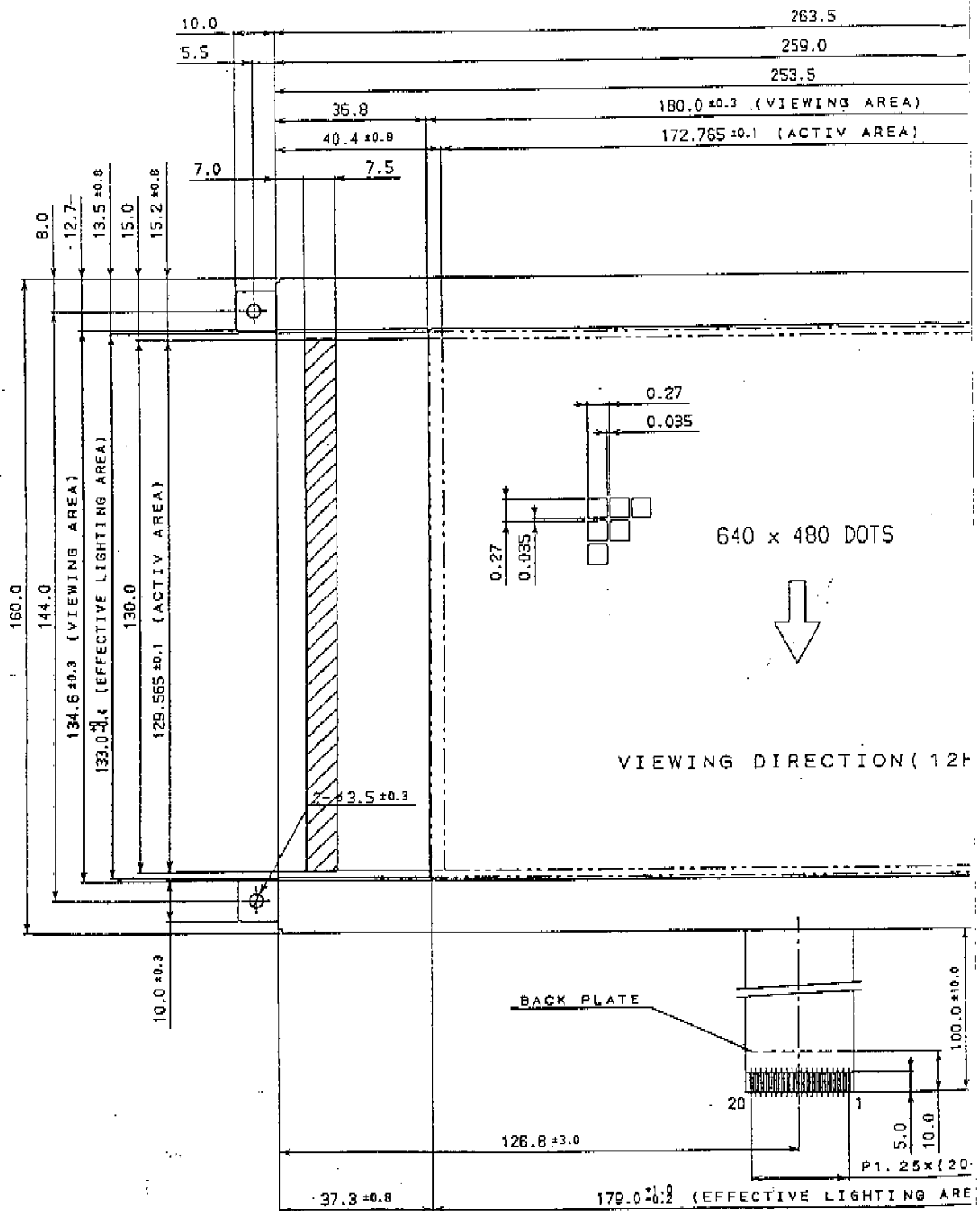
CFL CONNECTOR 2	
1	IND2
2	SWIT

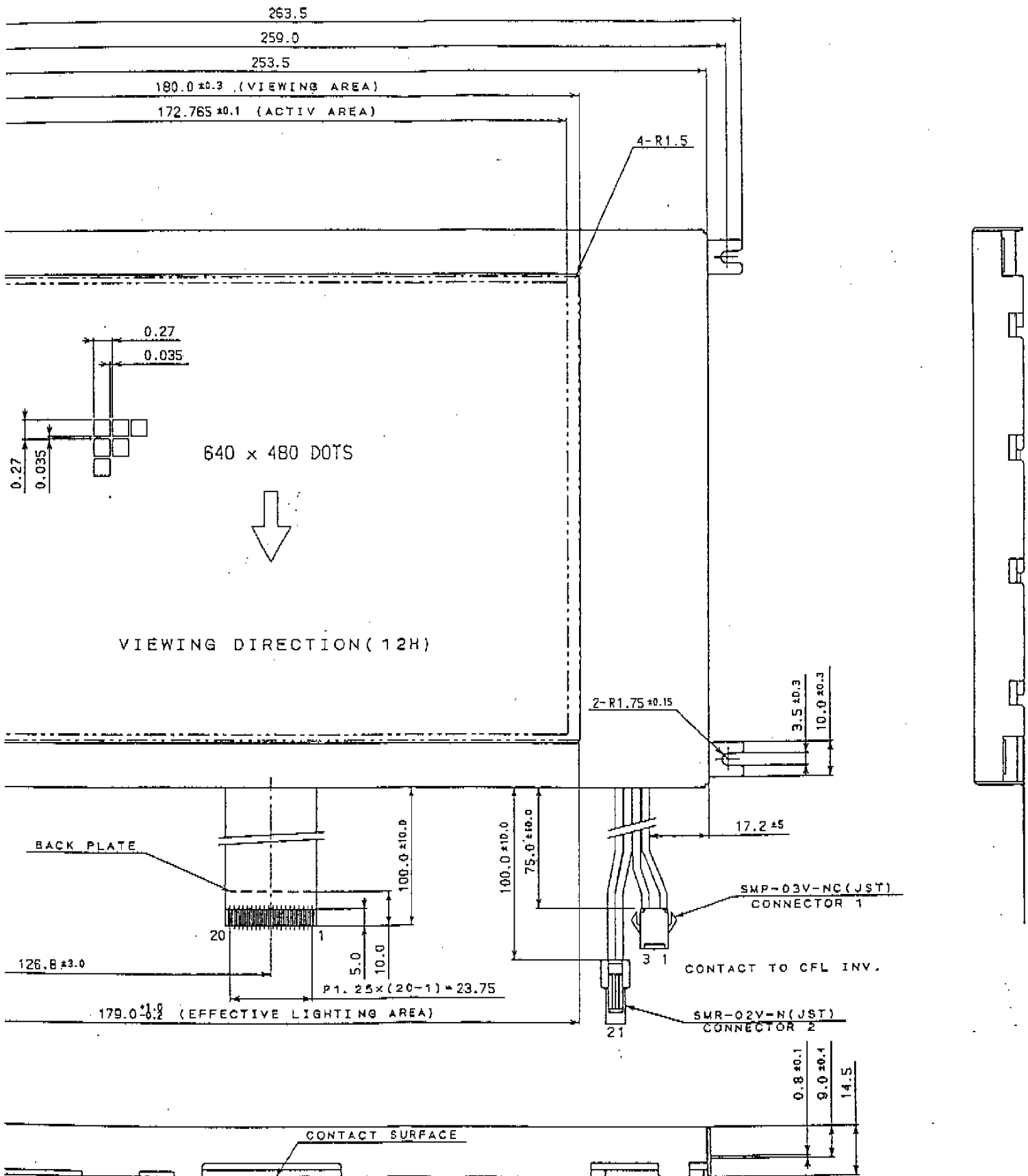
1	DATE	DATE	DATE
2	REV	REV	REV
3	REV	REV	REV
4	REV	REV	REV
5	REV	REV	REV
6	REV	REV	REV
7	REV	REV	REV
8	REV	REV	REV
9	REV	REV	REV
10	REV	REV	REV
EGS006F-NS-1			
OUTWARD DWS.			
SD-010412			
DATE CHECK DRAWN			
DATE			
11(1)			



NOTE

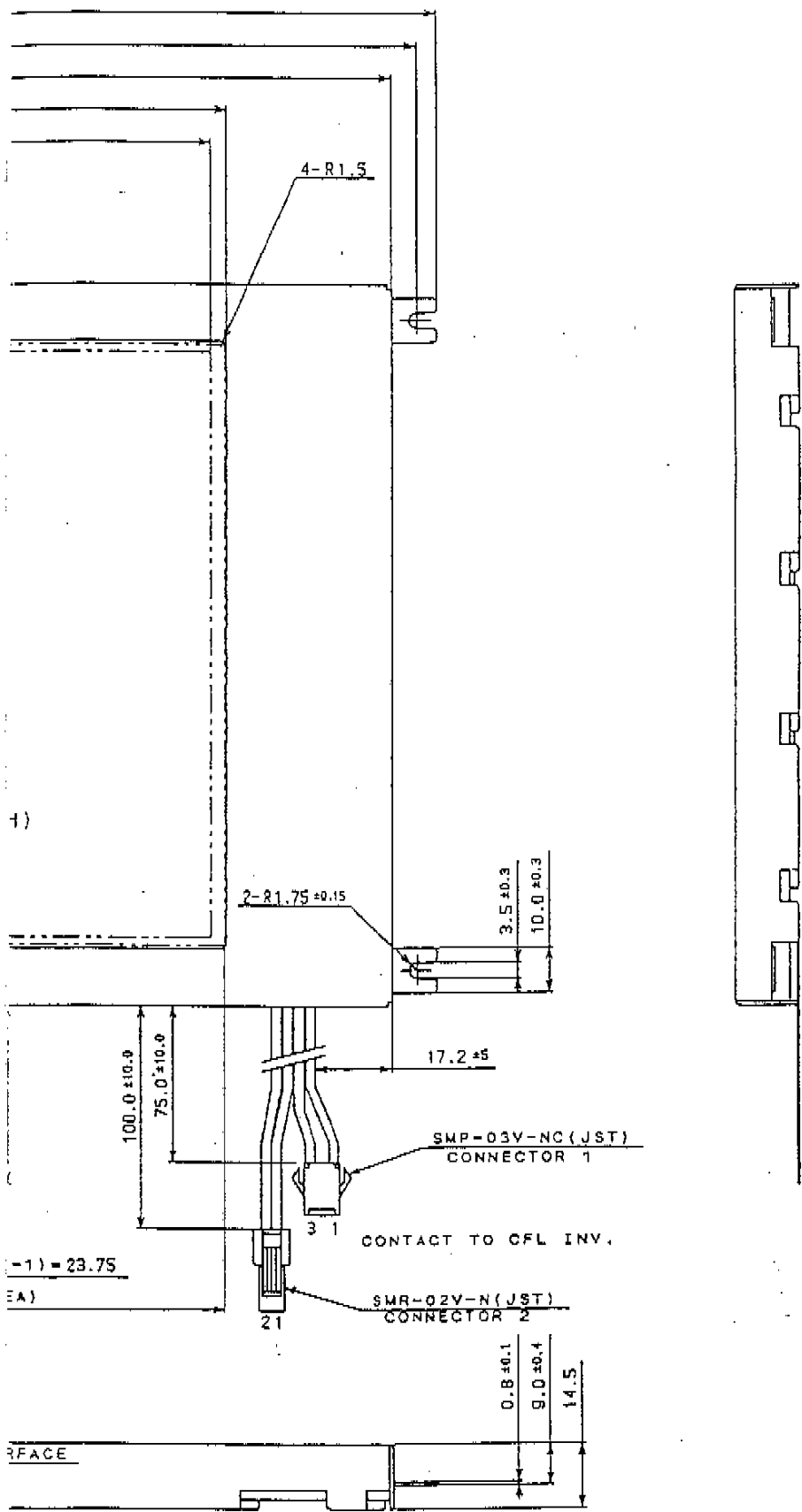
1. AREA/ELECTRIC PARTS ARE EXPOSED.





NOTE

1. AREA: ELECTRIC PARTS ARE



PIN NO.	SIGNAL
1	VDD
2	VSS
3	VLCD
4	LP
5	NC
6	NC
7	YSCL
8	DIN
9	XSCL
10	NC
11	UD0
12	UD1
13	UD2
14	UD3
15	LDO
16	LD1
17	LD2
18	LD3
19	EI
20	EO

CFL CONNECTOR 1	
PIN NO.	SIGNAL
1	VCFL2
2	NC
3	VCFL1

CFL CONNECTOR 2	
PIN NO.	SIGNAL
1	GND2
2	GND1

E	*	*	*
D	*	*	*
C	*	*	*
B	*	*	*
A	*	*	*
MODEL			
EG9006F-NS			
TITLE			
OUTWARD DWG.			
DWG NO			
SD-010412			
SCALE		TOL.	DATE
1/1	mm	±0.5	APR/ 6/ 90
MGR	CHIEF	CHECK	DRAWN
S.Yama	Kuroi		TXEDA

NOTE
 1. AREA: ELECTRIC PARTS ARE EXPOSED.