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S1D13705 Embedded Memory Color LCD Controller

Interfacing to an 8-bit Processor

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1 Introduction

This application note describes the hardware environment required to provide an interface between the S1D13705 Embedded Memory LCD Controller and a generic 8-bit microprocessor.

The designs described in this document are presented only as examples of how such interfaces might be implemented. This application note will be updated as appropriate. Please check the Epson Research and Development Website at http://www.erd.epson.com for the latest revision of this document before beginning any development.

We appreciate your comments on our documentation. Please contact us via email at documentation@erd.epson.com.

2 Interfacing to an 8-bit Processor

2.1 The Generic 8-bit Processor System Bus

Although the S1D13705 does not directly support an 8-bit CPU, with minimal external logic an 8-bit interface can be achieved.

Typically, the bus of an 8-bit microprocessor is straight forward with minimal CPU and system control signals. To connect a memory mapped device such as the S1D13705, only the write, read, and wait control signals, as well as the data and address lines, need to be interfaced. Since the S1D13705 is a 16-bit device, some external logic is required.

3 S1D13705 Bus Interface

This section is a summary of the host bus interface modes available on the S1D13705 and offers some detail on the Generic #2 Host Bus Interface used to implement the interface to an 8-bit processor.

The S1D13705 provides a 16-bit interface to the host microprocessor which may operate in one of several modes compatible with most of the popular embedded microprocessor families. The bus interface mode used in this example is:

- Generic #2 (this bus interface is ISA-like and can easily be modified to support an 8-bit CPU).

3.1 Host Bus Pin Connection

The following table shows the functions of each host bus interface signal.

Table 3-1: Host Bus Interface Pin Mapping

S1D13705 Pin Names	Generic #2	Description
AB[16:1]	A[16:1]	Address [16:1]
AB0	A0	Address A0
DB[15:0]	D[15:0]	Data
WE1#	BHE#	Byte High Enable
CS#	External Decode	Chip Select
BCLK	BCLK	Bus Clock
BS#	n/c	Must be tied to IO V_{DD}
RD/WR#	n/c	Must be tied to IO V_{DD}
RD#	RD#	Read
WE0#	WE#	Write
WAIT#	WAIT#	
RESET#	RESET#	

Note
If the CPU does not have address A16 all 80K Bytes of embedded memory will not be accessible.

For details on configuration, refer to the *S1D13705 Hardware Functional Specification*, document number X27A-A-001-xx.

3.2 Generic #2 Interface Mode

Generic #2 Host Bus Interface is a general, non-processor specific interface mode on the S1D13705 that is ideally suited to interface to an 8-bit processor bus.

The interface requires the following signals:

- BUSCLK is a clock input which synchronizes transfers between the host CPU and the S1D13705. It is separate from the input clock (CLKI) and is typically driven by the host CPU system clock. If the host CPU bus does not provide this clock, an asynchronous clock can be provided.
- The address inputs AB0 through AB16, and the data bus DB0 through DB15, connect directly to the CPU address and data bus, respectively.

Note
In an 8-bit environment D[7:0] must also be connected to DB[15:8] respectively (i.e. D7 connects to both DB15 and DB7, D6 connects to both DB14 and DB6, D5 connects to both DB13 and DB5, etc.). See Figure 4-1: "Typical Implementation of an 8-bit Processor to the S1D13705 Generic #2 Interface" .

- Chip Select (CS#) is driven by decoding the high-order address lines to select the proper memory address space.
- BHE# (WE1#) is the high byte enable for both read and write cycles.

Note
In an 8-bit environment, this signal is driven by inverting address line A0 thus indicating that odd addresses are to be R/W on the high byte of the data bus.

- WE0# is the enable signal for a write access, to be driven low when the host CPU is writing the 1375 memory or registers.
- RD# is the read enable for the S1D13705, to be driven low when the host CPU is reading data from the S1D13705.
- WAIT# is a signal which is output from the S1D13705 to the host CPU that indicates when data is ready (read cycle) or accepted (write cycle) on the host bus. Since host CPU accesses to the S1D13705 may occur asynchronously to the display update, it is possible that contention may occur in accessing the 1375 internal registers and/or refresh memory. The WAIT# line resolves these contentions by forcing the host to wait until the resource arbitration is complete. This signal is active low and may need to be inverted if the host CPU wait state signal is active high.
- The Bus Status (BS#) and Read/Write (RD/WR#) signals are not used in the bus interface for Generic #2 mode. However, BS# is used to configure the S1D13705 for Generic #2 mode and should be tied high (connected to IO V_{DD}). RD/WR# should also be tied high.

4 8-Bit Processor to S1D13705 Interface

4.1 Hardware Description

The interface between the S1D13705 and an 8-bit processor requires minimal glue logic. A decoder is used to generate the chip select for the S1D13705 based on where the S1D13705 is mapped into memory. Alternatively, if the processor supports a chip select module, it can be programmed to generate a chip select for the S1D13705 without the need of an address decoder.

An inverter inverts A0 to generate the Byte High Enable signal for the S1D13705. If the 8-bit host interface has an active high WAIT signal, it must be inverted as well.

In order to support an 8-bit microprocessor with a 16-bit peripheral, the low and high order bytes of the data bus must be connected together. The following diagram shows a typical implementation of an 8-bit processor interfaced to the S1D13705.

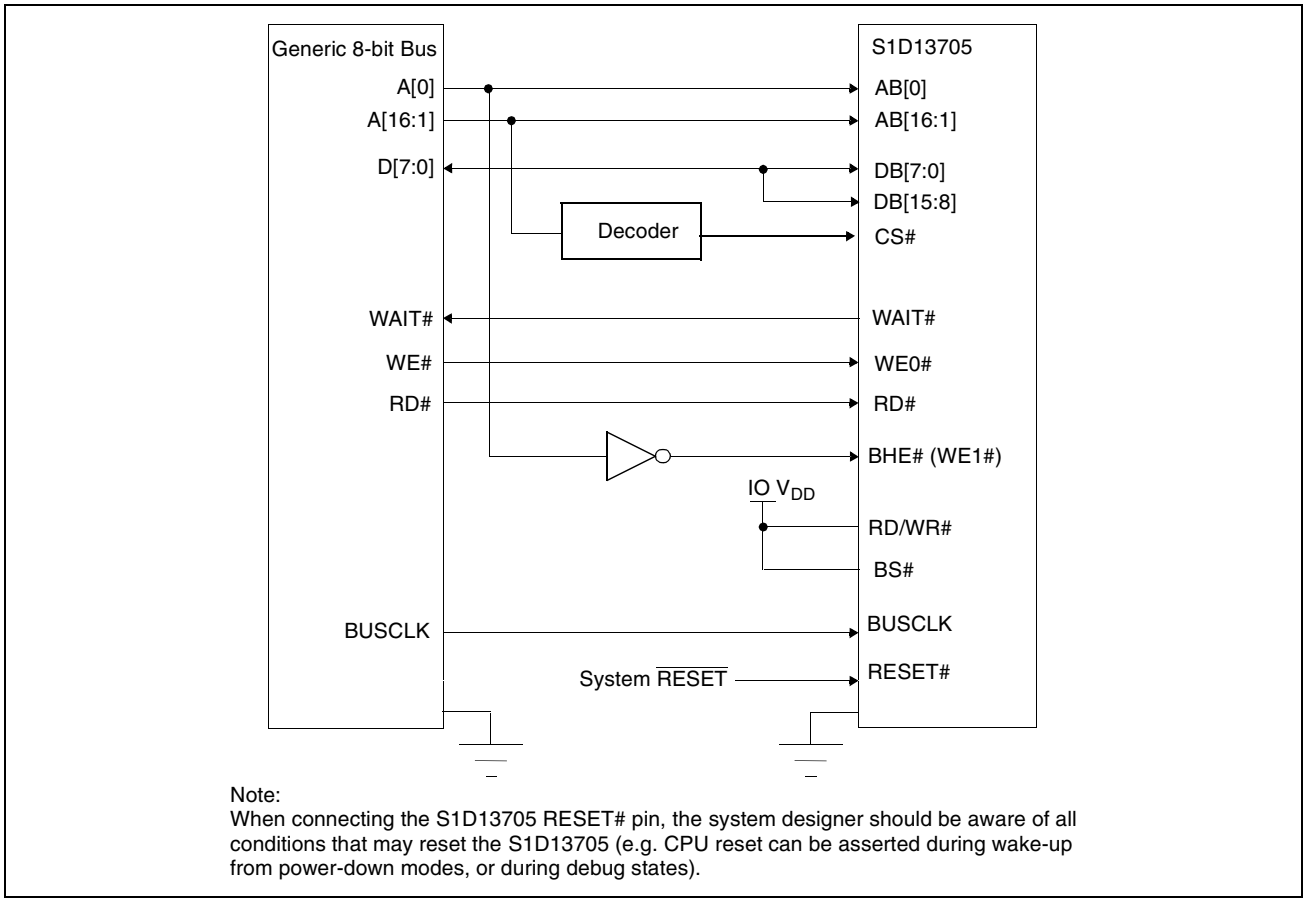

Figure 4-1: Typical Implementation of an 8-bit Processor to the S1D13705 Generic #2 Interface

4.2 S1D13705 Hardware Configuration

The S1D13705 uses CNF4 through CNF0 and BS# to allow selection of the bus mode and other configuration data on the rising edge of RESET#. Refer to the *S1D13705 Hardware Functional Specification*, document number X27A-A-001-xx for details.

The tables below show only those configuration settings important to the 8-bit processor interface. The endian must be selected based on the 8-bit processor used.

Table 4-1: Configuration Settings

Signal	Low	High
CNF0	See “Host Bus Selection” table below	See “Host Bus Selection” table below
CNF1		
CNF2		
CNF3	Little Endian	Big Endian
CNF4	Active low LCDPWR signal	Active high LCDPWR signal

= configuration for 8-bit processor host bus interface

Table 4-2: Host Bus Selection

CNF2	CNF1	CNF0	BS#	Host Bus Interface
1	1	1	1	Generic #2, 16-bit

= required configuration for this application.

4.3 Register/Memory Mapping

The S1D13705 needs a 128K byte block of memory to accommodate its 80K byte display buffer and its 32 byte register set. The starting memory address is located at 00000h of the 128K byte memory block while the internal registers are located in the upper 32 bytes of this memory block. (i.e. REG[0]= 1FFE0h).

An external decoder can be used to decode the address lines and generate a chip select for the S1D13705 whenever the selected 128K byte memory block is accessed. If the processor supports a general chip select module, its internal registers can be programmed to generate a chip select for the S1D13705 whenever the S1D13705 memory block is accessed.

5 Software

Test utilities and display drivers are available for the S1D13705. Full source code is available for both the test utilities and the drivers.

The test utilities are configurable for different panel types using a program called 13705CFG. The display drivers can be customized by the OEM for different panel types, resolutions and color depths only by modifying the source.

The S1D13705 test utilities and display drivers are available from your sales support contact or on the internet at http://www.erd.epson.com.

6 References

6.1 Documents

- Epson Research and Development, Inc., *S1D13705 Embedded Memory LCD Controller Hardware Functional Specification*; Document Number X27A-A-002-xx.
- Epson Research and Development, Inc., *S5U13705B00C Rev. 1.0 ISA Bus Evaluation Board User Manual;* Document Number X26A-G-005-xx.
- Epson Research and Development, Inc., *S1D13705 Programming Notes and Examples*; Document Number X26A-G-002-xx.

6.2 Document Sources

- Epson Reasearch and Development Website: http://www.eea.epson.com.

7 Technical Support

7.1 Epson LCD/CRT Controllers (S1D13705)

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