Technical Note

Differences between Standard Z8S180 and SL1960 Revision

TN005301-0506

Introduction

In 1997, a new revision of the 8S180 with an upgraded Z180 core was released. The latest revision has many benefits over the original version. However, there are some errata (listed at the end of this document) related to this latest revision that for some particular designs may be difficult to work around. For this reason, the original revision, SL1960, is still being offered.

The product specifications for both revisions are available for download at ZiLOG website (www.zilog.com). The different designations used for the two revisions are given below.

Original Revision	Latest Revision
SL1960	8S180 (no SL) - Date Codes of 9818 or later
Revision K	Revision N
8S180 - Date codes prior to 9818	SL1919 (used from 1997 to mid-1998)

The original revision, SL1960, is the first static Z8S180. It offers only the static capability and none of the peripheral upgrades found in the latest revision are added. Speed up to 20 MHz is offered to this revision.

The latest revision is the latest Z180 CPU core. This is the core used, not only in superintegrated parts such as the 80182 and 80185, but also in ASIC designs. This is ZiLOG's preferred core. Speed up to 33 MHz is offered for this revision.

This core offers all the functionality of the previous revisions, and also provides several new features that allow for greater performance.

Features	Benefits
Enhanced UART's	Up to 512 Kbps @ 33 MHz
Chain-linked DMA Channels	Less CPU Intervention
X2 CLOCK MULTIPLIER Mode	Use Slower, Less Expensive Crystals
LOW POWER SLEEP Mode	Low Power Consumption
Low Noise Crystal Option	Reduce Oscillator Drive to 30%
PHI Output Disable	Reduce EMI
Low Voltage Support	3.3 V @ 20 MHz for Portable Applications

The following section describes the additional features of the standard revision.

- Enhanced UART (up to 512 Kbps @ 33 MHz)

  The two UART channels in the S180 have been enhanced from the original S180 core. The addition of a 16-bit down counter that divides the processor clock by the value in a 16-bit time constant register (identical to the BRG in the SCC/ESCC) allows for programmability of up to 512 Kbps @ 33 MHz. In addition, a 4-byte receive FIFO has been added to buffer incoming data and reduce the chance of overrun errors.

- Chain-Linked DMA Channels

  The two DMS channels in the S180 now have capability to link both DMA channels to allow non-stop DMA data transfer, when the DMA's are programmed to take their request from the same peripheral device. This provides increased system performance with less CPU intervention.

- X2 CLOCK MULTIPLIER Mode

  When X2 CLOCK MULTIPLIER mode enabled, doubles the internal clock from that of the external clock effectively for a crystal frequency range of 10–6 MHz. This allows use of less expensive crystals resulting in a system level cost saving.

  Note that if an oscillator is used in power down modes such as standby, it will consume power (the specification for the oscillator is *input current*). Instead of using an oscillator, a crystal with the X2 clock multiplier feature can be used. The crystal will not consume any power, thereby saving power.

- LOW POWER SLEEP Mode

  Z8S180 not only consumes less power during normal operation than previous revisions; it has also been designed with three modes to further reduce the power consumption.

  - ZiLOG reduced ICC power consumption during STANDBY mode to a minimum of 10 μA by stopping the external crystal oscillators and internal clock.
  - The SLEEP mode reduces power consumption by placing the CPU in Stopped state, thereby consuming less current while the on-chip I/O device is operating.
  - The SYSTEM STOP mode places both the CPU and the on-chip peripheral in STOPPED mode, thereby reducing the power consumption even further.

- Low Noise Crystal Option

  This feature, when enabled, will select a low-noise option for the EXTAL and XTAL pins of the Z180. This option reduces the gain, in addition to reducing the output drive capability to 30% of its original drive capability. The low-noise crystal option is recommended for application where the crystal may be driven too hard by the oscillator.

- PHI Output Disable

  When this bit is set, the PHI output is not driven by the system clock. Rather, the PHI output will be forced to a High state. On production boards that do not use the PHI output, this feature can be used to reduce EMI.

- Low Voltage Support

  The Z8S180 device will be capable of supporting low-voltage at 3.3 V with a maximum frequency of 20 MHz. This is designated as the 8L180.

Z8S180 ERRATA

The following lists the problems and workarounds for the standard revision.

1. Precaution

When Transmit Enable is set to 0 (bit 4 of CSIO Control register), the Txs pin is High. The Txs pin is High even before the transmit starts and returns High on the rising CKS edge after the 8th bit has been transmitted. This may become an issue if the last bit sent is a 0, and the data is being sampled on the rising edge of the CKS clock because an incorrect High state may be sampled rather than the actual correct 8th bit.

Workaround

With little timing margin for sampling the 8th bit correctly, a 200 pF capacitor on TXS->RXS may be useful in rectifying this problem.

2. Precaution

When CTSLE of the STAT1 register is set (bit 2 of Reg 05H), bit 5 of the CNTLB1 register (Reg 03H) should reflect the state of the multiplexed RXS/CTS1 pin. Bit 5 in the CNTLB1 always reads 0.

3. Precaution

In the original revision SL1960, when an overrun error occurs, the microprocessor would set the OVRN error (bit 6 of the STAT0 or STAT1), but continue to send data in the FIFO (ASCI would resume receiving data).

For the latest revision, the ASCI's do not place any further received characters in the RX FIFO, until the software writes 0 to the ERF bit in the CNTRLA register.

Workaround

Reset, the Error Flag Reset (bit 3 of CNTLA0 or CNTLA1).

4. Precaution

Input pin and I/O pins include weak latch circuits to prevent excessive current draw by the receiver, if the pin is not externally driven. External pull-up or pull-down resistors should not be less than 15 KOhms to ensure that the resistors can control the state of the latch when power is supplied.

This publication is subject to replacement by a later edition. To determine whether a later edition exists, or to request copies of publications, contact:

ZiLOG Worldwide Headquarters
532 Race Street
San Jose, CA 95126
Telephone: 408.558.8500
Fax: 408.558.8300
www.zilog.com

Information Integrity

The information contained within this document has been verified according to the general principles of electrical and mechanical engineering. Any applicable source code illustrated in the document was either written by an authorized ZiLOG employee or licensed consultant. Permission to use these codes in any form, besides the intended application, must be approved through a license agreement between both parties. ZiLOG will not be responsible for any code(s) used beyond the intended application. Contact the local ZiLOG Sales Office to obtain necessary license agreements.

Document Disclaimer