Table 31: Timer/Counter Mode register (TMOD - address 89h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	T1GATE	T1C/$\overline{T}$	T1M1	T1M0	T0GATE	T0C/$\overline{T}$	T0M1	T0M0
Reset	0	0	0	0	0	0	0	0

Table 32: Timer/Counter Mode register (TMOD - address 89h) bit description

Bit	Symbol	Description
0	T0M0	Mode Select for Timer 0. These bits are used with the T0M2 bit in the TAMOD register to determine the Timer 0 mode (see Table 34).
1	T0M1	
2	T0C/$\overline{T}$	Timer or Counter selector for Timer 0. Cleared for Timer operation (input from CCLK). Set for Counter operation (input from T0 input pin).
3	T0GATE	Gating control for Timer 0. When set, Timer/Counter is enabled only while the $\overline{INT0}$ pin is HIGH and the TR0 control pin is set. When cleared, Timer 0 is enabled when the TR0 control bit is set.
4	T1M0	Mode Select for Timer 1. These bits are used with the T1M2 bit in the TAMOD register to determine the Timer 1 mode (see Table 34).
5	T1M1	
6	T1C/$\overline{T}$	Timer or Counter Selector for Timer 1. Cleared for Timer operation (input from CCLK). Set for Counter operation (input from T1 input pin).
7	T1GATE	Gating control for Timer 1. When set, Timer/Counter is enabled only while the $\overline{INT1}$ pin is HIGH and the TR1 control pin is set. When cleared, Timer 1 is enabled when the TR1 control bit is set.

Table 33: Timer/Counter Auxiliary Mode register (TAMOD - address 8Fh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	--	-	-	T1M2	-	-	-	T0M2
Reset	x	x	x	0	x	x	x	0

Table 34: Timer/Counter Auxiliary Mode register (TAMOD - address 8Fh) bit description

Bit	Symbol	Description
0	T0M2	Mode Select for Timer 0. These bits are used with the T0M2 bit in the TAMOD register to determine the Timer 0 mode (see Table 34).
1:3	-	reserved
4	T1M2	Mode Select for Timer 1. These bits are used with the T1M2 bit in the TAMOD register to determine the Timer 1 mode (see Table 34).
		The following timer modes are selected by timer mode bits TnM[2:0]: **000** — 8048 Timer 'TLn' serves as 5-bit prescaler. (Mode 0). **001** — 16-bit Timer/Counter 'THn' and 'TLn' are cascaded; there is no prescaler.(Mode 1). **010** — 8-bit auto-reload Timer/Counter. THn holds a value which is loaded into TLn when it overflows. (Mode 2). **011** — Timer 0 is a dual 8-bit Timer/Counter in this mode. TL0 is an 8-bit Timer/Counter controlled by the standard Timer 0 control bits. TH0 is an 8-bit timer only, controlled by the Timer 1 control bits (see text). Timer 1 in this mode is stopped. (Mode 3). **100** — Reserved. User must not configure to this mode. **101** — Reserved. User must not configure to this mode. **110** — PWM mode (see Section 8.5). **111** — Reserved. User must not configure to this mode.
5:7	-	reserved

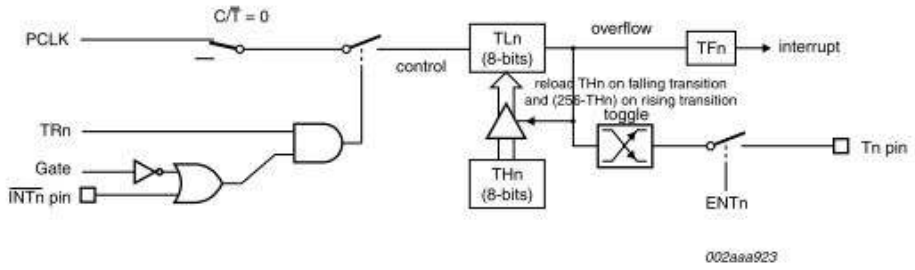

Fig 17. Timer/counter 0 or 1 in mode 6 (PWM auto-reload).

8.5 Mode 6

In this mode, the corresponding timer can be changed to a PWM with a full period of 256 timer clocks (see Figure 17). Its structure is similar to mode 2, except that:

- TFn (n = 0 and 1 for Timers 0 and 1 respectively) is set and cleared in hardware
- The LOW period of the TFn is in THn, and should be between 1 and 254, and
- The HIGH period of the TFn is always 256 – THn
- Loading THn with 00h will force the TX pin HIGH, loading THn with FFh will force the TX pin LOW

Note that interrupt can still be enabled on the LOW to HIGH transition of TFn, and that TFn can still be cleared in software like in any other modes.

Table 35: Timer/Counter Control register (TCON) - address 88h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
Reset	0	0	0	0	0	0	0	0

Table 36: Timer/Counter Control register (TCON - address 88h) bit description

Bit	Symbol	Description
0	IT0	Interrupt 0 Type control bit. Set/cleared by software to specify falling edge/LOW level triggered external interrupts.
1	IE0	Interrupt 0 Edge flag. Set by hardware when external interrupt 0 edge is detected. Cleared by hardware when the interrupt is processed, or by software.
2	IT1	Interrupt 1 Type control bit. Set/cleared by software to specify falling edge/LOW level triggered external interrupts.

Table 36: Timer/Counter Control register (TCON - address 88h) bit description

Bit	Symbol	Description
3	IE1	Interrupt 1 Edge flag. Set by hardware when external interrupt 1 edge is detected. Cleared by hardware when the interrupt is processed, or by software.
4	TR0	Timer 0 Run control bit. Set/cleared by software to turn Timer/Counter 0 on/off.
5	TF0	Timer 0 overflow flag. Set by hardware on Timer/Counter overflow. Cleared by hardware when the processor vectors to the interrupt routine, or by software. (except in mode 6, where it is cleared in hardware)
6	TR1	Timer 1 Run control bit. Set/cleared by software to turn Timer/Counter 1 on/off
7	TF1	Timer 1 overflow flag. Set by hardware on Timer/Counter overflow. Cleared by hardware when the interrupt is processed, or by software (except in mode 6, see above, when it is cleared in hardware).