Keywords: VCXO, MPEG2 CLK, AC-3 CLK, Audio DAC CLK, Jitter, Pulling range, MAX9485, STB CLK, DTV CLK

APPLICATION NOTE 2097

Using a VCXO (Voltage-Controlled Crystal Oscillator) as a Clock (CLK) Generator

Aug 24, 2004

Abstract: A VCXO (voltage controlled crystal oscillator) is an oscillator whose frequency is determined by a crystal, but can be adjusted by a small amount by changing a control voltage. VCXO clock (CLK) generators have been used in various applications, such as digital TV, digital audio, ADSL, and STB. This application note provides the general structure for a VCXO CLK generator, key performance measurements, guidelines for PCB design, and a test setup for MAX9485, a VCXO CLK Gen chip for MPEG2 and AC-3 audio applications.

Structure and Application of a VCXO CLK Generator

A VCXO, or voltage controlled crystal oscillator, oscillates with a frequency determined by a crystal, but which can be adjusted over a narrow range by a control voltage, usually in the range of 0V–2V or 0V–3V. The tuning range of the VCXO is about ±100ppm to ±200ppm. **Figure 1** shows the structure of a typical VCXO CLK generator and the crystal's circuit model.

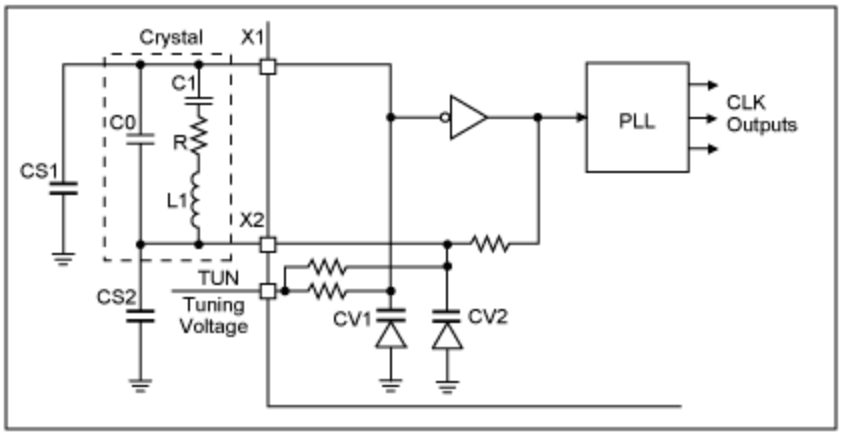

Figure 1. Block diagram of a typical VCXO CLK generator.

As the capacitance of the varactors CV1 and CV2 changes, the crystal's model is affected and the oscillation frequency changes. The two shunt external shunt capacitors CS1 and CS2 are used to adjust the tuning range and offset the center frequency. Mathematically, according to the crystal circuit in Figure 1, the resonating frequency of the crystal can be expressed as

$$f_C = \frac{1}{2\pi\sqrt{L_1 C_1}}\sqrt{1+\frac{C_1}{C_0+C_L}}$$

where C_L is the equivalent load capacitor that is a lumped sum from CV1, 2 and CS1, 2. More precisely, C_L = (CV1 + CS1) || (CV2 + CS2). Taking the first order approximation and considering the fact that $C_1 << C_0$ and C_L, we can obtain the frequency incremental around f_C:

$$\Delta f_C = \frac{-C_1}{4\pi\sqrt{L_1 C_1}(C_0+C_L)^2}\Delta C_L$$

Figure 2 shows a typical plot of f_C in terms of the value of CS1, where CS1 = CS2.

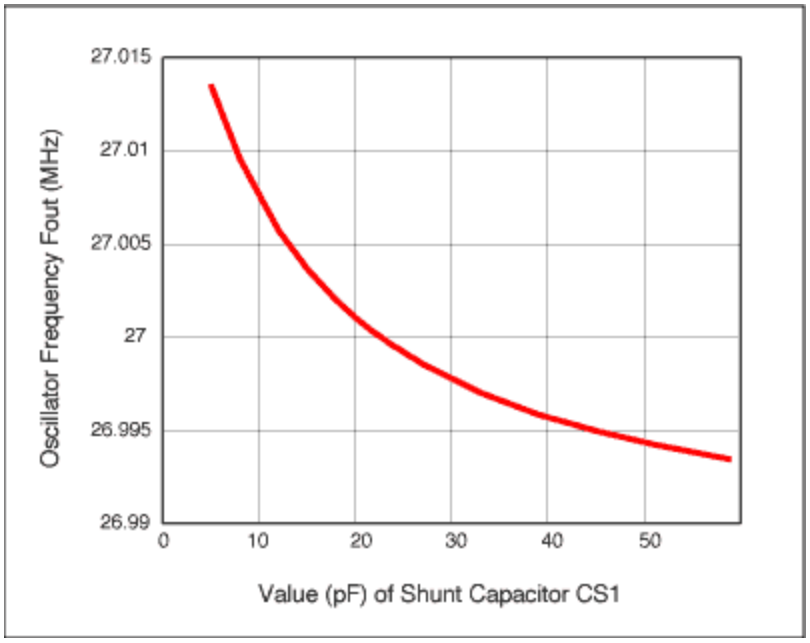

Figure 2. VCXO frequency vs. shunt capacitor CS1 (CS1 = CS2).

Using this micro-tuning feature, one usually combines a VCXO and PLL together to create CLK generators with micro-tuning.

VCXO CLK generators have been used in various applications, such as digital TV, digital audio, ADSL, and STB. Maxim's MAX9485 is such a CLK generator chip, designed for MPEG-2 and Dolby Digital audio (AC-3) applications [1]. It can provide almost all the frequencies used for audio digital to analog converters. It supports sampling frequencies from 12kHz up to 96kHz. Maxim is also developing VCXO CLK generators for other applications.

The Key Parameters of a VCXO CLK Generator

There are many parameters to characterize a VCXO CLK generator. The Most important ones are the tuning voltage range, center frequency, pulling (tuning) range, and the jitter of output CLK.

The tuning voltage range is the variation range of the VCXO control voltage. This voltage controls the varactor's capacitance. Usually it is in the range of 0V–2V or 3V. The center frequency is the frequency

in the middle of the VCXO's output frequency range. The pulling range is the ratio of the up (or down) frequency variation to the center frequency. This ratio is usually represented in ppm (part per million). This measurement provides the relative pulling range of VCXO. Normally, the pulling range is about 100ppm–200ppm, depending on the structure of VCXO and the selected crystal.

CLK jitter is the key measurement of a CLK generator. There are several jitter definitions. The two most often-used jitter measurements are called "period" jitter and "cycle-to-cycle" jitter. We will discuss more on them in Section 4. The jitter depends on the structure of CLK generator and it varies from chip to chip and the jitter requirement to a CLK generator is also varying from application to application.

Crystal Selection and Board Design

The quality and characteristics of a VCXO CLK generator can be affected by the selection of crystals and the PCB layout. In selection of crystal, beside the frequency, package, accuracy, and operation temperature range, for a VCXO application, users must pay attention on the equivalent series resistance and loading capacitance. The series resistance provides a power consumption measure of the crystal. The less the resistance value is, the easier the oscillator starts up. The loading capacitance is an important parameter for a crystal. First of all, it determines the resonating frequency of the crystal. Normally, the marked frequency of a crystal implies the resonating frequency of the crystal after connected the specified loading capacitance in parallel with it. It should be pointed out that this marked frequency is equal to the value obtained from Equation (1) when C_L equals to the specified load capacitance, but this is not the value from $1/(2\pi\sqrt{L_1C_1})$. Therefore, it is clear that the tuning range of a VCXO is closely related to the value of C_L. For a small value of load capacitance, the VCXO tuning range is limited in upper side; likewise a large value of the capacitance reduces the tuning range in lower side. The right value of loading capacitance to use is depending on the character of the VCXO. For instance, in MAX9485 design to balance the tuning range, the center of the tuning curve, and the ease of board design, we have chosen a 27MHz crystal with a 14pf load capacitance from Ecliptek (ECX-5527-27) [2]. With such a crystal, MAX9485 can provide a puling range of ±200ppm, see **Figure 3**. It should be mentioned that the pulling range of a crystal also varies with the package. Usually, a metal canned package has larger pulling range than surface mounted device (SMD). However, recently DAISHINKU Corp [5] has made a new SMD crystal that can provide a similar pulling range as a metal canned crystal. We have tested the SMD crystal (DSX530GA) and found out that the tuning range is about ±200ppm with two 4pf shunt capacitors, see **Figure 4**.

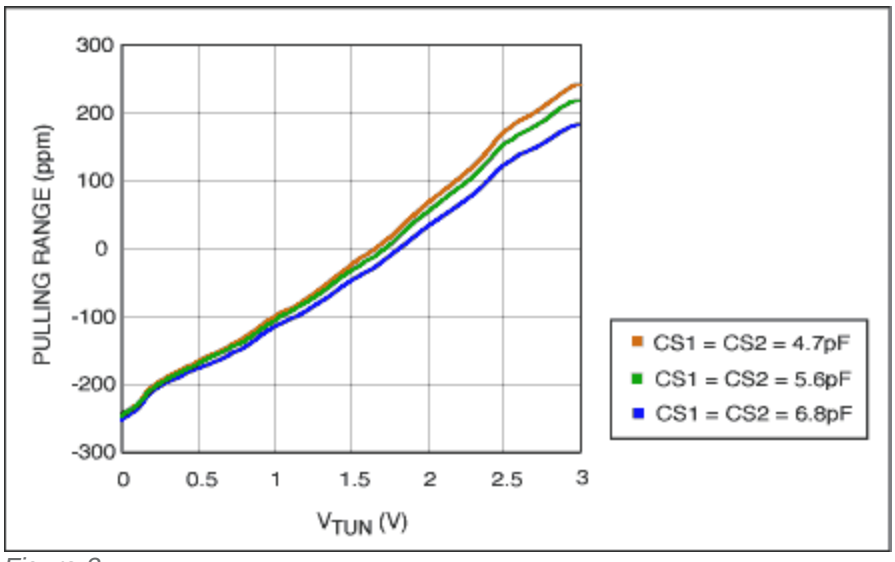

Figure 3.

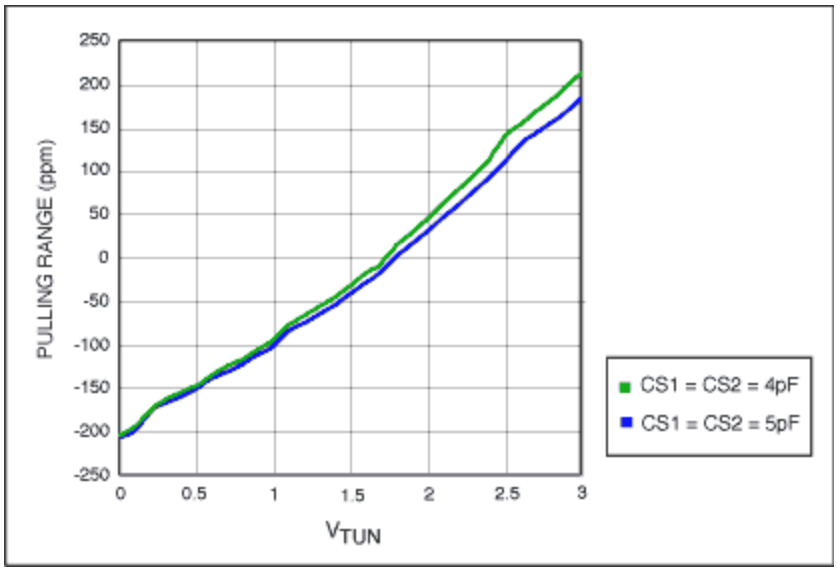

Figure 4.

To confine the tuning range of a VCXO, we can set the upper range by varying the external shunt capacitors. The value of the shunt capacitors is in the range of 4ps–7ps, depending on the board parasitic capacitance. On the other hand, the lower range is determined by the value of the internal veractor, which cannot be changed externally. In order to reduce the affect of the parasitic capacitance on the upper tuning range, in board layout we should minimize the parasitic capacitance of the crystal pins to the ground, providing good clearance between the pins to the plans of ground and power supply. For detailed board layout, refer to the MAX9485 evaluation (EV) kit [4].

Setup for Measuring Output CLK Jitter

For an oscillator, jitter is an important performance measurement. There are two most often-used jitter definitions: period jitter and cycle-to-cycle jitter, see **Figure 5** for the details. To measure the jitters, we can use the high-speed digital sampling scope to sample a big piece of data and calculate the jitters based on the definitions. The scopes from Tektronix (TDS 7254) or Lecroy (Wavepro 960) provide these measurements with equipped software. Also we can use high-speed digital scope to measure the period jitter in time domain [3]. Figure 5 shows the setup. By the time domain approach, we are unable to measure the cycle-to-cycle jitter. However, if jitter noise at every cycle is independent and identically distributed, then the cycle-to-cycle jitter is 1.414 times of the period jitter. MAX9485 can generate 21 different output frequencies based on different audio sampling frequency and frequency scaling factor. We have used the setup shown in **Figure 6** measuring the period jitter for all possible output CLK frequencies. **Table 1** shows the results of the measurement.

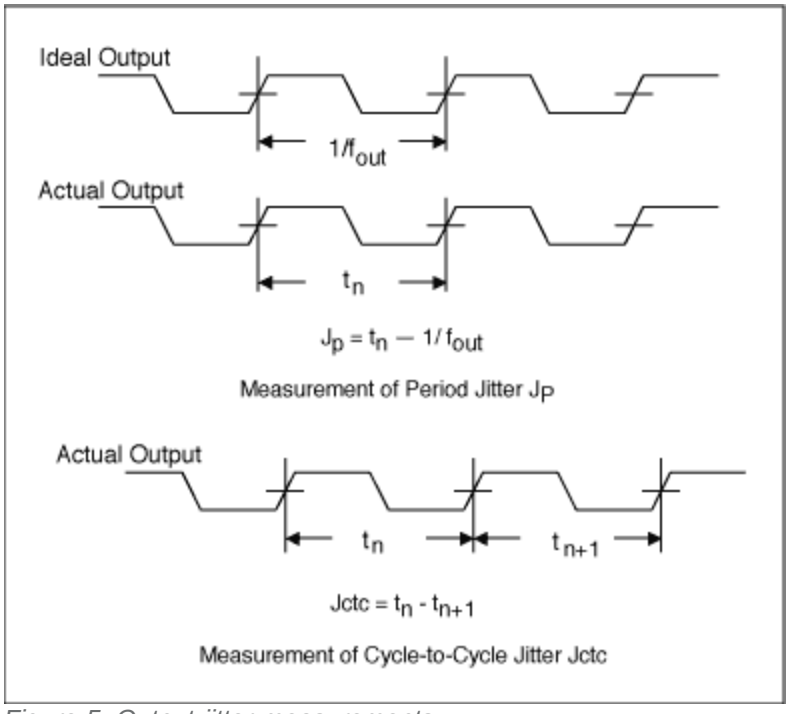

Figure 5. Output jitter measurements.

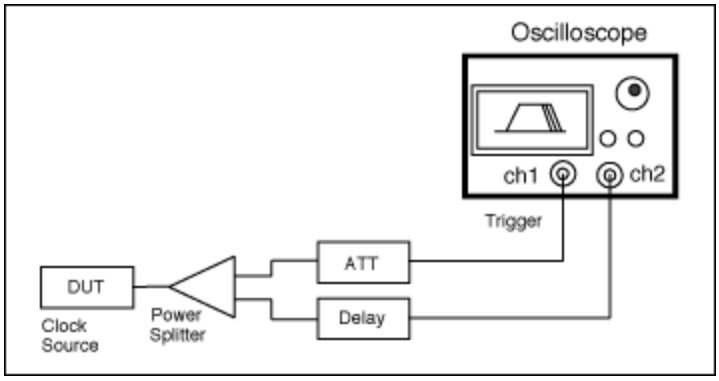

Figure 6. Self-trigger jitter measure setup.

Table 1. Period Jitter vs. Output Frequency

FOUT	Scaling factor	Fs	JP (RMS)	
(MHz)		(kHz)	(ps)	(UI)
73.728	768	96	21	0.00155
67.7376	768	88.2	23.2	0.00157
49.152	768	64	42.6	0.00209
36.864	768	48	40	0.00147
36.864	384	96	37	0.00136
33.8688	768	44.1	44	0.00149
33.8688	384	88.2	41.3	0.00140
24.5760	768	32	66	0.00162

24.5760	384	64	92	0.00226
24.5760	256	96	50	0.00123
22.5792	256	88.2	55.1	0.00124
18.4320	384	48	59	0.00109
16.9344	384	44.1	69	0.00117
16.3840	256	64	134	0.00220
12.2880	256	48	84.8	0.00104
12.2880	384	32	170	0.00209
11.2896	256	44.1	100	0.00113
9.126	768	12	106	0.00097
8.1920	256	32	250	0.00205
4.608	384	12	198	0.00091
3.072	256	12	324	0.00100

From this table we can see that in general the higher the frequency, the lower the jitter. However, if we use a relative measure to describe jitter, such as unit interval (UI), seen the last column of the table, the jitters are comparable. In addition, it is noticed that the frequencies 36.864MHz, 33.8688MHz, 24.5760MHz, and 12.288MHz can be generated by different sampling frequency Fs and scaling factors, which leads to different jitter measurement. Therefore, when these frequencies are used, users should select Fs and the scaling factor that generate lowest jitter.

References

1. MAX9485 data sheet
2. Ecliptek Corp.
3. Maxim application note 2744, "Jitter measurements for CLK generators or synthesizers"
4. MAX9485EVKIT
5. Daishinku Corp.

Related Parts		
MAX9485	Programmable Audio Clock Generator	Free Samples

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