Eat your vegetables: Why you should always follow switch-mode power layout guidelines

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Open any switching power-supply datasheet or design handbook and the message is the same: follow these layout guidelines, OR ELSE. Even if the schematic has all the proper connections and the bill of materials (BOM) has components rated for the application, many power-supply designs are doomed to fail due to poor layout. When troubleshooting a design that 'should work,' most problems can be traced back to the layout guidelines found in these handbooks and datasheets. Just like children should listen when parents tell them to eat their vegetables, engineers should follow layout guidelines when semiconductor manufacturers recommend them. For a simple buck converter, some of these guidelines include:

- Placing the input capacitor as close to the chip input as possible. When the high-side FET turns on, input capacitors deliver a high di/dt current pulse. Placing input capacitors close to the IC minimizes parasitic inductance between the input capacitors and high-side switch. This results in a lower voltage drop across the parasitic inductance (i.e. V=Ldi/dt).
- Keeping high-current paths as short and wide as possible. This will decrease trace inductance and resistance in high-current paths, which may significantly increase efficiency in high-current applications.
- Minimizing the loop area formed by the inductor switching node, output capacitors, and input capacitors. This helps keep high-current paths short and wide, and it also reduces the radiated electromagnetic interference (EMI) that may affect nearby components (including the power supply's feedback and compensation components).
- Routing high-speed switching nodes away from sensitive analog areas. If possible, keep the feedback resistors, compensation network, and soft-start capacitor (if used) outside of the high-current loops and as close to the IC as possible.
- Placing a GND plane immediately below all power components and traces carrying high switching currents. Doing so will reduce parasitic inductance. The top layer and second layer are ideal for GND plane placement so it can shield signals in other layers from the power-switching waveforms.
- If there is an exposed paddle, use multiple vias to connect it to the GND plane. Using as many vias as possible will increase both the thermal conductivity and electrical conductivity between the exposed paddle and GND plane, which will keep the IC cool and increase efficiency.

It's one thing to know the recommendations; it's another thing entirely to follow them. Unlike parents, who sometimes struggle to demonstrate the immediate benefits of eating vegetables to their kids, engineers can immediately demonstrate the consequences of poor power-supply layout to their bosses. To experience the effects of breaking each of these rules ourselves, we intentionally built boards that disobeyed the recommendations and characterized each one.

Quick and reliable power-supply design

To start our design, we named a general-purpose step-down application:

- +12V (+/-2%) input voltage
- +3.3V output voltage
- 0.1V load transient overshoot/undershoot maximum
- 5A maximum output current
- balance of efficiency and size

Since the intent of this design was to examine the effects of different board layouts, we needed to produce a well-designed schematic with appropriate component ratings (and de-ratings), a BOM with all orderable components, and a circuit we could simulate to compare the achieved performance versus the expected values. To generate a new design as quickly as possible, with all of the above capabilities, we used Maxim's EE-Sim design tool. We entered our input/output specifications and generated final simulation results with an orderable BOM. After entering the schematic into our CAD program, we had the circuit based on the MAX17506 step-down converter (**Figure 1**).

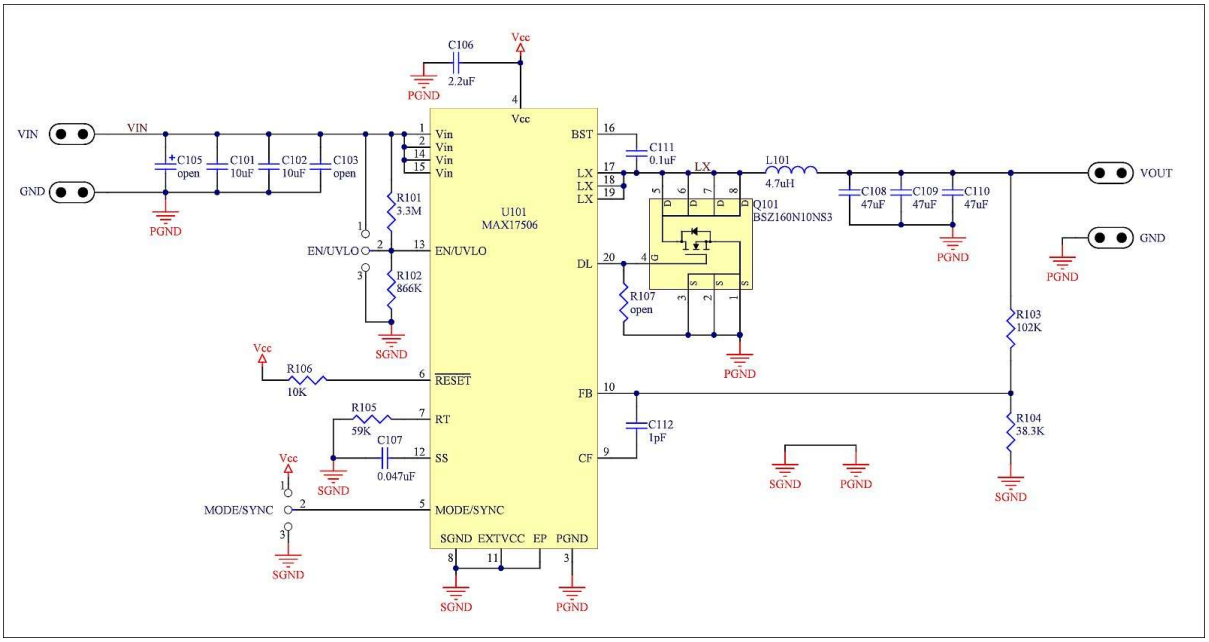

Figure 1 Final design for +3.3V, 16.5W step-down converter

To investigate different layout considerations, we built one ‘optimized’ board to compare with the simulation results and serve as our scientific control and five ‘variant’ boards that each disobeyed one of the rules listed above.

Board #1 – Optimized layout

The first optimal board layout is shown in **Figure 2**, with the top layer in red, second layer in orange, third layer in green, and bottom layer in blue. Note that:

- The input capacitors (C101, C102) are next to the input pins.
- The input path, output path, and LX node are all top-layer planes to minimize impedance.
- The input capacitors (C101, C102), output capacitors (C108, C109, C110), and inductor (L101) are

adjacent to each other to minimize the conduction loop.

- The feedback components (R103, R104, C112), frequency-setting resistor (R105), and soft-start capacitor (C107) are placed below the control IC, away from the high-current paths placed above the IC.
- There are layers upon layers of GND planes (way more than necessary) to help with high-current conduction.
- The exposed paddle is connected to the internal GND planes through nine vias.

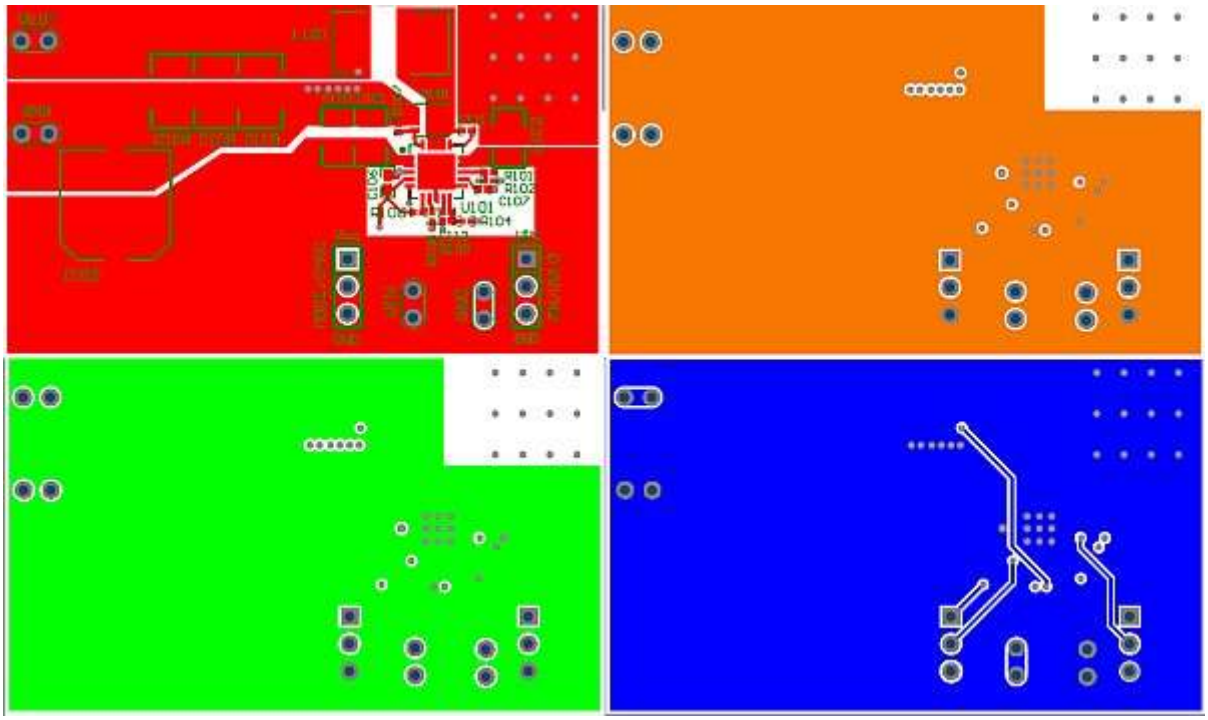

Figure 2 Optimal layout of the MAX17506 buck converter design

When the time came to validate the optimal layout versus the simulation results, the board was tested for efficiency, output voltage ripple, load transient performance, and the switching-node waveform. These results were compared to the original EE-Sim simulation results to judge how well the board was designed.

Efficiency: Simulation versus optimized layout

Perhaps the most scrutinized specification when evaluating any power converter's performance is its efficiency, or how well the converter transfers the input power to the output. After verifying that the board turned on successfully, power efficiency was the first comparison made between simulation and bench data. **Figure 3** shows the comparison of the expected versus achieved efficiencies.

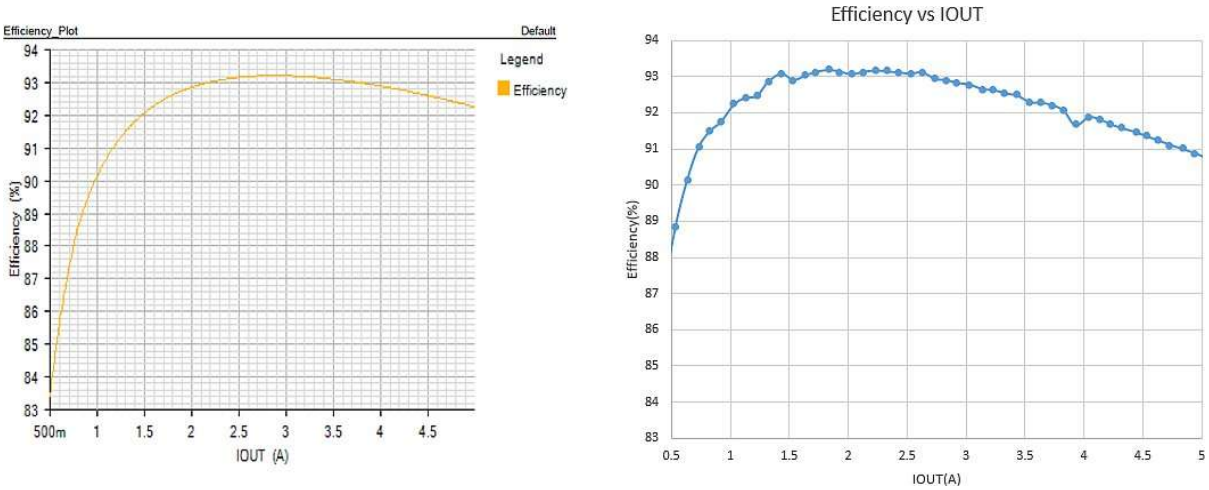

Figure 3 Simulation versus measured efficiency

Overall, the optimized board produced similar results to the EE-Sim efficiency simulation. The achieved efficiency was ~4% higher at a lighter load of 500mA, but ~1% lower at a full load of 5A. This established a good baseline to compare with the non-recommended layouts.

Load transient: Simulation versus optimized layout

Another heavily scrutinized performance benchmark for a power converter is how it responds to transient changes in the load current. These waveforms are also used to indirectly measure a converter's stability, as loop stability measurements require specialized equipment that may not be available. In our design parameters, we specified 0.1V maximum overshoot/undershoot, and **Figure 4** shows the simulated load transient response versus the achieved response.

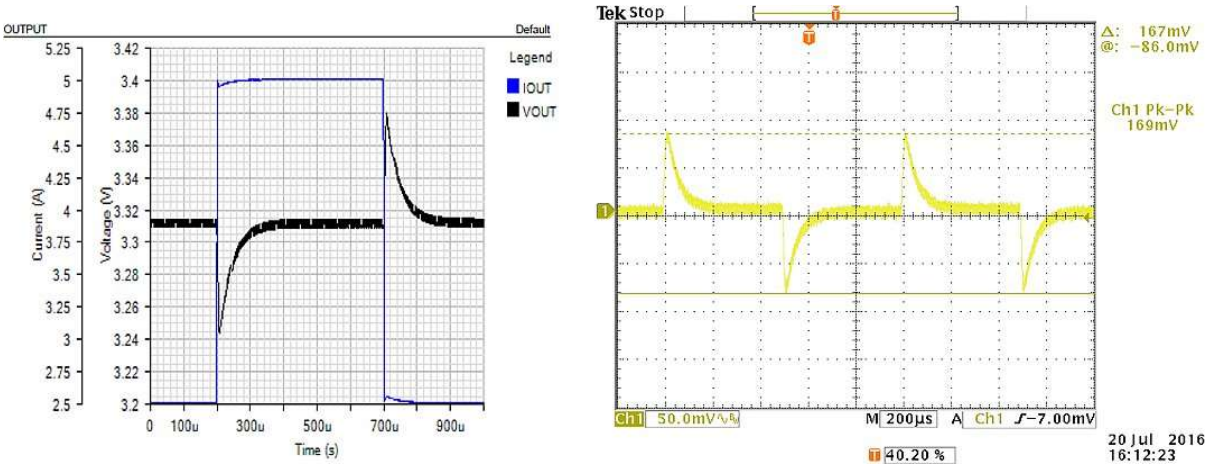

Figure 4 Simulated load transient response (left) versus achieved response (right).

In the simulation, a load step from 2.5A to 5A yielded a 70mV undershoot in output voltage that recovered within 190us, and the measured response yielded an 80mV undershoot that recovered within a 180us. When the load dropped from 5A to 2.5A, the simulation showed a 70mV overshoot that resolved in 180us and the measured response showed an 80mV overshoot that resolved within 180us. This near-perfect match in simulation and characterization inspired confidence in the layout of our first board.

Output voltage ripple: Simulation versus optimized layout

The output ripple of a converter depends on many factors, including the output capacitor equivalent series resistance (ESR), feedback network placement, load current, etc. Since we specified a 0.1V maximum overshoot/undershoot in our design, the voltage ripple for a static load current was expected to be much smaller. **Figure 5** shows the simulated output voltage ripple given a 2.5A load, as well as the measured ripple on our optimized layout board.

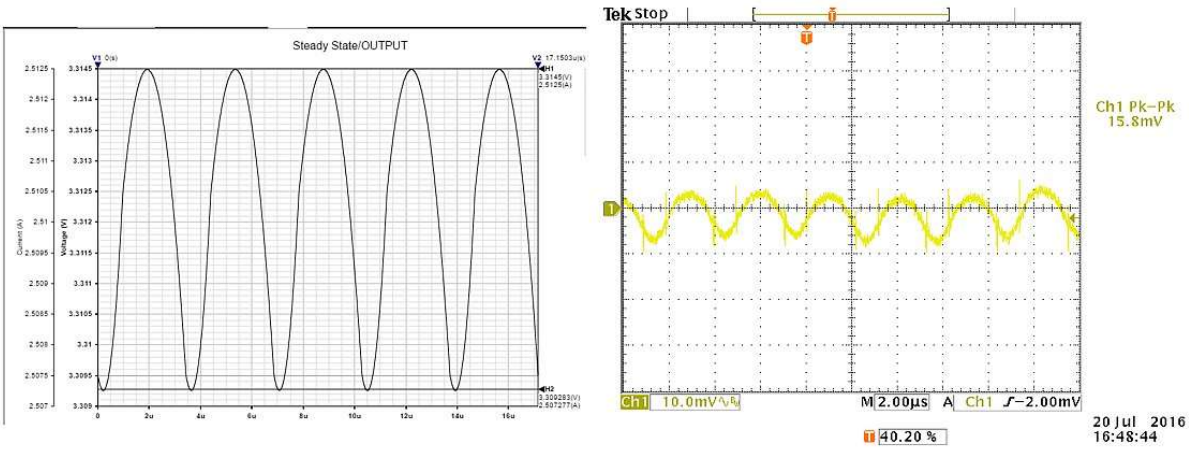

Figure 5 Simulated (left) versus measured (right) output ripple with 2.5A load

The simulated output voltage ripple was $5.2mV_{PP}$, and the measured output ripple was closer to $10mV_{PP}$. Additionally, while care was taken to minimize the measurement loop from the output to our oscilloscope probe to GND, there is still some expected switching interference coupled into the output voltage waveform due to the ESL effect of the capacitor.

Switching-node waveform: Simulation versus optimized layout

In the design, we configured the MAX17506 for a fixed frequency of 313kHz in pulse-width modulation (PWM) mode. Thus, for a static load current, the switching node should appear to be a square wave switching between GND and +12V with a near-constant duty cycle. **Figure 6** shows the simulated and measured switching-node waveforms.

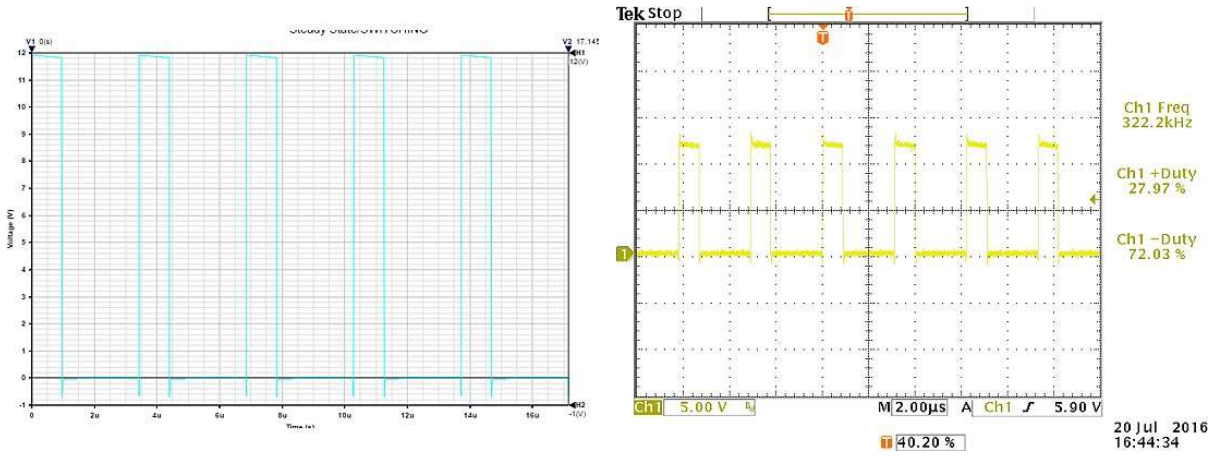

Figure 6 Simulated (left) versus measured (right) switching-node waveforms

With a target frequency of 313kHz, the expected switching period was 3.2us. For 2.5A, the switching

waveform in the simulation showed a 3.4us period and 1.1us on-time, and the measured switching waveform showed a 3.1us period and 0.9us on-time.

After comparing the efficiency, voltage ripple, load transient response, and switching node waveform of our initial design with the 'optimal' layout to the simulation results from EE-Sim, we established a baseline in-lab performance to serve as the basis of our layout study.

Board #2 – No exposed paddle vias to GND plane
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For the first layout modification, the vias connecting the MAX17506 exposed paddle to the internal GND plane layers were removed. A close-up of the layout modification is shown in **Figure 7**. Note that the 3×3 grid of vias is missing from all four layers.

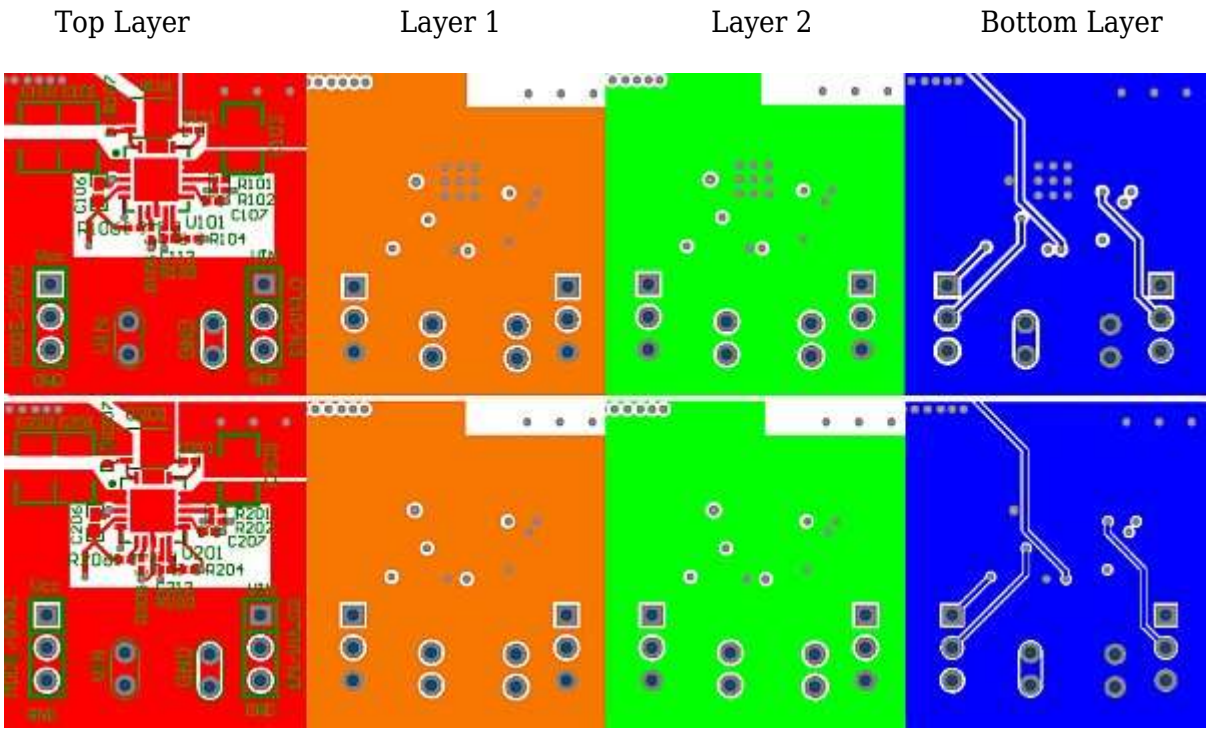


Figure 7 Close-up of layout modification on MAX17506. Optimal layout (top layer) versus no EP pad layout (bottom layer).

The MAX17506 exposed paddle could still conduct to the GND plane through other traces, but the removal of the vias directly underneath would dampen the circuit's ability to conduct heat away from the internal die. If the die temperature increases, the on-resistance of the internal FET will increase, causing a loss in efficiency and a further increase in temperature.

When characterizing the layout without exposed paddle (EP) vias, the circuit behaved similarly in output voltage ripple, load transient performance, and switching waveform under constant load. As expected, the IC was hot to the touch after a few seconds, and the efficiency of this second board degraded due to the increased temperature. With everything else held constant, this particular layout suffered a >1% decrease in efficiency (**Figure 8**) compared to the layout with nine vias placed for thermal conductivity.

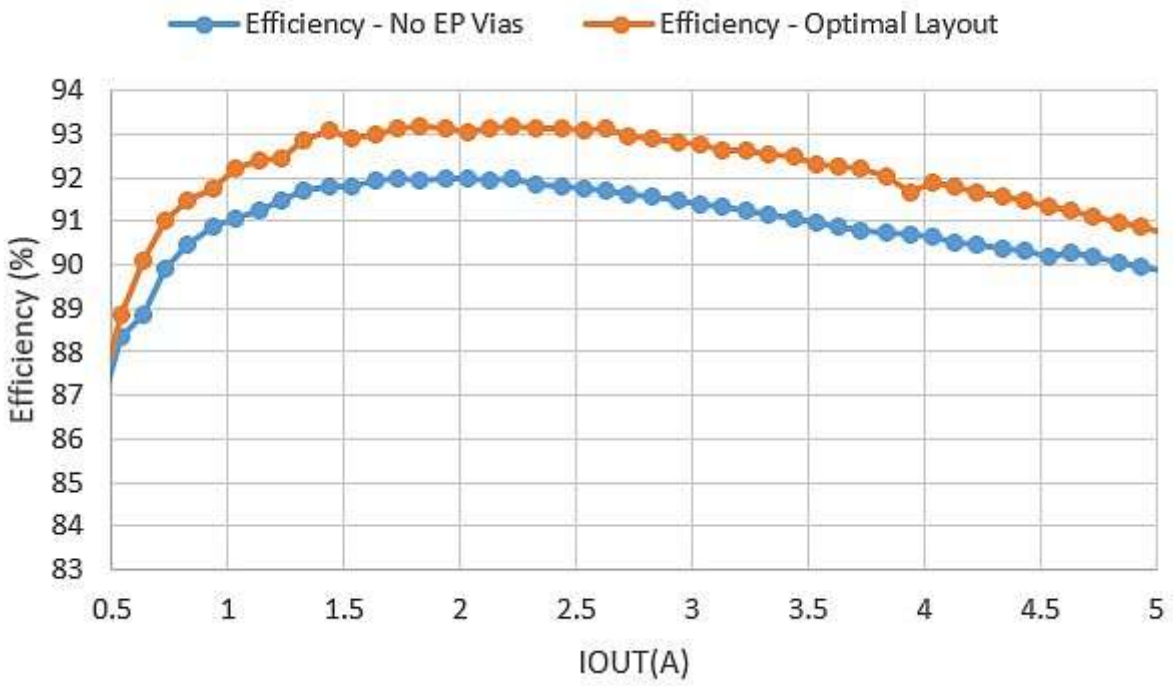


Figure 8 Decreased efficiency in layout without exposed paddle vias

Another important observation was the rapid increase in case temperature between the two boards. Under full load conditions, the IC on the no-EP-vias board is at 32.1°C after five seconds. By comparison, the temperature of the IC on the optimal layout board is only at 30.2 °C even after 45 seconds (**Figure 9**). While this rise in temperature may be tolerable for room-temperature testing, the layout of the second board severely reduces the maximum ambient temperature in which this circuit can reliably operate.

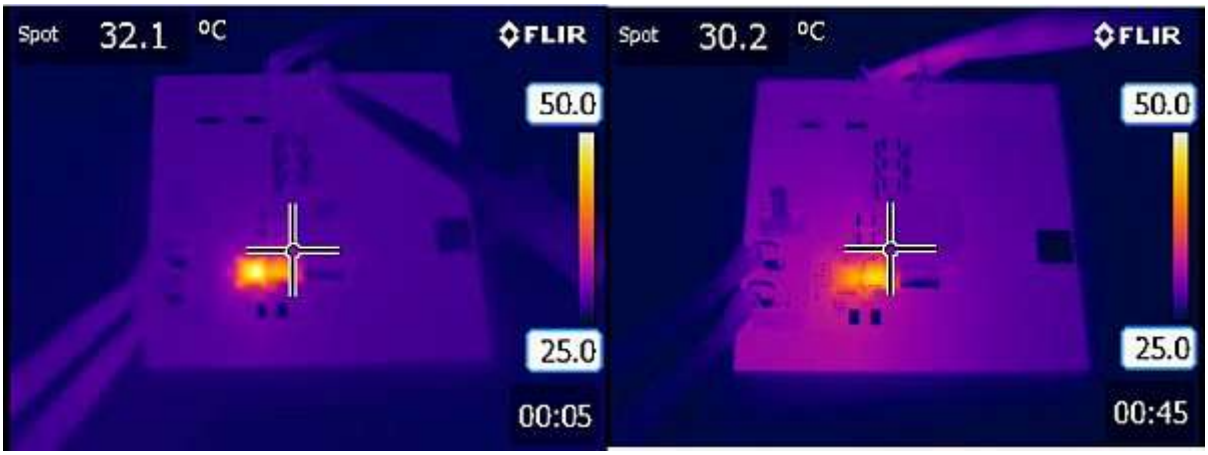


Figure 9 IC temperature on no-EP-vias board (left) versus IC temperature on optimal layout board (right)

Board #3 – Small power-path traces

The third board layout was modified to examine the effects of substituting wide power-path traces with narrow traces. **Figure 10** shows the modifications made to the top layer, with the optimal layout on the left and the modified layout on the right. Note that the V_{IN}, V_{OUT}, and GND top-layer planes are replaced with 20mil traces.

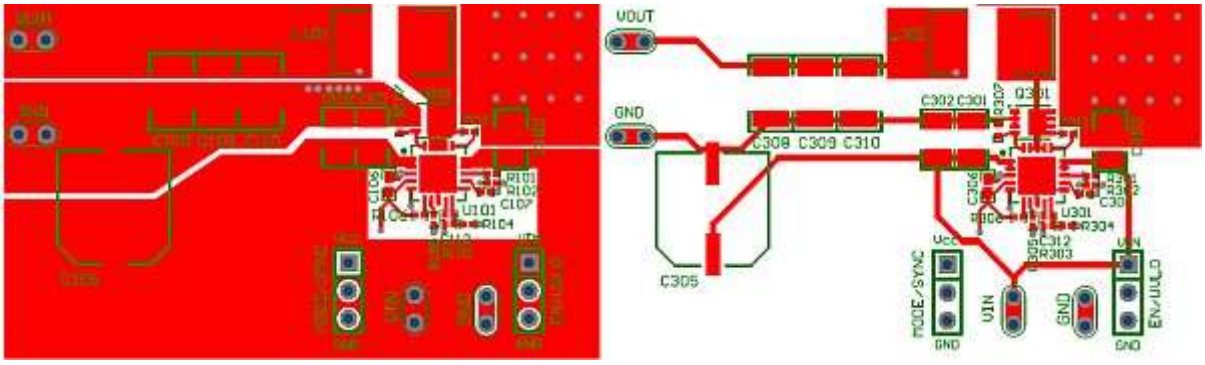


Figure 10 Optimal top-layer layout (left) versus modified top-layer layout (right)

Unsurprisingly, the reduction of the trace widths caused an increase in the conduction losses in the system, especially under heavy loads. The narrow-traces layout suffered a noticeable drop in efficiency when compared to the optimal layout board (**Figure 11**).

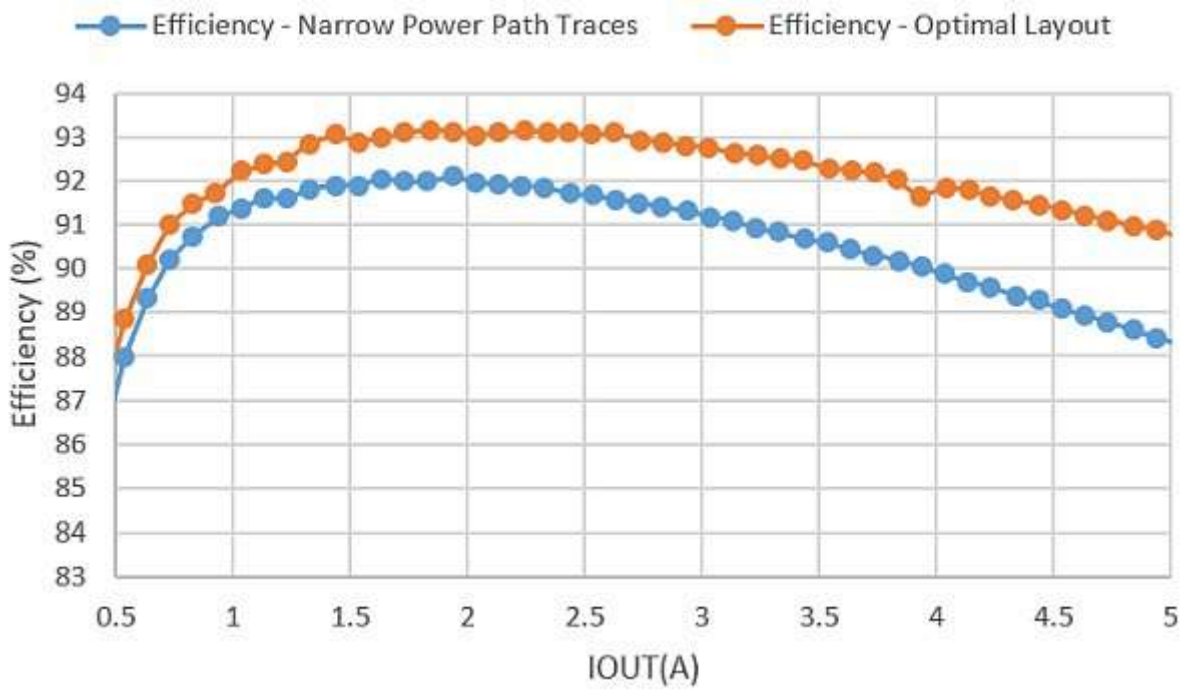


Figure 11 Efficiency drop in narrow-traces layout versus optimal layout board

Additionally, the lack of copper on the top layer contributed to increased voltage noise coupling into the output ripple and load transient waveforms. **Figure 12** shows the differences in measured waveforms between the optimal layout and narrow-trace layout. In the output voltage ripple measurement, the inductor switching waveform couples into the measurement, causing a 20× increase in peak-to-peak voltage. A similar waveform couples into the load transient measurement.

Output Ripple Load Transient

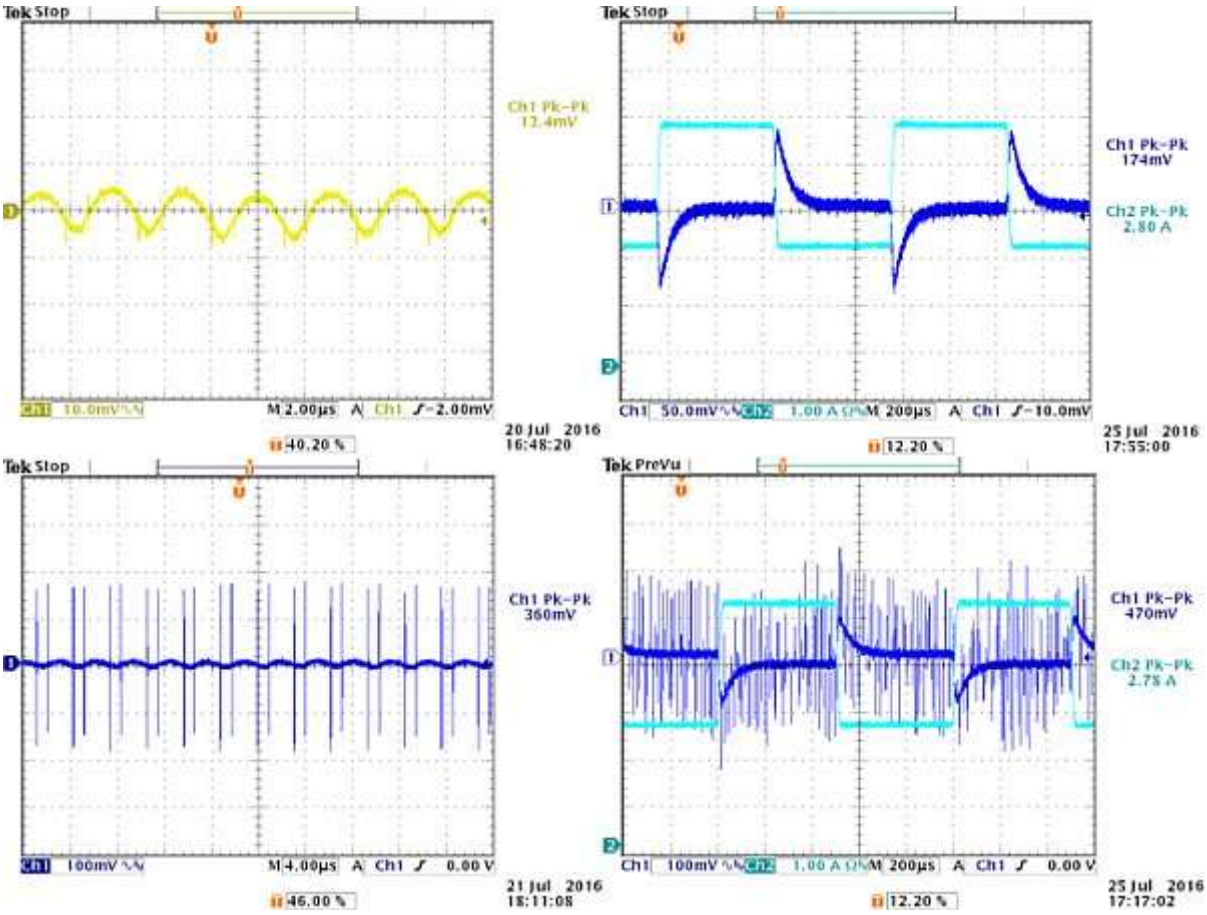
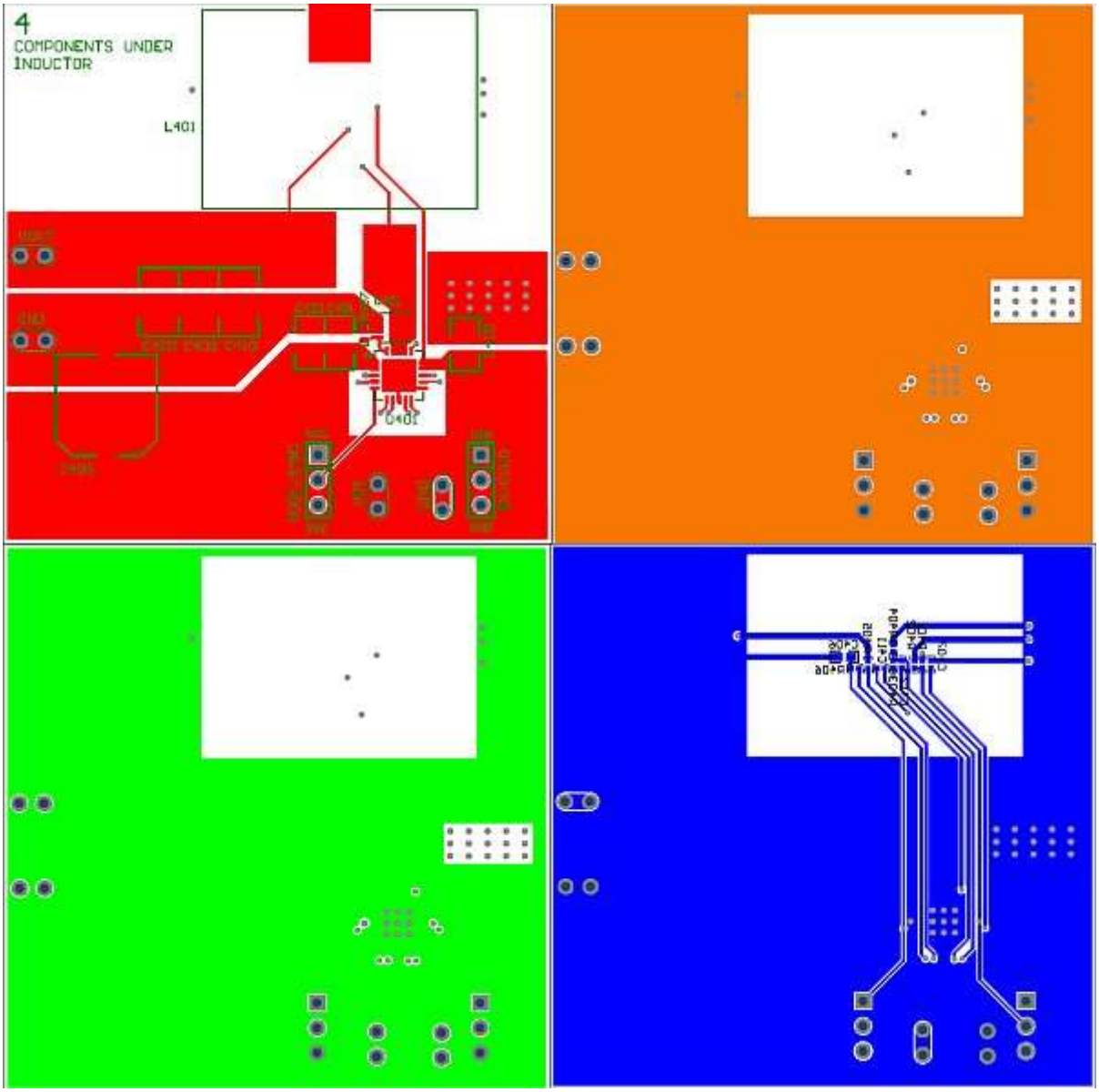


Figure 12 Differences in measured waveforms between optimal layout (top) and narrow-trace layout (below)

Board #4 – Sensitive analog component placement

The fourth board layout was modified to examine the effects of moving the sensitive analog components away from the converter IC and closer to the high-speed switching nodes. In order to do this, the resistors and capacitors related to feedback, high-side FET drive, compensation, soft-start, and OVLO/UVLO were moved to the bottom layer of the PCB. They were placed directly underneath the inductor, with all internal ground planes removed. A bigger inductor pad was placed so that we could also study the effects of using a shielded versus unshielded inductor. **Figure 13** shows the layout of the fourth board.

Top Layer Layer 1



Layer 2 Bottom Layer

Figure 13 Layout of sensitive analog component placement.

After moving the sensitive analog components and placing a shielded inductor over them, there was a minimal change in performance. Aside from a small amount of noise coupled from the switching node appearing in the output voltage ripple and load transient waveforms, the converter could regulate with near-equal performance. However, when the shielded inductor was switched out for an unshielded inductor, the results exceeded all expectations! The efficiency measurement in **Figure 14** only captures some of the performance changes. Across all other measurements shown in **Figure 15**, the unshielded inductor wreaked havoc on the converter operation.

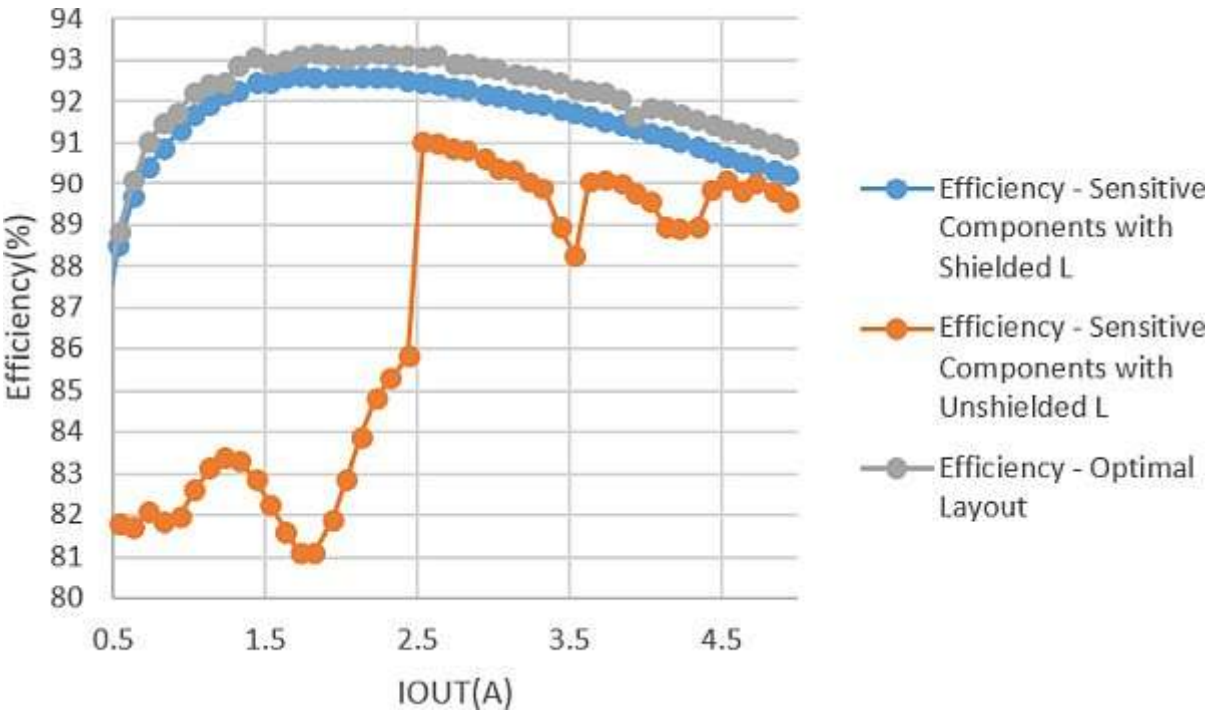


Figure 14 Efficiency impact from moving sensitive analog components

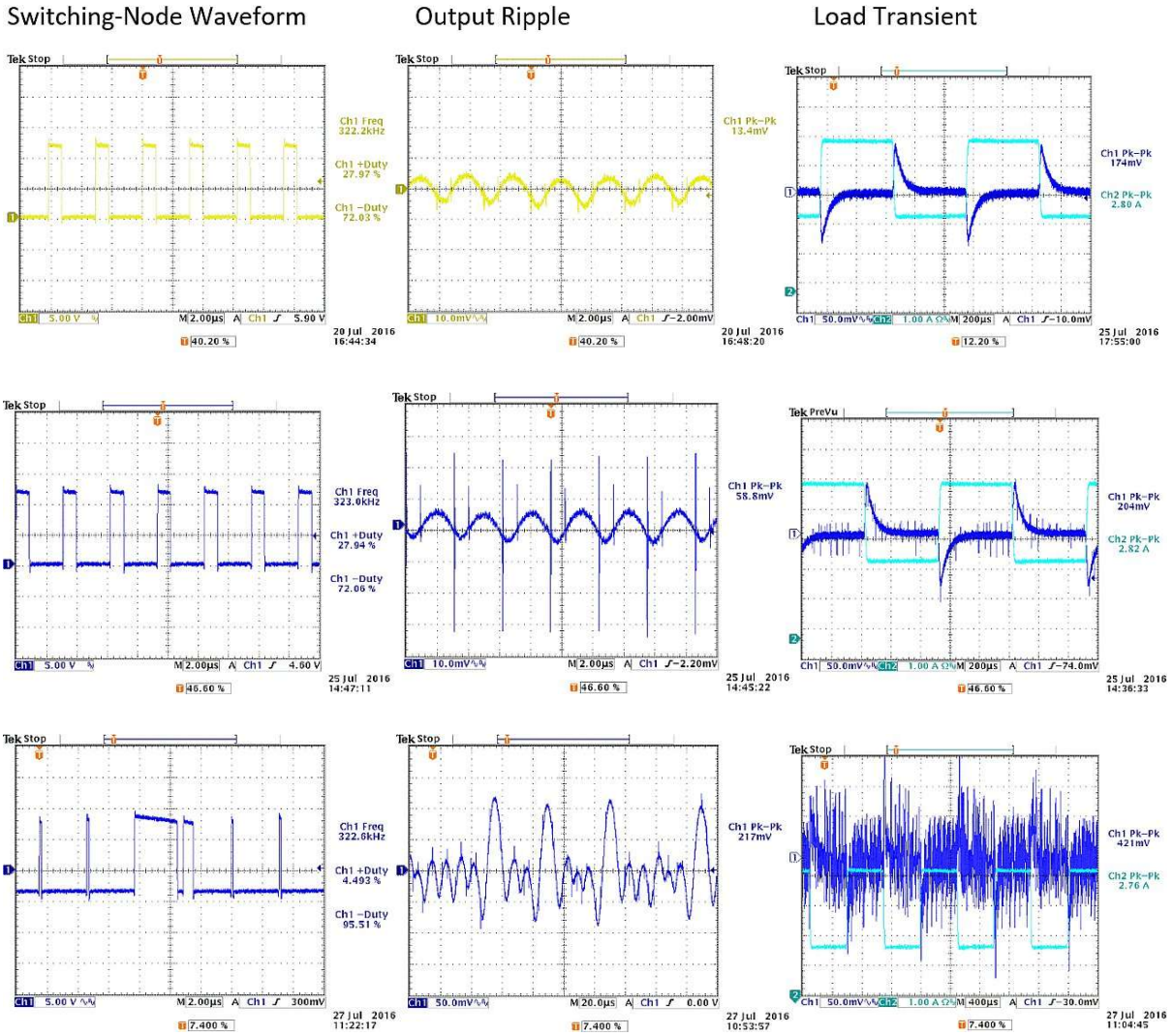


Figure 15 Measurements on optimal (top), shielded inductor (middle), and unshielded inductor (bottom) layout

Looking at the efficiency curve, the circuit with the unshielded inductor shows somewhat close but erratic results. Taking a further look at the other waveforms, the problems with this layout become more apparent. The amount of noise conducted into the feedback node produced an irregular switching waveform under constant load. The irregular switching further distorted the output waveform, causing an 18× increase in peak-to-peak output ripple. This problem exacerbates when examining the output under a load transient, as shown in the bottom-right waveform. Seeing the firsthand effects of placing the high-speed switching and sensitive analog components close together reveals exactly why manufacturers recommend keeping them separated!

Board #5 – Remote output component placement

The fifth board layout was modified to examine the effects of placing the output components several inches away instead of adjacent to the converter IC. Several tests were performed with this layout. The first experiment moved the inductor, low-side FET, and output capacitors approximately in 6.7 inches to 7.5 inches away. The second experiment had the other components remaining in their original location and only moved the output capacitors approximately eight inches away from the IC. The modified layout is shown in **Figure 16**.

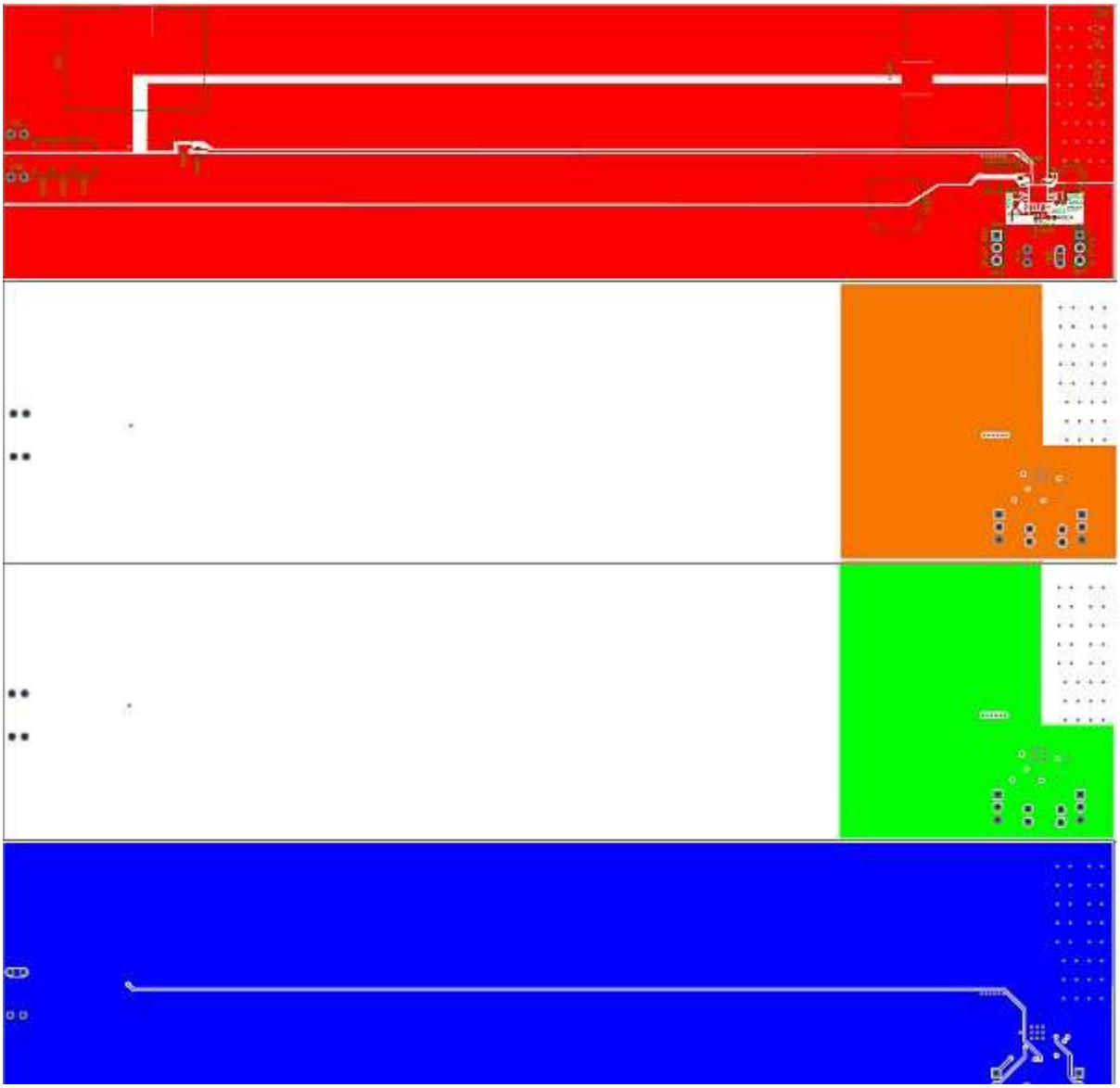


Figure 16 Remote output component placement layout

When all of the components were moved, the converter had a very difficult time operating under light loads. The circuit failed to turn on and generate the output when powered up in fixed PWM mode. When switched to PFM mode, which varies the switching frequency under light load conditions, the part generated an output voltage after the abnormal start-up waveform shown in **Figure 17** below.

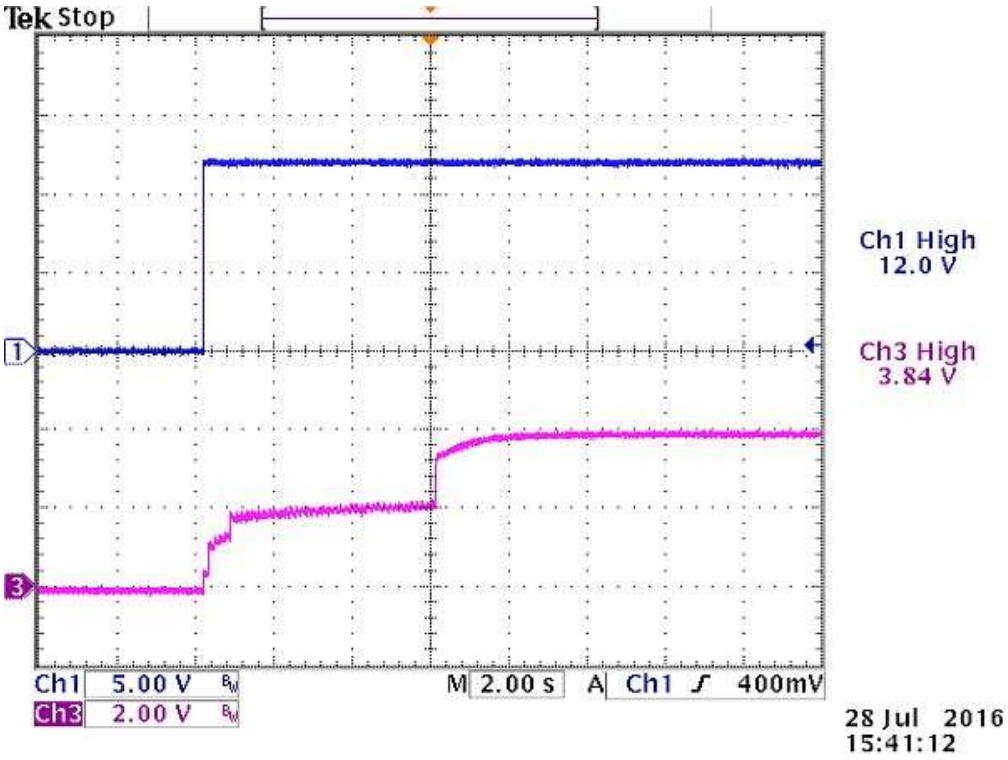


Figure 17 Abnormal start-up waveform

The output voltage was very sensitive to both changes in the input voltage and load current. For 12V input and no load, the output voltage would settle at +3.84V instead of +3.3V. Additionally, once the load current exceeded 1.5A, the circuit could no longer regulate the output voltage.

When the inductor and low-side FET were moved to their original locations, the circuit was able to perform quite well with the output capacitors kept further away from the IC. We suspected this was due to the large top-layer planes maintained on the board between the IC and output capacitors. If this copper was removed and replaced by other active circuitry, the effective capacitance would decrease while the impedance between the capacitance and converter IC would increase, thus reducing the overall performance.

Board #6 – Remote input capacitor placement

The last board layout was modified to examine the effects of moving the input components several inches away instead of adjacent to the converter IC. Several pads were placed at different locations to provide insight into input capacitor placement. The modified layout is shown below.

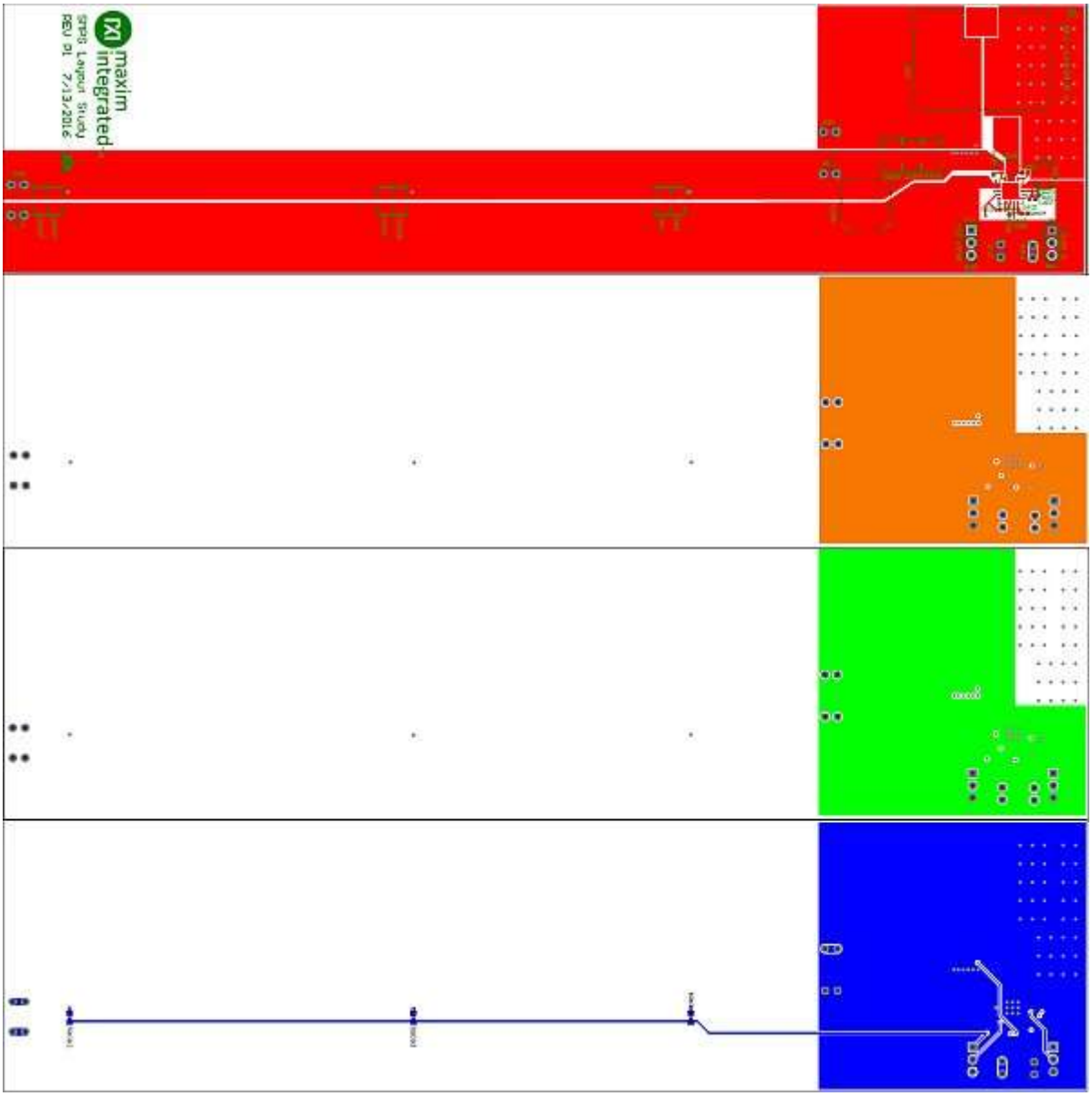


Figure 18 Layout modified to show remote input capacitor placement

The input capacitors were placed at 2.7 inches, 5.1 inches, and 7.8 inches away from the MAX17506. Even at the closest distance of 2.7 inches, the part would not start up under any load conditions. However, as long as a small amount of capacitance, even 1/10th of the specified value, was placed near the IC, it would be able to start up with a load on the output. Aside from a small amount of noise present in the output ripple and load transient waveforms, the converter operated in a similar way to the optimal layout configuration even with lower value of required capacitance, as long as the input capacitance was placed as close as possible to the IC.

In this article, we demonstrated several effects on the power-supply operation due to poor layout. To avoid these errors, it is important to follow the power-supply design guidelines suggested by the semiconductor manufacturer. Even with a perfect power-supply design, there will still be a high chance of poor performance if the layout is done poorly. Just as it is prudent to eat your vegetables, it is also critical to follow the datasheet or the design handbook.

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